IS31FL3242

4-RGB/12-CH LED DRIVER

August 2021

GENERAL DESCRIPTION

The IS31FL3242 is a 12 LED current sink LED driver programmed via 1MHz I2C compatible interface. Each LED can be dimmed individually with 12-bit PWM data and each current sink has 8-bit DC scaling (Color Calibration) data which allowing 4096 steps of linear PWM dimming and 256 steps of DC current adjustable level.

Additionally each LED open and short state can be detected, IS31FL3242 stores the open or short information in Open Short Registers. The Open Short Registers allowing MCU to read out via I2C compatible interface. Inform MCU whether there are LEDs open or short and the locations of open or short LEDs.

The IS31FL3242 operates from 2.7V to 5.5V and features a very low shutdown and operational current.

IS31FL3242 is available in QFN-20 (3mm×3mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 2.7V to 5.5V
- 12 current sinks
- Ultra-low operational current (0.5mA Typ. 0.65mA Max. at V_{CC}= 3.6V, 12-bit PWM mode, 500Hz)
- Accurate color rendition
  - 8/12-bit PWM/channel
  - 8-bit correction/channel
  - 8-bit global current adjust
- SDB rising edge reset I2C module
- 64kHz PWM frequency (8-bit PWM mode)
- 1MHz I2C-compatible interface
- Individual open and short error detect function
- 180 degree phase delay operation to reduce power noise
- Spread spectrum
- QFN-20 (3mm×3mm) package

APPLICATIONS

- Hand-held devices for LED display
- Gaming device (Mouse, Mouse MAT etc.)
- IOT device (AI speaker etc.)

TYPICAL APPLICATION CIRCUIT

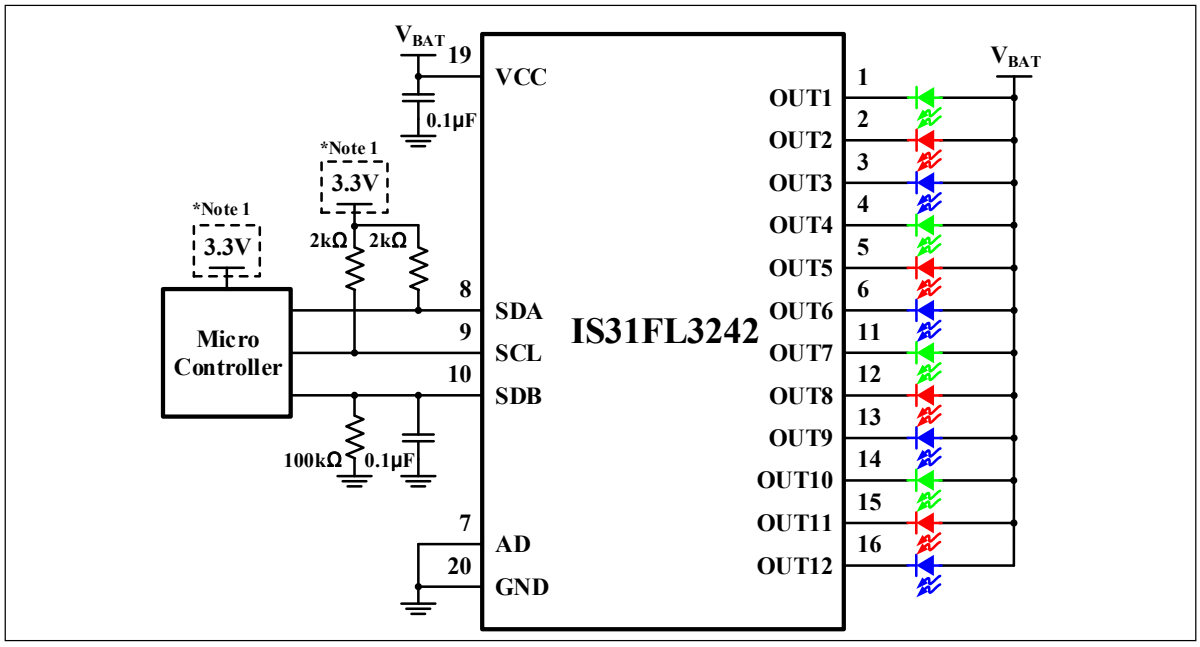


Figure 1 Typical Application Circuit: 4 RGBs

TYPICAL APPLICATION CIRCUIT (CONTINUED)

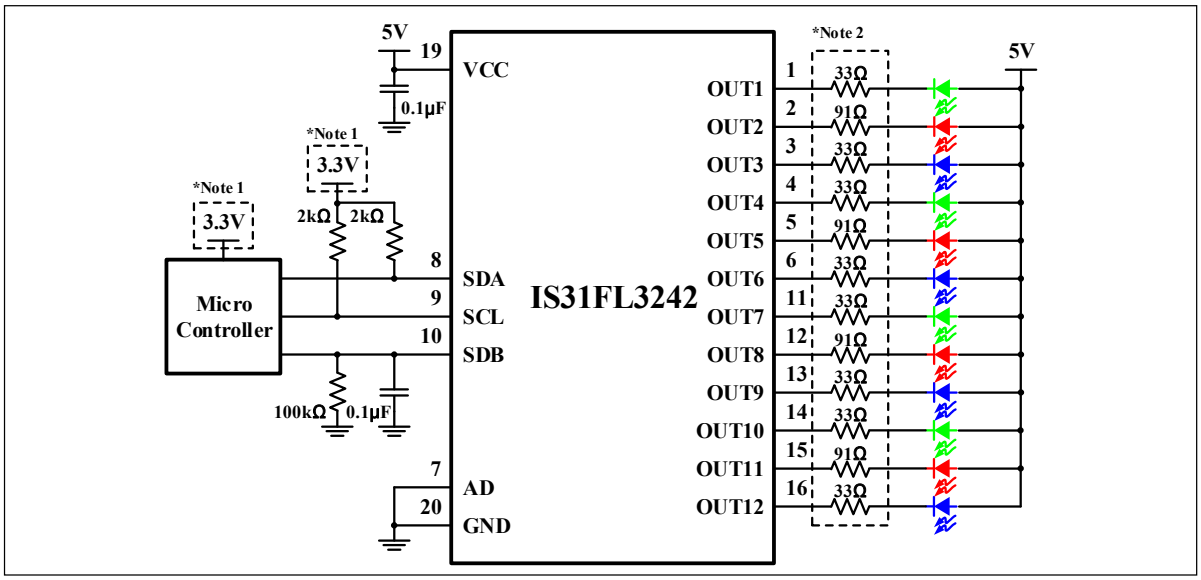
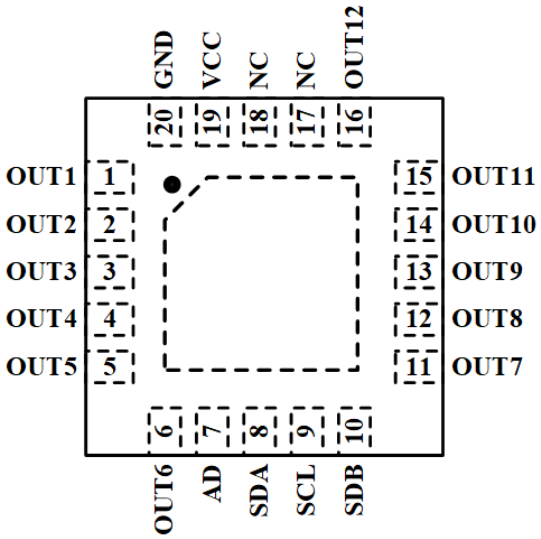


Figure 2 Typical Application Circuit: 4 RGBs, VCC=5V

Note 1: V_{IH} is the high level voltage for IS31FL3242, which is usually same as V_{CC} of Micro Controller, e.g. if V_{CC} of Micro Controller is 3.3V, V_{IH}= 3.3V. If V_{CC}= 5V and V_{IH} is lower than 2.8V, recommend to add level shift circuit.

Note 2: These optional resistors are for offloading the thermal dissipation ($P=I^2R$) away from the IS31FL3242 only, recommend maximum resistor value R_{LED}= (V_{LED+} -V_F -VHR_{OUT})/$I_{OUT(PEAK)}$, VLED+ is the power of LED, VF is the forward voltage of LED, VHR_{OUT} is the headroom of OUT pins.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-20	

PIN DESCRIPTION

No.	Pin	Description
1~6, 11~16	OUT1~OUT12	Current sink pin for LED.
7	AD	I2C address select bit.
8	SDA	I2C compatible serial data.
9	SCL	I2C compatible serial clock.
10	SDB	Shutdown pin.
17~18	NC	NC.
19	VCC	Power for IC.
20	GND	Ground.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3242-QFLS4-TR	QFN-20, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~+6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), θ_{JA}	57.5°C/W
ESD (HBM) ESD (CDM)	±6kV ±750kV

Note 3: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC}= 5V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{CC}= 5V, V_{SDB}= V_{CC}, all LEDs off, 8bit mode, PFS= "000" (64kHz), PSM= "1"		0.95	1.1	mA
		V_{CC}= 5V, V_{SDB}= V_{CC}, all LEDs off, 12bit mode, PFS= "111" (500Hz), PSM= "1"		0.57	0.75	
		V_{CC}= 3.6V, V_{SDB}= V_{CC}, all LEDs off, 8bit mode, PFS= "000" (64kHz), PSM= "1"		0.72	0.9	
		V_{CC}= 3.6V, V_{SDB}= V_{CC}, all LEDs off, 12bit mode, PFS= "111" (500Hz), PSM= "1"		0.5	0.65	
I_{SD}	Shutdown current	V_{SDB}= 0V		0.5	1	μA
		V_{SDB}= V_{CC}, Configuration Register written "0000 0000"		0.5	1	
I_{OUT}	Maximum constant current of OUTx	GCC= 0xFF, SL= 0xFF		48		mA
ΔI_{MAT}	Between channels	I_{OUT}= 42mA, GCC= 0xE0, SL= 0xFF	-6		6	%
ΔI_{ACC}	Between device to device	I_{OUT}= 42mA, GCC= 0xE0, SL= 0xFF	-6		6	%
ΔI_{MAT}	Between channels	LCAI= "1", I_{OUT}= 3mA, GCC= 0x30, SL= 0xFF	-6		6	%
ΔI_{ACC}	Between device to device	LCAI= "1", I_{OUT}= 3mA, GCC= 0x30, SL= 0xFF	-6		6	%
V_{HR}	Current sink headroom voltage OUTx	I_{SINK}= 42mA, GCC= 0xE0, SL= 0xFF		250	300	mV
f_{PWM}	PWM frequency	12bit mode, PFS= "100" (4kHz)	3.6	4	4.4	kHz
V_{OD}	OUTx pin open detect threshold	V_{CC}= 5V, I_{OUT}≥ 1mA, PWM> 6%, measured at OUTx	0.08	0.1	0.26	V
V_{SD}	LED short detect threshold	V_{CC}= 5V, I_{OUT}≥ 1mA, PWM> 6%, measured at (V_{CC}-V_{OUTx})	0.8	1.0	1.2	V
T_{SD}	Thermal shutdown	(Note 4)		158		°C
T_{SD_HY}	Thermal shutdown hysteresis	(Note 4)		18		°C

ELECTRICAL CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Logic Electrical Characteristics (SDA, SCL, SDB, AD)						
V_{IL}	Logic “0” input voltage	V_{CC}= 2.7V~5.5V	GND		0.4	V
V_{IH}	Logic “1” input voltage	V_{CC}= 2.7V~5.5V	1.4		V_{CC}	V
I_{IL}	Logic “0” input current	V_{INPUT}= 0V (Note 4)		5		nA
I_{IH}	Logic “1” input current	V_{INPUT}= V_{CC} (Note 4)		5		nA

DIGITAL INPUT I2C SWITCHING CHARACTERISTICS (NOTE 4)

Symbol	Parameter	Standard Mode		Fast Mode		Fast Mode Plus		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	Serial-clock frequency	-	100	-	400	-	1000	kHz
t_{BUF}	Bus free time between a STOP and a START condition	4.7	-	1.3	-	0.5	-	μs
$t_{HD, STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	0.26	-	μs
$t_{SU, STA}$	Repeated START condition setup time	4.7	-	0.6	-	0.26	-	μs
$t_{SU, STO}$	STOP condition setup time	4.0	-	0.6	-	0.26	-	μs
$t_{HD, DAT}$	Data hold time (Note 5)	0	-	0	-	0	-	μs
$t_{SU, DAT}$	Data setup time	250	-	100	-	50	-	ns
t_{LOW}	SCL clock low period	4.7	-	1.3	-	0.5	-	μs
t_{HIGH}	SCL clock high period	4.0	-	0.7	-	0.26	-	μs
t_R	Rise time of both SDA and SCL signals, receiving	-	1000	-	300	-	120	ns
t_F	Fall time of both SDA and SCL signals, receiving	-	300	-	300	-	120	ns

Note 4: Guaranteed by design.
Note 5: A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ (1.4V) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

DETAILED DESCRIPTION

I2C INTERFACE

IS31FL3242 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31FL3242 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin.

Table 1 Slave Address

AD	A7:A3	A2:A1	A0
GND	10001	00	0/1
SCL		01	
SDA		10	
VCC		11	

AD connected to GND, A2:A1=00;

AD connected to VCC, A2:A1=11;

AD connected to SCL, A2:A1=01;

AD connected to SDA, A2:A1=10;

The SCL line is uni-directional. The SDA line is bi-directional (open-drain) with a pull-up resistor (typically 2kΩ). The maximum clock frequency specified by the I2C standard is 1MHz. In this discussion, the master is the microcontroller and the slave is the IS31FL3242.

The timing diagram for the I2C is shown in Figure 3. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31FL3242's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31FL3242 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31FL3242, the register address byte is sent, most significant bit first. IS31FL3242 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31FL3242 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3242, load the address of the data register that the first data byte is intended for. During the IS31FL3242 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3242 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3242 (Figure 6).

READING OPERATION

Most of the registers can be read.

To read the register, after I2C start condition, the bus master must send the IS31FL3242 device address with the R/$\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed, then restart I2C, the bus master should send the IS31FL3242 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31FL3242 to the master (Figure 7).

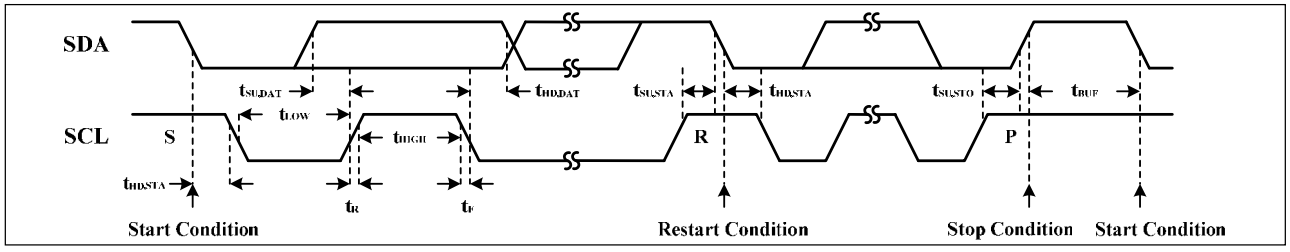


Figure 3 I2C Interface Timing

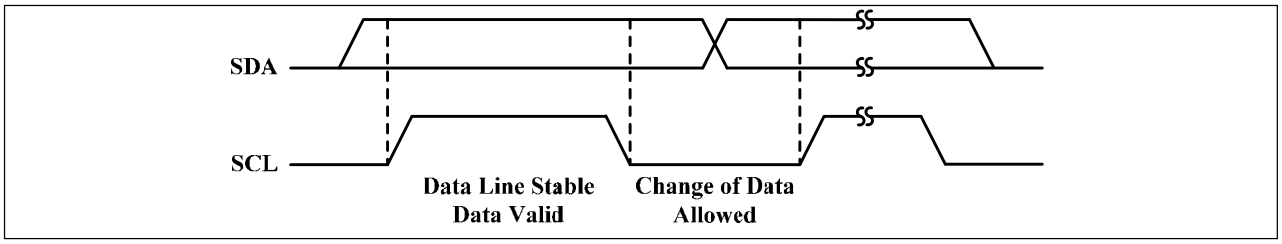


Figure 4 I2C Bit Transfer

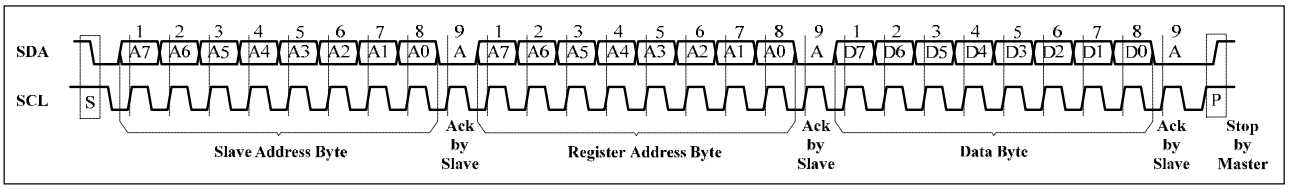


Figure 5 I2C Writing to IS31FL3242 (Typical)

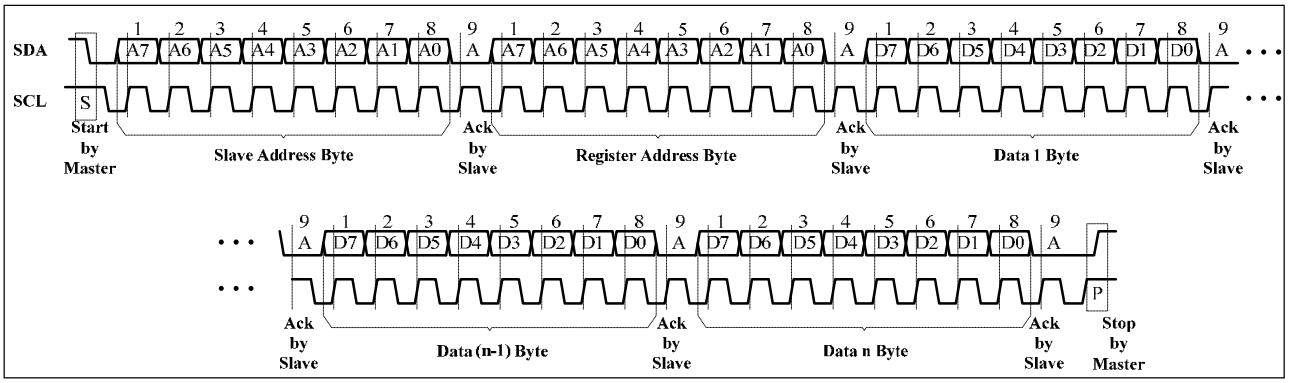


Figure 6 I2C Writing to IS31FL3242 (Automatic Address Increment)

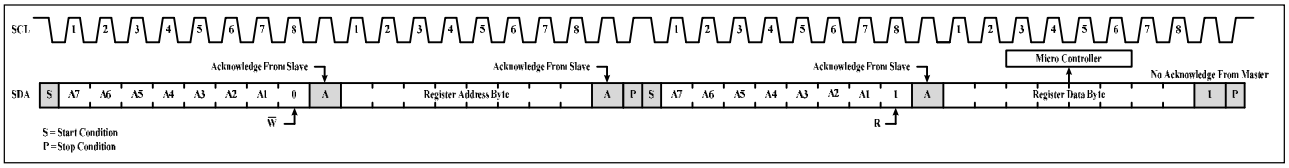


Figure 7 I2C Reading from IS31FL3242

Table 2 Register Definition

Address	Name	Function	Table	R/W	Default
00h	Configuration Register	Configure the operation mode	3	R/W	0011 0010
01h	Global Current Control Register	Set the global current	4	R/W	0000 0000
02h~0Dh	SL of each OUT	DC current for each OUTx (x=1~12)	5	R/W	0000 0000
0Eh~55h	PWM registers	PWM data of each dot	6	W	0000 0000
61h	FPS register	PWM frequency setting	7	R/W	0000 0000
62h~6Dh	Open/short	Open/short information	8	R	0000 0000
6Eh	Spread Spectrum Register	Spread spectrum function enable	9	R/W	0000 0000
7Fh	Reset Register	Reset all register to POR state	-	W	0000 0000

Table 3 00h Configuration Register

Bit	D7	D6	D5:D4	D3	D2	D1	D0
Name	-	PWMM	-	-	PSM	PHC	SSD
Default	0	0	11	0	0	1	0

The Configuration Register sets operating mode of IS31FL3242.

PWMM PWM Resolution Mode
0 12-bit mode
1 8-bit mode

PSM Shutdown OP when PWM off (to save ICC)
0 Do not shutdown OP
1 Shutdown OP

PHC Phase Choice
0 0 degree phase delay
1 OUT1, OUT3, OUT5, OUT7… 0 degree phase delay,
OUT2, OUT4, OUT6, OUT8…180 degree phase delay (Default)

SSD Software Shutdown Control
0 Software shutdown
1 Normal operation

When SSD is “0”, IS31FL3242 works in software shutdown mode and to normal operate the SSD bit should set to “1”.

Table 4 01h Global Current Control Register

Bit	D7:D0
Name	GCC
Default	0000 0000

The Global Current Control Register modulates all OUTx (x=1~12) DC current which is noted as $I_{OUT(PEAK)}$ in 256 steps.

I_{OUT} is computed by the Formula (1):

$$I_{OUT(PEAK)} = 48mA \times \frac{GCC}{256} \times \frac{SL}{256} \quad (1)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (2)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n. SL is the current scaling register value defined in register 02h~0Dh.

To make sure the IC works at normal current amplify status, the GCC should not less than 0x20.

Table 5 02h~0Dh SL Register

Bit	D7:D0
Name	SLx
Default	0000 0000

The Current Scaling Control Register modulates each OUTx (x=1~12) DC current which is noted as I_{OUT} in 256 steps.

I_{OUT} is computed by the Formula (1):

$$I_{OUT(PEAK)} = 48mA \times \frac{GCC}{256} \times \frac{SL}{256} \quad (1)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (2)$$

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (3)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n. GCC is the Global Current Control register value defined in register 01h.

SLx

00000000 0/256 DC current
00000001 1/256 DC current
….

11111111 255/256 DC current

Table 6 0Eh~25h PWM Register

Reg	0Fh (11h, 13h…)		0Eh (10h, 12h…)
Bit	D7:D4	D3:D0	D7:D0
Name	-	PWM_H	PWM_L
Default	0000	0000	0000 0000

PWM_H High bits of PWM Register
PWM_L Low bits of PWM Register

Each dot has 2 bytes to modulate the PWM duty in 4096 steps.

0Fh/0Eh is the PWM register of OUT1, 11h/10h is the PWM register of OUT2,

…

25h/24h is the PWM register of OUT12

The value of the PWM Registers decides the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (4):

$$I_{LED} = \frac{PWM}{4096} \times I_{OUT(PEAK)} \quad (4)$$

$$PWM = \sum_{n=0}^{11} D[n] \cdot 2^n \quad (5)$$

When PWMM= “1” (D6 of register 00h), each dot has 1 byte to modulate the PWM duty in 256 steps. I_{LED} computed by Formula (6):

$$I_{LED} = \frac{PWM}{256} \times I_{OUT(PEAK)} \quad (6)$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (7)$$

Table 7 61h Open Short Enable Register

Bit	D7	D6:D4	D3:D2	D1	D0
Name	LCAI	PFS	MDT	SEN	OEN
Default	0	000	00	0	0

LCAI bit is a current multiplier of all output’s current.

When LCAI= “0”, $I_{OUT(PEAK)}$ follow the formula below or refer formula (1).

$$I_{OUT(PEAK)} = 48mA \times \frac{GCC}{256} \times \frac{SL}{256} \quad (1)$$

When LCAI= “1”, the output current will become 1/4 of above setting, which is:

$$I_{OUT(PEAK)} = 12mA \times \frac{GCC}{256} \times \frac{SL}{256} \quad (8)$$

For applications of $I_{OUT(PEAK)}$= 8mA~48mA, LCAI should be set to “0”.

For applications of $I_{OUT(PEAK)}$= 0~8mA, recommend to set LCAI to “1” to ensure good Δ_{IMAT} and Δ_{IOUT}.

OEN Open detect enable
0 Open detect disable
1 Open detect enable

SEN Short detect enable
0 Short detect disable
1 Short detect enable

MDT Minimum on duty cycle when detect
00 6%
01 3%
1x 12% (only can be active at PWM mode= 8bit)

PFS PWM frequency setting
000 64kHz for 8-bit mode, 4kHz for 12-bit mode
001 32kHz for 8-bit mode, 4kHz for 12-bit mode
010 16kHz for 8-bit mode, 4kHz for 12-bit mode
011 8kHz for 8-bit mode, 4kHz for 12-bit mode

100	4kHz for 8-bit mode/12-bit mode
101	2kHz for 8-bit mode/12-bit mode
110	1kHz for 8-bit mode/12-bit mode
111	500Hz for 8-bit mode/12-bit mode

LCAI	Low current accuracy improve bit
0	No effect
1	Improve the accuracy of low current

Table 8-1 62h Open Register (Read Only)

Bit	D7:D6	D5:D0
Name	-	OUT6:OUT1
Default	00	00 0000

Table 8-2 63h Open Register (Read Only)

Bit	D7:D6	D5:D0
Name	-	OUT12:OUT7
Default	00	00 0000

Table 8-3 68h Short Register (Read Only)

Bit	D7:D6	D5:D0
Name	-	OUT6:OUT1
Default	00	00 0000

Table 8-4 69h Short Register (Read Only)

Bit	D7:D6	D5:D0
Name	-	OUT12:OUT7
Default	00	00 0000

When OEN (61h) is set to “1”, open detection will be trigger once, and the open information will be stored at 62h~63h.

When SEN (61h) set to “1”, short detection will be trigger once, and the short information will be stored at 68h~69h.

In order to have accurate open and short result, before set OEN/SEN bit, the GCC should set to 0x0F and the PWM value should >6%.

Table 9 6Eh Spread Spectrum Register

Bit	D7:D5	D4	D3:D0
Name	-	SSP	-
Default	000	0	0000

When SSP enable, it will adjust the range (±5.6%) and cycle time (2099μs) of spread spectrum function.

SSP	Spread Spectrum Function Enable
0	Disable
1	Enable

7Fh Reset Register

Once user writes the Reset Register with 0xAE, IS31FL3242 will reset all the IS31FL3242 registers to their default value. On initial power-up, the IS31FL3242 registers are reset to their default values for a blank display.

APPLICATION INFORMATION

CURRENT SETTING

The maximum output current $I_{OUT(PEAK)}$ of OUT1~OUT12 can be adjusted by the GCC register in 256 steps, and each OUTx's $I_{OUT(PEAK)}$ can be adjusted by SL register in 256 steps as described in Formula (1).

$I_{OUT(PEAK)}$ is computed by the Formula (1):

$$I_{OUT(PEAK)} = 48mA \times \frac{GCC}{256} \times \frac{SL}{256} \quad (1)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (2)$$

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (3)$$

Where D[n] stands for the individual bit value, 1 or 0, in location n. GCC is the Global Current Control register value defined in register 01h, SL is the current scaling register value defined in register 02h~0Dh.

The LCAI bit in 61h is a current multiplier of all output's current.

When LCAI = "0", $I_{OUT(PEAK)}$ follow the formula below or refer formula (1).

When LCAI = "1", the output current will become 1/4 of above setting, which is:

$$I_{OUT(PEAK)} = 12mA \times \frac{GCC}{256} \times \frac{SL}{256} \quad (8)$$

For applications of $I_{OUT(PEAK)}$=8mA~48mA, LCAI should be set to "0", for applications of IOUT(PEAK)=0~8mA, recommend to set LCAI to "1" to ensure good Δ_{IMAT} and Δ_{IOUT}.

Some applications may require the IOUT of each channel need to be adjusted independently. For example, if OUT1 drives 1 LED and OUT2 drives 2 parallel LEDs, and they should have the same average current like 18mA, we can set the $I_{OUT(Max)}$ to 36mA, and GCC=0xFF, 4Ch=0x80, 4Dh=0xFF, the OUT1 sinks about 18mA and OUT2 sinks 36mA which can have two LEDs in parallel.

Another example, OUT1, OUT2 and OUT3 drive an RGB LED, OUT1 is Red LED, OUT2 is Green LED and OUT 3 is Blue LED, with same GCC and same SL bits, when OUT1 OUT2 and OUT3 have the same PWM value, the LED may look a litter pink, or not so white, in this case, the SL bits can be used to adjust the single I_{OUTx} of some output and make it pure white color. We call this SL bits another name: white balance registers.

PWM CONTROL

The PWM Registers (0Eh~55h) can modulate LED brightness of each channel with 256/4096 steps. For example, if the data in PWM_H register is "0000 0000" and in PWM_L register is "0000 0100", then the PWM is the fourth step.

The average LED current I_{LED} of each LED is also decided by PWM value of each LED. Each LED has 2 bytes to modulate the PWM duty in 4096 steps.

I_{LED} computed by Formula (4):

$$I_{LED} = \frac{PWM}{4096} \times I_{OUT(PEAK)} \quad (4)$$

$$PWM = \sum_{n=0}^{11} D[n] \cdot 2^n \quad (5)$$

When PWMM= "1" (D6 of register 00h), each dot has a byte to modulate the PWM duty in 256 steps. ILED computed by Formula (6):

$$I_{LED} = \frac{PWM}{256} \times I_{OUT(PEAK)} \quad (6)$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (7)$$

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

PWM FREQUENCY SELECT

The IS31FL3242 output channels operate with a default 12-bit PWM resolution and the PWM frequency of 4kHz. Because all the OUTx channels are almost synchronized, the DC power supply will experience large instantaneous current surges when the OUTx channels turn ON. These current surges will generate an AC ripple on the power supply which cause stress to the decoupling capacitors. When the AC ripple is applied to a monolithic ceramic capacitor chip (MLCC) it will expand and contract causing the PCB to flex and generate audible hum in the range of between 300Hz to 18kHz, to avoid this hum, there are many countermeasures, such as selecting the capacitor type and value which will not cause the PCB to flex and contract.

An additional option for avoiding audible hum is to set the IS31FL3242's output PWM frequency above/below the audible range. The PFS bits (61h) can be used to set the switching frequency to 500Hz~64kHz as shown in Table 8, higher than 20kHz is out of the audible range.

OPEN/SHORT DETECT FUNCTION

IS31FL3242 has open and short detect bit for each LED.

When OEN (61h) is set to “1”, open detection will be trigger once, and the open information will be stored at 62h~63h.

When SEN (61h) set to “1”, short detection will be trigger once, and the short information will be stored at 68h~69h.

In order to have accurate open and short result, before set OEN/SEN bit, the GCC should set to 0x0F and the PWM value should >6%.

SPREAD SPECTRUM FUNCTION

PWM current switching of LED outputs can be particularly troublesome when the EMI is concerned. To optimize the EMI performance, the IS31FL3242 includes a spread spectrum function. By enable the SSP bit (6Eh) the IS31FL3242 will adjust the range (±5.6%) and cycle time (2099μs) of spread spectrum function. The spread spectrum can spread the total electromagnetic emitting energy into a wider range that significantly degrades the peak energy of EMI. With spread spectrum, the EMI test can be passed with smaller size and lower cost filter circuit.

INTERFACE RESET

The I2C will be reset if the SDB pin is pull-high from 0V to logic high, at the operating SDB rising edge, the interface operation is not allowed.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting the SSD bit of the Control Register (00h) to “0”, the IS31FL3242 will operate in software shutdown mode. When the IS31FL3242 is in software shutdown, all current sources are switched off, so the LEDs are OFF but all registers accessible. Typical current consume is 0.5μA (V_{CC}=5V).

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical the current consumption is 0.5μA (V_{CC}=5V).

The chip releases hardware shutdown when the SDB pin is pulled high. The rising edge of SDB pin will reset the I2C module, but the register information retains. During hardware shutdown the registers are accessible.

If the VCC supply drops below 1.75V but remains above 0.1V during SDB pulled low, please re-initialize all Registers before SDB pulled high.

LAYOUT

The IS31FL3242 consumes lots of power so good PCB layout will help improve the reliability of the chip. Please consider below factors when layout the PCB.

Power Supply Lines

When designing the PCB layout pattern, the first step should consider about the supply line and GND connection, especially those traces with high current, also the digital and analog blocks’ supply line and GND should be separated to avoid the noise from digital block affect the analog block.

At least one 0.1μF capacitor, if possible with a more 1μF capacitor is recommended to connected to the ground at power supply pin of the chip, and it needs to close to the chip and the ground net of the capacitor should be well connected to the GND plane.

Thermal Consideration

The over temperature of the chip may result in deterioration of the properties of the chip. The thermal pad of IS31FL3242 should connect to GND net and need to use 4 or 9 vias connect to GND copper area, the GND area should be as large area as possible to help radiate the heat from the IS31FL3242.

Current Rating Example

For an $I_{OUT(PEAK)}$=20mA application, the current rating for each net is as follows:

• VCC pin maximum current is 2mA when V_{CC}=5V, but the VLED+ net is provided total current of all outputs, its current can as much as 20mA×12=240mA, recommend trace width for VCC pin: 0.20mm~0.3mm, recommend trace width for VLED+ net: 0.30mm~0.5mm

• Output pins=20mA, recommend trace width is 0.2mm~0.254mm

• All other pins<3mA, recommend trace width is 0.15mm~0.254mm

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

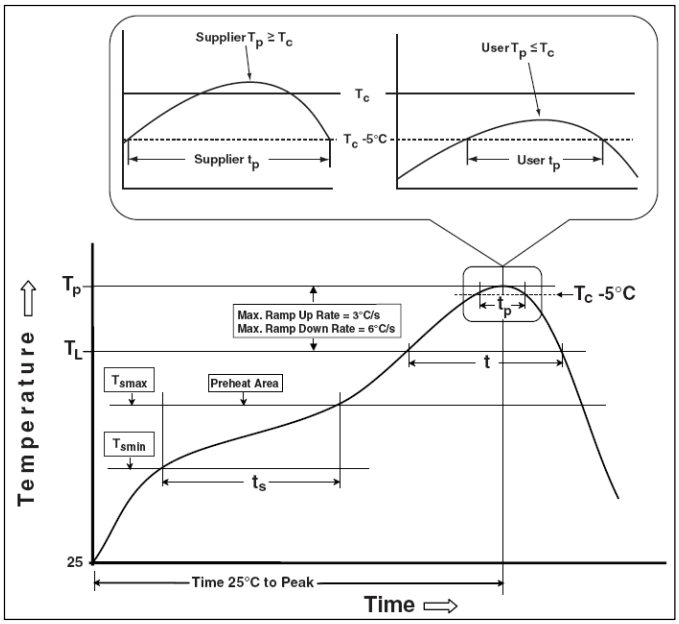
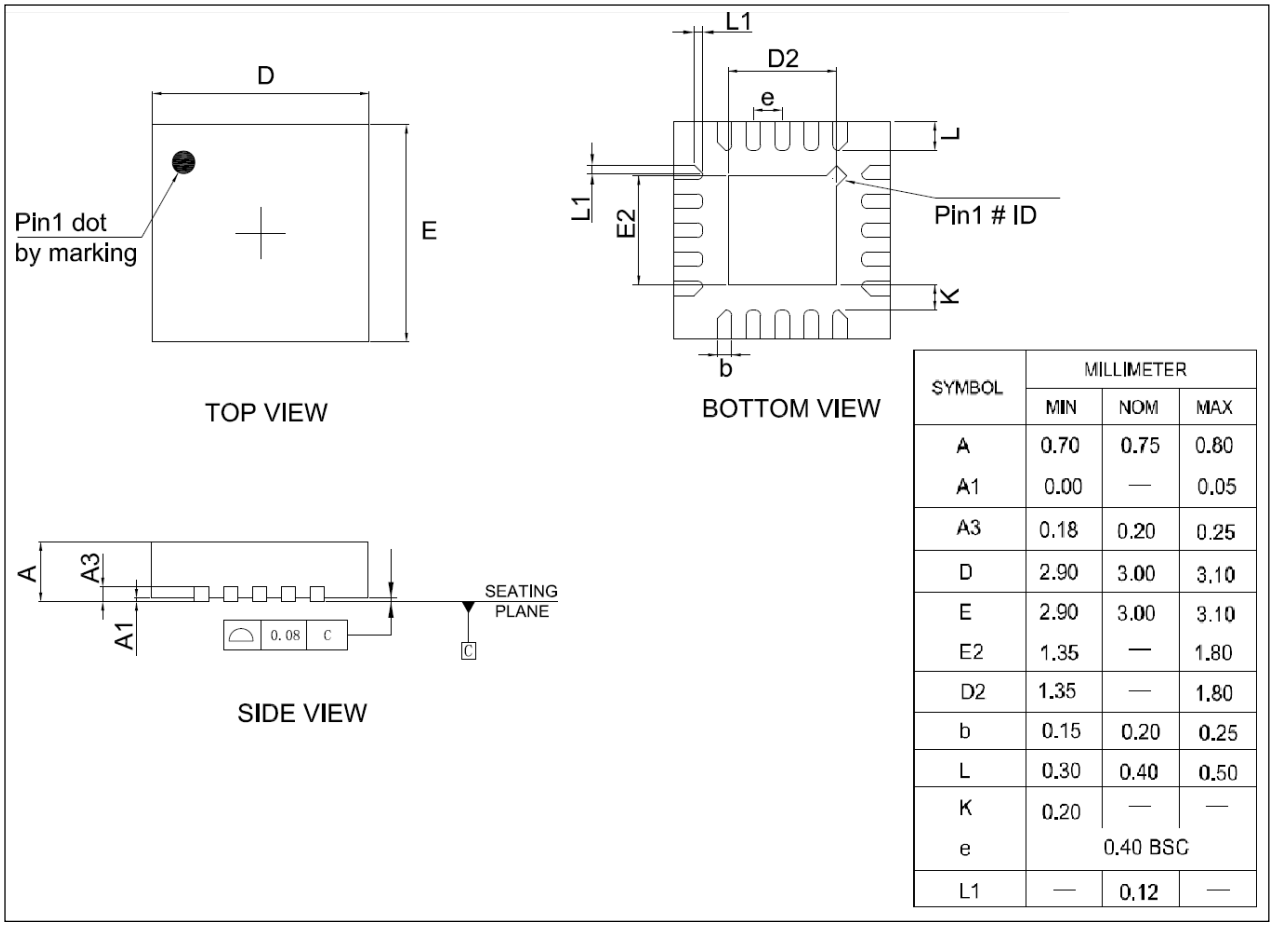


Figure 8 Classification Profile

PACKAGE INFORMATION

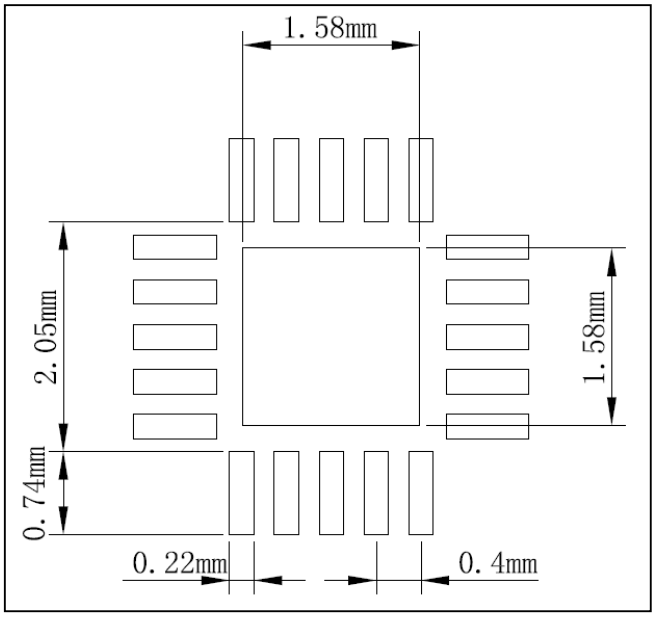
QFN-20



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3	0.18	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E2	1.35	—	1.80
D2	1.35	—	1.80
b	0.15	0.20	0.25
L	0.30	0.40	0.50
K	0.20	—	—
e	0.40 BSC		
L1	—	0.12	—

RECOMMENDED LAND PATTERN

QFN-20



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2021.05.12
B	Update $t_{HD, DAT}$, correct D7 0f 00h register	2021.07.19