

KSH122 / KSH122I NPN Silicon Darlington Transistor

Features

- D-PAK for Surface Mount Applications
- High DC Current Gain
- Built-in Damper Diode at E-C
- · Lead Formed for Surface Mount Applications (No Suffix)

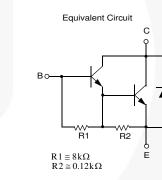
D-PAK

1.Base 2.Collector 3.Emitter

- Straight Lead (I-PAK, " I " Suffix)
- Electrically Similar to Popular TIP122
- Complement to KSH127

Applications

- Switching Regulators
- Converters
- Power Amplifiers



Ordering Information

Part Number	Top Mark	Package	Packing Method
KSH122TF	KSH122	TO-252 3L (DPAK)	Tape and Reel
KSH122TM	KSH122	TO-252 3L (DPAK)	Tape and Reel
KSH122ITU	KSH122-I	TO-251 3L (IPAK)	Rail

I-PAK

March 2016 Recharged Stress St

Description

Designed for general-purpose power and switching, such as output or driver stages in applications.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_c = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Value	Unit	
V _{CBO}	Collector-Base Voltage	100	V	
V _{CEO}	Collector-Emitter Voltage	100	V	
V _{EBO}	Emitter-Base Voltage	5	V	
۱ _C	Collector Current (DC)	8	Α	
I _{CP}	Collector Current (Pulse)	16	Α	
Ι _Β	Base Current	120	mA	
р	Collector Dissipation (T _C =25°C)	20.00	W	
P _C	Collector Dissipation (T _A =25°C)	1.75		
Т _Ј	Junction Temperature	150	°C	
T _{STG}	Storage Temperature - 65 to 15			

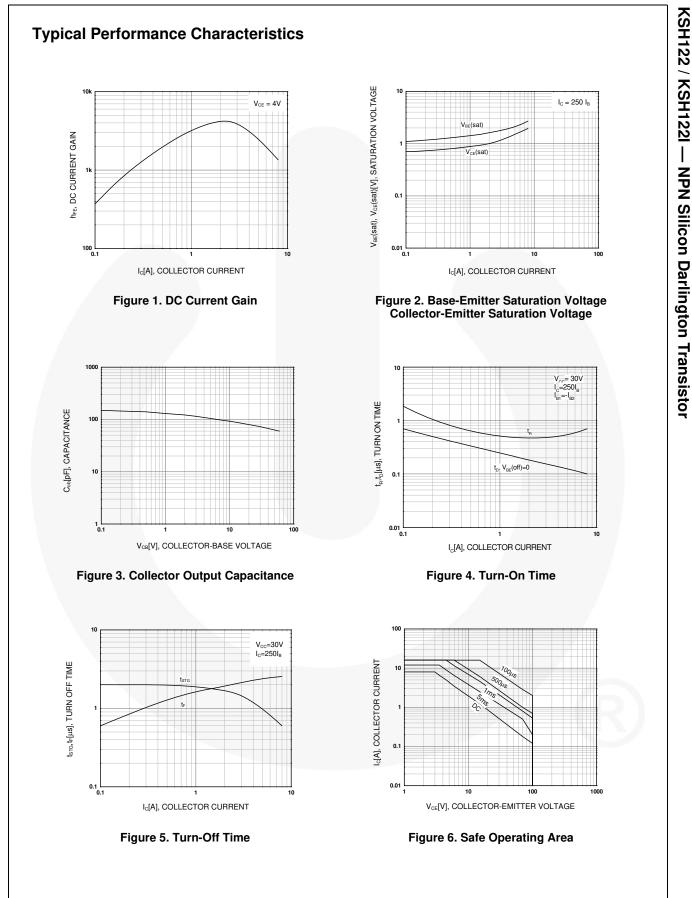
Electrical Characteristics

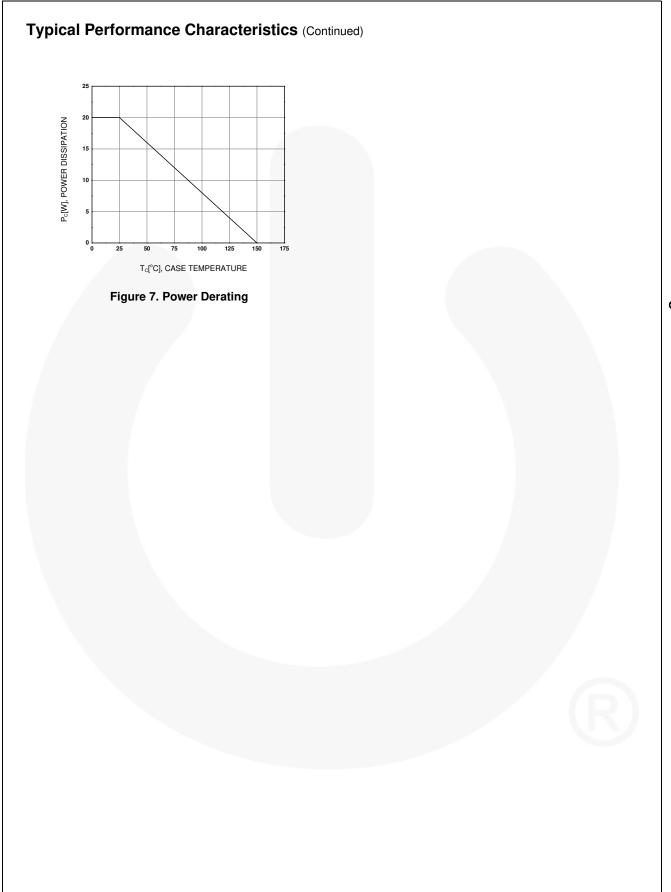
Values are at $T_A = 25^{\circ}C$ unless otherwise noted.

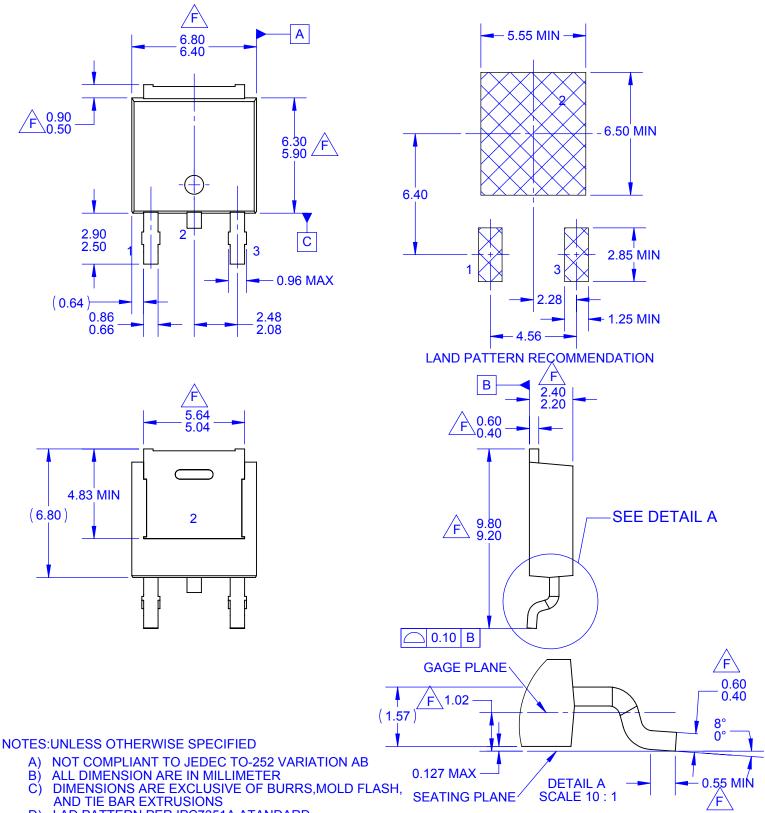
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
V _{CEO} (sus)	Collector-Emitter Sustaining Voltage ⁽¹⁾	I _C = 30 mA, I _B = 0	100			V
I _{CEO}	Collector Cut-Off Current	$V_{CE} = 50 \text{ V}, \text{ I}_{B} = 0$			10	μA
I _{CBO}	Collector Cut-Off Current	$V_{CB} = 100 \text{ V}, I_{E} = 0$			10	μA
I _{EBO}	Emitter Cut-Off Current	$V_{EB} = 5 V, I_{C} = 0$			2	mA
h _{FE} [DC Current Gain ⁽¹⁾	$V_{CE} = 4 V, I_{C} = 4 A$	1000		12000	
		$V_{CE} = 4 V, I_{C} = 8 A$	100			
V _{CE} (sat) Collector-Emitter S Voltage ⁽¹⁾	Collector-Emitter Saturation	I _C = 4 A, I _B = 16 mA			2	V
	Voltage ⁽¹⁾	I _C = 8 A, I _B = 80 mA			4	v
V _{BE} (sat)	Base-Emitter Saturation Voltage ⁽¹⁾	I _C = 8 A, I _B = 80 mA	- /		4.5	V
V _{BE} (on)	Base-Emitter On Voltage ⁽¹⁾	$V_{CE} = 4 V, I_{C} = 4 A$			2.8	V
C _{ob}	Output Capacitance	V _{CB} = 10 V, I _E = 0, f = 0.1 MHz			200	pF

Note:

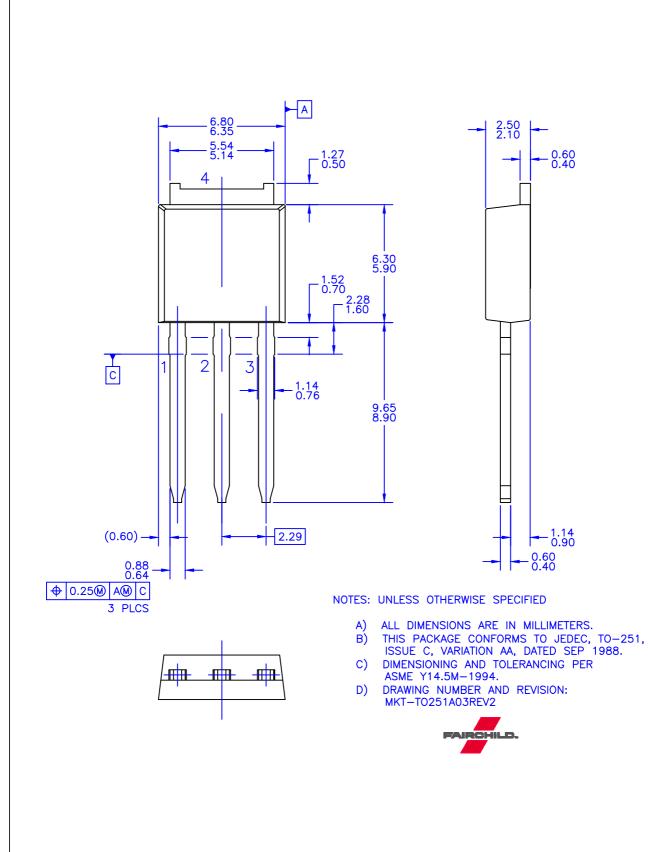
1. Pulse test: pw \leq 300 $\mu s,$ duty cycle \leq 2%.

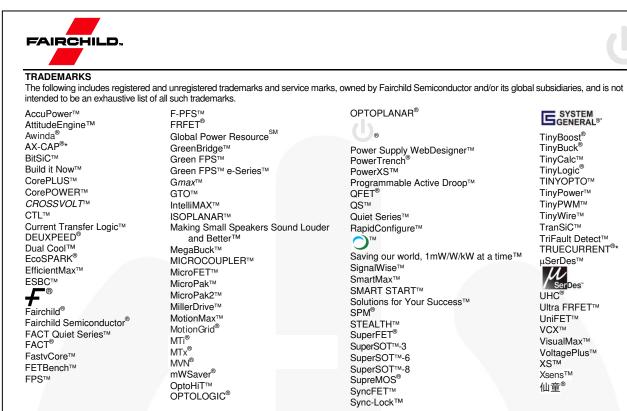






- D) LAD PATTERN PER IPC7351A ATANDARD TO228P991X239-3N
- E)
- DRAWING FILE NAME:MKT-TO252D03REV3. DOES NOT COMPLY JEDEC STANDARD VALUE. F
- G) FAIRCHILD SEMICONDUCTOR.





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