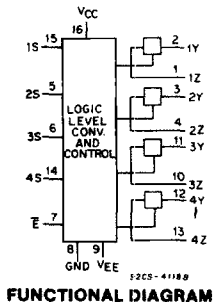


High-Speed CMOS Logic



Quad Analog Switch with Level Translation

Type Features:

- Wide analog-input-voltage range ($V_{CC}-V_{EE}$): 0-10 V
- Low "ON" resistance: 45 Ω typ. @ $V_{CC}=4.5$ V
35 Ω typ. @ $V_{CC}=6$ V
30 Ω typ. @ $V_{CC}-V_{EE}=9$ V
- Fast switching and propagation delay times
- Low "OFF" leakage current
- Built-in "Break-before-make" switching
- Logic-level translation to enable 5 V logic to accommodate ± 5 V analog signals

Family Features:

- Wide operating temperature range:
CD74HC/HCT: -40 to +125°C
- CD54HC/CD74HC types:
2 V to 10 V operation
High noise immunity:
 $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} ; @ $V_{CC} = 5$ V
- CD54HCT/CD74HCT types:
Direct LSTTL input logic compatibility
 $V_{IL} = 0.8$ V max., $V_{IH} = 2$ V min.
CMOS input compatibility
 $I_I \leq 1 \mu A$ @ V_{OL} , V_{OH}
- Alternate Source is Philips/Sigmetics

The RCA CD54/74HC/HCT4316 contains four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

In addition these devices contain logic-level translation circuits that provide for analog signal switching of voltages between ± 5 V via 5 V logic. Each switch is turned on by a high-level voltage on its select input (S) when the common Enable (E) is Low. A High E disables all switches. The digital inputs can swing between V_{CC} and Gnd; the analog inputs/outputs can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. Voltage ranges are shown in Figs. 2 and 3.

The CD54HC4316 and CD54HCT4316 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4316 and CD74HCT4316 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

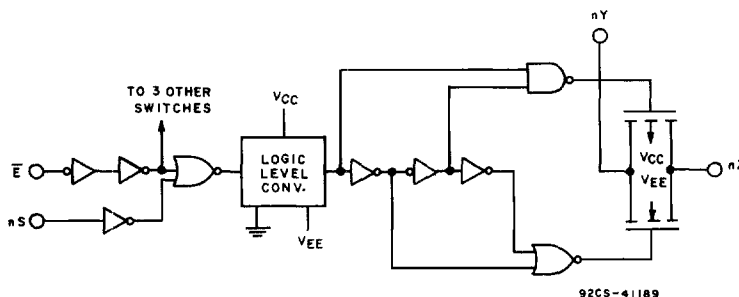


Fig. 1 - Logic diagram (one switch).

TRUTH TABLE

INPUTS		SWITCH
\bar{E}	S	
L	L	OFF
L	H	ON
H	X	OFF

H = High Level Voltage
L = Low Level Voltage
X = Don't Care

CD54/74HC4316 CD54/74HCT4316

MAXIMUM RATINGS, Absolute-Maximum Values: (All voltages referenced to Gnd unless otherwise shown)

DC SUPPLY-VOLTAGE ($V_{CC}-V_{EE}$)	-0.5 to +10.5 V
DC SUPPLY-VOLTAGE (V_{CC})	-0.5 to +7 V
DC SUPPLY-VOLTAGE (V_{EE})	+0.5 to -7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V)	± 20 mA
DC SWITCH DIODE CURRENT, I_{OK} (FOR $V_i < V_{EE} - 0.5$ V OR $V_i > V_{CC} + 0.5$ V)	± 20 mA
DC SWITCH CURRENT (FOR $V_i > V_{EE} - 0.5$ V OR $V_i < V_{CC} + 0.5$ V)	± 25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	± 50 mA
DC V_{EE} CURRENT (I_{EE})	-20 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at $8\text{ mW}/^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F, H)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F, H)	Derate Linearly at $8\text{ mW}/^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at $6\text{ mW}/^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+125^\circ\text{C}$
STORAGE TEMPERATURE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$
Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm) with solder contacting lead tips only	$+300^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A =Full Package-Temperature Range) V_{CC}^*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
Supply-Voltage Range (For T_A =Full Package-Temperature Range) $V_{CC}-V_{EE}$	2	10	V
CD54/74HC Types, CD54/74HCT Types, See Fig. 2			
Supply-Voltage Range (For T_A =Full Package-Temperature Range) V_{EE}^*	0	-6	V
CD54/74HC Types, CD54/74HCT, See Fig. 3			
DC Input Control Voltage, V_i	Gnd	V_{CC}	V
Analog Switch I/O Voltage, V_{IS}	V_{EE}	V_{CC}	V
Operating Temperature, T_A :			
CD74 Types	-40	+125	$^\circ\text{C}$
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r, t_f :			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

Recommended Operating Area as a Function of Supply Voltages

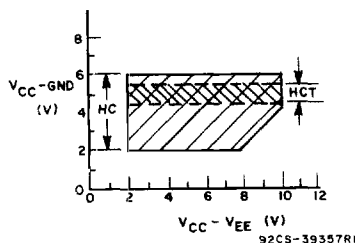


Fig. 2

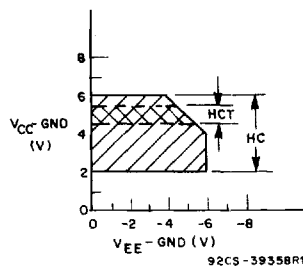


Fig. 3

CD54/74HC4316

CD54/74HCT4316

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25° C, Input t_r,t_f=6 ns)

CHARACTERISTIC	C _L (pF)	TYPICAL VALUES		UNITS
		HC	HCT	
Turn "ON" Time E̅ to Out nS to Out t _{PZH}	15	17	18	ns
		14	17	
Turn "ON" Time E̅ to Out nS to Out t _{PZL}		17	24	
		14	18	
Turn "OFF" Time E̅ to Out nS to Out t _{PLZ} , t _{PHZ}		17	21	
		14	18	
Power Dissipation Capacitance* C _{PD}	—	42	47	pF

*C_{PD} is used to determine the dynamic power consumption, per package.

$$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + C_S) V_{CC}^2 f_o \text{ where}$$

f_i = input frequency

f_o = output frequency

C_L = output load capacitance

C_S = switch capacitance

V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	V _{EE}	V _{CC}	LIMITS										UNITS				
			25° C				-40° C to +85° C				-55° C to +125° C						
			HC		HCT		74HC		74HCT		54HC			54HCT			
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		Min.	Max.		
Propagation Delay Switch In to Out t _{PLH} t _{PHL}	0	2	—	60	—	—	—	75	—	—	—	90	—	—	ns		
			0	4.5	—	12	—	12	—	15	—	15	—	18		—	
			0	6	—	10	—	—	—	13	—	—	—	15		—	
			-4.5	4.5	—	8	—	8	—	10	—	10	—	12		—	
Turn "ON" Time E̅ to Out t _{PZH} t _{PZL}	0	2	—	205	—	—	—	255	—	—	—	310	—	—	ns		
			0	4.5	—	41	—	44	—	51	—	55	—	62		—	
			0	6	—	35	—	—	—	43	—	—	—	53		—	
			-4.5	4.5	—	37	—	42	—	47	—	53	—	56		—	
	0	2	—	205	—	—	—	255	—	—	—	310	—	—			
			0	4.5	—	41	—	56	—	51	—	70	—	62		—	
			0	6	—	35	—	—	—	43	—	—	—	53		—	
			-4.5	4.5	—	37	—	42	—	47	—	53	—	56		—	
	Turn "ON" Time nS to Out t _{PZH} t _{PZL}	0	2	—	175	—	—	—	220	—	—	—	265	—		—	
				0	4.5	—	35	—	40	—	44	—	53	—		60	
				0	6	—	30	—	—	—	37	—	—	—		45	—
				-4.5	4.5	—	34	—	34	—	43	—	43	—		51	—
0		2	—	175	—	—	—	220	—	—	—	265	—	—			
			0	4.5	—	35	—	50	—	44	—	63	—	53	—		
			0	6	—	30	—	—	—	37	—	—	—	45	—		
			-4.5	4.5	—	34	—	34	—	43	—	43	—	51	—		
Turn "OFF" Time E̅ to Out t _{PLZ} , t _{PHZ}		0	2	—	205	—	—	—	255	—	—	—	310	—	—		
				0	4.5	—	41	—	50	—	51	—	63	—	62	—	
				0	6	—	35	—	—	—	43	—	—	—	53	—	
				-4.5	4.5	—	37	—	46	—	47	—	58	—	56	—	
Turn "OFF" Time nS to Out t _{PLZ} , t _{PHZ}	0	2	—	175	—	—	—	220	—	—	—	265	—	—			
			0	4.5	—	35	—	44	—	44	—	55	—	53	—		
			0	6	—	30	—	—	—	37	—	—	—	45	—		
			-4.5	4.5	—	34	—	40	—	43	—	50	—	51	—		
Input (Control) Capacitance C _I	—	—	—	10	—	10	—	10	—	10	—	10	—	pF			

CD54/74HC4316 CD54/74HCT4316

ANALOG CHANNEL CHARACTERISTICS - Typical Values at $T_A = 25^\circ\text{C}$

CHARACTERISTIC	TEST CONDITIONS	V _{CC} V	HC	HCT	UNITS
Switch Frequency Response Bandwidth at -3 dB (Fig. 15)	Fig. 6 Notes 1 and 2	4.5	>200	>200	MHz
Crosstalk Between Any Two Switches (Fig. 16)	Fig. 7 Notes 2 and 3	4.5	TBE	TBE	dB
Total Harmonic Distortion	1 kHz, Fig. 8	$V_{IS}=4 V_{PP}$	0.078	0.078	%
		$V_{IS}=8 V_{PP}$	0.018	0.018	
Control to Switch Feedthrough Noise	Fig. 9	4.5	TBE	TBE	mV
		9	TBE	TBE	
Switch "OFF" Signal Feedthrough (Fig. 16)	Fig. 10 Notes 2 and 3	4.5	-62	-62	dB
Switch Input Capacitance	C _S	—	5	5	pF

Notes:

1. Adjust input level for 0 dBm at output, $f = 1$ MHz.
2. V_{IS} is centered at $V_{CC}/2$.
3. Adjust input for 0 dBm at V_{IS} .

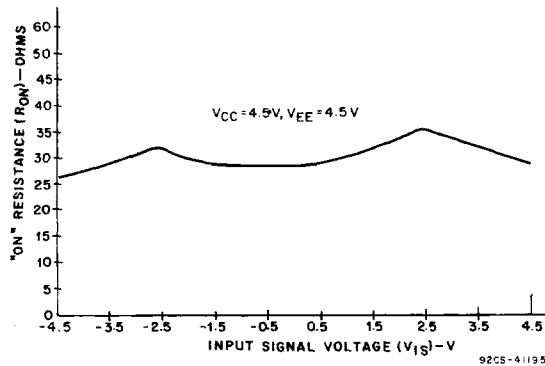


Fig. 4 - Typical "ON" resistance vs. input signal voltage.

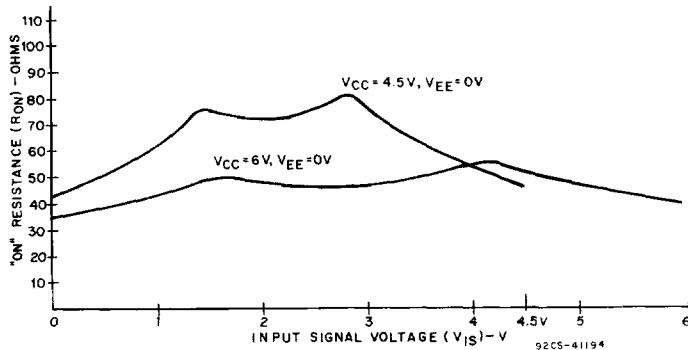


Fig. 5 - Typical "ON" resistance vs. input signal voltage.

CD54/74HC4316 CD54/74HCT4316

ANALOG TEST CIRCUITS

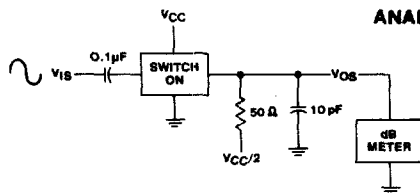


Fig. 6 - Frequency response test circuit.

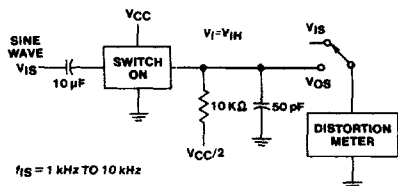


Fig. 8 - Total harmonic distortion test circuit.

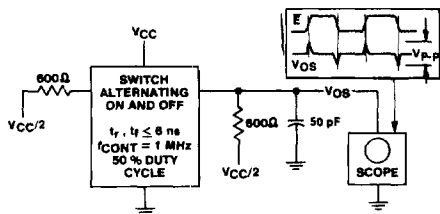


Fig. 9 - Control-to-switch feedthrough noise test circuit.

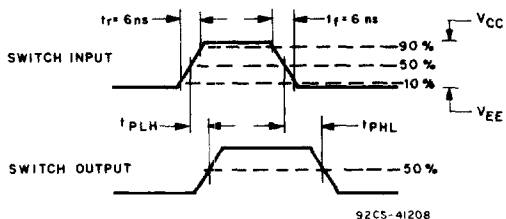


Fig. 11 - Switch propagation - delay times waveforms.

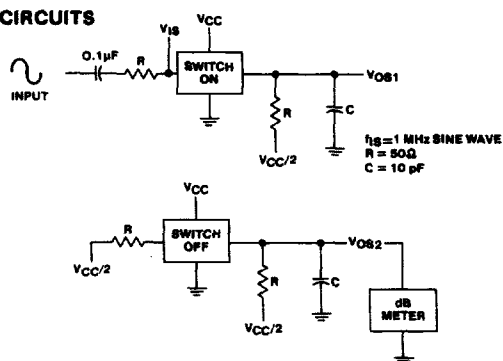


Fig. 7 - Crosstalk between two switches test circuit.

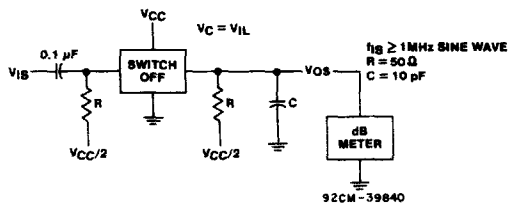


Fig. 10 - Switch off signal feedthrough.

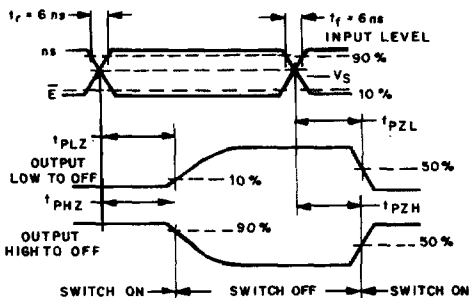


Fig. 12 - Switch turn-on and turn-off propagation delay times waveforms.

	54/74HC	54/74HCT
Input Level	V _{CC}	3 V
Switching Voltage, V _s	50% V _{CC}	1.3 V

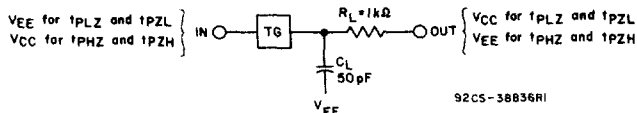


Fig. 13 - Switch on/off propagation delay time test circuit.

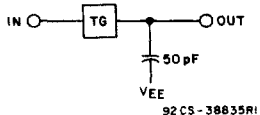


Fig. 14 - Switch-in to switch-out propagation delay time test circuit.

CD54/74HC4316 CD54/74HCT4316

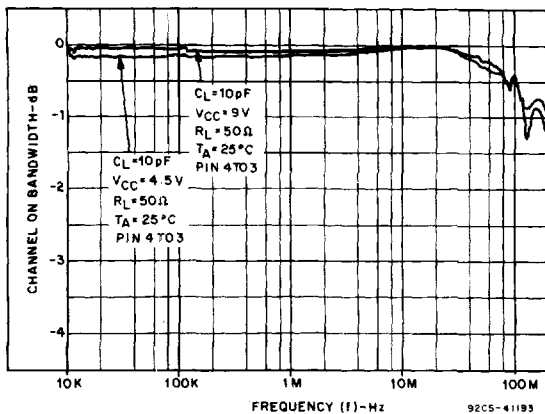


Fig. 15 - Switch frequency response.

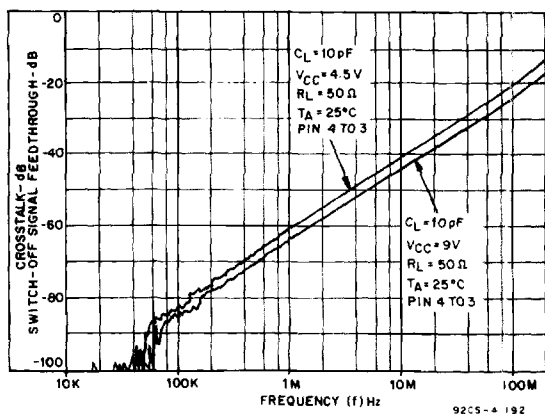


Fig. 16 - Switch-off signal feedthrough and crosstalk vs. frequency.