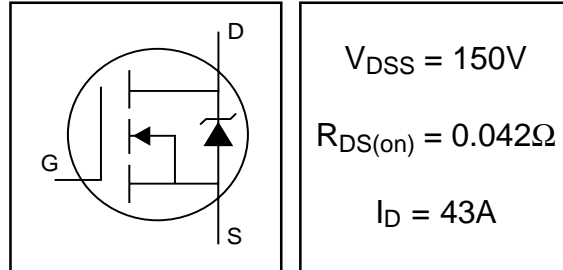


IRFP3415PbF

HEXFET® Power MOSFET

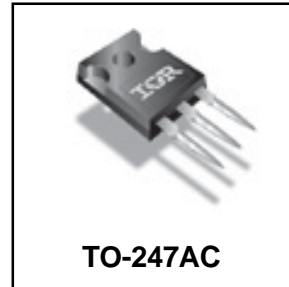
- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free



Description

Fifth Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.



Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---------------------------------|---|-----------------------|-------|
| $I_D @ T_C = 25^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ | 43 | A |
| $I_D @ T_C = 100^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ | 30 | |
| I_{DM} | Pulsed Drain Current ① | 150 | |
| $P_D @ T_C = 25^\circ\text{C}$ | Power Dissipation | 200 | W |
| | Linear Derating Factor | 1.3 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| E_{AS} | Single Pulse Avalanche Energy ② | 590 | mJ |
| I_{AR} | Avalanche Current ③ | 22 | A |
| E_{AR} | Repetitive Avalanche Energy ④ | 20 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ⑤ | 5.0 | V/ns |
| T_J T_{STG} | Operating Junction and Storage Temperature Range | -55 to + 175 | °C |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case) | |
| | Mounting torque, 6-32 or M3 screw | 10 lbf•in (1.1N•m) | |

Thermal Resistance

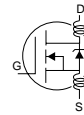
| | Parameter | Typ. | Max. | Units |
|-----------------|-------------------------------------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case | — | 0.75 | °C/W |
| $R_{\theta CS}$ | Case-to-Sink, Flat, Greased Surface | 0.24 | — | |
| $R_{\theta JA}$ | Junction-to-Ambient | — | 40 | |

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------------------------|--------------------------------------|------|------|-------|----------|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 150 | — | — | V | $V_{GS} = 0V, I_D = 250\mu A$ |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.17 | — | V/°C | Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 0.042 | Ω | $V_{GS} = 10V, I_D = 22A$ ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS} = V_{GS}, I_D = 250\mu A$ |
| g_{fs} | Forward Transconductance | 19 | — | — | S | $V_{DS} = 50V, I_D = 22A$ |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | 25 | μA | $V_{DS} = 150V, V_{GS} = 0V$ |
| | | — | — | 250 | | $V_{DS} = 120V, V_{GS} = 0V, T_J = 150^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS} = 20V$ |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS} = -20V$ |
| Q_g | Total Gate Charge | — | — | 200 | nC | $I_D = 22A$ |
| Q_{gs} | Gate-to-Source Charge | — | — | 17 | | $V_{DS} = 120V$ |
| Q_{gd} | Gate-to-Drain ("Miller") Charge | — | — | 98 | | $V_{GS} = 10V$, See Fig. 6 and 13 ④ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 12 | — | ns | $V_{DD} = 75V$ |
| t_r | Rise Time | — | 55 | — | | $I_D = 22A$ |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 71 | — | | $R_G = 2.5\Omega$ |
| t_f | Fall Time | — | 69 | — | | $R_D = 3.3\Omega$, See Fig. 10 ④ |
| L_D | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6mm (0.25in.) from package and center of die contact |
| L_S | Internal Source Inductance | — | 7.5 | — | | |
| C_{iss} | Input Capacitance | — | 2400 | — | pF | $V_{GS} = 0V$ |
| C_{oss} | Output Capacitance | — | 640 | — | | $V_{DS} = 25V$ |
| C_{rss} | Reverse Transfer Capacitance | — | 340 | — | | $f = 1.0\text{MHz}$, See Fig. 5 |



Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------|---|------|------|------|---------|---|
| I_S | Continuous Source Current (Body Diode) | — | — | 43 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| I_{SM} | Pulsed Source Current (Body Diode) ① | — | — | 150 | | |
| V_{SD} | Diode Forward Voltage | — | — | 1.3 | V | $T_J = 25^\circ\text{C}, I_S = 22A, V_{GS} = 0V$ ④ |
| t_{rr} | Reverse Recovery Time | — | 260 | 390 | ns | $T_J = 25^\circ\text{C}, I_F = 22A$ |
| Q_{rr} | Reverse Recovery Charge | — | 2.2 | 3.3 | μC | $di/dt = 100A/\mu s$ ④ |

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② $V_{DD} = 25V$, starting $T_J = 25^\circ\text{C}$, $L = 2.4\text{mH}$
 $R_G = 25\Omega, I_{AS} = 22A$. (See Figure 12)
- ③ $I_{SD} \leq 22A, di/dt \leq 820A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

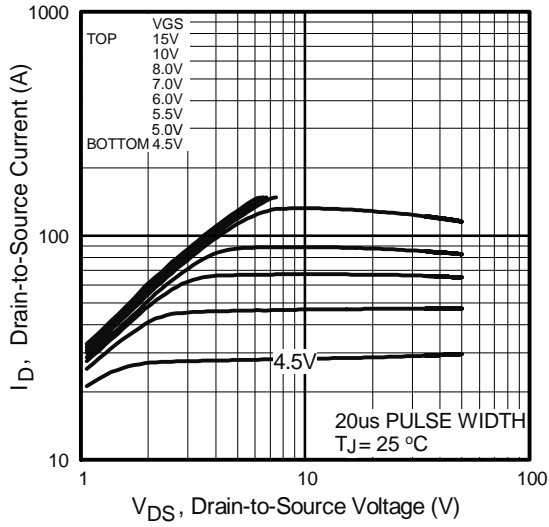


Fig 1. Typical Output Characteristics

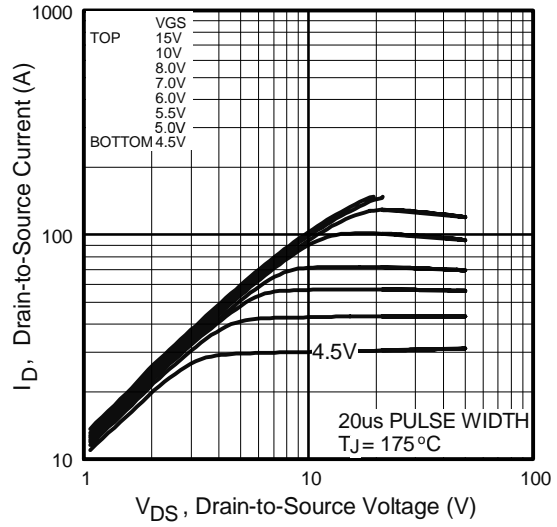


Fig 2. Typical Output Characteristics

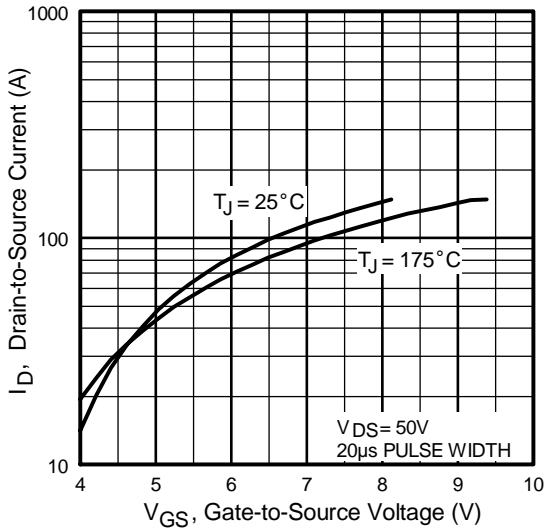


Fig 3. Typical Transfer Characteristics

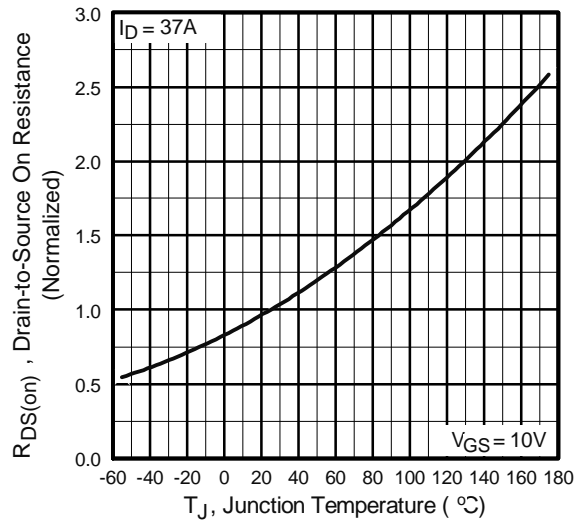


Fig 4. Normalized On-Resistance Vs. Temperature

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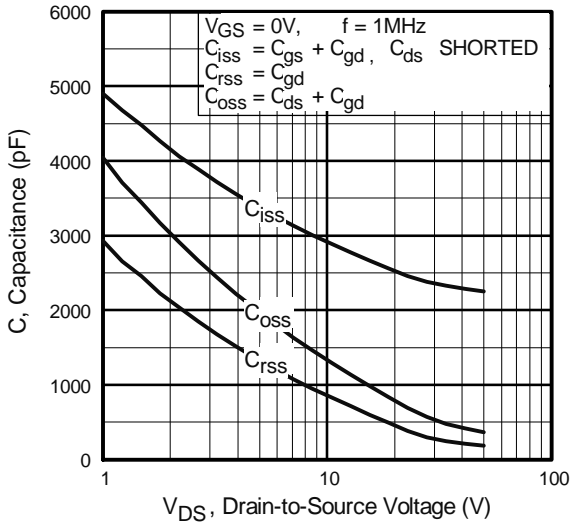


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

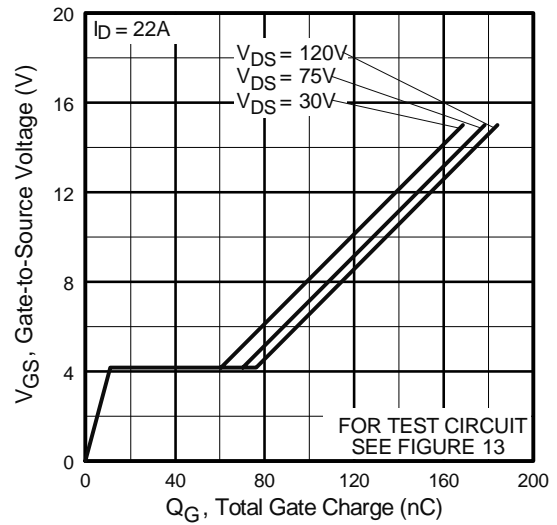


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

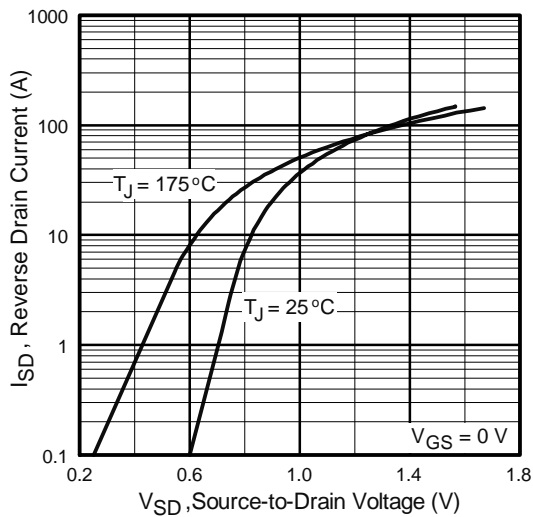


Fig 7. Typical Source-Drain Diode Forward Voltage

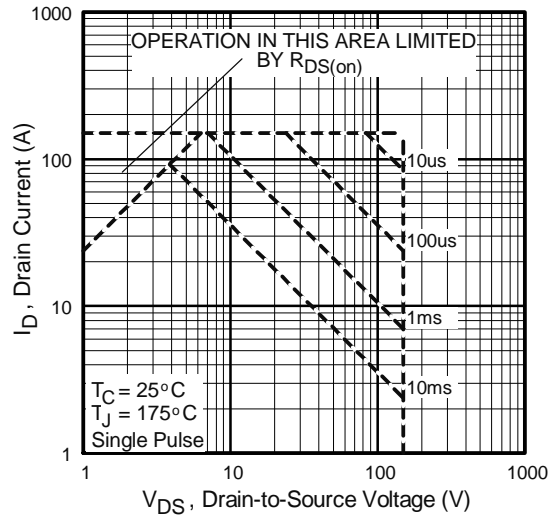


Fig 8. Maximum Safe Operating Area

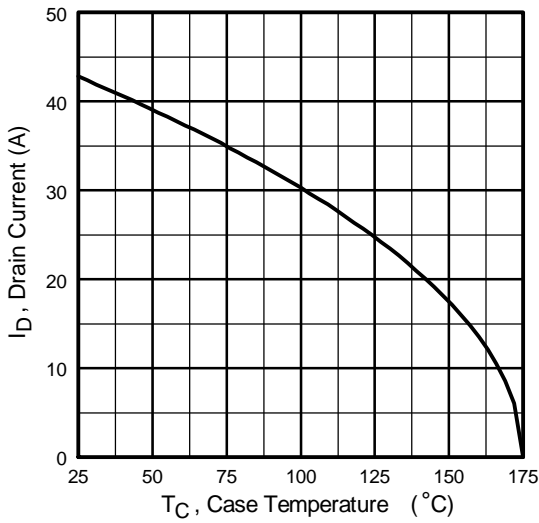


Fig 9. Maximum Drain Current Vs. Case Temperature

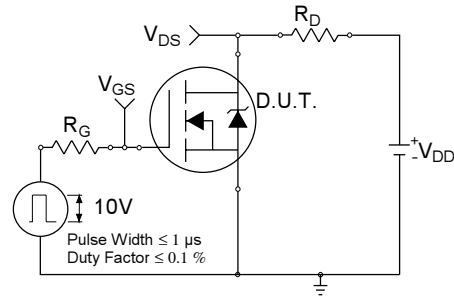


Fig 10a. Switching Time Test Circuit

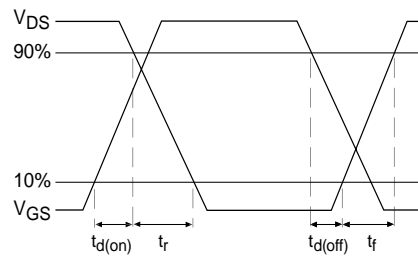


Fig 10b. Switching Time Waveforms

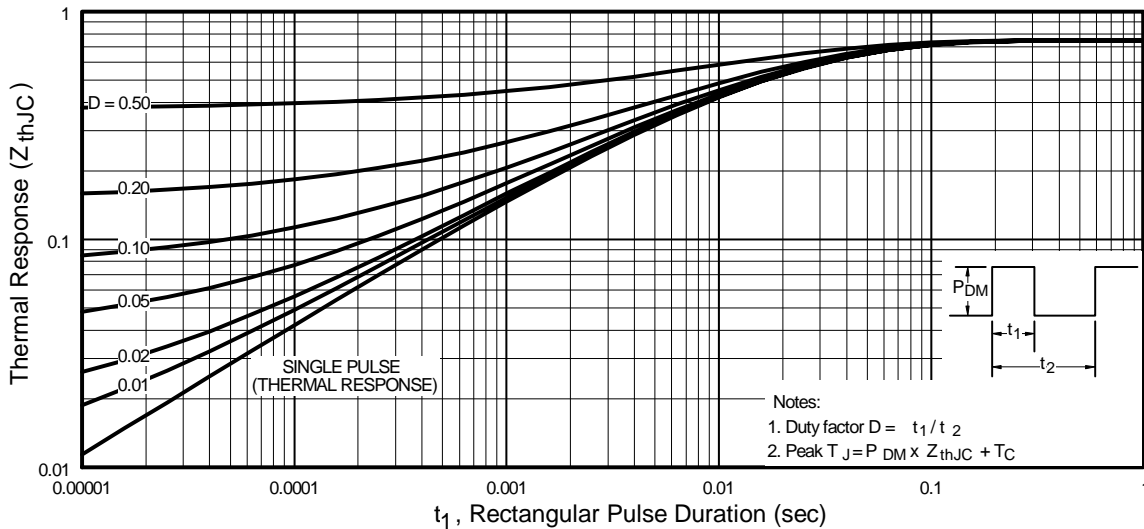


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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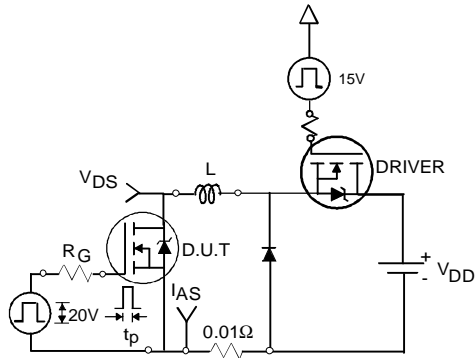


Fig 12a. Unclamped Inductive Test Circuit

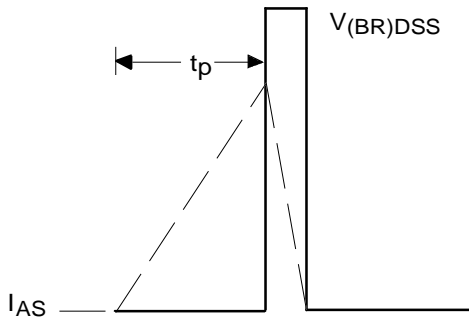


Fig 12b. Unclamped Inductive Waveforms

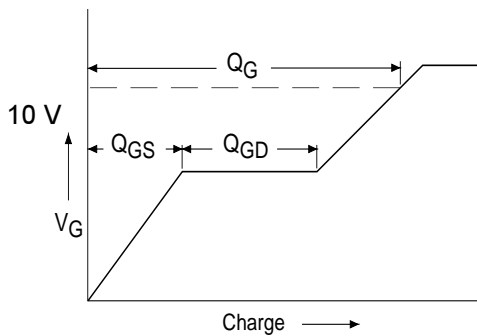


Fig 13a. Basic Gate Charge Waveform

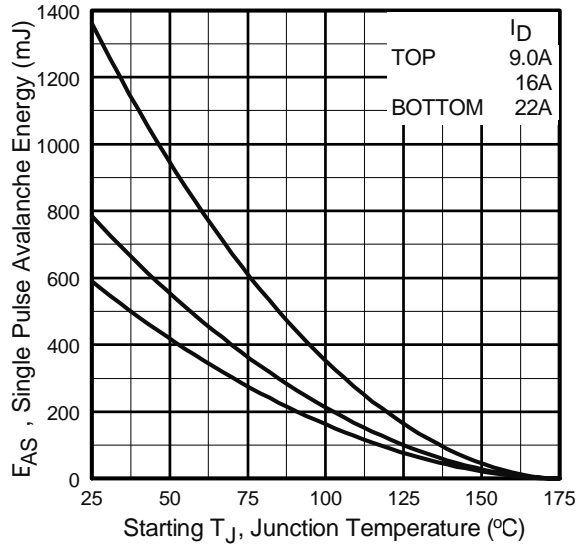


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

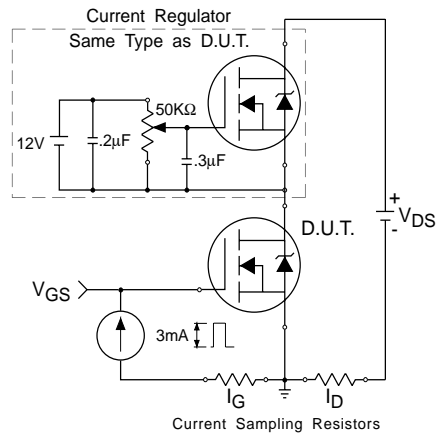
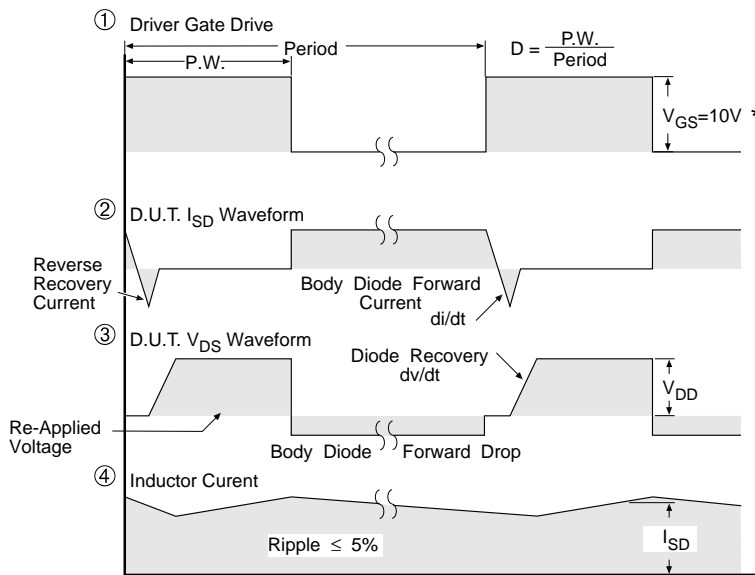
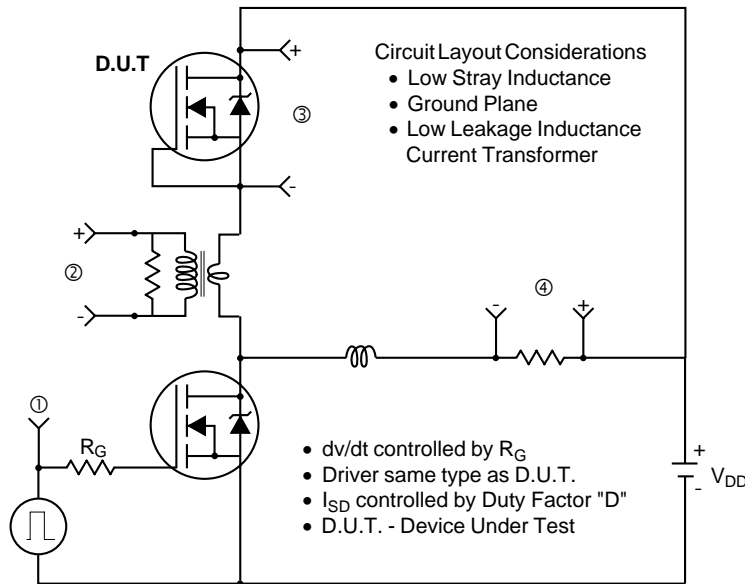


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

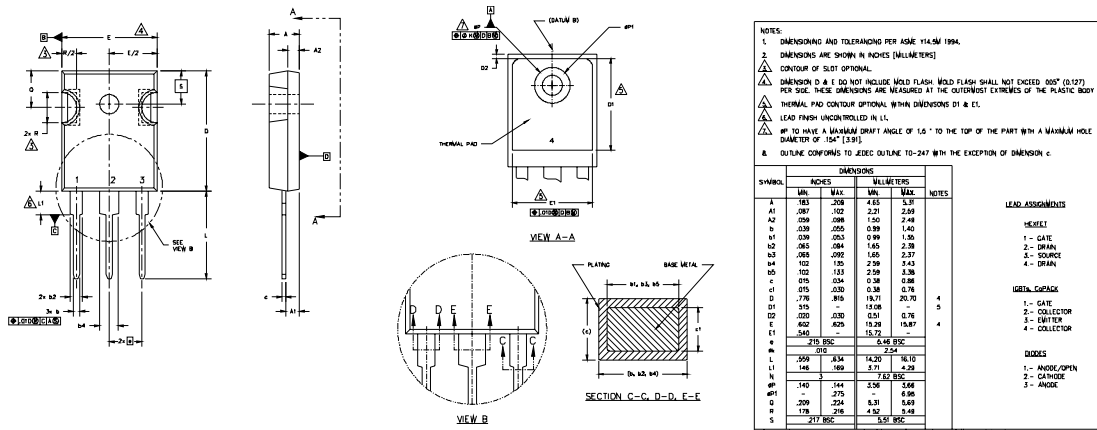
Fig 14. For N-Channel HEXFET® Power MOSFETs

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TO-247AC Package Outline

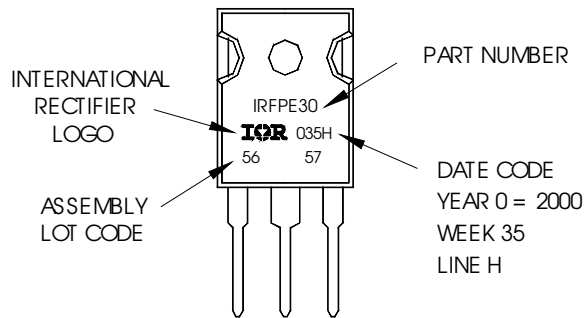
Dimensions are shown in millimeters (inches)



TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFP3415
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line
position indicates "Lead-Free"



Data and specifications subject to change without notice.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>

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