Low Power, High Output Current, Dual-Port ADSL/ADSL2+ Line Driver

AD8396

FEATURES

- 2 differential DSL channels comprised of current feedback, high output current amplifiers
- Integrated feedback and gain resistors
- Integrated biasing network
- Ideal for use as ADSL/ADSL2+ dual-channel Central Office (CO) line drivers
- Low power consumption
  - Dual-supply operation from ±6 V to ±12 V
  - Single-supply operation from 12 V to 24 V
  - 10.8 mA quiescent supply current in full power mode
  - 1.4 mA quiescent supply current in shutdown mode
  - Less than 700 mW internal power dissipation while driving 20.4 dBm line power, 1:1 transformer
- High output voltage and current drive
  - 43.4 V p-p differential output voltage
- Low distortion
  - −66 dBc typical MTPR @ 20.4 dBm, 26 kHz to 2.2 MHz
- High speed: 170 V/µs differential slew rate

APPLICATIONS

- ADSL/ADSL2+ CO line drivers

GENERAL DESCRIPTION

The AD8396 is comprised of four high output current, low power consumption operational amplifiers. It is particularly well suited for the CO driver interface in digital subscriber line systems, such as ADSL and ADSL2+. The driver can deliver 20.4 dBm to a line while compensating for losses due to hybrid insertion and back-termination resistors.

The low power consumption, high output current, high output voltage swing, and robust thermal packaging enable the AD8396 to be used as the CO line driver in ADSL and other xDSL systems.

The AD8396 is available in a 4 mm × 4 mm 16-lead LFCSP.

PIN CONFIGURATION

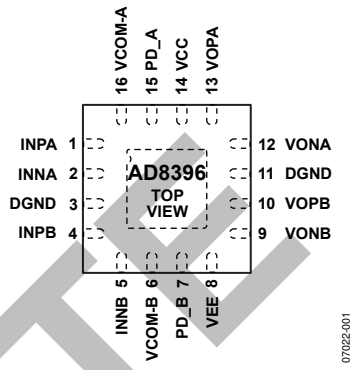

Figure 1.

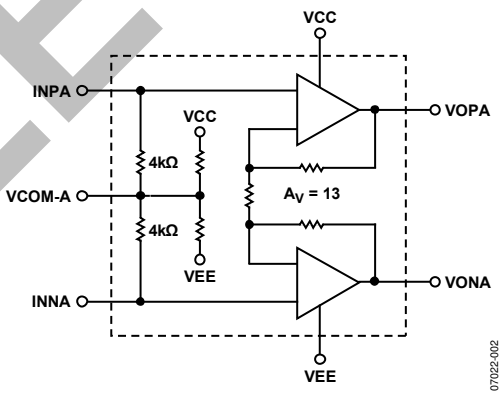

Figure 2. Channel A Internal Schematics

Rev. C

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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REVISION HISTORY

8/09—Revision C: Initial Version

SPECIFICATIONS

(V_{CC} – V_{EE}) = 24 V, R_L = 100 Ω, G_{DIFF} = 13 (fixed), PD = (0), T = 25°C, typical DSL application circuit, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
−3 dB Small-Signal Bandwidth		8		MHz	V_{OUT} = 0.1 V p-p, differential
−3 dB Large-Signal Bandwidth		8		MHz	V_{OUT} = 2 V p-p, differential
Slew Rate		170		V/µs	V_{OUT} = 4 V p-p, differential
Differential Gain	12.8	13	13.2	V/V	
NOISE/DISTORTION PERFORMANCE					
Second Harmonic Distortion		−90		dBc	f_C = 2 MHz, V_{OUT} = 2 V p-p, differential
Third Harmonic Distortion		−62		dBc	f_C = 2 MHz, V_{OUT} = 2 V p-p, differential
Multitone Input Power Ratio (MTPR)		−66		dBc	26 kHz to 2.2 MHz, Z_{LINE} = 100 Ω, differential load
Differential Output Noise		140		nV/√Hz	f = 10 kHz
INPUT CHARACTERISTICS					
RTO Offset Voltage	−15	−0.7	+15	mV	Single-ended
	−15	+0.3	+15	mV	Differential
RTO Offset Voltage @ PD = (1)	−30	+0.1	+30	mV	Differential
Input Bias Current	−5	−1.5	+5	µA	
Input Resistance		8		kΩ	Differential
Input Capacitance		1		pF	Differential
OUTPUT CHARACTERISTICS					
Differential Output Voltage Swing	42.6	43.4	44	V p-p	ΔV_{OUT}, R_L = 100 Ω
Single-Ended Output Voltage Swing	21.3	21.7	22	V p-p	ΔV_{OUT}, R_L = 50 Ω
Output Leakage Current	−100		+100	µA	PD = (1)
POWER SUPPLY					
Operating Range, Dual Supply	±6		±12	V	
Operating Range, Single Supply	12		24	V	
Total Quiescent Current					
PD = (0)	9.0	10.8	13.0	mA	
PD = (1) Shutdown State	0	1.4	3.0	mA	
Common-Mode Voltage	−10	+0.2	+10	mV	V_{CM}
PD = (0) Threshold			0.8	V	(0) = 0 V
PD = (1) Threshold	1.6			V	(1) = 5 V
PD = (0) Input Current	−100	−47	+100	µA	(0) = 0 V
PD = (1) Input Current	−100	+1	+100	µA	(1) = 5 V
+Power Supply Rejection Ratio		−80	−60	dB	$\Delta V_{OS, DM (RTI)}/\Delta V_{CC}$, ΔV_{CC} = ±1 V, differential
−Power Supply Rejection Ratio		−80	−60	dB	$\Delta V_{OS, DM (RTI)}/\Delta V_{EE}$, ΔV_{EE} = ±1 V, differential

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, $V_{CC} - V_{EE}$	26.4 V
Power Dissipation	See Figure 3
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified in still air with exposed pad soldered to 4-layer JEDEC test board. θ_{JC} is specified at the exposed pad.

Table 3.

Package Type	θ_{JA}	θ_{JC}	Unit
16-Lead LFCSP	56	9.1	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the AD8396 is limited by its junction temperature on the die.

The maximum safe junction temperature of plastic encapsulated devices, as determined by the glass transition temperature of the plastic, is 150°C. Exceeding this limit can temporarily cause a shift in the parametric performance due to a change in the stresses exerted on the die by the package. Exceeding this limit for an extended period can result in device failure.

Figure 3 shows the maximum power dissipation in the package vs. the ambient temperature for the 16-lead LFCSP on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

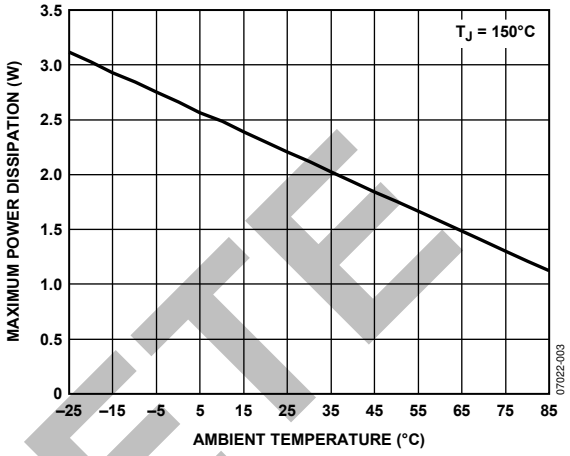


Figure 3. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming that the load R_L is referenced to midsupply, the total drive power is $V_S/2 \times I_{OUT}$, part of which is dissipated in the package and part in the load ($V_{OUT} \times I_{OUT}$).

RMS output voltages should be considered. If R_L is referenced to V_{EE}, as in single-supply operation, the total power is $V_S \times I_{OUT}$.

In single supply with R_L to V_{EE}, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more copper in direct contact with the package leads from PCB traces, through-holes, ground, and power planes reduces θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

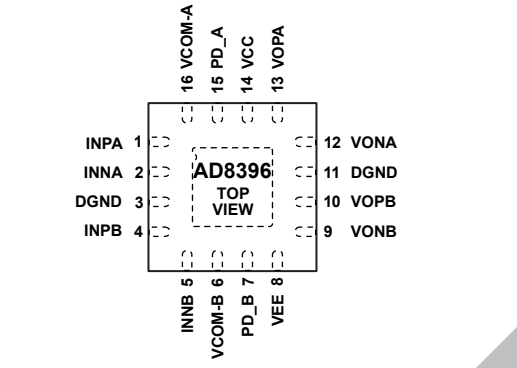


Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INPA	Port A Input P
2	INNA	Port A Input N
3, 11	DGND	Ground
4	INPB	Port B Input P
5	INNB	Port B Input N
6	VCOM-B	Port B Bias
7	PD_B	Port B Shutdown
8	VEE	Negative Power Supply
9	VONB	Port B Output N
10	VOPB	Port B Output P
12	VONA	Port A Output N
13	VOPA	Port A Output P
14	VCC	Positive Power Supply
15	PD_A	Port A Shutdown
16	VCOM-A	Port A Bias
Exposed Pad		No Connection

TYPICAL PERFORMANCE CHARACTERISTICS

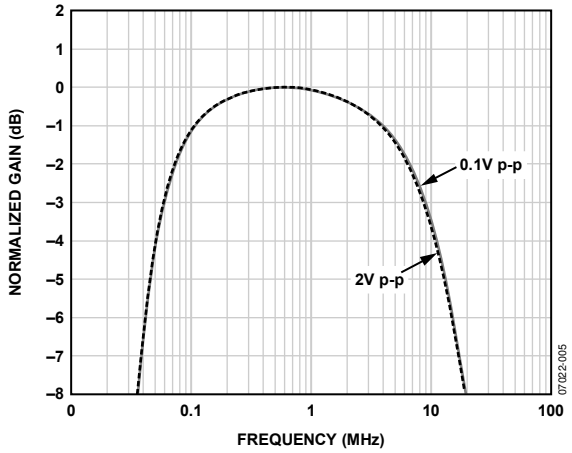


Figure 5. Differential Gain vs. Frequency, R_L = 100 Ω

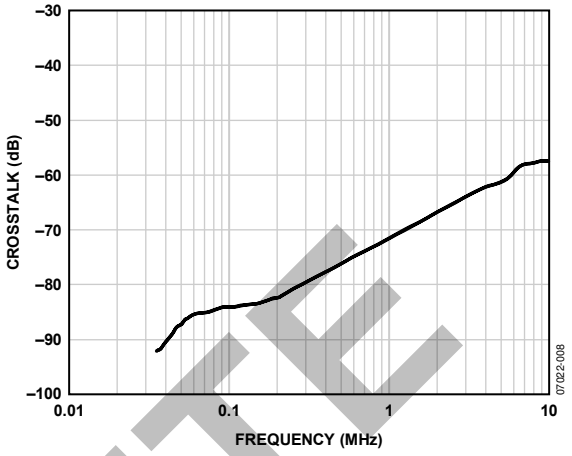


Figure 8. Crosstalk vs. Frequency, Typical ADSL/ADSL2+ Application Circuit, V_{OUT} = 2 V p-p, R_L = 100 Ω

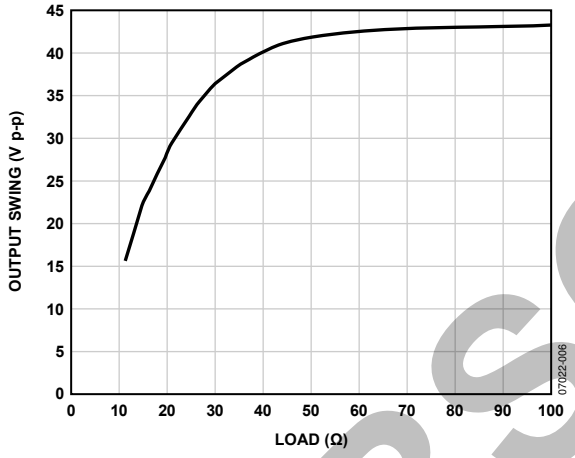


Figure 6. DC Differential Output Swing vs. Load

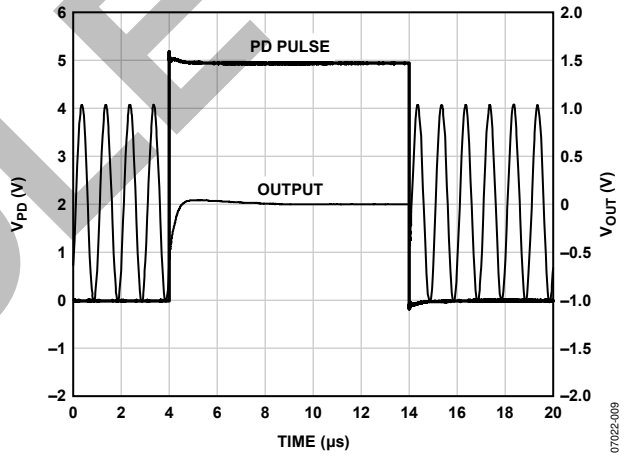


Figure 9. Power-Down/Power-Up Transition

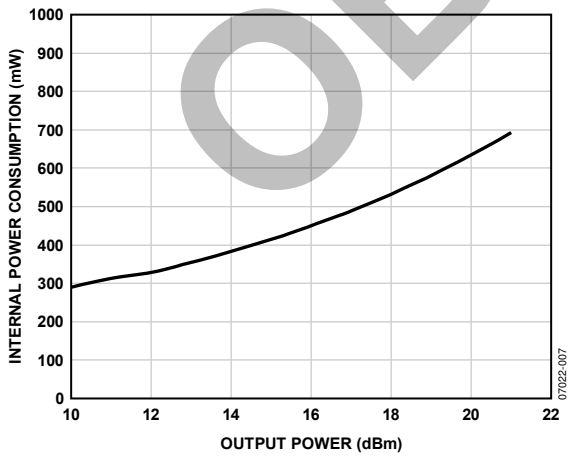


Figure 7. Internal Power Consumption vs. Output Power, Typical ADSL/ADSL2+ Application Circuit, 100 Ω Resistive Load Only

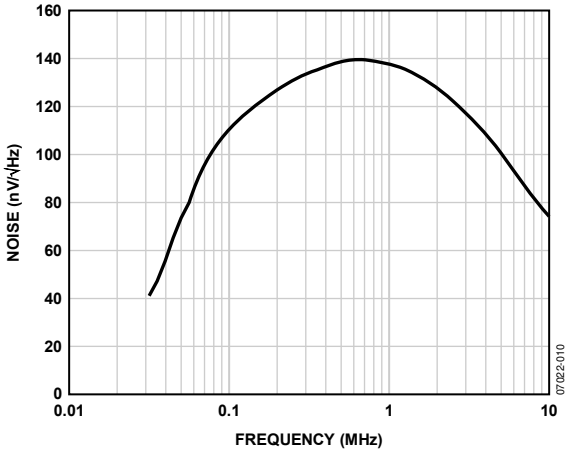


Figure 10. Differential Output Noise vs. Frequency, Typical ADSL/ADSL2+ Application Circuit

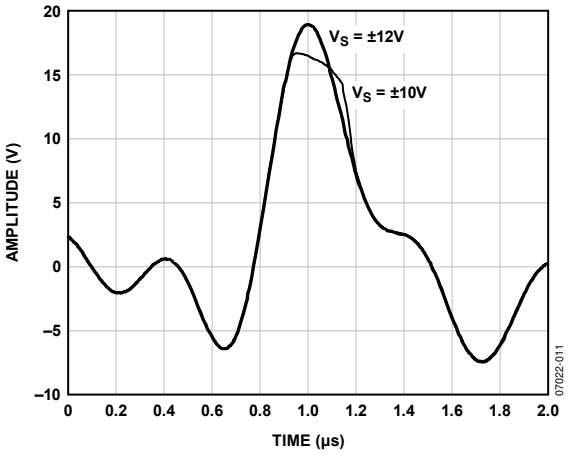


Figure 11. Output Overdrive Recovery, Typical ADSL/ADSL2+ Application Circuit, V_{OUT} = 3.3 V_{RMS}, CF = 5.47, R_L = 100 Ω

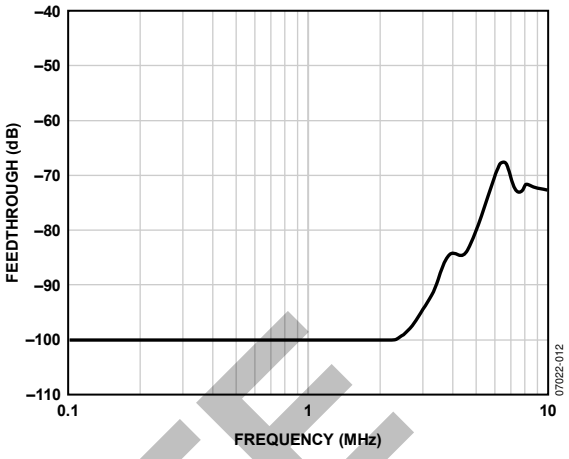


Figure 12. Feedthrough vs. Frequency, Typical ADSL/ADSL2+ Application Circuit, V_{OUT} = 2 V p-p, R_L = 100 Ω

THEORY OF OPERATION

The AD8396 is a current feedback amplifier with high output current capability. With a current feedback amplifier, the current into the inverting input is the feedback signal, and the open-loop behavior is that of a transimpedance, dV_O/dI_{IN} or T_Z.

The open-loop transimpedance is analogous to the open-loop voltage gain of a voltage feedback amplifier. Figure 13 shows a simplified model of a current feedback amplifier. Because R_{IN} is proportional to $1/g_m$, the equivalent voltage gain is $T_Z \times g_m$, where g_m is the transconductance of the input stage. Basic analysis of the follower with the gain circuit yields

$$\frac{V_O}{V_{IN}} = G \times \frac{T_Z(S)}{T_Z(S) + (G \times R_{IN}) + R_F}$$

where:
$G = 1 + R_F/R_G$
$R_{IN} = 1/g_m \approx 50\ \Omega$

Because $G \times R_{IN} << R_F$ for low gains, a current feedback amplifier has relatively constant bandwidth vs. gain. The 3 dB point is set when $|T_Z| = R_F$.

In a nonideal amplifier, there are additional poles that contribute excess phase, and there is a value for R_F below which the amplifier is unstable. Tolerance for peaking and desired flatness determines the optimum R_F in each application.

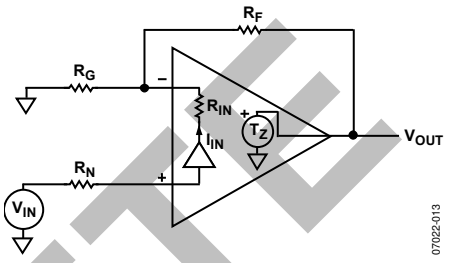


Figure 13. Simplified Block Diagram

APPLICATIONS INFORMATION

SUPPLIES, GROUNDING, AND LAYOUT

The AD8396 can be powered from either single or dual supplies, with the total supply voltage ranging from 12 V to 24 V. For optimum performance, use well-regulated low ripple supplies.

As with all high speed amplifiers, pay close attention to supply decoupling, grounding, and overall board layout. Provide low frequency supply decoupling with 10 µF tantalum capacitors from each supply to ground. In addition, decouple all supply pins with 0.1 µF quality ceramic chip capacitors placed as close as possible to the driver. Use an internal low impedance ground plane to provide a common ground point for all driver and decoupling capacitor ground requirements. Whenever possible, use separate ground planes for analog and digital circuitry.

Follow high speed layout techniques to minimize parasitic capacitance.

Keep input and output traces as short as possible and as far apart from each other as practical to minimize crosstalk. Keep all differential signal traces as symmetrical as possible.

POWER MANAGEMENT

A digitally programmable logic pin switches each port of the AD8396 between active bias and shutdown states. The PD_A pin controls Port A and the PD_B pin controls Port B. These pins can be controlled directly with either 3.3 V or 5 V CMOS logic with the DGND pins as a reference. If left unconnected, the PD pins float high, placing the amplifier in the shutdown state. See the Specifications section for the quiescent current for each of the available bias states.

TYPICAL ADSL/ADSL2+ APPLICATION

In a typical ADSL/ADSL2+ application, a differential line driver takes the signal from the analog front end (AFE) and drives it onto the twisted pair telephone line. Referring to the typical circuit representation in Figure 14, the differential input appears at V_{IN+} and V_{IN-} from the AFE, while the differential output is transformer coupled to the telephone line at TIP and RING. The common-mode operating point, generally midway between the supplies, is set internally and is available at VCOM.

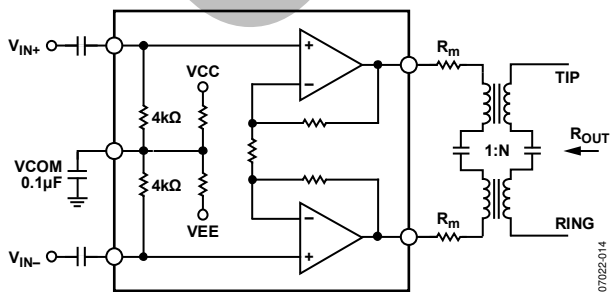


Figure 14. Typical ADSL/ADSL2+ Application Circuit

MULTITONE POWER RATIO (MTPR)

The DMT signal used in ADSL/ADSL2+ systems carries data in discrete tones or bins, which appear in the frequency domain in evenly spaced 4.3125 kHz intervals. In applications using this type of waveform, MTPR is a commonly used measure of linearity. Generally, designers are concerned with two types of MTPR: in-band and out-of-band. In-band MTPR is defined as the measured difference from the peak of one tone that is loaded with data to the peak of an adjacent tone that is intentionally left empty. Out-of-band MTPR is more loosely defined as the spurious emissions that occur in the receive band located between 25.875 kHz and the first downstream tone at 138 kHz. Figure 15 and Figure 16 show the AD8396 in-band MTPR for a 5.5 crest factor waveform for empty bins in the ADSL and extended ADSL2+ bandwidths.

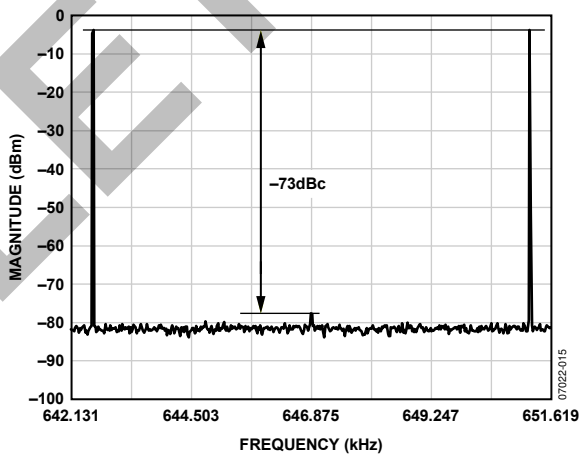


Figure 15. In-Band MTPR at 646.875 kHz

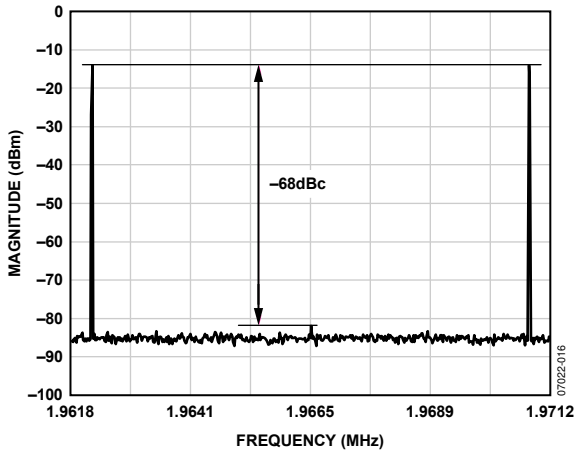
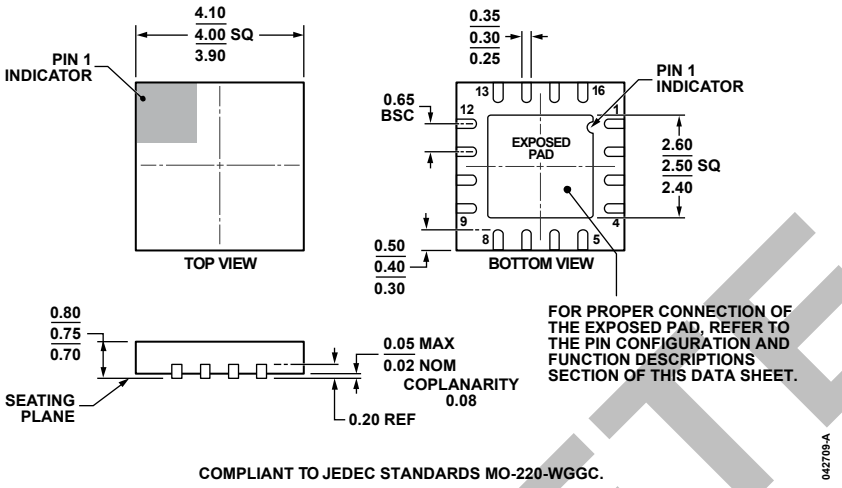


Figure 16. In-Band MTPR at 1.9665 MHz

LIGHTNING AND AC POWER FAULT

When the AD8396 is an ADSL/ADSL2+ line driver, it is transformer coupled to the twisted pair telephone line. In this environment, the AD8396 is subject to large line transients, resulting from events, such as lightning strikes or downed power lines. Additional circuitry is required to protect the AD8396 from damage due to these events.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 17. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm, Very Very Thin Quad
(CP-16-26)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8396ACPZ-R2[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-16-26
AD8396ACPZ-RL[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-16-26
AD8396ACPZ-R7[1]	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-16-26

[1] Z = RoHS Compliant Part.

NOTES

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