

# DATA SHEET

## **CBTD16212**

24-bit level shifting bus exchange switch  
with 12-bit output enables

Product data

2001 Sep 28

File under Integrated Circuits ICL03

# 24-bit level shifting bus exchange switch with 12-bit output enables

CBTD16212

## FEATURES

- 5 Ω switch connection between two ports
- TTL compatible control input levels
- Designed to be used in level shifting applications
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- ESD protection exceeds 1500 V HBM per JESD22-114A and 1000 V CDM per JESD22-C101

## DESCRIPTION

The CBTD16212 provides 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

A diode to  $V_{CC}$  is integrated into the circuit to allow for level shifting between 5 V inputs and 3.3 V outputs.

The CBTD16212 operates as 24-bit bus switch or a 12-bit bus exchanger, which provides data exchanging between the four signal ports via the data-select (S0–S2) terminals.

The CBT16212 is characterized for operation from –40 to +85 °C.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25\text{ °C}; GND = 0\text{ V}$	TYPICAL	UNIT
$t_{pd}$	Propagation delay An to Bn	$C_L = 50\text{ pF}; V_{CC} = 5\text{ V}$	0.25	ns
$C_{IN}$	Input capacitance	$V_I = 0\text{ V or }V_{CC}$	4.5	pF
$C_{OUT}$	Output capacitance	Outputs disabled; $V_O = 0\text{ V or }V_{CC}$	11.5	pF
$r_{on}$	A1 to A2	$V_{CC} = 5.5\text{ V}; V_I = 0\text{ V}$	5	Ω

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
56-Pin Plastic SSOP	–40 to +85 °C	CBTD16212DL	SOT371-1
56-Pin Plastic TSSOP	–40 to +85 °C	CBTD16212DGG	SOT364-1

### NOTE:

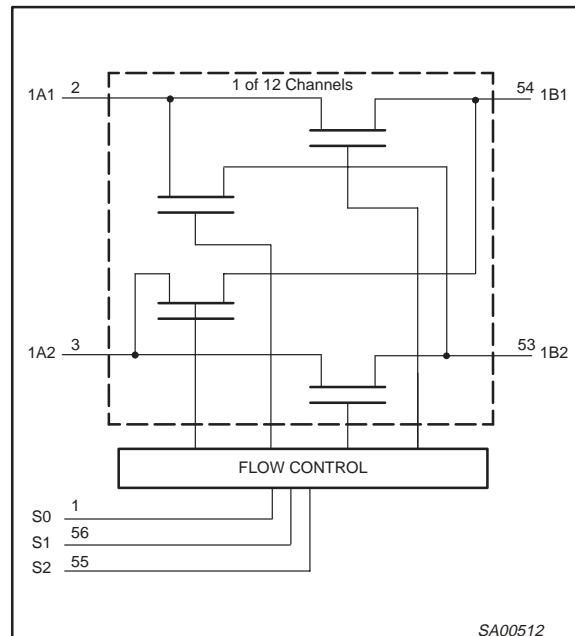
- Standard packing quantities and other packaging data is available at [www.philipslogic.com/support/packages](http://www.philipslogic.com/support/packages).

## FUNCTION TABLE

S2	S1	S0	A1	A2	FUNCTION
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 = B1
L	H	L	B2	Z	A1 = B2
L	H	H	Z	B1	A2 = B1
H	L	L	Z	B2	A2 = B2
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 = B1, A2 = B2
H	H	H	B2	B1	A1 = B2, A2 = B1

H = High voltage level  
L = Low voltage level  
Z = High impedance “off” state

## LOGIC SYMBOL

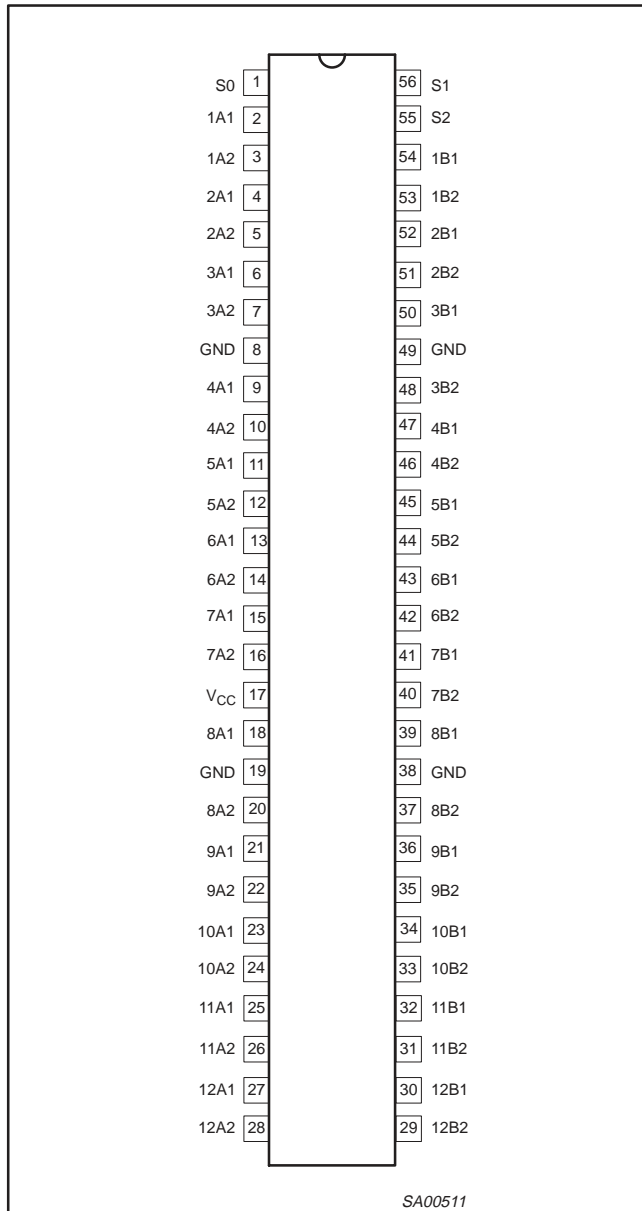


SA00512

# 24-bit level shifting bus exchange switch with 12-bit output enables

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## PIN CONFIGURATION



## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 56, 55	S0, S1, S2	Data select
2, 4, 6, 9, 11, 13, 15, 18, 21, 23, 25, 27	1A1–12A1	A1 channel
3, 5, 7, 10, 12, 14, 16, 20, 22, 24, 26, 28	1A2–12A2	A2 channel
54, 52, 50, 47, 45, 43, 41, 39, 36, 34, 32, 30	1B1, 12B1	B1 channel
53, 51, 48, 46, 44, 42, 40, 37, 35, 33, 31, 29	1B2, 12B2	B2 channel
8, 19, 38, 49	GND	Ground (0 V)
17	V <sub>CC</sub>	Positive supply voltage

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## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +7.0	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-50	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		-0.5 to +7.0	V
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	output in Off or High state	-0.5 to +5.5	V
I <sub>OUT</sub>	DC output current	output in Low state	128	mA
T <sub>stg</sub>	Storage temperature range		-65 to 150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V <sub>CC</sub>	DC supply voltage	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0	—	V
V <sub>IL</sub>	Low-level Input voltage	—	0.8	V
T <sub>amb</sub>	Operating free-air temperature range	-40	+85	°C

## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			T <sub>amb</sub> = -40 to +85 °C			
			Min	Typ <sup>1</sup>	Max	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.5 V; I <sub>I</sub> = -18 mA	—	—	-1.2	V
V <sub>P</sub>	Output high pass voltage	See Figure 1, page 6	—	—	-1.2	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> = 5.5 V	—	—	10	μA
		V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or 5.5 V	—	—	±1	
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	—	—	3.5	mA
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 5.5 V, one input at 3.4 V, other inputs at V <sub>CC</sub> or GND	—	—	2.5	mA
C <sub>I</sub>	Control pins	V <sub>I</sub> = 3 V or 0 V	—	4.5	—	pF
C <sub>IO(OFF)</sub>	Port OFF capacitance	V <sub>O</sub> = 3 V or 0 V; S <sub>0</sub> , S <sub>1</sub> , S <sub>2</sub> = 0 V	—	11.5	—	pF
r <sub>on</sub> <sup>3</sup>	A1 to A2	V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 0 V; I <sub>I</sub> = 64 mA	—	5	8	Ω
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 0 V; I <sub>I</sub> = 30 mA	—	5	8	
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 2.4 V; I <sub>I</sub> = 15 mA	—	16	35	

### NOTES:

- All typical values are at V<sub>CC</sub> = 5 V, T<sub>amb</sub> = 25 °C
- This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.
- Measured by the voltage drop between the A and the B terminals at the indicated current through the switch.  
On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

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## AC CHARACTERISTICS

GND = 0 V;  $t_R$ ;  $C_L = 50$  pF

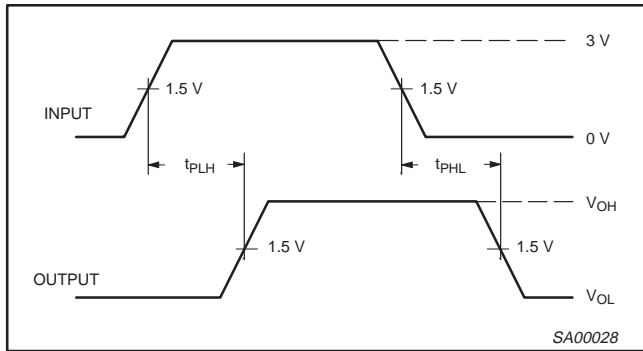
SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$		UNIT
				Min	Max	
$t_{pd}$	Propagation delay <sup>1</sup>	A or B	B or A	—	0.25	ns
$t_{en}$	Output enable time to High and Low level	S	A or B	2	11.5	ns
$t_{dis}$	Output disable time from High and Low level	S	A or B	1.5	8.5	ns

**NOTE:**

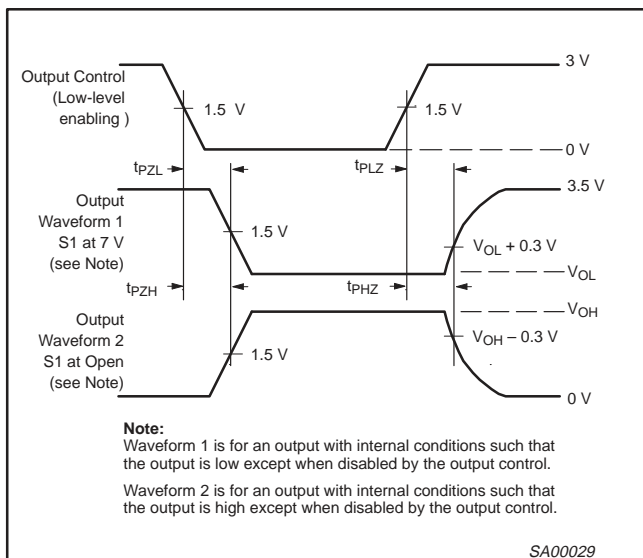
1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

## AC WAVEFORMS

$V_M = 1.5\text{ V}$ ,  $V_{IN} = \text{GND to } 3.0\text{ V}$



Waveform 1. Input (An) to Output (Yn) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

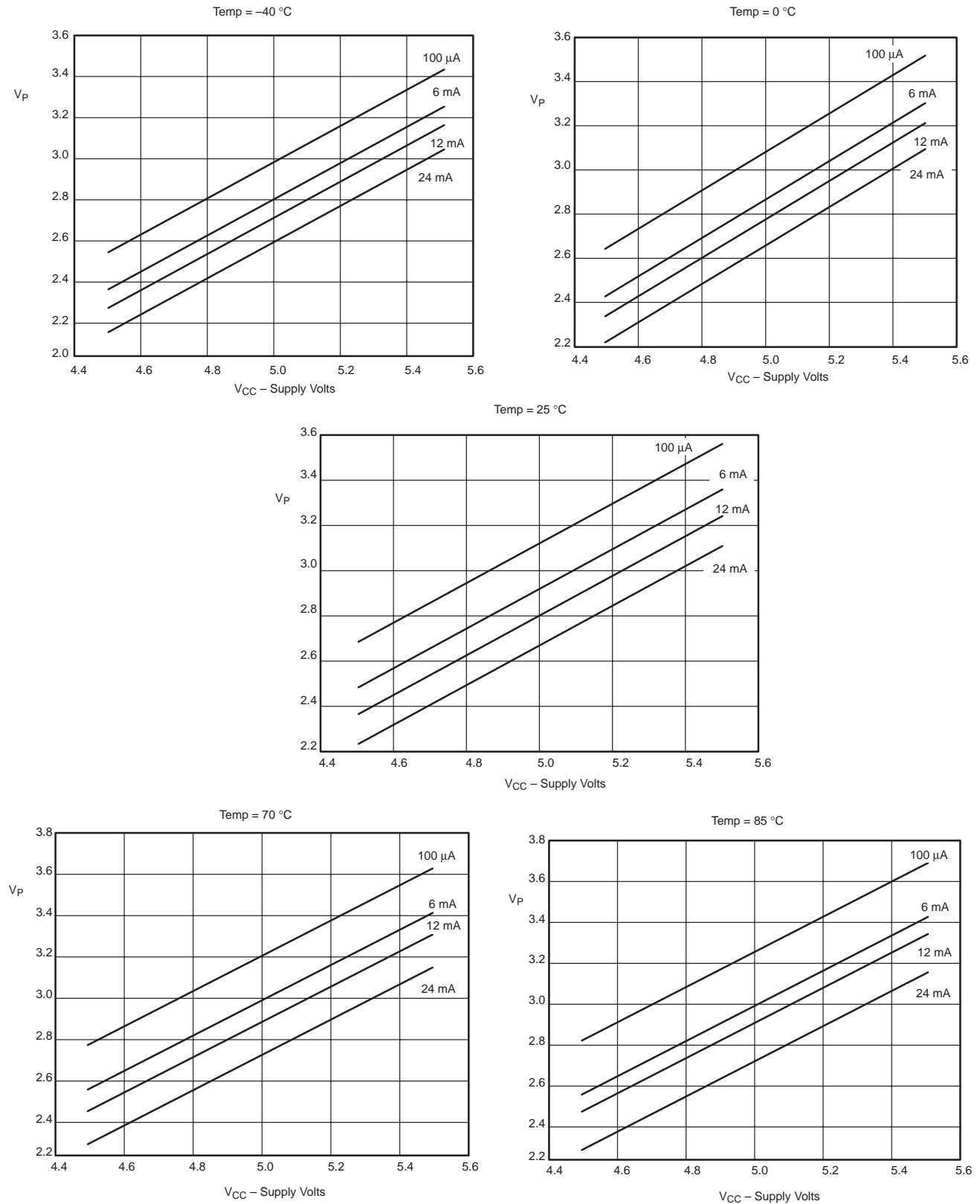
## TEST CIRCUIT AND WAVEFORMS

TEST	S1
$t_{pd}$	open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	open

**DEFINITIONS**  
 $C_L =$  Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

# 24-bit level shifting bus exchange switch with 12-bit output enables

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SW00840

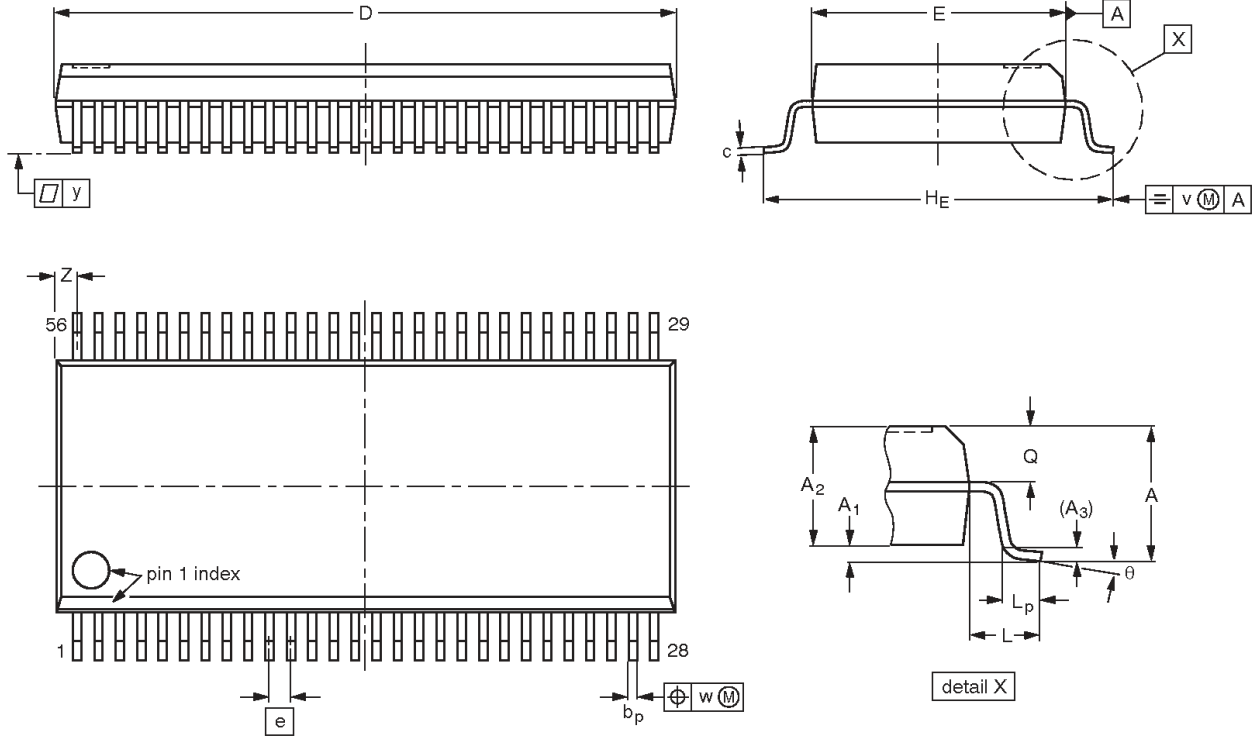
Figure 1. Typical characteristics

24-bit level shifting bus exchange switch  
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SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

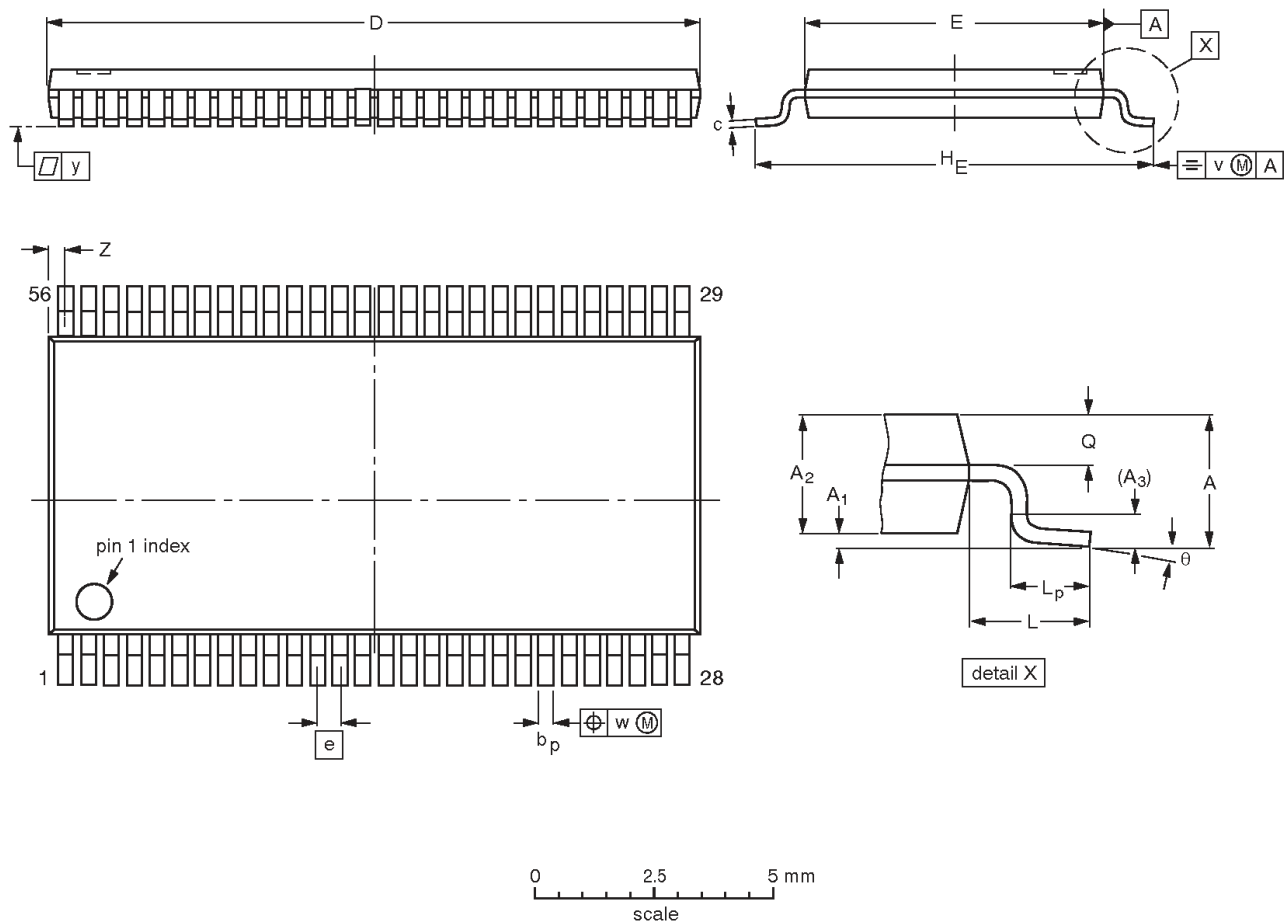
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118				95-02-04 99-12-27

# 24-bit level shifting bus exchange switch with 12-bit output enables

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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



**DIMENSIONS (mm are the original dimensions).**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	$\theta$
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT364-1		MO-153				95-02-10 99-12-27



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**NOTES**

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