BLC10G22XS-400AVT

Power LDMOS transistor

Rev. 1 — 30 April 2018

AMPLEON

Product data sheet

1. Product profile

1.1 General description

400 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 2110 MHz to 2200 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty production test circuit.
V_{DS} = 28 V; I_{Dq} = 800 mA (main); $V_{GS(amp)peak}$ = 1.0 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	2110 to 2200	28	56	17.0	47.0	–29.6 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

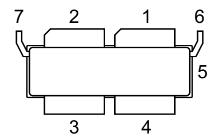
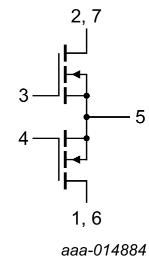
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 2110 MHz to 2200 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain2 (peak)		
2	drain1 (main)		
3	gate1 (main)		
4	gate2 (peak)		
5	source [1]		
6	video decoupling (peak)		
7	video decoupling (main)		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC10G22XS-400AVT	-	air cavity plastic earless flanged package; 6 leads	SOT1258-4

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–6	+9	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–6	+9	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature	operating [1]	–40	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 28 V; I_{Dq} = 800 mA (main); $V_{GS(amp)peak}$ = 1.0 V; T_{case} = 80 °C		
		P_L = 56 W	0.29	K/W
		P_L = 74 W	0.27	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.44 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 144 mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 800 mA	-	2.2	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V	-	26.5	-	A
I_{GSS}	gate leakage current	V_{GS} = 9 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 7.2 A	-	15.0	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 5.04 A	-	93	128	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.98 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 298 mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 1600 mA	-	2.2	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V	-	47	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 14.9 A	-	28.5	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 10.43 A	-	50	74	mΩ

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 2112.5 MHz; f_2 = 2167.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 800 mA (main); $V_{GS(amp)peak}$ = 1.0 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 2110 MHz to 2200 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 56 W	15.3	16.3	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 56 W	-	−14	−9	dB
η_D	drain efficiency	$P_{L(AV)}$ = 56 W	42	46	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 56 W	-	−29	−24	dBc

Table 8. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 2112.5 MHz; f_2 = 2167.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 800 mA (main); $V_{GS(amp)peak}$ = 1.0 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at a frequency of 2200 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_O	output peak-to-average ratio	$P_{L(AV)}$ = 56 W	6.3	6.9	-	dB
$P_{L(M)}$	peak output power	$P_{L(AV)}$ = 56 W	380	440	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC10G22XS-400AVT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 800 mA; $V_{GS(amp)peak}$ = 1.0 V; f = 2112.5 MHz; P_L = 155 W (5 dB OBO); 100 % clipping

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 800 mA (main); V_{DS} = 28 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
2110	1.6 – j6.1	1.5 – j2.9	205	61.5	17.2
2140	2.1 – j6.5	1.5 – j2.9	205	62.0	17.3
2170	2.6 – j7.0	1.4 – j3.3	205	60.0	17.2
Maximum drain efficiency load					
2110	1.6 – j6.1	2.4 – j2.4	160	68.0	19.1
2140	2.1 – j6.5	2.4 – j2.3	158	67.5	19.2
2170	2.6 – j7.0	2.0 – j2.2	160	67.0	19.1

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 10. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 1600 mA (peak); V_{DS} = 28 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
2110	1.9 – j5.4	1.3 – j3.3	390	60.0	16.2
2140	2.4 – j5.7	1.4 – j3.5	390	57.5	16.3
2170	3.1 – j6.1	1.3 – j3.7	390	55.0	16.1
Maximum drain efficiency load					
2110	1.9 – j5.4	1.8 – j2.7	340	63.6	17.6
2140	2.4 – j5.7	1.9 – j2.6	315	63.4	18.1
2170	3.1 – j6.1	1.9 – j2.7	320	63.6	18.2

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

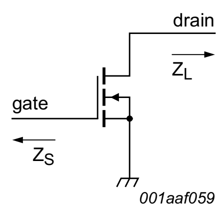


Fig 1. Definition of transistor impedance

7.3 Recommended impedances for Doherty design

Table 11. Typical impedance of main at 1 : 1 load

Measured load-pull data of main device; I_{Dq} = 800 mA (main); V_{DS} = 28 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
2110	1.7 – j5.5	2.1 – j3.8	165	38.0	20.8
2140	2.0 – j5.8	2.1 – j3.5	170	38.0	20.8
2170	2.3 – j6.1	2.0 – j3.3	175	38.5	21.1

[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 56 W.

Table 12. Typical impedance of main device at 1 : 2.5 load

Measured load-pull data of main device; I_{Dq} = 800 mA (main); V_{DS} = 28 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
2110	1.7 – j5.5	3.6 – j0.8	85	53.2	23.5
2140	2.0 – j5.8	3.5 – j0.6	78	53.4	23.5
2170	2.3 – j6.1	3.3 – j0.4	70	53.2	24.0

[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 56 W.

Table 13. Typical impedance of peak device at 1 : 1 load

Measured load-pull data of peak device; I_{Dq} = 1600 mA (peak); V_{DS} = 28 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
2110	1.7 – j4.8	1.8 – j3.5	350	25.5	19.7
2140	2.0 – j5.0	1.8 – j3.2	345	25.8	19.9
2170	2.4 – j5.2	1.8 – j3.1	340	26.4	20.4

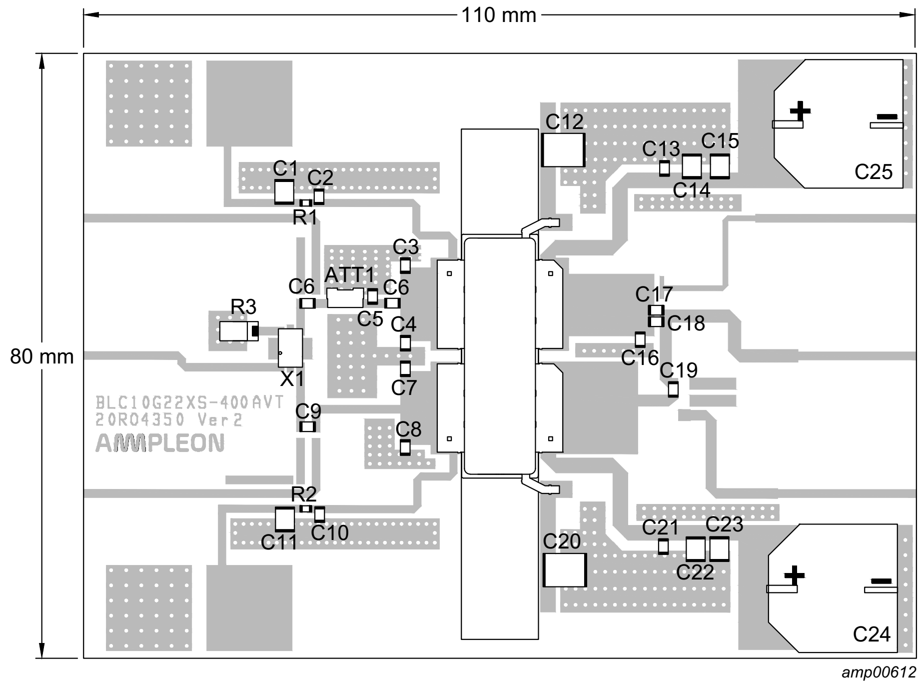
[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 56 W.

Table 14. Off-state impedances of peak device

f	Z_{off}
(MHz)	(Ω)
2110	2.9 – j2.9
2140	2.3 – j1.8
2170	2.0 – j1.0

7.4 Test circuit



Printed-Circuit Board (PCB): Rogers 4350B; thickness = 0.508 mm; thickness copper plating = 35 μm. See Table 15 for a list of components.

Fig 2. Component layout

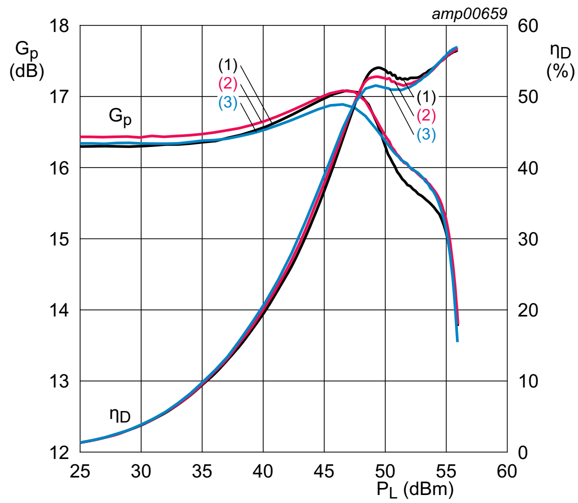
Table 15. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C11, C14, C15, C22, C23,	multilayer ceramic chip capacitor	10 μF, 50 V	Murata: GRM32ER71H106KA12L, SMD 1210
C2, C6, C9, C10, C13, C19, C21	multilayer ceramic chip capacitor	15 pF, 250 V	Murata: GQM2195C2E150FB15, SMD 805
C3, C4, C7, C8	multilayer ceramic chip capacitor	1.0 pF, 250 V	Murata: GQM2195C2E1ROBB15, SMD 0805
C5	multilayer ceramic chip capacitor	0.8 pF, 250 V	Murata: GQM2195C2E1ROBB15, SMD 0805
C12, C20	multilayer ceramic chip capacitor	4.7 μF, 100 V	C5750X7R2A475KT/A
C16	multilayer ceramic chip capacitor	0.5 pF, 250 V	Murata: GQM2195C2E1ROBB15, SMD 0805
C17, C18	multilayer ceramic chip capacitor	1.8 pF, 250 V	Murata: GQM2195C2E1R8BB15, SMD 0805
C24, C25	electrolytic capacitor	470 μF, 63 V	
R1, R2	resistor	5.1 Ω, 1 %	SMD 805
R3	resistor	50 Ω, 25 W	Anaren: C16A50Z4
X1	hybrid coupler	2 dB, 90°	Anaren: Xinger III, X3C20F1-02
ATT1	attenuator	1 dB	Anaren: D10AA1Z4

7.5 Graphical data

7.5.1 Pulsed CW



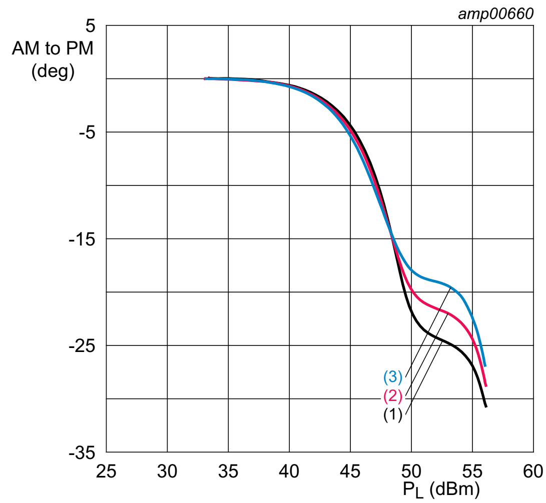
V_{DS} = 28 V; I_{Dq} = 800 mA; $V_{GS(amp)peak}$ = 1.0 V.

(1) f = 2210 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 800 mA; $V_{GS(amp)peak}$ = 1.0 V.

(1) f = 2210 MHz

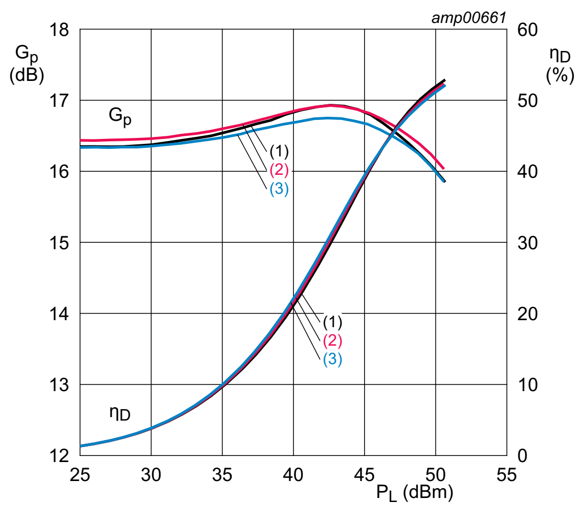
(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 4. Normalized AM to PM as a function of output power; typical values

7.5.2 1-Carrier W-CDMA

Test signal: 3GPP test model 1; 1 to 64 DPCH (100 % clipping): PAR = 7.5 dB per carrier at 0.01 % probability on CCDF per carrier.



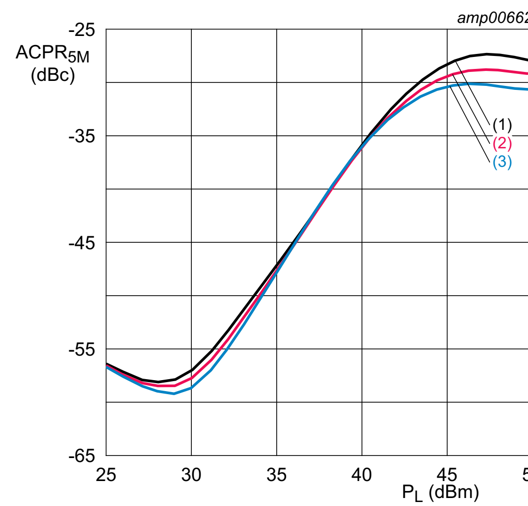
V_{DS} = 28 V; I_{Dq} = 800 mA; $V_{GS(amp)peak}$ = 1.0 V.

(1) f = 2210 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



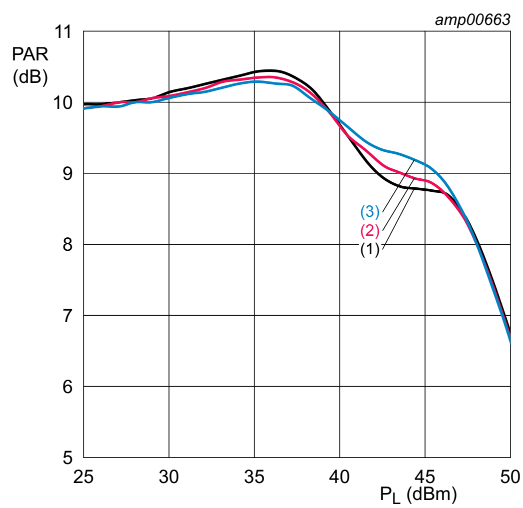
V_{DS} = 28 V; I_{Dq} = 800 mA; $V_{GS(amp)peak}$ = 1.0 V.

(1) f = 2210 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 800 mA; $V_{GS(amp)peak}$ = 1.0 V.

(1) f = 2210 MHz

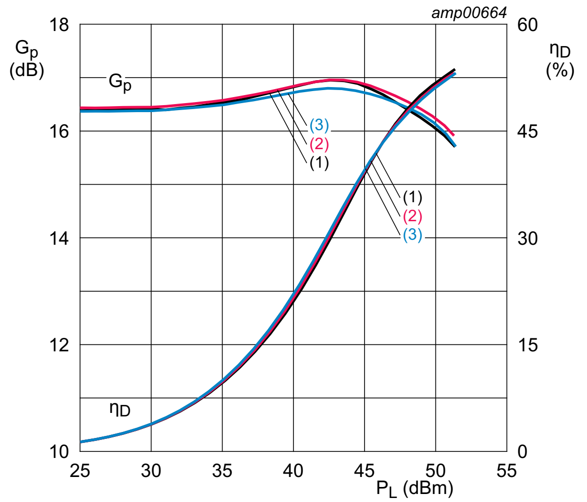
(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 7. Peak-to-average power ratio as a function of output power; typical values

7.5.3 2-Carrier W-CDMA

Test signal: 3GPP test model 1; 1 to 64 DPCH (46 % clipping): PAR = 7.5 dB per carrier at 0.01 % probability on CCDF per carrier.



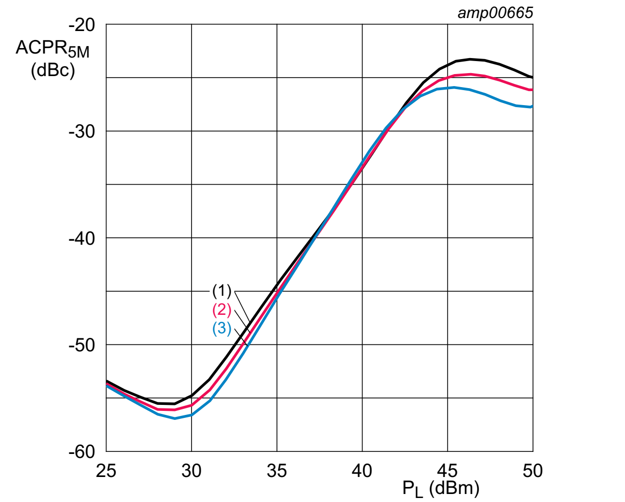
V_{DS} = 28 V; I_{Dq} = 800 mA; $V_{GS(amp)peak}$ = 1.0 V.

(1) f = 2210 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 8. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 800 mA; $V_{GS(amp)peak}$ = 1.0 V.

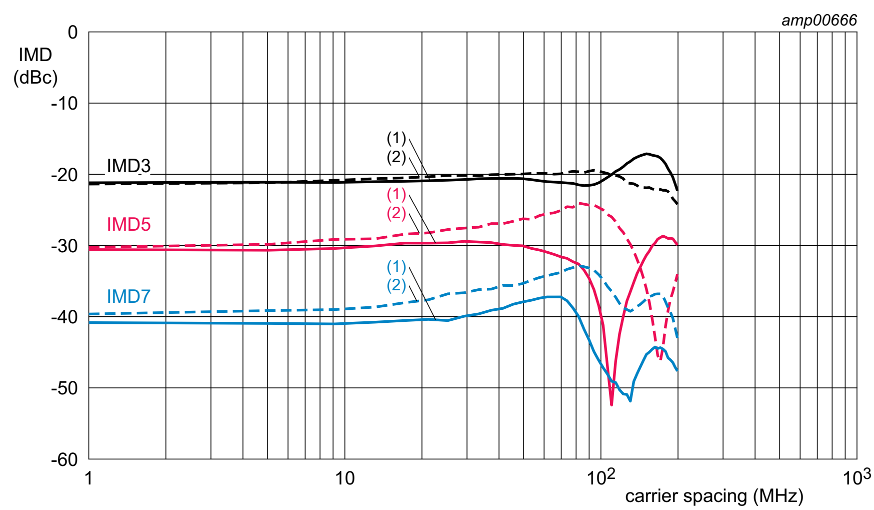
(1) f = 2210 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 9. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

7.5.4 2-Tone VBW



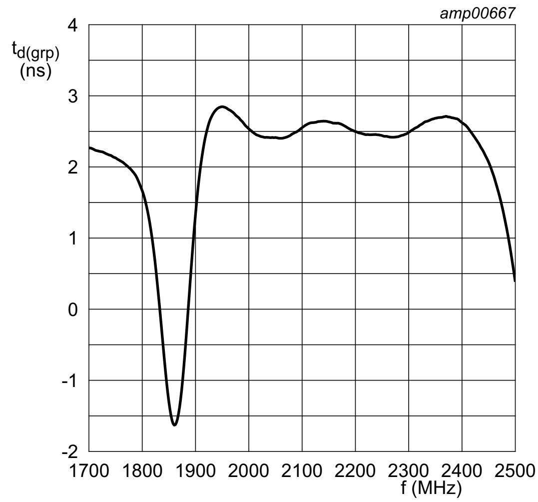
V_{DS} = 28 V; I_{Dq} = 800 mA; $V_{GS(amp)peak}$ = 1.0 V.

(1) IMD low

(2) IMD high

Fig 10. VBW capability

7.5.5 Group delay

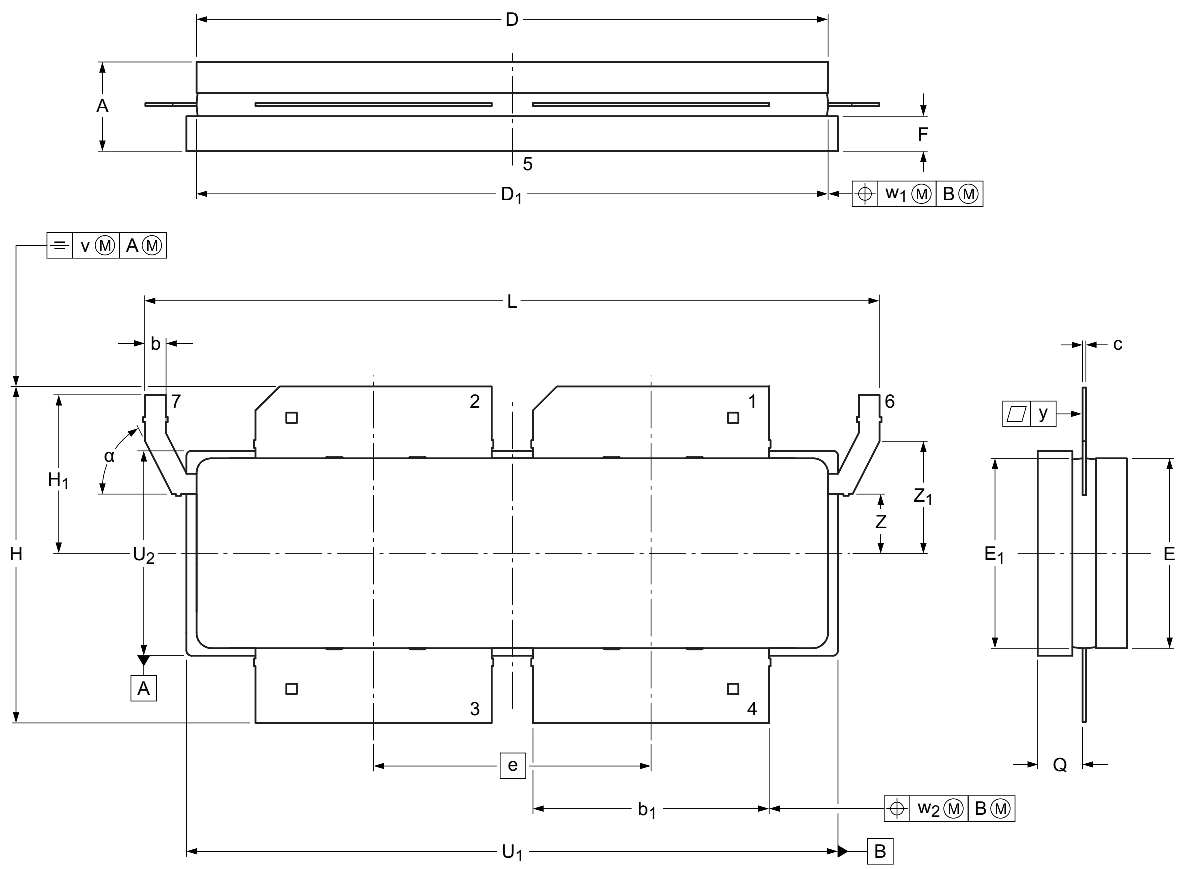


V_{DS} = 28 V; I_{Dq} = 800 mA; $V_{GS(amp)peak}$ = 1.0 V.

Fig 11. Group delay time as a function of frequency; typical values

8. Package outline

Air cavity plastic earless flanged package; 6 leads **SOT1258-4**



y	α	Z	Z_1
0.1	65°	3.17	5.79
	61°	2.67	5.29

0 10 mm
scale

Dimensions

Unit		A	b	b_1	c	D	D_1	E	E_1	e	L	F	H	H_1	Q(1)	U_1	U_2	v	w_1	w_2
mm	max	4.52	1.12	11.78	0.18	31.44	31.34	9.60	9.50		36.42	1.73	16.71	8.12	2.25	32.33	10.23	0.5	0.5	0.5
	nom									13.72										
	min	4.12	0.91	11.58	0.13	31.04	31.14	9.20	9.30		36.22	1.53	16.51	7.62	2.03	32.13	10.03			

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1258-4_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1258-4						17-08-31

Fig 12. Package outline SOT1258-4

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 16. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of 1000 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

10. Abbreviations

Table 17. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC10G22XS-400AVT v.1	20180430	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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13. Contact information

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14. Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

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