19-2321; Rev 0; 4/02

MAXIM

±15kV ESD-Protected USB Level Translator in UCSP with USB Detect

General Description

The MAX3341E USB level translator converts logic-level signals to USB signals, and USB signals to logic-level signals. An internal 1.5kΩ USB termination resistor supports full-speed (12Mbps) USB operation. The MAX3341E provides built-in ±15kV ESD-protection circuitry on the USB I/O pins, D+ and D-, and V_{CC}.

The MAX3341E operates with logic supply voltages as low as 1.8V, ensuring compatibility with low-voltage ASICs. The suspend mode lowers supply current to less than 50µA. A unique enumerate feature allows changes in USB communication protocol while power is applied. The MAX3341E is fully compliant with USB specification 1.1, and full-speed operation under USB specification 2.0.

The MAX3341E has a USB detect that monitors the USB bus for insertion and signals this event.

The MAX3341E is available in the miniature 4 × 4 UCSP™, as well as the small 16-pin TSSOP, and is specified over the extended temperature range, -40°C to +85°C.

Applications

Cell Phones

PC Peripherals

Information Appliances

Data Cradles

PDAs

MP3 Players

Digital Cameras

UCSP is a trademark of Maxim Integrated Products, Inc.

Features

- ♦ **±15kV ESD Protection On D+ and D-**
- ♦ **Complies with USB Standard 1.1 (Full Speed 2.0)**
- ♦ **USB Skew Independent of Input Skew**
- ♦ **Separate VP and VM Inputs/Outputs**
- ♦ **V_L Down to 1.8V Allows Connection with Low-Voltage ASICs**
- ♦ **Reenumerate with Power Applied**
- ♦ **USB Detect Function**
- ♦ **Allows Single-Ended or Differential Logic I/O**
- ♦ **Internal Linear Regulator Allows Direct Powering from the USB**
- ♦ **Internal Termination Resistor for Full-Speed Operation**
- ♦ **Three-State Outputs**
- ♦ **No Power-Supply Sequencing Required**
- ♦ **Driver Active in Suspend Mode**
- ♦ **Available in Miniature Chip-Scale Package**

Ordering Information

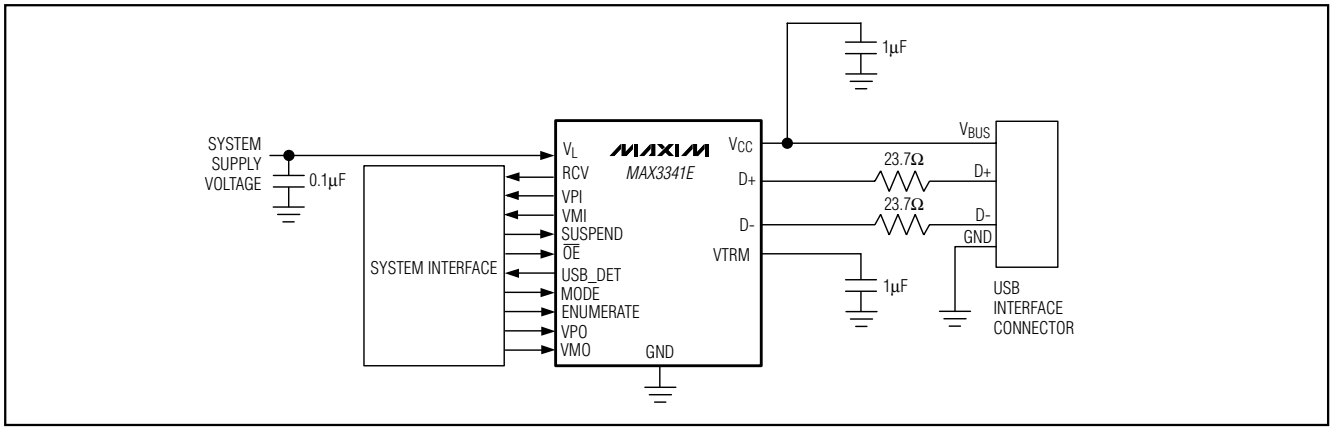
PART	TEMP RANGE	PIN-PACKAGE
MAX3341EEUD	-40°C to +85°C	16 TSSOP
MAX3341EEBE*	-40°C to +85°C	4 × 4 UCSP**

**Future product—contact factory for availability.*

***UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and environment. See the UCSP Reliability Notice in the UCSP Reliability section of this data sheet for more information.*

Pin Configurations appear at end of data sheet.

Typical Operating Circuit



±15kV ESD-Protected USB Level Translator in UCSP with USB Detect

ABSOLUTE MAXIMUM RATINGS

(All Voltages Refer to GND Unless Otherwise Noted.)
Supply Voltage (V_{CC}) .....-0.3V to +6V
Output of Internal Regulator (VTRM) (Note 1).....-0.3V to +6V
Input Voltage (D+, D-) (Notes 1, 2) .....-0.3V to +6V
System Supply Voltage (V_L).....-0.3V to +6V
RCV, SUSP, VMO, MODE, VPO, $\overline{OE}$, VMI,
VPI, USB_DET, ENUM.....-0.3V to (V_L + 0.3V)
Short-Circuit Current (D+, D-) to V_{CC} or
Ground (Note 3) .....Continuous
Maximum Continuous Current (all other pins).....±15mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin TSSOP (derate 7.1mW/°C above +70°C) 571mW
4 × 4 UCSP (derate 8.2 mW/°C above +70°C).....659mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C

Note 1: Guaranteed for V_{CC} < +3.7V only.
Note 2: Absolute Maximum Rating for input voltage (D+, D-) with V_{CC} > +3.7V is -0.3V to (V_{CC} +0.3V).
Note 3: External 23.7Ω resistors connected to D+ and D-.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4V to 5.5V bypassed with 1µF to GND, GND = 0, V_L = 1.8V to 3.6V, D+ to GND = 15kΩ, D- to GND = 15kΩ, ENUM = V_L, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5V, V_L = 2.5V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB Supply Voltage	V_{CC}		4		5.5	V
USB Supply Current	I_{CC}	Data rate = 12Mbps, C_L = 50pF (Figure 6b)		10	20	mA
USB SUSP Supply Current	$I_{CC(SUSP)}$	SUSP = high, ENUM = low, $\overline{OE}$ = high			50	µA
		SUSP = high, $\overline{OE}$ = low			85	
		SUSP = high, ENUM = high, $\overline{OE}$ = high			85	
V_{CC} Supply Current	I_{CC}(< 3V)	V_{CC} < 3V			80	µA
D+/D- Leakage Current	$I_{D+/D-}$(3V)	V_{CC} = 3V; D+, D- < 3.6V			10	µA
V_L Suspend Supply Current	$I_{L(SUSP)}$	SUSP = high, 0 < V_{CC} < 5.5V			20	µA
LOGIC-SIDE I/O						
V_L Input Range	V_L		1.8		3.6	V
Input High Voltage	V_{IH}	SUSP, MODE, ENUM, $\overline{OE}$, VMO, VPO	2/3 × V_L			V
Input Low Voltage	V_{IL}	SUSP, MODE, ENUM, $\overline{OE}$, VMO, VPO			0.4	V
Output Voltage High	V_{OH}	VPI, VMI, RCV, USB_DET; I_{SOURCE} = 1mA	V_L - 0.2			V
Output Voltage Low	V_{OL}	VPI, VMI, RCV, USB_DET; I_{SINK} = -1mA			0.4	V
Input Leakage Current		SUSP, MODE, ENUM, $\overline{OE}$, VMO, VPO = 0 or V_L		±1	±10	µA
USB-SIDE I/O						
Output Voltage Low	V_{OL}	D+ or D-			0.3	V
Output Voltage High	V_{OH}	D+ or D-	2.8		3.6	V
Input Impedance	Z_{IN}	Three-state driver	1			MΩ
Single-Ended Input Voltage High	V_{IH}		2.0			V
Single-Ended Input Voltage Low	V_{IL}				0.8	V
Receiver Single-Ended Hysteresis	V_{HYS}			200		mV
Differential Input Sensitivity	V_{DIFF}		200			mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4V to 5.5V bypassed with 1µF to GND, GND = 0, V_L = 1.8V to 3.6V, D+ to GND = 15kΩ, D- to GND = 15kΩ, ENUM = V_L, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5V, V_L = 2.5V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Common-Mode Voltage Range	V_{CM}		0.8		2.5	V
Driver Output Impedance	Z_{OUT}	Including 23.7Ω (±1%) external resistors	28.5		43.5	Ω
Internal Resistor	R_{PU}		1.425	1.500	1.575	kΩ
Termination Voltage	VTRM		3.0	3.3	3.6	V
USB_DET Threshold	V_{USBLH}				4.0	V
	V_{USBHL}		3.7			
USB_DET Hysteresis	V_{USBHYS}			25		mV
LINEAR REGULATOR						
Power-Supply Rejection Ratio	PSRR	f = 10kHz, C_{OUT} = 1µF, D+/D- load		30		dB
External Capacitor	C_{OUT}	Compensation of linear regulator	1			µF
ESD PROTECTION (V_{CC}, D+, D-)						
Human Body Model				±15		kV
IEC1000-4-2 Air-Gap Discharge				±15		kV
IEC1000-4-2 Contact Discharge				±8		kV

TIMING CHARACTERISTICS

(V_{CC} = 4V to 5.5V, GND = 0, V_L = 1.8V to 3.6V, D+ to GND = 15kΩ, D- to GND = 15kΩ, ENUM = V_L, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5V, V_L = 2.5V, T_A = +25°C.) (Figures 2–6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{OE}$ to Transmit Delay Enable Time	t_{PZD}	Figure 6c	15		80	ns
$\overline{OE}$ to Driver Three-State Delay Driver Disable Time	t_{PDZ}	Figure 6c			25	ns
USB Detect Signal Delay	t_{DUSB}	Figure 6b		7.5		µs
TRANSMITTER						
VPO/VMO to D+/D- Propagation Delay	$t_{PLH1(drv)}$	MODE = high , Figure 6c			30	ns
	$t_{PHL1(drv)}$	MODE = high, Figure 6c			30	
VPO to D+/D- Propagation Delay	$t_{PLH0(drv)}$	MODE = low, Figure 6c			35	ns
	$t_{PHL0(drv)}$	MODE = low, Figure 6c			35	
Rise Time D+/D-	t_R		4		20	ns
Fall Time D+/D-	t_F		4		20	ns
Rise- and Fall-Time Matching	t_R/t_F	(Note 4)	90		110	%
Output Signal Crossover	V_{CRS}		1.3		2	V
DIFFERENTIAL RECEIVER (Figure 6a)						
D+/D- to RCV Propagation Delay	$t_{PLH(RCV)}$				30	ns
	$t_{PHL(RCV)}$				30	
Rise Time RCV	t_R				15	ns
Fall Time RCV	t_F				15	ns

±15kV ESD-Protected USB Level Translator in UCSP with USB Detect

TIMING CHARACTERISTICS (continued)

(V_{CC} = 4V to 5.5V, GND = 0, V_L = 1.8V to 3.6V, D+ to GND = 15kΩ, D- to GND = 15kΩ, ENUM = V_L, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5V, V_L = 2.5V, T_A = +25°C.) (Figures 2–6)

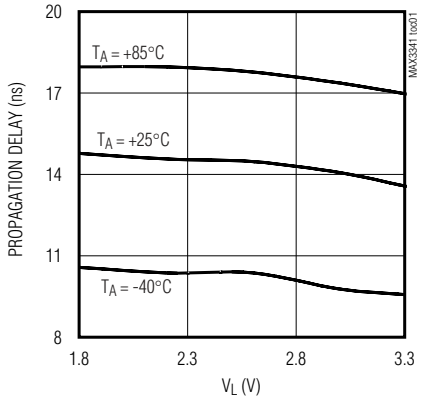
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINGLE-ENDED RECEIVERS						
D+/D- to VPI or VMI Propagation Delay	$t_{PLH(SE)}$	Figure 6a			15	ns
	$t_{PHL(SE)}$	Figure 6a			15	
Rise Time VPI and VMI	$t_{R(SE)}$	Measured from 10% to 90%,Figure 6a			15	ns
Fall Time VPI and VMI	$t_{F(SE)}$	Measured from 90% to 10%, Figure 6a			15	ns
Time to Detect Single-Ended Zero	t_{SE0}		14		140	ns

Note 4: Production tested at +25°C and +85°C only. Limit at -40°C guaranteed by correlation.

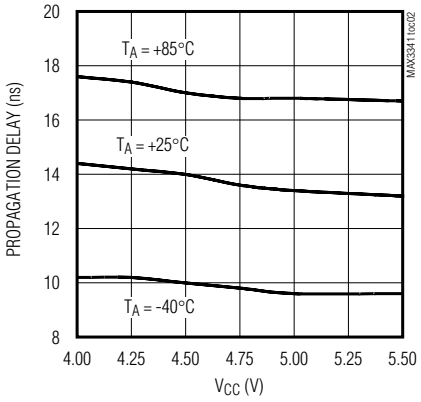
Typical Operating Characteristics

(V_{CC} = 5V, V_L = 3.3V, T_A = +25°C, unless otherwise noted.)

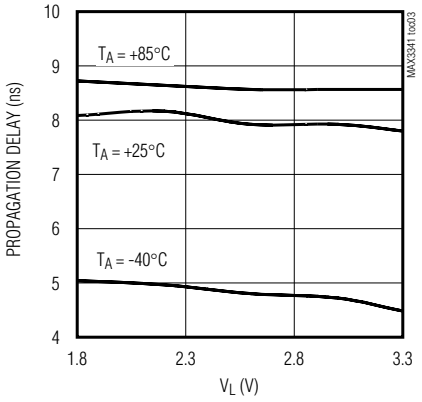
DIFFERENTIAL RECEIVER PROPAGATION DELAY vs. V_L



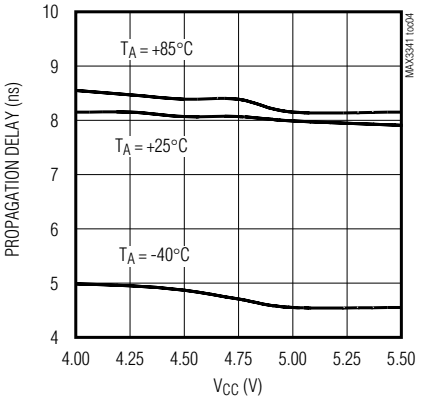
DIFFERENTIAL RECEIVER PROPAGATION DELAY vs. V_{CC}



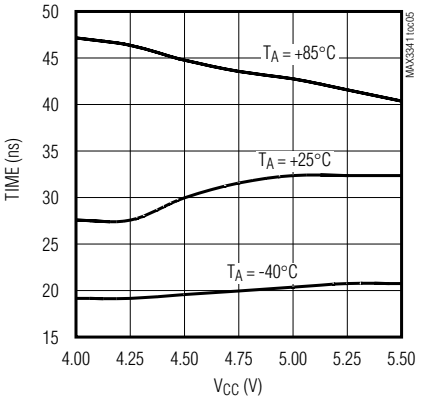
SINGLE-ENDED RECEIVER PROPAGATION DELAY vs. V_L



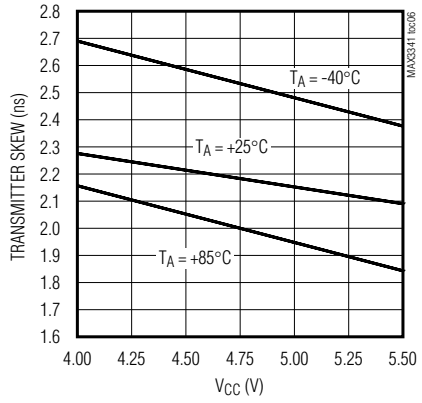
SINGLE-ENDED RECEIVER PROPAGATION DELAY vs. V_{CC}



TIME TO ENTER SUSPEND MODE vs. V_{CC}



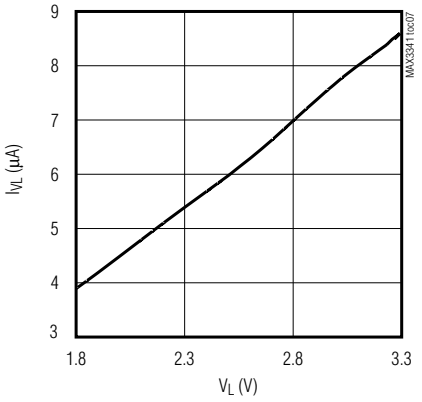
TRANSMITTER SKEW vs. V_{CC}



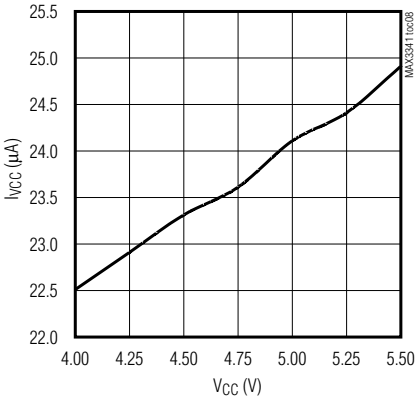
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_L = 3.3V, T_A = +25°C, unless otherwise noted.)

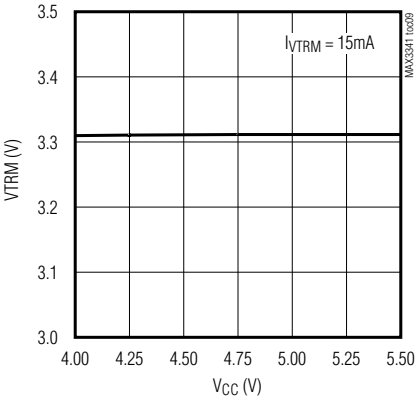
LOGIC CURRENT CONSUMPTION IN SUSPEND MODE



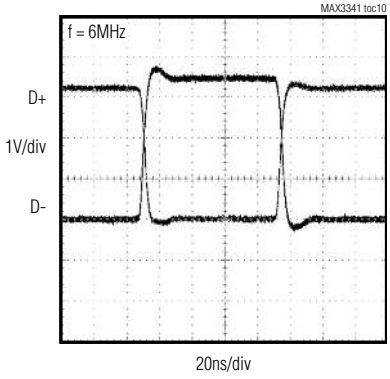
CURRENT CONSUMPTION IN SUSPEND MODE



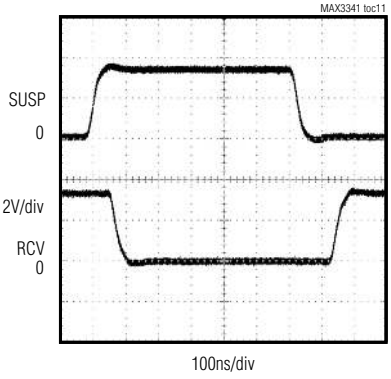
VTRM vs. V_{CC}



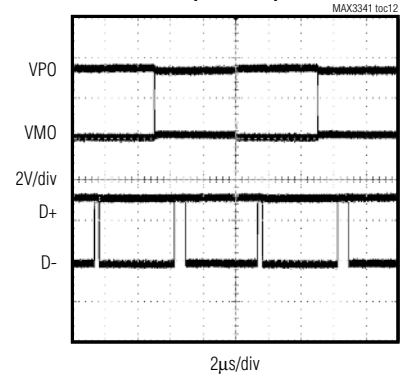
RISE-AND-FALL TIME MATCHING



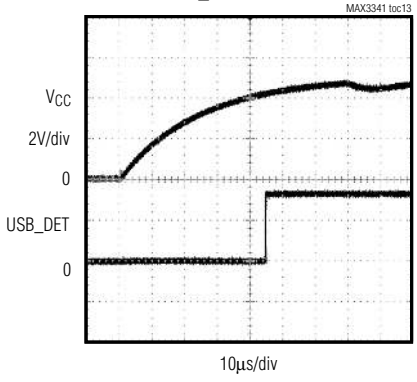
SUSPEND RESPONSE



TRANSMISSION IN SUSPEND MODE (SUSP = 1)



USB_DET RESPONSE



±15kV ESD-Protected USB Level Translator in UCSP with USB Detect

Pin Description

PIN		NAME	FUNCTION
TSSOP	UCSP		
1	D2	RCV	Receiver Output. Single-ended CMOS output. RCV responds to the differential input on D+ and D-.
2	D1	VPO	ASIC Voltage Positive Output. Logic-level data into the MAX3341E.
3	C2	MODE	Mode-Control Input. Selects differential (mode 1) or single-ended (mode 0) input for the system side when converting logic-level signals to USB level signals. Force MODE high to select mode 1. Force MODE low to select mode 0.
4	C1	VMO	ASIC Voltage Minus Output. Logic-level data into the MAX3341E.
5	B1	$\overline{OE}$	Output Enable. Drive $\overline{OE}$ low to enable data transmission on D+ and D-. Drive $\overline{OE}$ high to disable data transmission or to receive data.
6	B2	SUSP	Suspend Input. Drive SUSP low for normal operation. Drive SUSP high for low-power state. In low-power state, RCV is low, and VPI/VMI are active.
7	A1	VPI	ASIC Voltage Positive Input. Logic-level data output from the MAX3341E.
8	A2	VMI	ASIC Voltage Minus Input. Logic-level data output from the MAX3341E.
9	B3	ENUM	Enumerate. Drive ENUM high to connect the internal 1.5kΩ resistor from D+ to 3.3V. Drive ENUM low to disconnect the internal 1.5kΩ resistor.
10	A3	V_{CC}	USB-Side Power-Supply Input. Connect V_{CC} to the incoming USB power supply. Bypass V_{CC} to GND with a 1µF ceramic capacitor.
11	A4	GND	Ground
12	B4	D-	Negative USB Differential Data Input/Output. Connect to the USB's D- signal through a 23.7Ω ±1% resistor.
13	C4	D+	Positive USB Differential Data Input/Output. Connect to the USB's D+ signal through a 23.7Ω ±1% resistor.
14	D4	VTRM	Regulated Output Voltage. 3.3V output derived from the V_{CC} input. Bypass VTRM to GND with a 1µF (min) low-ESR capacitor such as ceramic or plastic film types.
15	D3	V_L	System-Side Power-Supply Input. Connect to the system's logic-level power supply, 1.8V to 3.6V.
16	C3	USB_DET	USB Detector Output. A high at USB_DET signals to the ASIC that V_{CC} is present. A low at USB_DET indicates that V_{CC} is not present.

Detailed Description

The MAX3341E is a bidirectional level translator that converts single-ended or differential logic-level signals to differential USB signals, and converts differential USB signals to single-ended or differential logic-level signals. The MAX3341E includes an internal 1.5kΩ pullup resistor that connects and disconnects D+ to VTRM (*Functional Diagram*). The MAX3341E is tolerant to power sequencing with either $V_{CC} > V_L$ or $V_L > V_{CC}$. Additionally, the USB I/O, D+ and D-, and V_{CC} are ESD protected to ±15kV. The MAX3341E can receive USB power (V_{CC}) directly from the USB connection, and operates with logic supplies (V_L) down to 1.8V while still meeting the USB physical layer specifications. The MAX3341E supports full-speed (12Mbps) USB specification 2.0 operation.

The MAX3341E has a unique enumerate feature that functions when power is applied. Driving ENUM low disconnects the internal 1.5kΩ termination resistor from D+ enumerating the USB. This is useful if changes in communication protocol are required while power is applied, and while the USB cable is connected.

Device Control

D+ and D-

D+ and D- are the USB side transmitter I/O connections, and are ESD protected to ±15kV using the Human Body Model, ±15kV using IEC 1000-4-2 Air-Gap Discharge, and ±8kV using IEC 1000-4-2 Contact Discharge, making the MAX3341E ideal for applications where a robust transmitter is required. A 23.7Ω resistor is required on D+ and D- for normal operation (see *External Resistors*).

The MAX3341E contains unique circuitry to ensure the USB skew is independent of the input skew on VPO and VMO. Input skews of up to 10ns are ignored and do not show up on the output.

ENUM

USB specification 2.0 requires a 1.5kΩ pullup resistor on D+ for full-speed (12Mbps) operation. Controlled by enumerate (ENUM), the MAX3341E provides this internal 1.5kΩ resistor. Drive ENUM high to connect the pullup resistor from D+ to VTRM. Drive ENUM low to disconnect the pullup resistor from D+ to VTRM.

VPO/VMO, VPI/VMI, and $\overline{OE}$

The MAX3341E system-side inputs are VPO and VMO. Data from an ASIC comes into the MAX3341E through VPO and VMO. VPO and VMO operate either differentially with VPO as the positive terminal and VMO as the negative terminal, or single ended with VPO as the data input (see *MODE* section).

The MAX3341E system-side outputs are VPI, VMI, and RCV. The MAX3341E sends data to an ASIC through VPI, VMI, and RCV. VPI and VMI are outputs to the single-ended receivers and RCV is the output of the differential receiver.

Output enable ($\overline{OE}$) controls data transmission. Drive $\overline{OE}$ low to enable data transmission on D+ and D-. Drive $\overline{OE}$ high to disable data transmission or receive data.

MODE

MODE is a control input that selects whether differential or single-ended logic signals are recognized by the system side of the MAX3341E. Drive MODE high to select differential mode with VPO as the positive terminal and VMO as the negative terminal. Drive MODE low to select single-ended mode with VPO as the data input (Table 1).

VTRM

VTRM is the 3.3V output of the internal linear voltage regulator. VTRM powers the internal circuitry of the USB side of the MAX3341E. Connect a 1µF (min) low-ESR ceramic or plastic capacitor from VTRM to GND, as close to VTRM as possible.

VCC

In most applications, V_{CC} is derived from the USB 5V output. If supplying V_{CC} with an alternative power supply such as a lithium-ion battery, the V_{CC} input range is 4.0V to 5.5V. If V_{CC} drops below 4.0V, supply current drops to 10µA avoiding excessive battery drain, and D+/D- enter a high-impedance state allowing other devices to drive the lines. Bypass V_{CC} to GND with a 1µF ceramic capacitor as close to the device as possible.

USB Detect

USB detect output (USB_DET) signals to the ASIC that V_{CC} is present. A high at USB_DET indicates that V_{CC} is present, while a low at USB_DET indicates that V_{CC} is not present.

SUSP

Suspend (SUSP) is a control input. Force SUSP high to place the MAX3341E in a low-power state. In this state, the quiescent supply current into V_{CC} is less than 50µA and RCV goes low.

In suspend mode, VPI and VMI remain active as receive outputs and VTRM stays on. The MAX3341E continues to receive data from the USB, allowing the µP to sense activity on the D+/D- lines and wake up the MAX3341E.

The MAX3341E can also transmit data to D+ and D- while in suspend mode. This function is used to signal a remote wakeup by driving a signal on D+ and D- for a period of 1ms to 15ms. Slew rate control is not active during suspend mode, and data can only be sent at data rates up to 200kps.

Data Transfer

Receiving Data from the USB

Data received from the USB are output to VPI/VMI in either of two ways, differentially or single ended. To receive data from the USB, force $\overline{OE}$ high and SUSP low. Differential data arriving at D+/D- appear as differential logic signals at VPI/VMI, and as a single-ended logic signal at RCV. If both D+ and D- are low, then VPI and VMI are low, signaling a single-ended zero condition on the bus; RCV is undefined (Table 1).

Transmitting Data to the USB

The MAX3341E outputs data to the USB differentially on D+ and D-. The logic driving signals may be either differential or single ended. For sending differential logic, force MODE high, force $\overline{OE}$ and SUSP low, and apply data to VPO and VMO. D+ then follows VPO, and D- follows VMO. To send single-ended logic signals, force

±15kV ESD-Protected USB Level Translator in UCSP with USB Detect

Table 1a. Truth Table Transmit (SUSP = 0, $\overline{OE}$ = 0, ENUM = X)

INPUT			OUTPUT					
MODE	VPO	VMO	D+	D-	RCV	VPI	VMI	RESULT
0	0	0	0	1	0	0	1	LOGIC 0
0	0	1	0	0	X	0	0	SE0
0	1	0	1	0	1	1	0	LOGIC 1
0	1	1	0	0	X	0	0	SE0
1	0	0	0	0	X	0	0	SE0
1	0	1	0	1	0	0	1	LOGIC 0
1	1	0	1	0	1	1	0	LOGIC 1
1	1	1	1	1	X	1	1	UNDEFINED

Table 1b. Truth Table Receive (SUSP = 0, $\overline{OE}$ = 1, ENUM = X)

INPUT		OUTPUT			
D+	D-	RCV	VPI	VMI	RESULT
0	0	X	0	0	SE0
0	1	0	0	1	LOGIC 0
1	0	1	1	0	LOGIC 1
1	1	X	1	1	UNDEFINED

Table 1c. Truth Table Transmit in Suspend* (SUSP = 1, $\overline{OE}$ = 0, ENUM = X)

INPUT			OUTPUT					
MODE	VPO	VMO	D+	D-	RCV	VPI	VMI	RESULT
0	0	0	0	1	0	0	1	LOGIC 0
0	0	1	0	0	0	0	0	SE0
0	1	0	1	0	0	1	0	LOGIC 1
0	1	1	0	0	0	0	0	SE0
1	0	0	0	0	0	0	0	SE0
1	0	1	0	1	0	0	1	LOGIC 0
1	1	0	1	0	0	1	0	LOGIC 1
1	1	1	1	1	0	1	1	UNDEFINED

**Timing specifications are not guaranteed for D+ and D-.*

Table 1d. Truth Table Receive in Suspend* (SUSP = 1, $\overline{OE}$ = 1, MODE = X, VPO/VMO = X, ENUM = X)

INPUT		OUTPUT			
D+	D-	RCV	VPI	VMI	RESULT
0	0	0	0	0	VPI/VMI ACTIVE
0	1	0	0	1	VPI/VMI ACTIVE
1	0	0	1	0	VPI/VMI ACTIVE
1	1	0	1	1	VPI/VMI ACTIVE

**Timing specifications are not guaranteed for D+ and D-.*

MODE, SUSP, and $\overline{OE}$ low, and apply data to VPO/VMO. When VMO is high, a single-ended zero condition is sent on the bus and RCV is undefined (Table 1).

ESD Protection

To protect the MAX3341E against ESD, D+ and D- have extra protection against static electricity to protect the device up to ±15kV. The ESD structures withstand high ESD in all states—normal operation, suspend, and powered down. In order for the 15kV ESD structures to work correctly, a 1µF or greater capacitor must be connected from VTRM to GND.

ESD protection can be tested in various ways; the D+ and D- input/output pins are characterized for protection to the following limits:

1) ±15kV using the Human Body Model
2) ±8kV using the IEC 1000-4-2 Contact Discharge method
3) ±15kV using the IEC 1000-4-2 Air-Gap method

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 1a shows the Human Body Model, and Figure 1b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX3341E helps the user design equipment that meets level 4 of IEC 1000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 1000-4-2 is a higher peak current in IEC 1000-4-2, because series resistance is lower in the IEC 1000-4-2 model. Hence, the ESD withstand voltage measured to IEC 1000-4-2 is generally lower than that measured using the Human Body Model. Figure 1c shows the IEC 1000-4-2 model.

The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

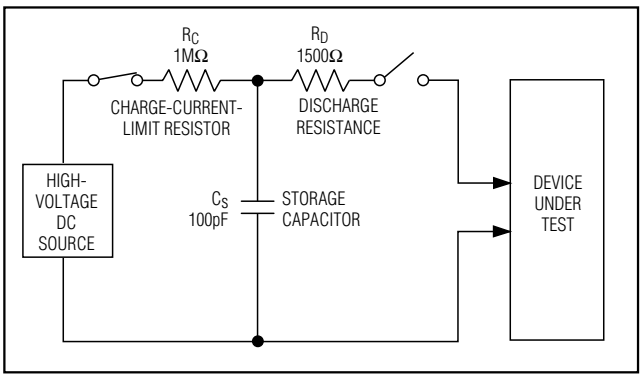


Figure 1a. Human Body ESD Test Models

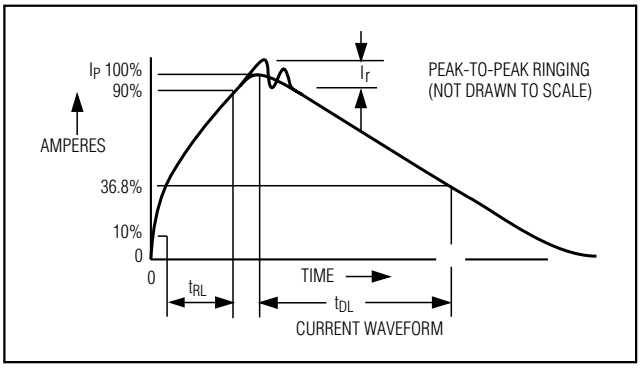


Figure 1b. Human Body Model Current Waveform

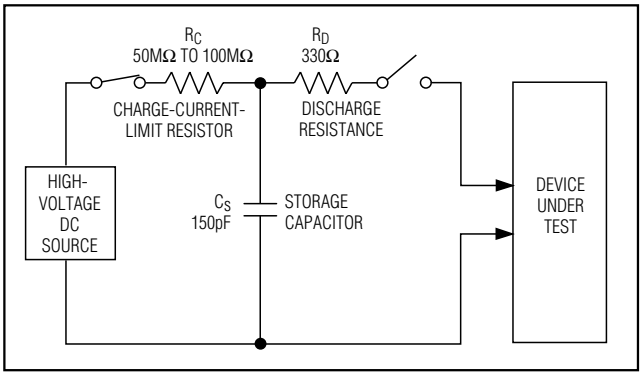


Figure 1c. IEC 1000-4-2 ESD Test Model

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that

±15kV ESD-Protected USB Level Translator in UCSP with USB Detect

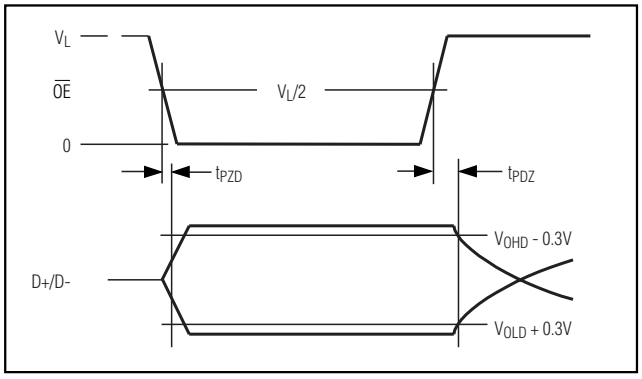


Figure 2. Enable and Disable Timing, Transmitter

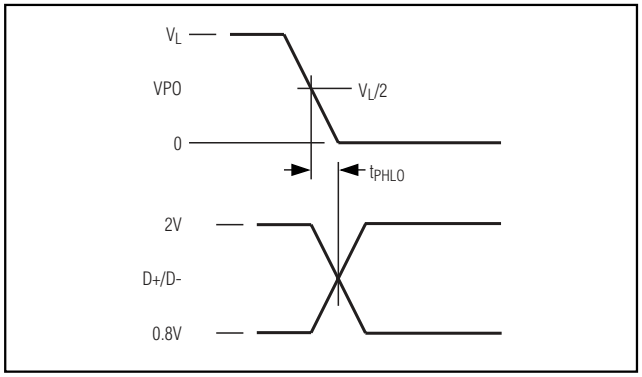


Figure 3. Mode 0 Timing

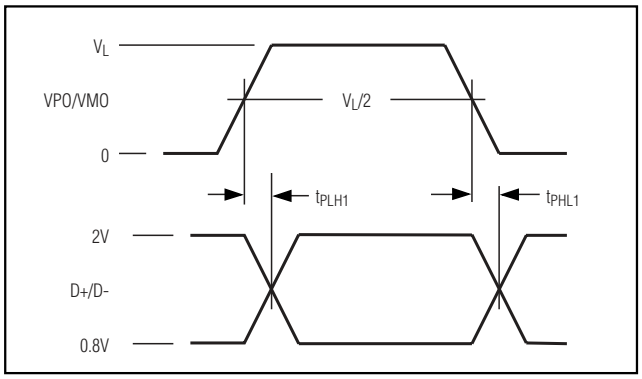


Figure 4. Mode 1 Timing

occurs with handling and assembly during manufacturing. All pins require this protection during manufacturing. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

Applications Information

External Components

External Resistors

Two external 23.7Ω ±1%, 1/2W resistors are required for USB connection. Place the resistors in between the MAX3341E and the USB connector on the D+ and D- lines. See *Typical Operating Circuit*.

External Capacitors

Use three external capacitors for proper operation. Use a 0.1µF ceramic for decoupling V_L, a 1µF ceramic for decoupling V_{CC}, and a 1.0µF (min) ceramic or plastic filter capacitor on VTRM. Return all capacitors to GND.

UCSP Reliability

The UCSP represents a unique packaging form factor that may not perform equally to a packaged product through traditional mechanical reliability tests. CSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering use of a CSP package. Performance through Operating Life Test and Moisture Resistance remains uncompromised as it is primarily determined by the wafer-fabrication process.

Mechanical stress performance is a greater consideration for a CSP package. CSPs are attached through direct solder contact to the user's PC board, foregoing the inherent stress relief of a packaged product lead frame. Solder joint contact integrity must be considered. Table 2 shows the testing done to characterize the CSP reliability performance. In conclusion, the UCSP is capable of performing reliably through environmental stresses as indicated by the results in Table 2. Additional usage data and recommendations are detailed in the UCSP application note, which can be found on Maxim's website at www.maxim-ic.com.

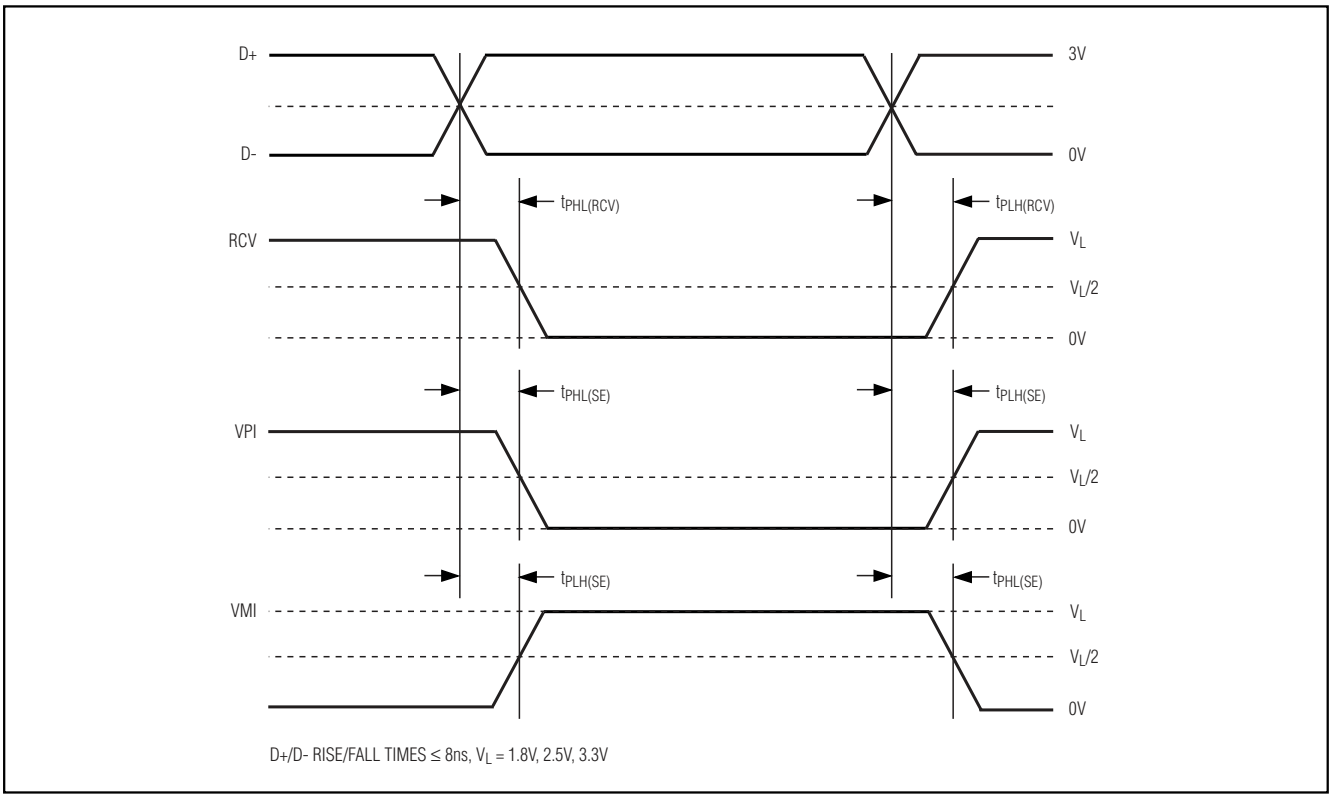


Figure 5. D+/D- to RCV, VPI, VMI Propagation Delays

±15kV ESD-Protected USB Level Translator in UCSP with USB Detect

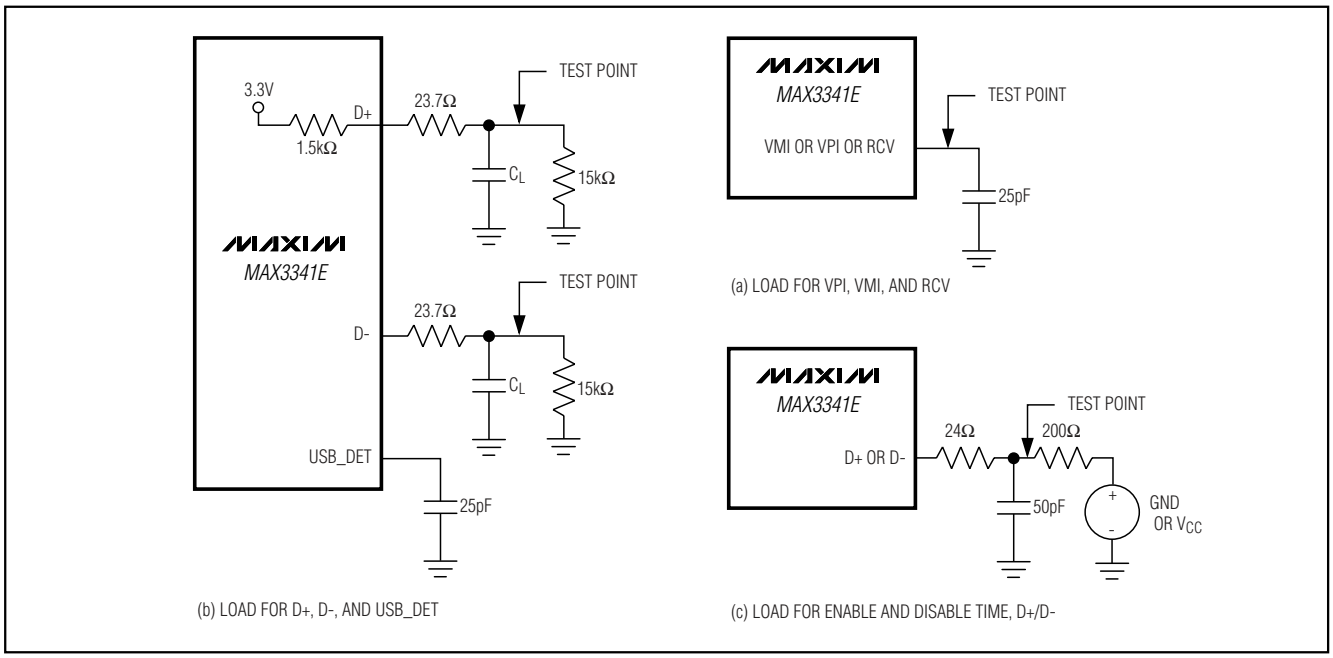


Figure 6. Test Circuits

Table 2. Reliability Test Data

TEST	CONDITIONS	DURATION	NO. OF FAILURES PER SAMPLE SIZE
Temperature Cycle	-35°C to +85°C, -40°C to +100°C	150 cycles, 900 cycles	0/10, 0/200
Operating Life	T_A = +70°C	240hr	0/10
Moisture Resistance	+20°C to +60°C, 90% RH	240hr	0/10
Low-Temperature Storage	-20°C	240hr	0/10
Low-Temperature Operational	-10°C	24hr	0/10
Solderability	8hr steam age	—	0/15
ESD	±2000V, Human Body Model	—	0/5
High-Temperature Operating Life	T_J = +150°C	168hr	0/45

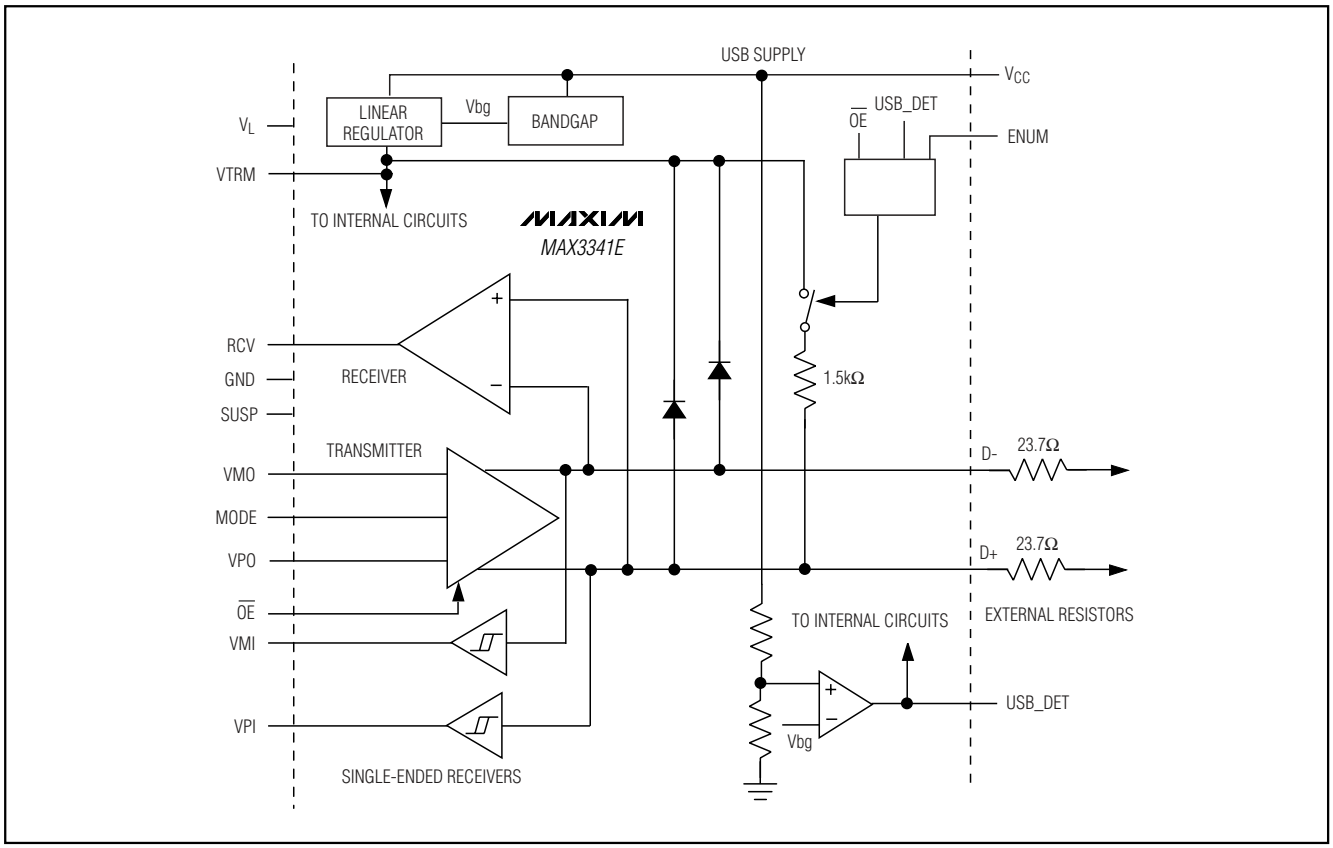
Chip Information

TRANSISTOR COUNT: 2162

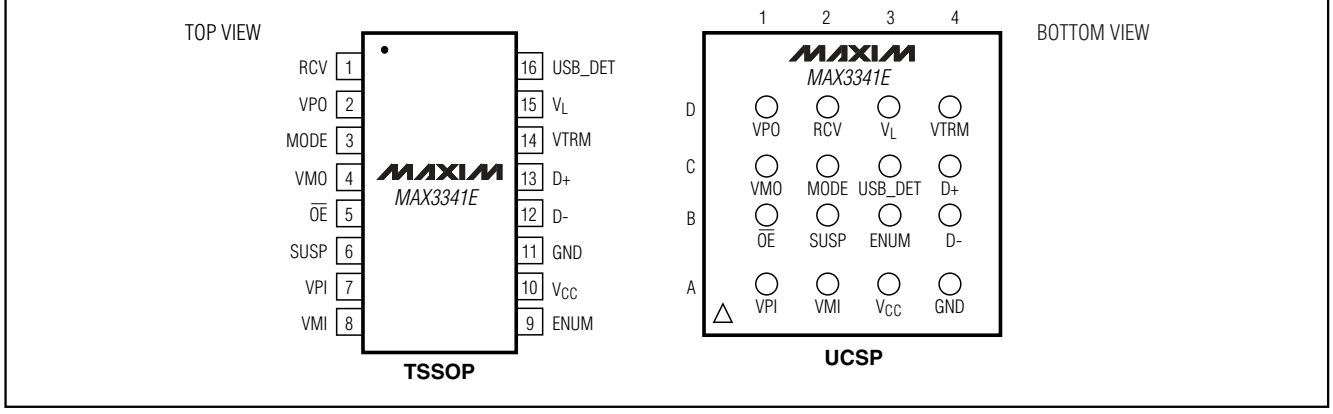
PROCESS: BiCMOS

±15kV ESD-Protected USB Level Translator in UCSP with USB Detect

Functional Diagram



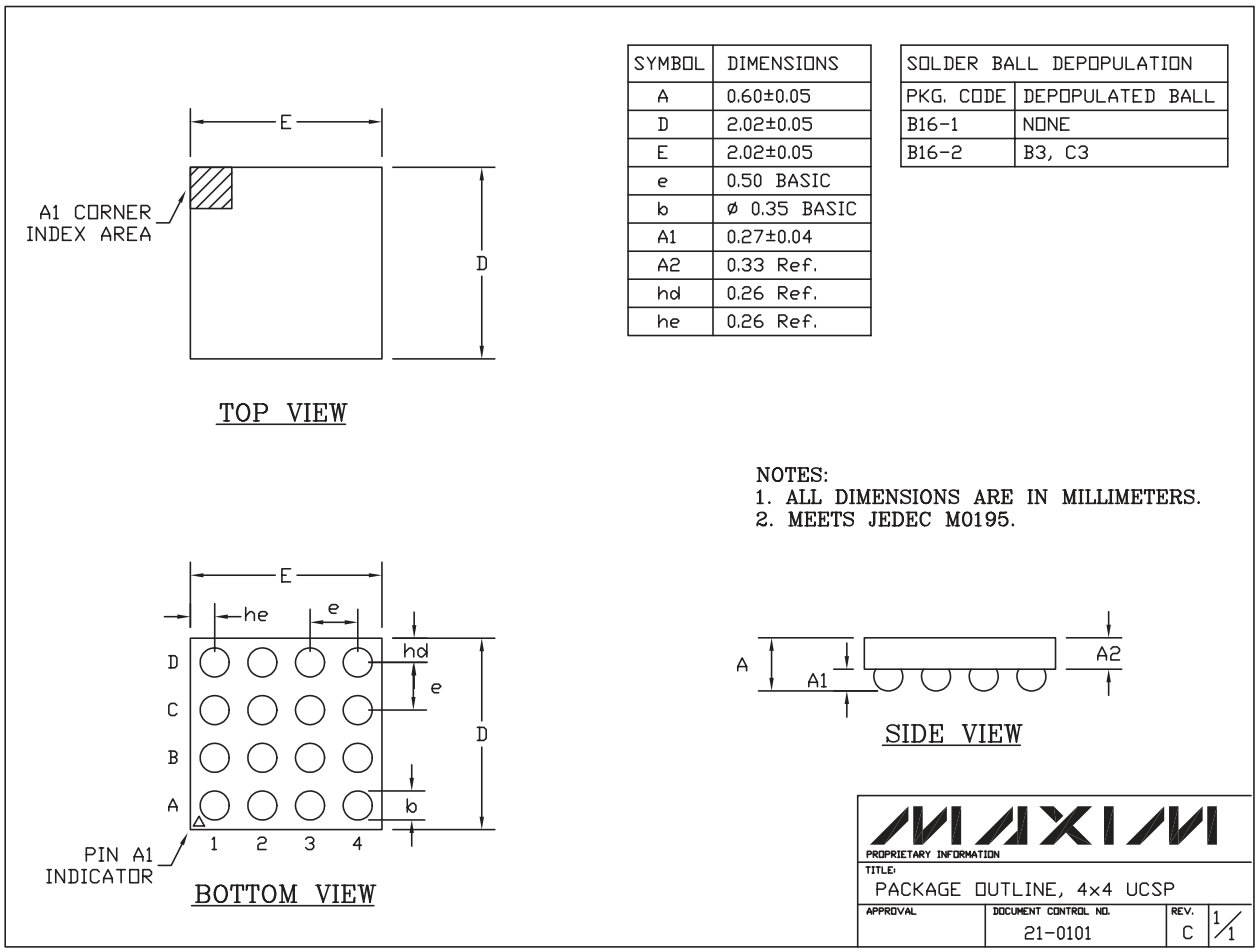
Pin Configurations



±15kV ESD-Protected USB Level Translator in UCSP with USB Detect

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



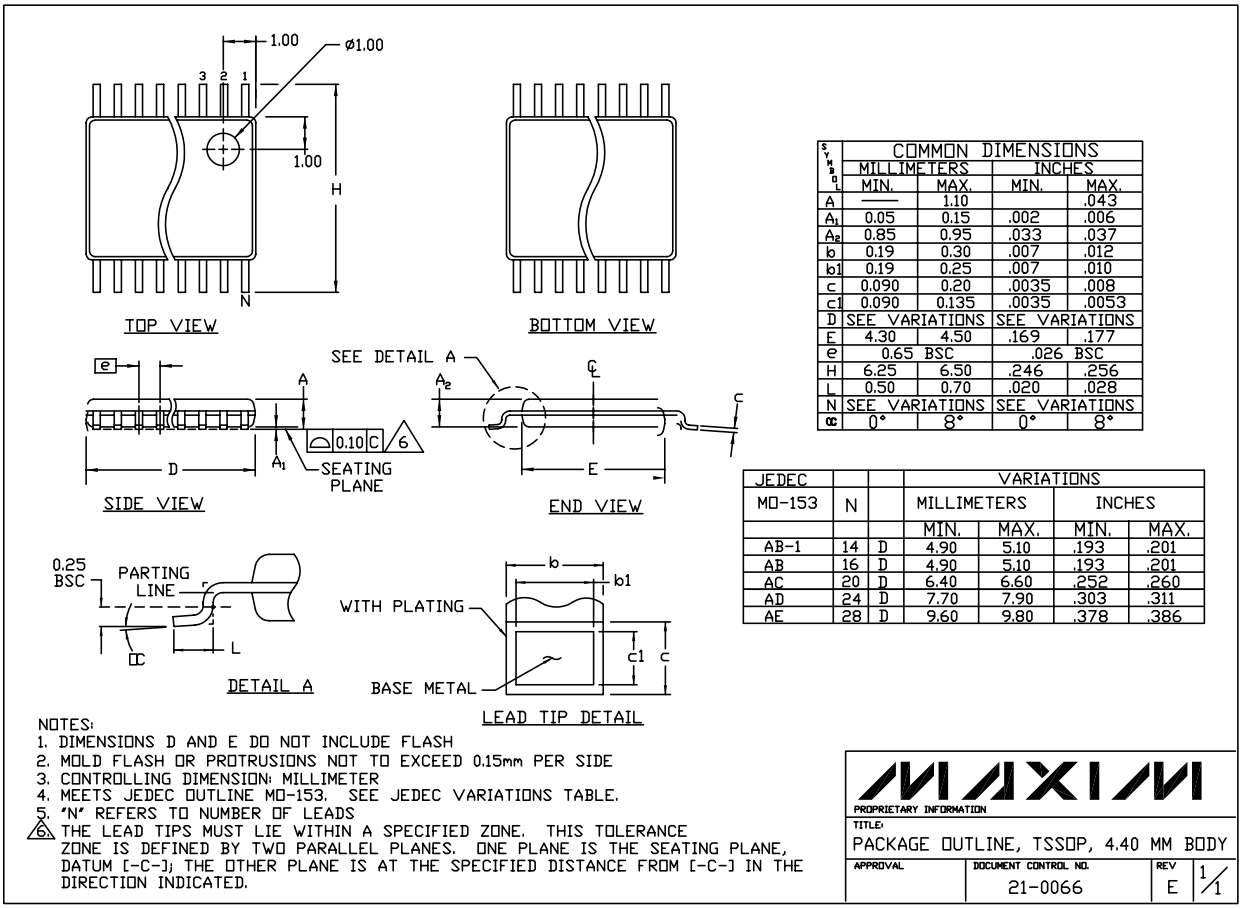
SYMBOL	DIMENSIONS
A	0.60±0.05
D	2.02±0.05
E	2.02±0.05
e	0.50 BASIC
b	ø 0.35 BASIC
A1	0.27±0.04
A2	0.33 Ref.
hd	0.26 Ref.
he	0.26 Ref.

SOLDER BALL DEPOPULATION	
PKG. CODE	DEPOPULATED BALL
B16-1	NONE
B16-2	B3, C3

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP,NO PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0066	E	1/1