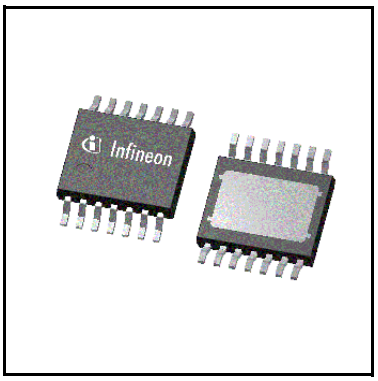
OPTIREG™ Linear TLT807B0EPV

Low dropout adjustable standby voltage regulator for truck applications



Features

- Adjustable output voltage at ±2% accuracy for output current up to 70 mA
- Very low current consumption: typically 36 µA
- Very low dropout voltage
- Input voltage up to 42 V
- Overvoltage protection up to 58 V (< 400 ms)
- Enable input, active high
- Protection functions:
  - Output current limitation for overload and short circuit conditions
  - Reverse polarity protection
  - Overtemperature shutdown
- Wide temperature range -40°C to 150°C
- Infineon automotive quality
- Grade 1 for extended mission profiles
- Green Product (RoHS compliant)

Potential applications

- 24 V applications, such as:
  - Truck applications
  - Commercial Agricultural Vehicle (CAV) applications
  - Construction vehicle applications
- x-EV applications
- Applications that are permanently connected to the battery

Product validation

Qualified for automotive applications with extended lifetime requirements. Product validation according to AEC-Q100.

Description

The TLT807B0EPV is a monolithic integrated low dropout adjustable voltage regulator in a small surface mounted package for the harsh environment of automotive applications.

Type	Package	Marking
TLT807B0EPV	PG-TSDSO-14	T807B0

Table of contents

1 Block diagram

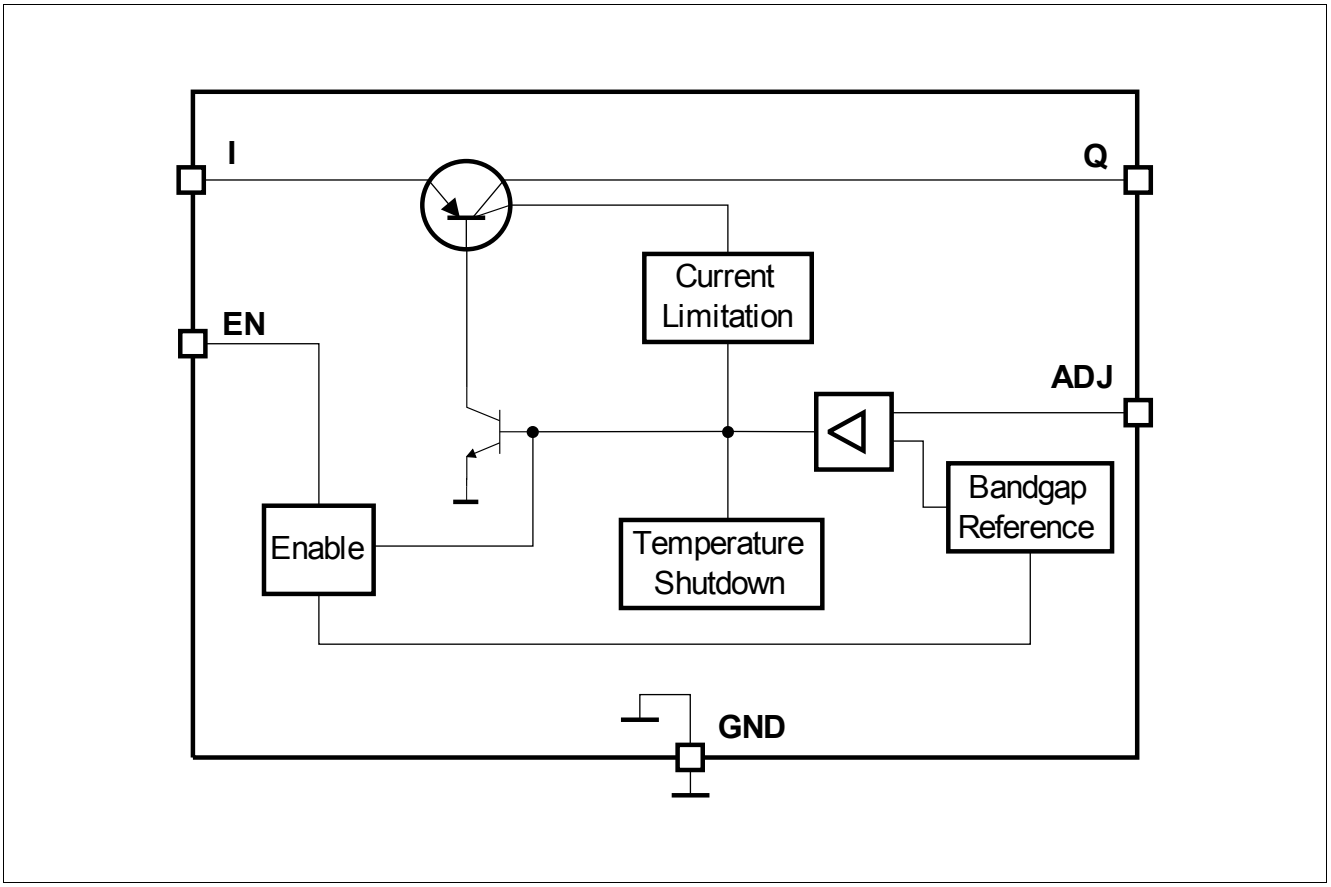


Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment PG-TSDSO-14

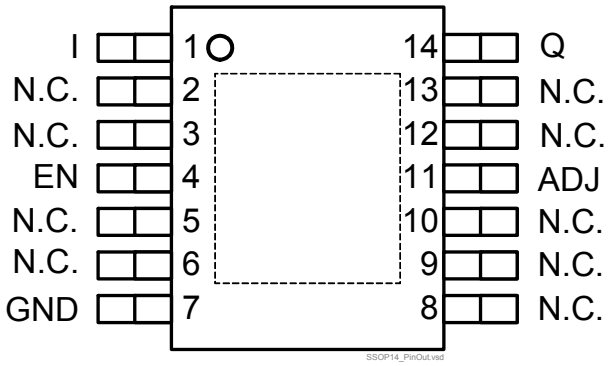


Figure 2 Pin assignment

2.2 Pin definitions and functions PG-TSDSO-14

Pin No.	Symbol	Function
1	I	**Input** In order to compensate line influence, it is recommended to connect a small ceramic capacitor (for example 100 nF) to GND, close to the pins.
4	EN	**Enable input** with integrated pull-down resistor. • “high” signal enables the TLT807B0EPV • “low” signal disables the TLT807B0EPV
7	GND	**Ground**
11	ADJ	**Voltage adjustment** Connect a resistive divider to determine the output voltage.
14	Q	**Output** Connect an output capacitor C_Q to GND close to the pins. C_Q must maintain the capacitance and ESR values specified in **“Functional range” on Page 7**
2, 3, 5, 6, 8, 9, 10, 12, 13	N.C.	**Not connected**
Exposed Pad	EP	**Exposed pad** Connect to GND and heatsink area

3 General product characteristics

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings[1)]

T_j = -40°C to 150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input I, Enable EN							
Voltage	V_I, V_{EN}	-42	–	45	V	–	P_4.1.1
Voltage	V_I, V_{EN}	-42	–	58	V	t < 400 ms	P_4.1.2
Output Q							
Voltage	V_Q	-0.3	–	36	V	–	P_4.1.3
Adjust ADJ							
Voltage	V_{ADJ}	-0.3	–	16	V	–	P_4.1.4
Temperature							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.5
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.6
ESD susceptibility							
ESD susceptibility to GND	$V_{ESD,HBM}$	-2	–	2	kV	Human Body Model (HBM)[2)]	P_4.1.7
ESD susceptibility to GND	$V_{ESD,CDM}$	-750	–	750	V	Charged Device Model (CDM)[3)] at all pins	P_4.1.8

1) Not subject to production test, specified by design
2) ESD susceptibility Human Body Model “HBM” according to AEC-Q100-002 - JESD22-A114
3) ESD susceptibility Charged Device Model “CDM” according to ESDA STM5.3.1

Note:

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 2 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range	V_I	4.7or $V_{Q,nom} + V_{dr}$	–	42	V	–[1]	P_4.2.1
Output capacitor's requirements for stability[2]	C_Q	1	–	–	µF	–[3]	P_4.2.2
Output capacitor's ESR requirements for stability	$ESR(C_Q)$	–	–	4	Ω	–	P_4.2.3
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.4

1) The minimum input voltage is the higher one of the following values: 4.7 V and $V_{Q,nom} + V_{dr}$.
2) Not subject to production test, specified by design.
3) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

3.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal Resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
TLT807B0EPV (PG-TSDSO-14)							
Junction to case[1]	R_{thJC}	–	14	–	K/W	Measured to heat slug	P_4.3.1
Junction to ambient	R_{thJA}	–	47	–	K/W	FR4 2s2p board[2]	P_4.3.2
Junction to ambient	R_{thJA}	–	143	–	K/W	FR4 1s0p board, footprint only[3]	P_4.3.3
Junction to ambient	R_{thJA}	–	66	–	K/W	FR4 1s0p board, 300 mm² heatsink area[3]	P_4.3.4
Junction to ambient	R_{thJA}	–	56	–	K/W	FR4 1s0p board, 600 mm² heatsink area[3]	P_4.3.5

1) Not subject to production test, specified by design.
2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip and package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.
3) Specified R_{thJA} value is according to Jedec JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 x 70 µm Cu).

4 Block description and electrical characteristics

4.1 Voltage regulation

The output voltage V_Q feeds a resistive divider. The fraction voltage from the output of the resistive divider feeds the ADJ pin. The TLT807B0EPV compares the voltage at the ADJ pin to an internal voltage reference, and drives the pass transistor accordingly.

Stability

The control loop stability of the TLT807B0EPV depends on:

- output capacitor C_Q
- load current
- chip temperature

To ensure stable operation, the output capacitor C_Q must maintain the capacitance and ESR values specified in **"Functional range" on Page 7**. For details see the typical performance graph **Output capacitor series resistor ESR(CQ) versus Output current IQ**. Size the output capacitor according to the application's needs, so that it can buffer load steps.

Compensation for line influence

An input capacitor C_I is recommended to compensate line influence. An additional reverse polarity protection diode and a combination of several capacitors for filtering should be used. Connect the capacitors close to the pins of the TLT807B0EPV.

Current limit

If the output current exceeds the specified limit, for example in case of a short circuit, the TLT807B0EPV limits the output current, which leads to a decrease of the output voltage.

Overtemperature shutdown

In fault condition, for example due to permanent short-circuit at the output, the overtemperature shutdown circuit switches off the power stage to prevent the TLT807B0EPV from immediate destruction. After the TLT807B0EPV cools down, the regulator restarts. If the fault condition persists, oscillatory thermal behaviour occurs. As a consequence, the junction temperature exceeds the specified maximum value, which reduces the lifetime of the TLT807B0EPV significantly.

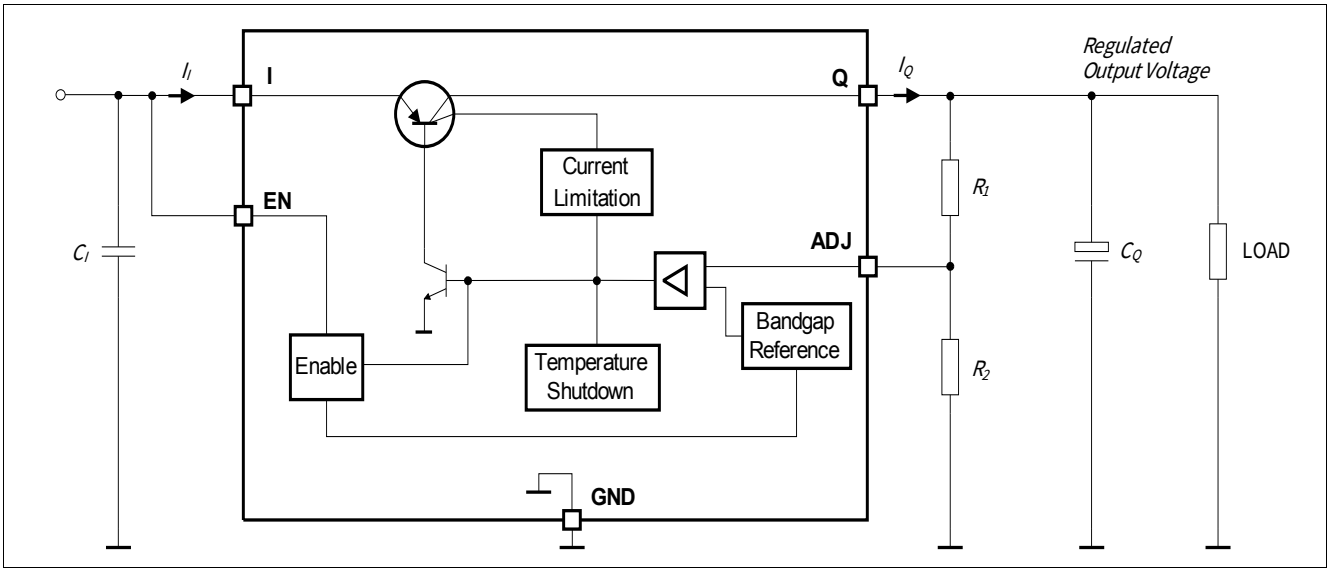


Figure 3 Block diagram voltage regulation

Table 4 Electrical characteristics voltage regulation

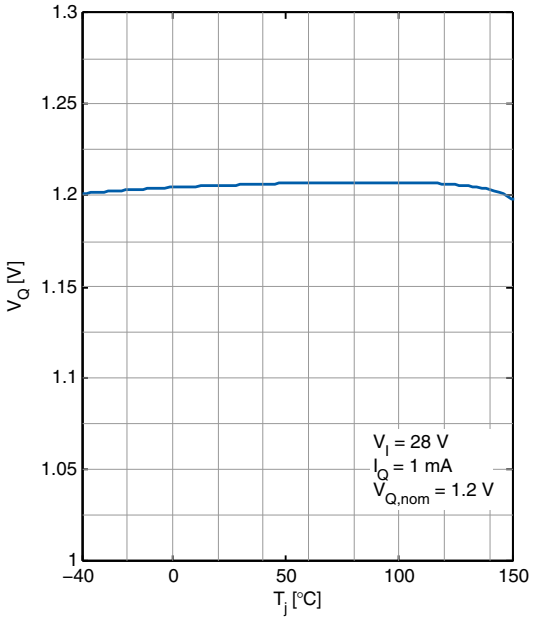
V_I = 28 V; T_j = -40°C to 150°C; all voltages with respect to ground; positive current flowing out of the pin (unless otherwise specified); typical values are given at T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reference voltage	V_{Ref}	–	1.2	–	V	–	P_5.1.1
Output voltage accuracy[1]	V_Q	-2	–	+2	%	100 µA ≤ I_Q ≤ 70 mA, 6 V ≤ V_I ≤ 36 V,	P_5.1.2
Output voltage adjustable range	V_Q	1.2	–	20	V	–	P_5.1.3
Dropout voltage	V_{dr}	–	250	500	mV	I_Q = 70 mA, V_Q = 5 V, V_{dr} = V_I – V_Q [2]	P_5.1.4
Load regulation	$\Delta V_{Q,\,load}$	-30	-10	10	mV	I_Q = 1 mA to 70 mA, V_I = 6 V, V_Q = 5 V	P_5.1.5
Line regulation	$\Delta V_{Q,\,line}$	-20	5	20	mV	V_I = 6 V to 36 V, I_Q = 1 mA, V_Q = 5 V	P_5.1.6
Output current limitation	$I_{Q,max}$	71	160	280	mA	[2]	P_5.1.10
Power Supply Ripple Rejection[3]	*PSRR*	–	60	–	dB	f_r = 100 Hz, V_r = 0.5 Vpp, V_Q = 5 V	P_5.1.11
Overtemperature shutdown threshold	$T_{j,sd}$	151	175	200	°C	T_j increasing	P_5.1.15
Overtemperature shutdown threshold hysteresis	$T_{j,sdh}$	–	15	–	°C	T_j decreasing	P_5.1.16

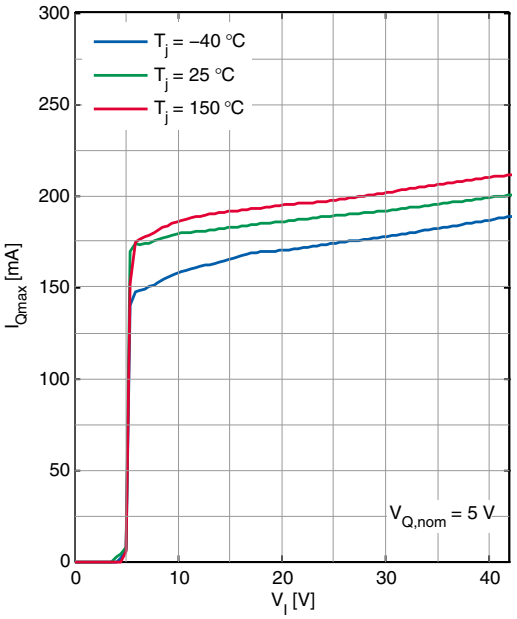
1) Referring to the device tolerance only, the tolerance of the resistor divider can cause additional deviation. Parameter is tested with the ADJ pin directly connected to the output pin Q.
2) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 28 V.
3) Not subject to production test, specified by design.

4.2 Typical performance characteristics voltage regulation

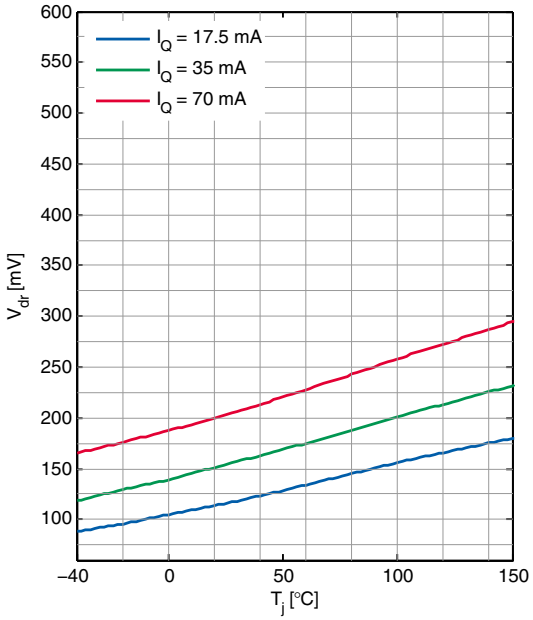
Output voltage V_Q versus Junction temperature T_j



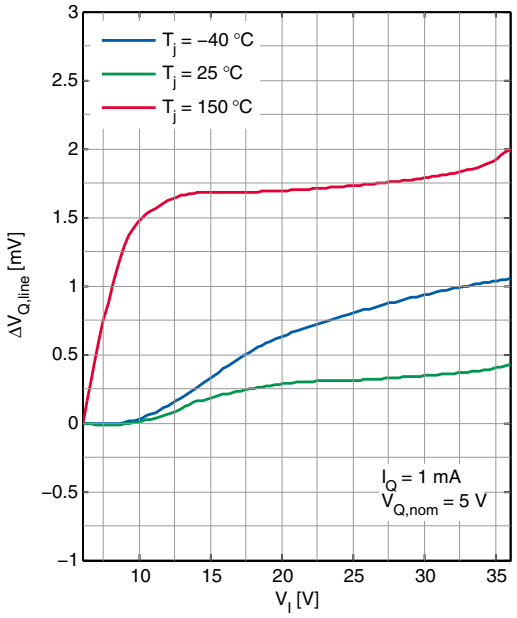
Maximum Output current $I_{Q,max}$ versus Input voltage V_I



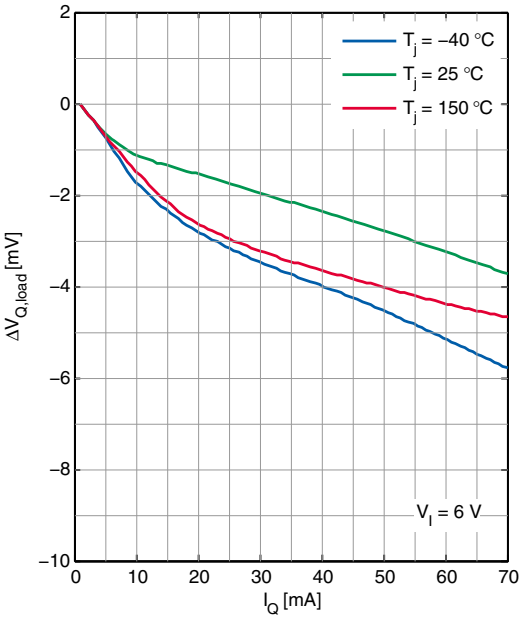
Dropout voltage V_{dr} versus Junction temperature T_j



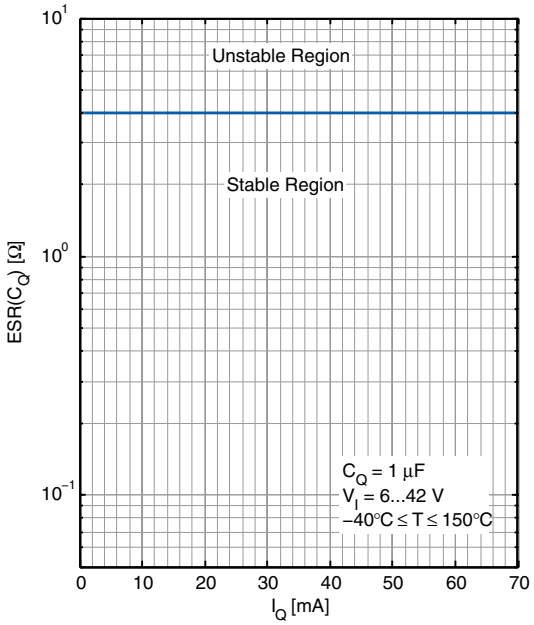
Line regulation $\Delta V_{Q,line}$ versus Input voltage V_I



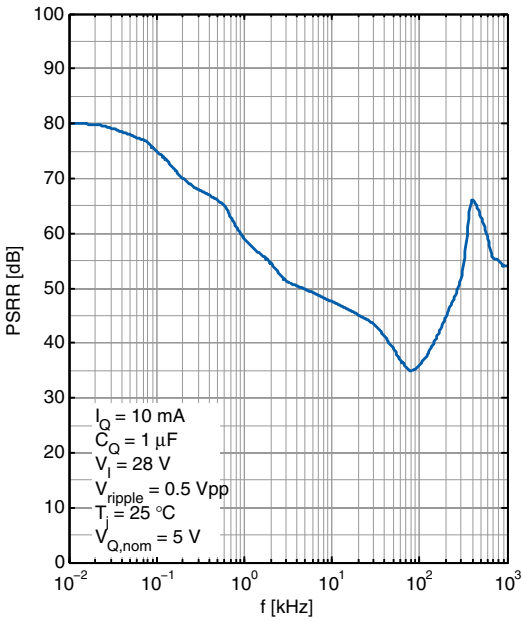
Load regulation $\Delta V_{Q,load}$ versus Output current change I_Q



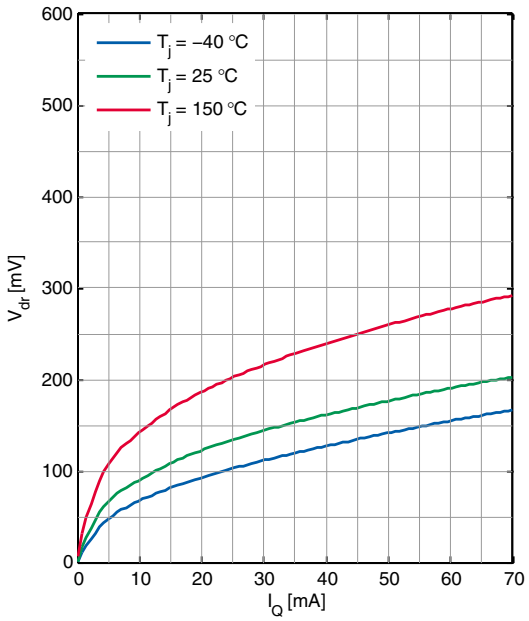
Output capacitor series resistor $ESR(C_Q)$ versus Output current I_Q



Power Supply Ripple Rejection $PSRR$ versus ripple frequency f_r



Drop voltage V_{dr} versus Output current I_Q



4.3 Current consumption

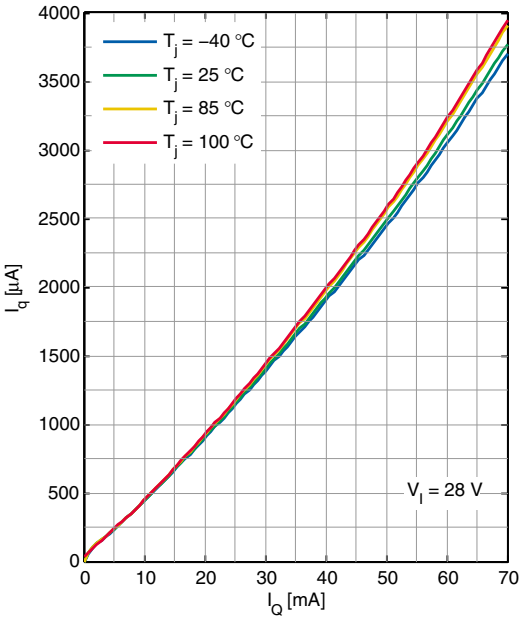
Table 5 Electrical characteristics current consumption

V_I = 28 V; T_j = -40°C to 150°C; all voltages with respect to ground; positive current flowing out of the pin (unless otherwise specified); typical values are given at T_j = 25°C

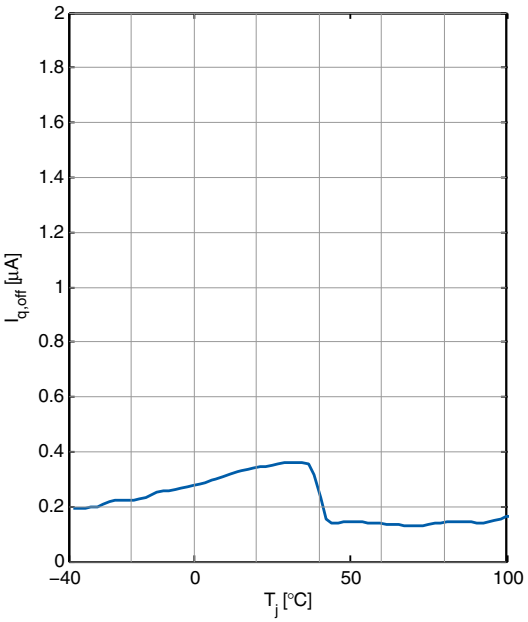
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption $I_q = I_I$	$I_{q,off}$	–	–	1.5	µA	V_{EN} = 0 V, T_j < 100°C	P_5.3.1
Current consumption $I_q = I_I - I_Q$	I_q	–	36	48	µA	I_Q = 100 µA, T_j < 85°C	P_5.3.2
Current consumption $I_q = I_I - I_Q$	I_q	–	36	54	µA	I_Q = 100 µA	P_5.3.3
Current consumption $I_q = I_I - I_Q$	I_q	–	4	6	mA	I_Q = 70 mA	P_5.3.4

4.4 Typical performance characteristics current consumption

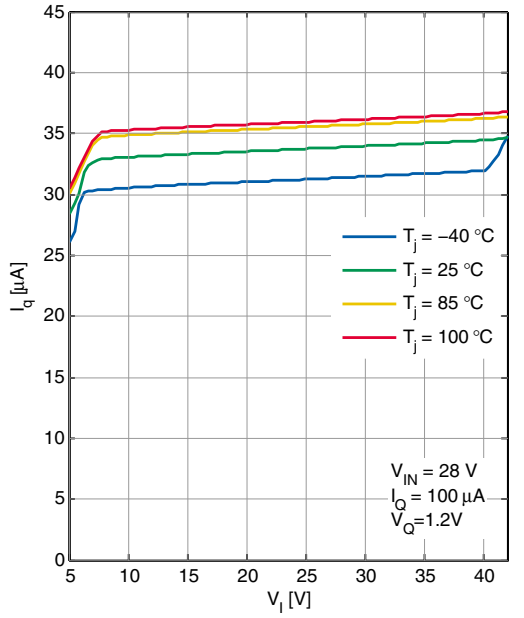
Current consumption I_q versus Output current I_Q



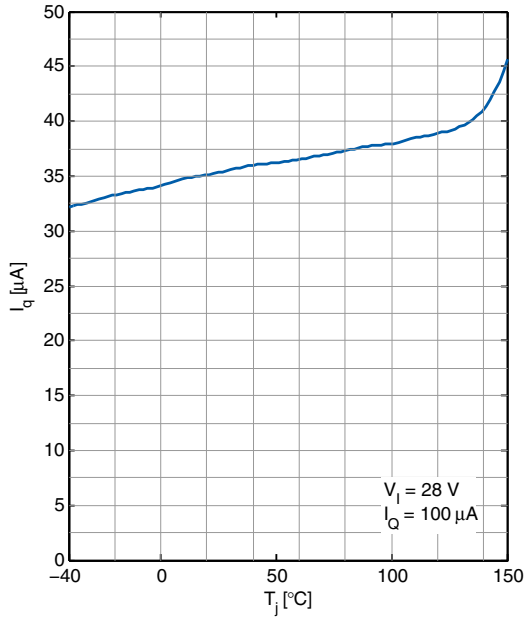
Current consumption $I_{q,off}$ versus Junction temperature T_j



Current consumption I_q versus Input voltage V_I



Current consumption I_q versus Junction temperature T_j



4.5 Enable

The enable feature switches the TLT807B0EPV on and off via the voltage applied to the EN pin:

- connect a “high” signal (for example battery voltage) to enable the TLT807B0EPV
- connect a “low” signal (for example GND) to disable the TLT807B0EPV

The hysteresis of the enable function prevents the TLT807B0EPV from toggling between on-state and off-state due to signals with slow slopes at the EN pin.

Table 6 Electrical characteristics enable

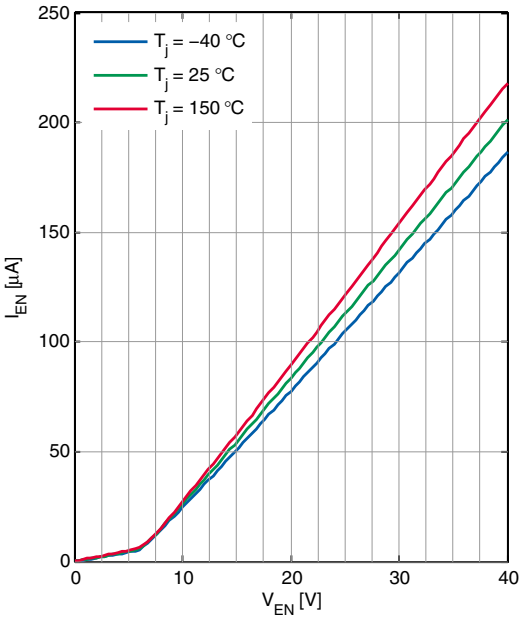
V_I = 28 V; T_j = -40°C to 150°C; all voltages with respect to ground; positive current flowing out of the pin (unless otherwise specified); typical values are given at T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable “high” level voltage	$V_{EN,ON}$	2	–	–	V	–	P_5.5.1
Enable “low” level voltage	$V_{EN,OFF}$	–	–	0.8	V	$T_j \leq 125°C$[1)]	P_5.5.2
Enable “low” level voltage	$V_{EN,OFF}$	–	–	0.4	V	–	P_5.5.3
Enable input current	$I_{EN,ON}$	–	4	8	µA	V_{EN} = 5 V	P_5.5.5

1) Not subject to production test, specified by design.

4.6 Typical performance characteristics enable

Enable input current I_{EN} versus Input voltage V_{EN}



5 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

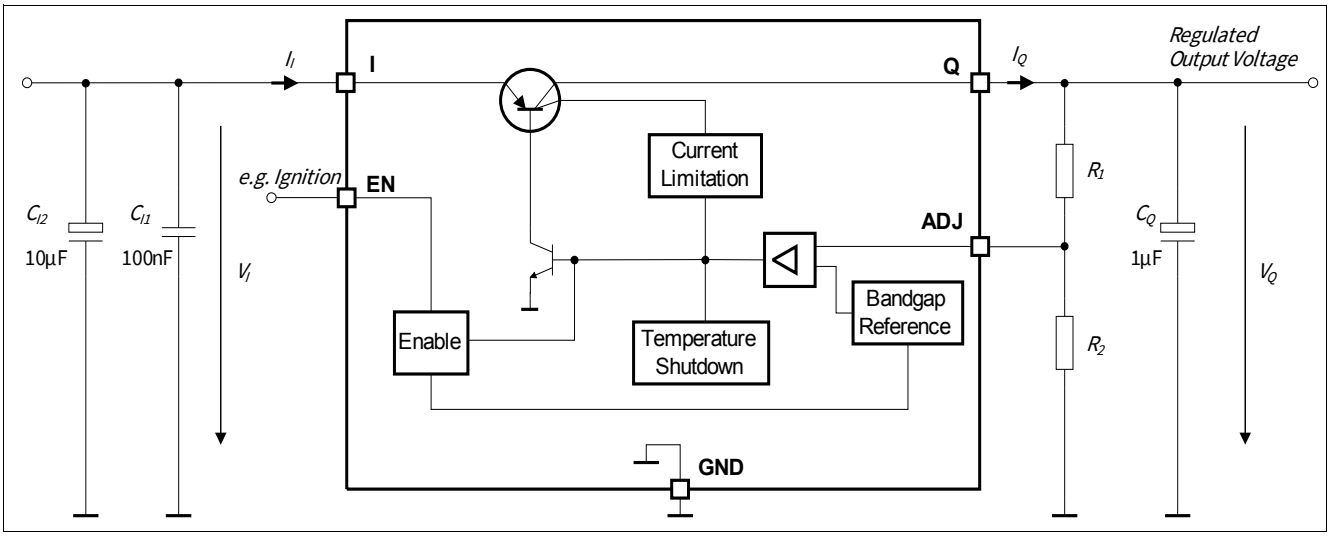


Figure 4 Application diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

The resistor divider for a specific output voltage can be calculated according to **Chapter 5.1**. V_{ADJ} corrseponds to V_{Ref} and is typically 1.2 V. Additionally the sum of the resistor devider should not exceed the value as stated in **Equation (5.2)**.

$$\frac{R_1}{R_2} = \frac{V_Q}{V_{ADJ}} - 1 \tag{5.1}$$

$$R_1 + R_2 \leq 250\,k\Omega \tag{5.2}$$

6 Package information

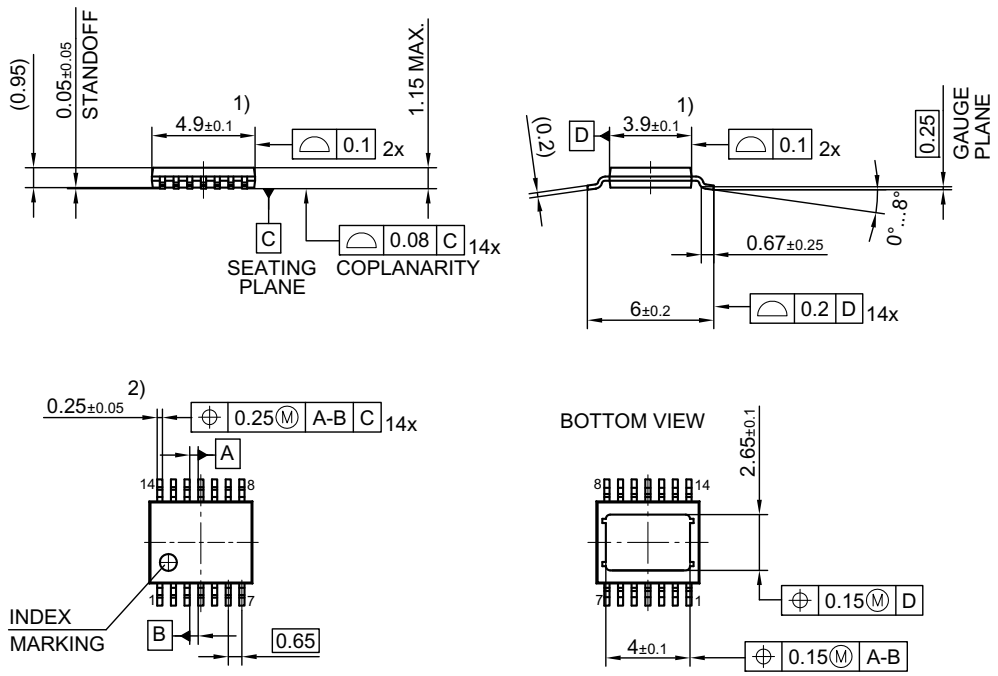


Figure 5 PG-TSDSO-14

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

7 Revision history

Revision	Date	Changes
1.01	2019-03-07	Editorial changes
1.00	2017-05-09	Data Sheet Initial version

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Edition 2019-03-07
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about any aspect of this document?
Email: erratum@infineon.com

Document reference
Z8F54612515

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