DEM-BUF-SOT-1A Demonstration Fixture

1 Description

The DEM-BUF-SOT-1A demonstration fixture is an unpopulated printed circuit board (PCB) for buffers (BUFs) in SOT23-5 packages. Figure 1 shows the package pinout for this PCB. For more information on these op amps, and good PCB board layout techniques, see the individual buffer data sheets.

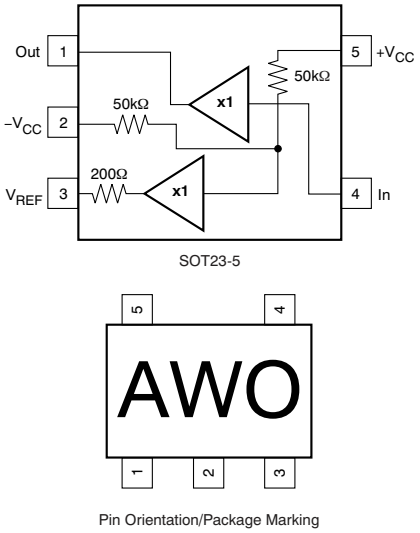


Figure 1. Package Pinout

2 Circuit

The circuit schematic illustrated in Figure 2 shows the connections for all possible components. Each configuration will only use some of the components.

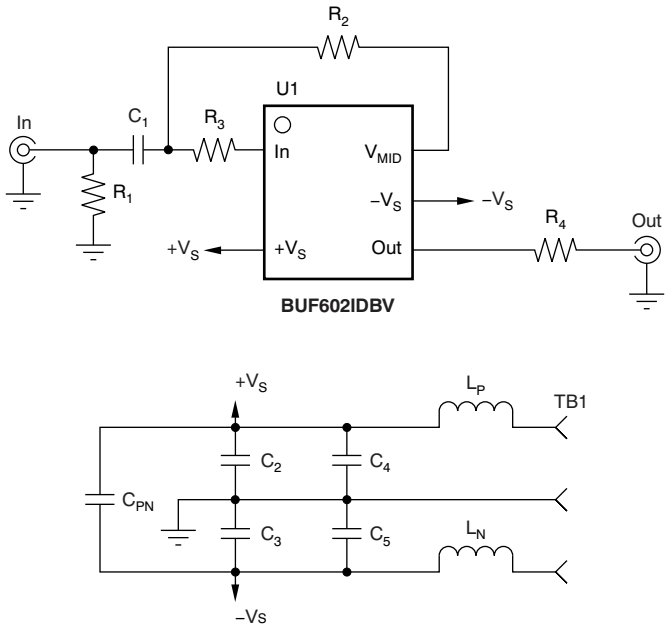


Figure 2. Schematic

3 Components

Components that have RF performance similar to those listed in Table 1 may be substituted.

Table 1. Component Descriptions

PART	DESCRIPTION
C_4, C_5	Tantalum chip capacitor, SMD EIA size 3216, 20V
C_{FN}, C_2, C_3	Multi-layer ceramic chip capacitor, SMD 0805, 50V
In, Out	SMA or SMB board jack (Amphenol 901-144-8)
L_P, L_N	EMI-suppression ferrite chip, SMD 0805 (Steward LI 0805 B 900 R)
TB	Terminal block, 3.5mm centers (On-Shore Technology ED555/3DS)
Rx	Metal film chip resistor, SMD 0603, 1/8W

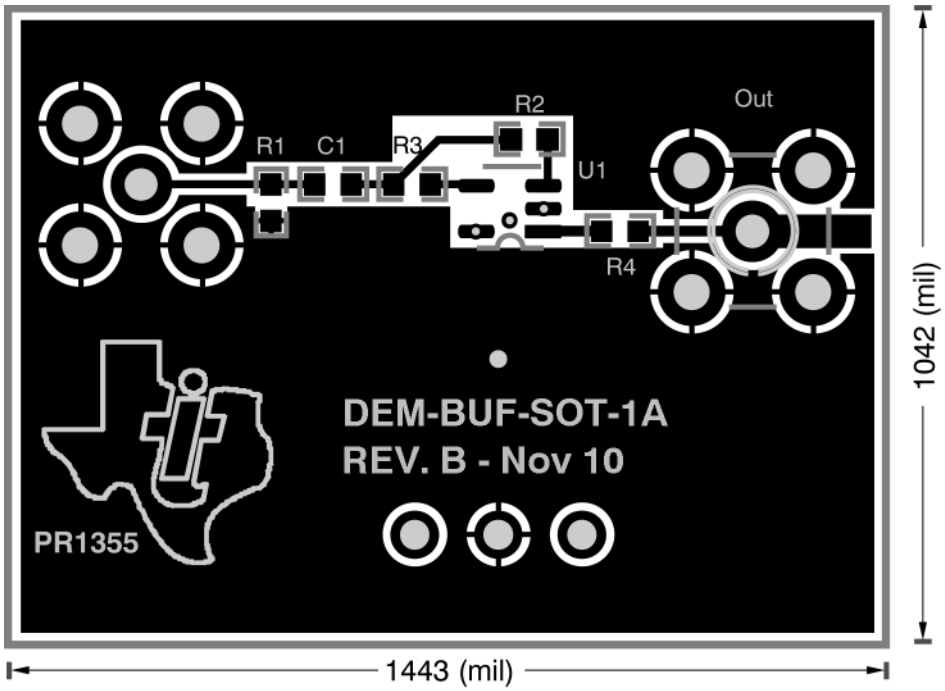
The location of the following components is illustrated in Figure 3. R_1 is the input resistance matching the source impedance. C_1 is a placeholder component, and can be either a 25Ω resistor for DC-coupled applications or a capacitor for AC-coupled applications. When using C_1 for AC-coupled applications, consider using the on-chip mid-reference supply for adequate bypassing. R_4 is the output resistor. R_2 is added to connect the mid-reference supply to the input, if required. L_P and L_N are ferrite chips that can reduce interactions with the power supply at high frequencies; if not desired, they can be replaced with 0Ω resistors. The power supplies are each respectively bypassed with two capacitors: C_2 and C_4 for the positive supply, and C_3 and C_5 for the negative supply. C_4 and C_5 are usually set between 2.2µF and 6.8µF, where C_2 and C_3 are 0.1µF ceramic capacitors. C_{PN}, usually set at 10,000pF, is connected between the positive and negative power supplies.

4 Board Layout

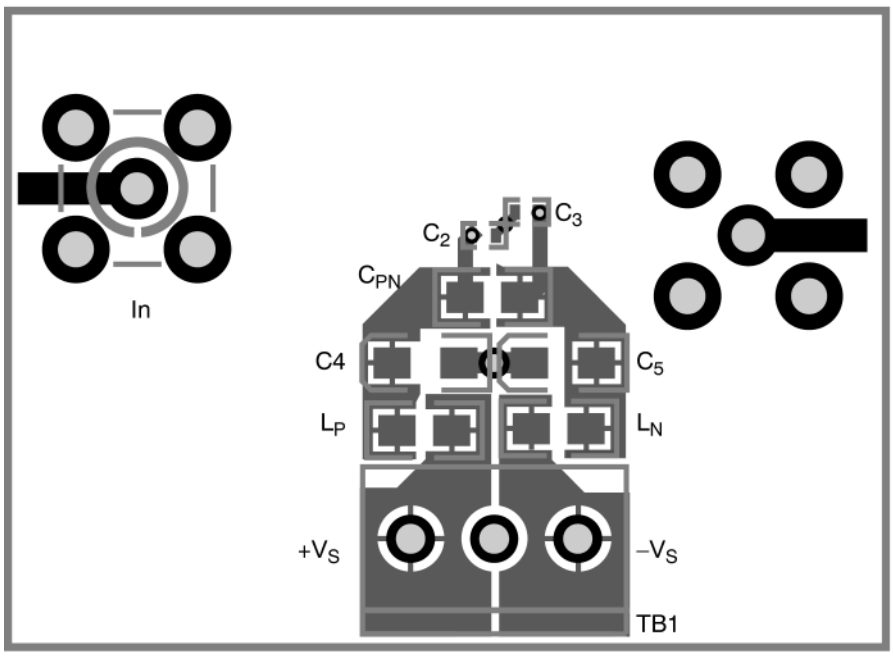
This demonstration fixture is a two-layer PCB. The ground plane has been opened up around op amp pins sensitive to capacitive loading. Power supplies are laid out to keep current-loop areas to a minimum. The SMA (or SMB) connectors may be mounted either vertically or horizontally onto the board edge. The location and type of capacitors used for power-supply bypassing are crucial to high-frequency amplifiers. The tantalum capacitors, C_4 and C_5, do not need to be as close to pins 2 and 5 on the PCB and may be shared with other amplifiers. See the individual op amp data sheets for more information on proper board layout techniques and component selection.

5 Measurement Tips

This demonstration fixture, and the component values shown, is designed to operate in a 50Ω environment. Most data sheet plots are obtained under these conditions. It is easy to change the component values for different input and output impedance levels. Do not use very high impedance probes; they represent a heavy capacitive load to the BUFs and will alter their response. Instead, use low-impedance (≤ 500Ω) probes with adequate bandwidth. The probe input capacitance and resistance set an upper limit on the measurement bandwidth. If a high-impedance probe must be used, place a 100Ω resistor on the probe tip to isolate its capacitance from the circuit.



(a) Top Layer



(b) Bottom Layer

Note: The board name shown in the silkscreen for an earlier version the fixture is DEM-BUF6xxD with the Revision A design finalized in May 2004.

Figure 3. DEM-BUF-SOT-1A Demonstration Board Layout

Revision History

Changes from Original (February, 2006) to A Revision	Page
• Updated Figure 3. Added footnote	4

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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