# INTEGRATED CIRCUITS



Product data Replaces 74ABT16373B/74ABTH16373B of 1998 Feb 27 2004 Feb 27





### 74ABT16373B

#### **FEATURES**

- 16-bit transparent latch
- $\bullet$  Multiple V\_{CC} and GND pins minimize switching noise
- Power-up 3-State
- Live insertion/extraction permitted
- Power-up reset
- 3-State output buffers
- Output capability: +64 mA/-32 mA
- I<sub>CCL</sub> –19 mA maximum
- Latch-up protection exceeds 500 mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

#### DESCRIPTION

The 74ABT16373B high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16373B device is a dual octal transparent latch coupled to two sets of eight 3-State output buffers. The two sections of the device are controlled independently by Enable (nE) and Output Enable (n $\overline{\text{OE}}$ ) control gates.

The data on each set of D inputs are transferred to the latch outputs when the Latch Enable (nE) input is HIGH. The latch remains transparent to the data inputs while nE is HIGH, and stores the data that is present one set-up time before the HIGH-to-LOW enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. Each active-LOW Output Enable ( $n\overline{OE}$ ) controls eight 3-State buffers independent of the latch operation.

When  $n\overline{OE}$  is LOW, the latched or transparent data appears at the outputs. When  $n\overline{OE}$  is HIGH, the outputs are in the high-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN CONFIGURATIO	N		
		1	
1 <del>0</del> E	1 0	48	1E
1Q0	2	47	1D0
1Q1 🗄	3	46	1D1
GND	4	45	GND
1Q2 [	5	44	1D2
1Q3	6	43	1D3
V <sub>CC</sub>	7	42	V <sub>CC</sub>
1Q4	8	41	1D4
1Q5 [	9	40	1D5
GND 1	10	39	GND
1Q6 1	11	38	1D6
1Q7 <b>1</b>	12	37	1D7
2Q0 1	13	36	2D0
2Q1 1	14	35	2D1
GND 1	15	34	GND
2Q2 1	16	33	2D2
2Q3 1	17	32	2D3
V <sub>CC</sub> 1	18	31	V <sub>CC</sub>
2Q4 1	19	30	2D4
2Q5 2	20	29	2D5
GND 2	21	28	GND
2Q6 2	22	27	2D6
2Q7 2	23	26	2D7
2 <del>0E</del> 2	24	25	2E
		I 640	00270

#### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T <sub>amb</sub> = 25 °C; GND = 0 V	TYPICAL	UNIT
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Dn to Qn	$C_L$ = 50 pF; $V_{CC}$ = 5 V	2.5 2.0	ns
C <sub>IN</sub>	Input capacitance	$V_{I} = 0 V \text{ or } V_{CC}$	4	pF
C <sub>OUT</sub>	Output capacitance	$V_{O} = 0 V \text{ or } V_{CC}$ ; 3-State	7	pF
I <sub>CCZ</sub>	Quicecont cumply current	Outputs disabled; $V_{CC} = 5.5 V$	500	μΑ
I <sub>CCL</sub>	Quescent supply current	Outputs low; $V_{CC} = 5.5 V$	8	mA

### ORDERING INFORMATION

 $T_{amb} = -40 \circ C \text{ to } +85 \circ C$ 

Type number	Package	Package			
	Name	Description	Version		
74ABT16373BDL	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1		
74ABT16373BDGG	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1		

### 74ABT16373B

#### **PIN DESCRIPTION**

PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	1 <del>0E</del> , 2 <del>0E</del>	Output enable inputs (active-LOW)
48, 25	1E, 2E	Enable inputs (active-HIGH)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0 V)
7, 18, 31, 42	V <sub>CC</sub>	Positive supply voltage

### LOGIC SYMBOL



### LOGIC DIAGRAM



### LOGIC SYMBOL (IEEE/IEC)



### 74ABT16373B

#### **FUNCTION TABLE**

INPUTS		INTERNAL OUTPUTS			
nOE	nE	nDx	REGISTER	nQ0 – nQ7	OPERATING MODE
L	H H	L H	L H	L H	Enable and read register
L	$\stackrel{\downarrow}{\rightarrow}$	i h	L H	L H	Latch and read register
L	L	Х	NC	NC	Hold
H H	L H	X Dn	NC Dn	Z Z	Disable outputs

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW E transition

L = LOW voltage level

I = LOW voltage level one set-up time prior to the HIGH-to-LOW E transition

NC= No change

X = Don't care

Z = High-impedance "off" state

 $\downarrow$  = HIGH-to-LOW E transition

#### ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +7.0	V
I <sub>IK</sub>	DC input diode current	V <sub>1</sub> < 0 V	-18	mA
VI	DC input voltage <sup>3</sup>		-1.2 to +7.0	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0 V	-50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	output in Off or HIGH state	-0.5 to +5.5	V
	DC output current	output in LOW state	128	<b>m</b> A
'OUT		output in HIGH state	-64	
T <sub>stg</sub>	Storage temperature range		–65 to 150	°C

NOTES:

 Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

 The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

#### **RECOMMENDED OPERATING CONDITIONS**

SYMBOL	DADAMETED		LIMITS		
STMBOL	PARAMETER	MIN	MAX	UNIT	
V <sub>CC</sub>	DC supply voltage	4.5	5.5	V	
VI	Input voltage	0	V <sub>CC</sub>	V	
V <sub>IH</sub>	HIGH-level input voltage	2.0	-	V	
V <sub>IL</sub>	LOW-level Input voltage	-	0.8	V	
I <sub>ОН</sub>	HIGH-level output current	-	-32	mA	
I <sub>OL</sub>	LOW-level output current	-	64	mA	
Δt/Δv	Input transition rise or fall rate	0	10	ns/V	
Tamb	Operating free-air temperature range	-40	+85	°C	

#### Product data

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#### **DC ELECTRICAL CHARACTERISTICS**

SYMBOL	PARAMETER	TEST CONDITIONS	T <sub>amb</sub> = +25 °C			T <sub>amb</sub> = −40 °C to +85 °C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>IK</sub>	Input clamp voltage	$V_{CC} = 4.5 \text{ V}; I_{IK} = -18 \text{ mA}$	-	-0.9	-1.2		-1.2	V
		$V_{CC}$ = 4.5 V; $I_{OH}$ = –3 mA; $V_{I}$ = $V_{IL}$ or $V_{IH}$	2.5	2.9	-	2.5	-	V
V <sub>OH</sub>	High-level output voltage	$V_{CC}$ = 5.0 V; $I_{OH}$ = -3 mA; $V_I$ = $V_{IL}$ or $V_{IH}$	3.0	3.4	-	3.0	-	V
		$V_{CC}$ = 4.5 V; $I_{OH}$ = –32 mA; $V_{I}$ = $V_{IL}$ or $V_{IH}$	2.0	2.4	-	2.0	-	V
V <sub>OL</sub>	Low-level output voltage	$V_{CC}$ = 4.5 V; $I_{OL}$ = 64 mA; $V_{I}$ = $V_{IL}$ or $V_{IH}$	-	0.42	0.55	-	0.55	V
V <sub>RST</sub>	Power-up output voltage <sup>3</sup>	$V_{CC}$ = 5.5 V; $I_{O}$ = 1 mA; $V_{I}$ = GND or $V_{CC}$	-	0.13	0.55	-	0.55	V
lı	Input leakage current	$V_{CC}$ = 5.5 V; $V_{I}$ = $V_{CC}$ or GND	-	±0.01	±1	-	±1	μA
I <sub>OFF</sub>	Power-off leakage current	$V_{CC}$ = 0.0 V; $V_O$ or $V_I$ $\leq$ 4.5 V	-	±5.0	±100	-	±100	μA
I <sub>PU</sub> /I <sub>PD</sub>	Power-up/down 3-State output current <sup>4</sup>	$V_{CC}$ = 2.1 V; $V_{O}$ = 0.5 V; $V_{I}$ = GND or $V_{CC};$ $V_{OE}$ = GND	-	±5.0	±50	-	±50	μΑ
I <sub>OZH</sub>	3-State output HIGH current	$V_{CC}$ = 5.5 V; $V_{O}$ = 5.5 V; $V_{I}$ = $V_{IL}$ or $V_{IH}$	-	0.5	10	-	10	μΑ
I <sub>OZL</sub>	3-State output LOW current	$V_{CC}$ = 5.5 V; $V_{O}$ = 0.0 V; $V_{I}$ = $V_{IL}$ or $V_{IH}$	-	-0.5	-10		-10	μA
Ι <sub>Ο</sub>	Output current <sup>1</sup>	$V_{CC} = 5.5 \text{ V}; V_{O} = 2.5 \text{ V}$	-50	-70	-180	-50	-180	mA
I <sub>CEX</sub>	Output HIGH leakage current	$V_{CC}$ = 5.5 V; $V_{O}$ = 5.5 V; $V_{I}$ = GND or $V_{CC}$	-	0.1	50	-	50	μΑ
Іссн		$V_{CC}$ = 5.5 V; Outputs HIGH; V <sub>I</sub> = GND or V <sub>CC</sub>	-	0.5	2	-	2	mA
I <sub>CCL</sub>	Quiescent supply current	$V_{CC}$ = 5.5 V; Outputs Low; V <sub>I</sub> = GND or V <sub>CC</sub>	-	8	19	-	19	mA
I <sub>CCZ</sub>		$V_{CC}$ = 5.5 V; Outputs 3-State; V <sub>I</sub> = GND or V <sub>CC</sub>	-	0.5	2	-	2	mA
Δl <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	$V_{CC}$ = 5.5 V; one input at 3.4 V, other inputs at $V_{CC}$ or GND	-	5	100	_	100	μΑ

NOTES:

Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
 This is the increase in supply current for each input at 3.4 V.

This is the increase in supply current for each input at 3.4 v.
 For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
 This parameter is valid for any V<sub>CC</sub> between 0 V and 2.1 V, with a transition time of up to 10 msec. From V<sub>CC</sub> = 2.1 to V<sub>CC</sub> = 5 V ± 10% a transition time of up to 100 µsec is permitted.
 Unused pins at V<sub>CC</sub> or GND.

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### AC CHARACTERISTICS

GND = 0 V,  $t_R$  =  $t_F$  = 2.5 ns,  $C_L$  = 50 pF,  $R_L$  = 500  $\Omega$ 

			LIMITS					
SYMBOL	PARAMETER	WAVEFORM	T <sub>amb</sub> = +25 °C V <sub>CC</sub> = +5.0 V			T <sub>amb</sub> = -40 ° V <sub>CC</sub> = +5.	UNIT	
			MIN	ТҮР	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay nDx to nQx	2	1.5 1.1	2.5 2.0	3.8 3.1	1.5 1.1	4.4 3.8	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay nE to nQx	1	1.6 1.3	2.5 2.1	3.8 3.1	1.6 1.3	4.4 3.6	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to HIGH and LOW level	4 5	1.2 1.3	2.3 2.3	3.5 3.5	1.2 1.3	4.6 4.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from HIGH and LOW level	4 5	1.9 1.7	3.1 2.6	4.5 3.8	1.9 1.7	5.3 4.2	ns

### AC SET-UP REQUIREMENTS

GND = 0 V,  $t_R = t_F$  = 2.5 ns,  $C_L$  = 50 pF,  $R_L$  = 500  $\Omega$ 

			LIMITS				
SYMBOL	PARAMETER	WAVEFORM	T <sub>amb</sub> = V <sub>CC</sub> =	= +25 °C = +5.0 V	$T_{amb}$ = -40 °C to +85 °C V <sub>CC</sub> = +5.0 V ± 0.5 V	UNIT	
			MIN	ТҮР	MIN		
t <sub>s</sub> (H) t <sub>s</sub> (L)	Set-up time, HIGH or LOW nDx to nE	3	1.0 1.0	0.0 0.3	1.0 1.0	ns	
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, HIGH or LOW nDx to nE	3	0.5 0.5	-0.2 0.0	0.5 0.5	ns	
t <sub>w</sub> (H)	Enable pulse width HIGH	1	2.5	1.0	2.5	ns	

#### AC WAVEFORMS

For all waveforms,  $V_M = 1.5$  V.



Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



Waveform 2. Propagation Delay for Data to Outputs

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# 16-bit transparent latch (3-State)



Waveform 3. **Data Set-up and Hold Times** 



Waveform 4. 3-State Output Enable Time to HIGH Level and Output Disable Time from HIGH Level

### **TEST CIRCUIT AND WAVEFORM**



Waveform 5. 3-State Output Enable Time to LOW Level and Output Disable Time from LOW Level



- C<sub>L</sub> = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- Termination resistance should be equal to Z<sub>OUT</sub> of R<sub>T</sub> = pulse generators.

500 ns	2.5 ns	2.5 ns
		SA00654

tw

1 MHz

74ABT

3.0 V

### 74ABT16373B



### 74ABT16373B



# 74ABT16373B

### **REVISION HISTORY**

Rev	Date	Description
_3	20040227	Product data (9397 750 12821); 853-1751 ECN 01–A15429 of 27 January 2004. Replaces data sheet 74ABT_H16373B_2 of 1998 Feb 27 (9397 750 03491). Modifications:
		<ul> <li>Delete all references to 74ABTH16373B (product discontinued).</li> </ul>
_2	19980227	Product specification (9397 750 03491); ECN 853-1751 19027 of 27 February 1998. Supersedes data of 1995 Aug 03.
_1	19950803	

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#### Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 01-04

9397 750 12985

Document order number:

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