National Semiconductor

July 2001

# CLC405
# Low Cost, Low Power, 110MHz Op Amp with Disable

## General Description

The CLC405 is a low cost, wideband (110MHz) op amp featuring a TTL-compatible disable which quickly switches off in 18ns and back on in 40ns. While disabled, the CLC405 has a very high input/output impedance and its total power consumption drops to a mere 8mW. When enabled, the CLC405 consumes only 35mW and can source or sink an output current of 60mA. These features make the CLC405 a versatile, high speed solution for demanding applications that are sensitive to both power and cost.

Utilizing National's proven architectures, this current feedback amplifier surpasses the performance of alternative solutions and sets new standards for low power at a low price. This power conserving op amp achieves low distortion with −72dBc and −70dBc for second and third harmonics respectively. Many high source impedance applications will benefit from the CLC405's 6MΩ input impedance. And finally, designers will have a bipolar part with an exceptionally low 100nA non-inverting bias current.

With 0.1dB flatness to 50MHz and low differential gain and phase errors, the CLC405 is an ideal part for professional video processing and distribution. However, the 110MHz −3dB bandwidth ($A_V$ = +2) coupled with a 350V/µs slew rate also make the CLC405 a perfect choice in cost sensitive applications such as video monitors, fax machines, copiers, and CATV systems.

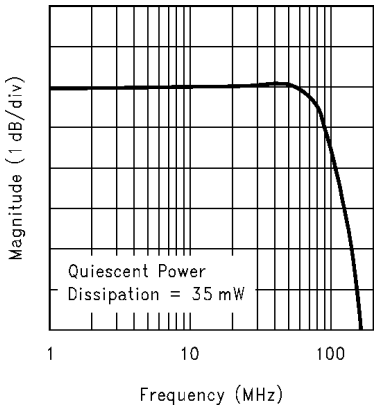
## Features

- Low cost
- Very low input bias current:100nA
- High input impedance: 6MΩ
- 110MHz −3dB bandwidth ($A_v$=+2)
- Low power: $I_{cc}$=3.5mA
- Ultra fast enable/disable times
- High output current: 60mA

## Applications

- Desktop video systems
- Multiplexers
- Video distribution
- Flash A/D driver
- High speed switch/driver
- High source impedance applications
- Peak detector circuits
- Professional video processing
- High resolution monitors

**Frequency Response ($A_V$ = +2V/V)**

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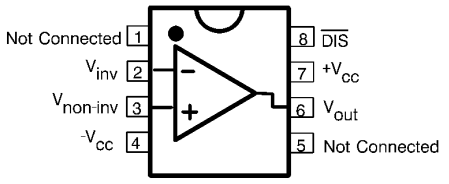
## Connection Diagram

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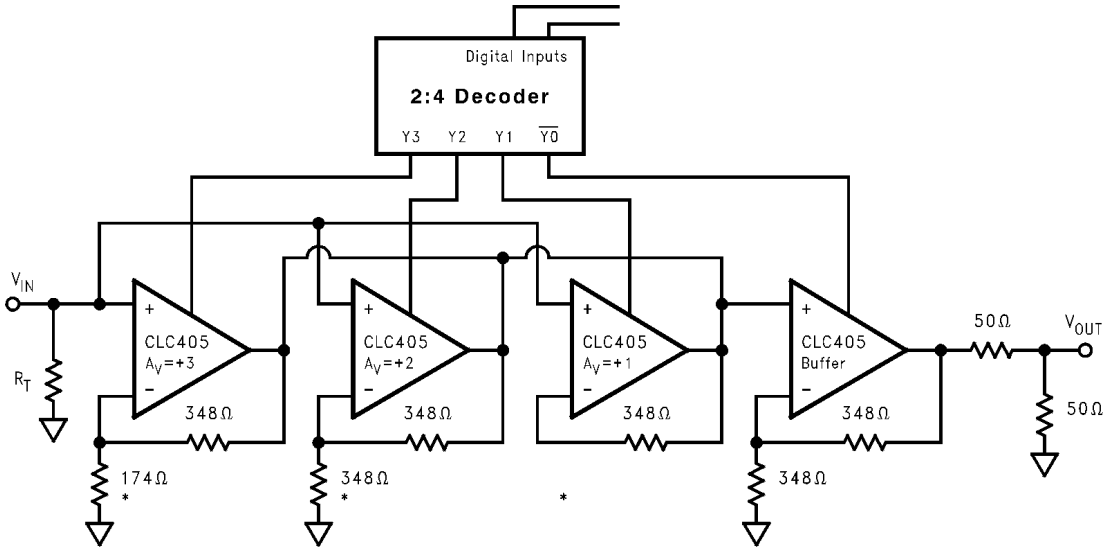
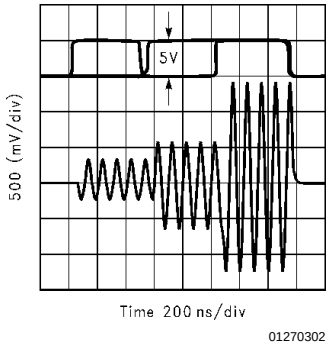
**Pinout**
**DIP & SOIC**

## Typical Application




**Wideband Digitally Controlled Programmable Gain Amplifier**




**Channel Switching**

## Ordering Information

| Package | Temperature Range Industrial | Part Number | Package Marking | NSC Drawing |
|---|---|---|---|---|
| 8-pin plastic DIP | −40˚C to +85˚C | CLC405AJP | CLC405AJP | N08E |
| 8-pin plastic SOIC | −40˚C to +85˚C | CLC405AJE | CLC405AJE | M08A |

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | ±7V |
| $I_{OUT}$ is short circuit protected to ground | |
| Common Mode Input Voltage | $\pm V_{CC}$ |
| Junction Temperature | +150˚C |
| Storage Temperature Range | −65˚C to +150˚C |
| Lead Temperature (soldering 10 sec) | +300˚C |

## Operating Ratings

| Thermal Resistance | | |
|---|---|---|
| Package | ($\theta_{JC}$) | ($\theta_{JA}$) |
| MDIP | 75˚C/W | 130˚C/W |
| SOIC | 130˚C/W | 150˚C/W |

## Electrical Characteristics

$A_V$ = +2, $R_f$ = 348Ω: $V_{CC}$ = ±5V, $R_L$ = 100Ω unless specified

| Notes | Parameter | | Conditions | Typ | Min/Max (Note 2) | | | Units |
|---|---|---|---|---|---|---|---|---|
| Ambient Temperature | | | CLC405AJ | +25˚C | +25˚C | 0 to 70˚C | −40 to 85˚C | |
| **Frequency Domain Response** | | | | | | | | |
| | −3dB Bandwidth | | $V_{OUT}$ <1.0$V_{PP}$ | 110 | 75 | 50 | 45 | MHz |
| (Note 3) | | | $V_{OUT}$ < 5.0$V_{PP}$ | 42 | 31 | 27 | 26 | MHz |
| | −3dB Bandwidth $A_V$ = +1 | | $V_{OUT}$ <0.5$V_{PP}$ ($R_f$ = 2K) | 135 | – | – | – | MHz |
| | ±0.1dB Bandwidth | | $V_{OUT}$ < 1.0$V_{PP}$ | 50 | 15 | – | – | MHz |
| | Gain Flatness | | $V_{OUT}$<1.0$V_{PP}$ | | | | | |
| | Peaking | | DC to 200MHz | 0 | 0.6 | 0.8 | 1.0 | dB |
| | Rolloff | | <30MHz | 0.05 | 0.3 | 0.4 | 0.5 | dB |
| | Linear Phase Deviation | | <20MHz | 0.3 | 0.6 | 0.7 | 0.7 | deg |
| | Differential Gain | | NTSC, $R_L$ = 150Ω | 0.01 | 0.03 | 0.04 | 0.05 | % |
| (Note 4) | | | NTSC, $R_L$ = 150Ω | 0.01 | | | | % |
| | Differential Phase | | NTSC, $R_L$=150Ω | 0.25 | 0.4 | 0.5 | 0.55 | deg |
| (Note 4) | | | NTSC, $R_L$ = 150Ω | 0.08 | | | | deg |
| **Time Domain Response** | | | | | | | | |
| | Rise and Fall Time | | 2V Step | 5 | 7.5 | 8.2 | 8.4 | ns |
| | Settling Time to 0.05% | | 2V Step | 18 | 27 | 36 | 39 | ns |
| | Overshoot | | 2V Step | 3 | 12 | 12 | 12 | % |
| | Slew Rate | $A_V$ = +2 | 2V Step | 350 | 260 | 225 | 215 | V/µs |
| | | $A_V$ = −1 | 1V Step | 650 | – | – | – | V/µs |
| **Distortion And Noise Response** | | | | | | | | |
| (Note 5) | 2nd Harmonic Distortion | | $2V_{PP}$, 1MHz/10MHz | −72/−52 | −46 | −45 | −44 | dBc |
| (Note 5) | 3rd Harmonic Distortion | | $2V_{PP}$, 1MHz/10MHz | −70/−57 | −50 | −47 | −46 | dBc |
| | Equivalent Input Noise | | | | | | | |
| | Non-Inverting Voltage | | >1MHz | 5 | 6.3 | 6.6 | 6.7 | nV/$\sqrt{Hz}$ |
| | Inverting Current | | >1MHz | 12 | 15 | 16 | 17 | pA/$\sqrt{Hz}$ |
| | Non-Inverting Current | | >1MHz | 3 | 3.8 | 4 | 4.2 | pA/$\sqrt{Hz}$ |
| **Static DC Performance** | | | | | | | | |
| (Note 6) | Input Offset Voltage | | | 1 | 5 | 7 | 8 | mV |
| | Average Drift | | | 30 | 50 | | 50 | µV/˚C |
| (Note 6) | Input Bias Current | | Non-Inverting | 100 | 900 | 1600 | 2800 | nA |
| | Average Drift | | | 3 | | 8 | 11 | nA/˚C |
| (Note 6) | Input Bias Current | | Inverting | 1 | 5 | 7 | 10 | µA |
| | Average Drift | | | 17 | | 40 | 45 | nA/˚C |

## Electrical Characteristics (Continued)

$A_V$ = +2, $R_f$ = 348Ω: $V_{CC}$ = ±5V, $R_L$ = 100Ω unless specified

| Notes | Parameter | Conditions | Typ | Min/Max (Note 2) | | | Units |
|---|---|---|---|---|---|---|---|
| | Power Supply Rejection Ratio | DC | 52 | 47 | 46 | 45 | dB |
| | Common Mode Rejection Ratio | DC | 50 | 45 | 44 | 43 | dB |
| (Note 6) | Supply Current | $R_L$ = ∞ | 3.5 | 4.0 | 4.1 | 4.4 | mA |
| (Note 6) | Disabled | $R_L$ = ∞ | 0.8 | 0.9 | 0.95 | 1 | mA |
| **Switching DC Performance** | | | | | | | |
| | Turn On Time | | 40 | 55 | 58 | 58 | ns |
| | Turn Off Time | to > 50dB attn. @ 10MHz | 18 | 26 | 30 | 32 | ns |
| | Off Isolation | 10MHz | 59 | 55 | 55 | 55 | dB |
| | High Input Voltage | $V_{IH}$ | | 2 | 2 | 2 | V |
| | Low Input Voltage | $V_{IL}$ | | 0.8 | 0.8 | 0.8 | V |
| **Miscellaneous Performance** | | | | | | | |
| | Input Resistance | Non- Inverting | 6 | 3 | 2.4 | 1 | MΩ |
| | Input Resistance | Inverting | 182 | | | | Ω |
| | Input Capacitance | Non- Inverting | 1 | 2 | 2 | 2 | pF |
| | Common Mode Input Range | | ±2.2 | 1.8 | 1.7 | 1.5 | V |
| | Output Voltage Range | $R_L$ = 100Ω | +3.5,−2.8 | +3.1,−2.7 | +2.9,−2.6 | +2.4,−1.6 | V |
| | Output Voltage Range | $R_L$ = ∞ | +4.0,−3.3 | +3.9,−3.2 | +3.8,−3.1 | +3.7,−2.8 | V |
| | Output Current | | 40 | 40 | 38 | 20 | mA |
| | Output Resistance, Closed Loop | | 0.06 | 0.2 | 0.25 | 0.4 | Ω |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

**Note 2:** Max/min ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

**Note 3:** At temps <0˚C, spec is guaranteed for $R_L$ 500Ω.

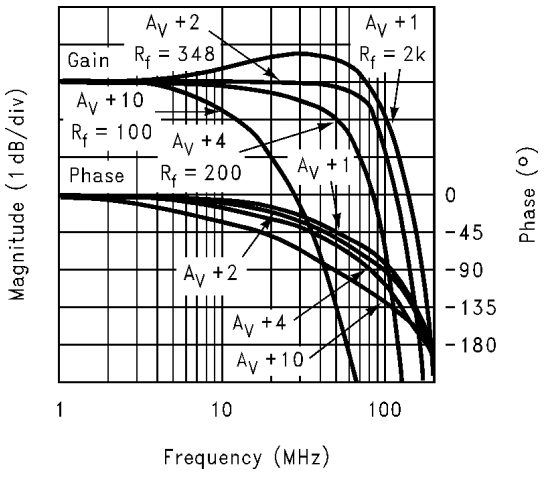
**Note 4:** An 825Ω=pull-down resistor is connected between $V_O$ and − $V_{CC}$

**Note 5:** Guaranteed at 10MHz

**Note 6:** AJ-level: spec. is 100% tested at +25˚C.

## Typical Performance Characteristics ($A_V$ = +2, $R_f$ = 348Ω: $V_{CC}$ = ±5V, $R_L$ = 100Ω Unless Specified).

**Non-Inverting Frequency Response**

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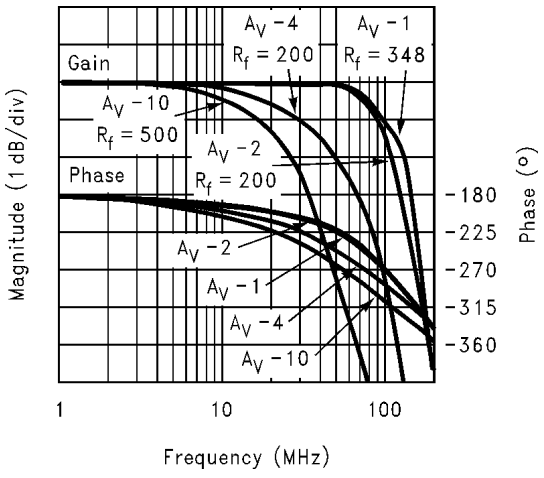
**Inverting Frequency Response**

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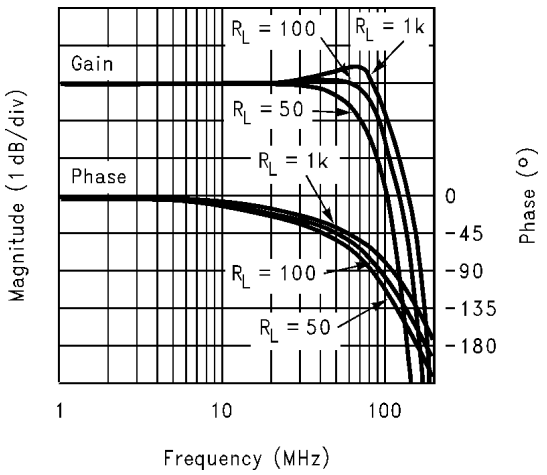
## Typical Performance Characteristics ($A_V$ = +2, $R_f$ = 348Ω: $V_{CC}$ = ±5V, $R_L$ = 100Ω Unless Specified). (Continued)

**Frequency Response for Various $R_L$S**

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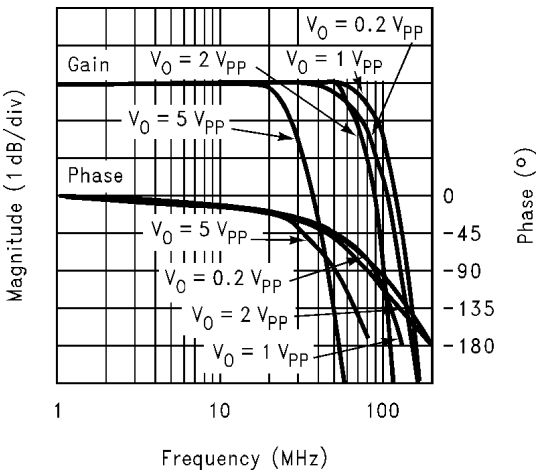
**Frequency Response vs. $V_{OUT}$**

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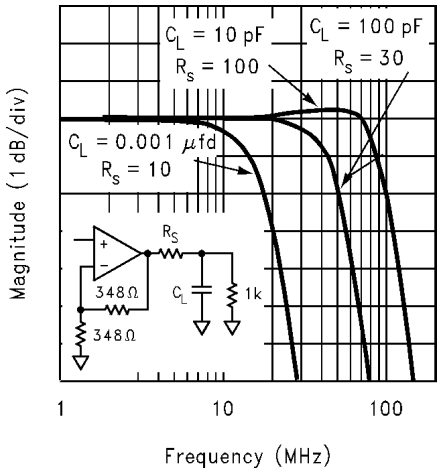
**Frequency Response vs. Capacitive Load**

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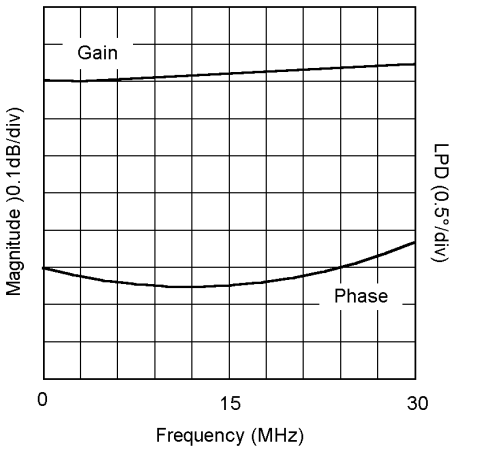
**Gain Flatness & Linear Phase Deviation**

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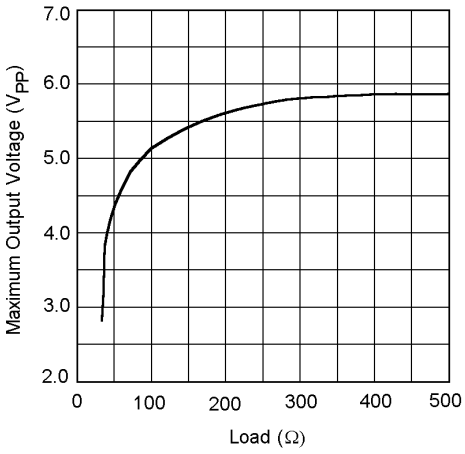
**Maximum Output Voltage vs. $R_L$**

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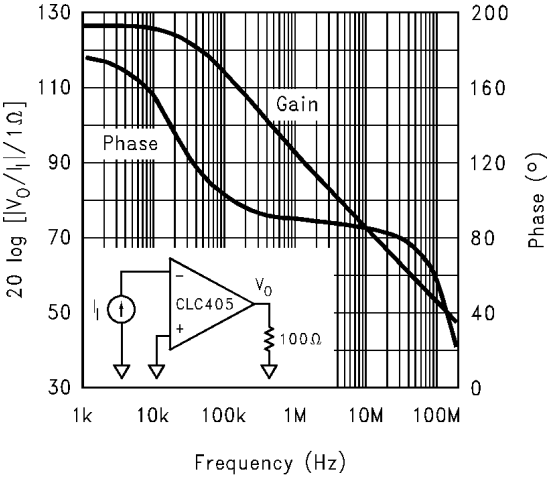
**Open Loop Transimpedance Gain, Z(s)**

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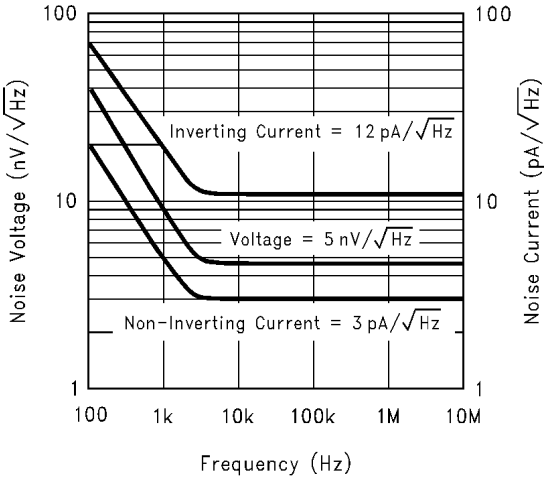
## Typical Performance Characteristics ($A_V$ = +2, $R_f$ = 348Ω: $V_{CC}$ = ±5V, $R_L$ = 100Ω Unless Specified). (Continued)

**Equivalent Input Noise**

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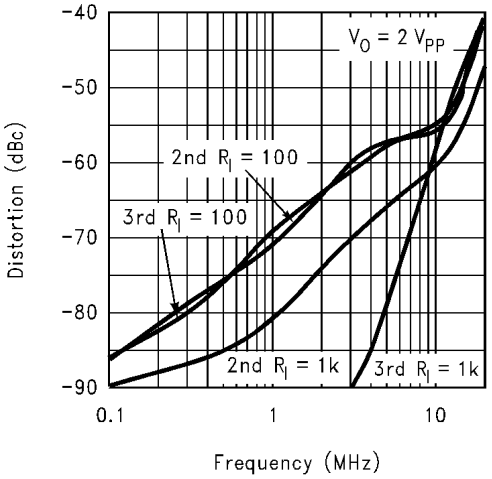
**2nd & 3rd Harmonic Distortion**

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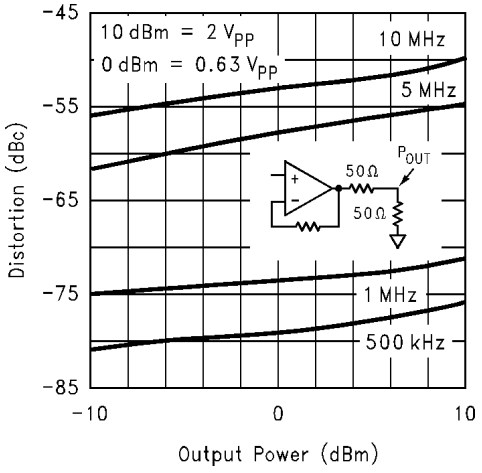
**2nd Harmonic Distortion vs. $P_{OUT}$**

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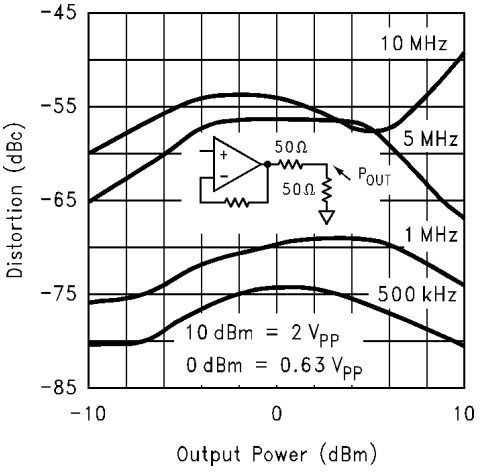
**3rd Harmonic Distortion vs. $P_{OUT}$**

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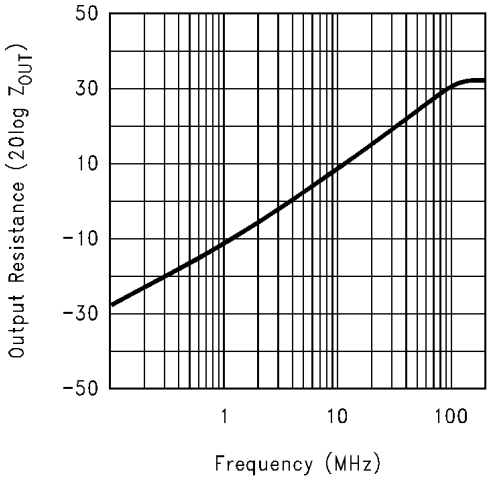
**Output Resistance vs. Frequency**

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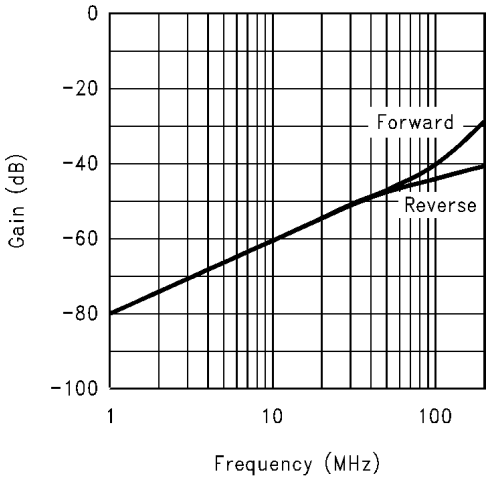
**Forward and Reverse Gain During Disable**

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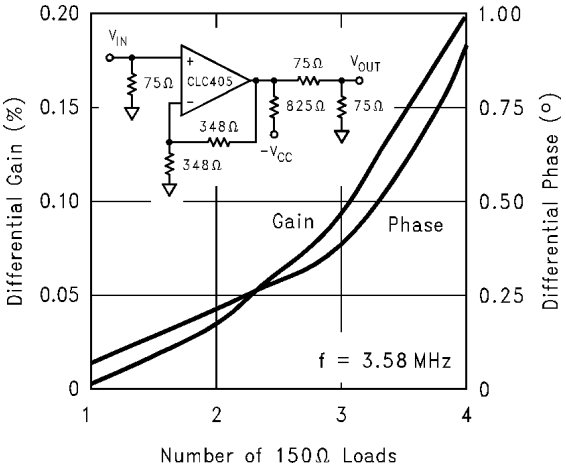
## Typical Performance Characteristics ($A_V$ = +2, $R_f$ = 348Ω: $V_{CC}$ = ±5V, $R_L$ = 100Ω Unless Specified). (Continued)

**Differential Gain and Phase**

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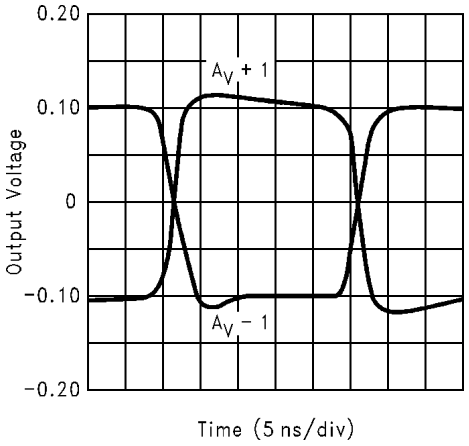
**Small Signal Pulse Response**

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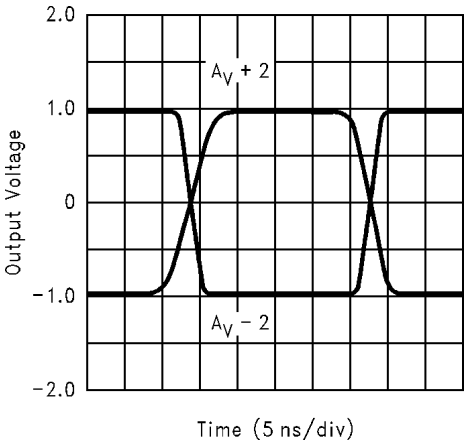
**Large Signal Pulse Response**

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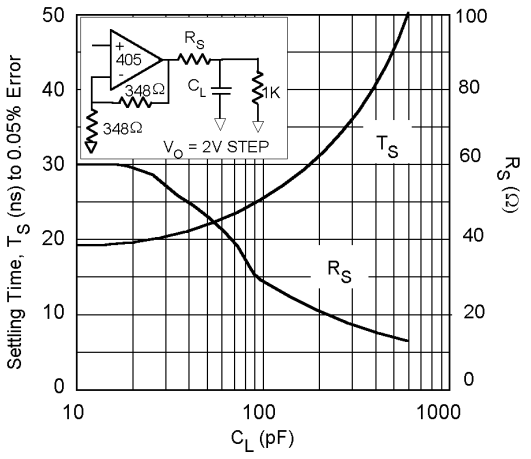
**Settling Time vs. Capacitive Load**

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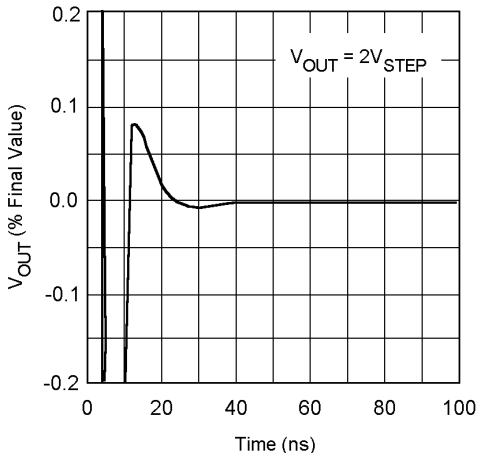
**Short Term Settling Time**

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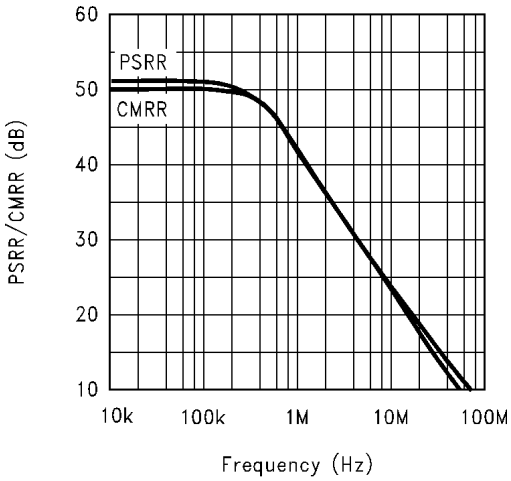
**PSRR and CMRR**

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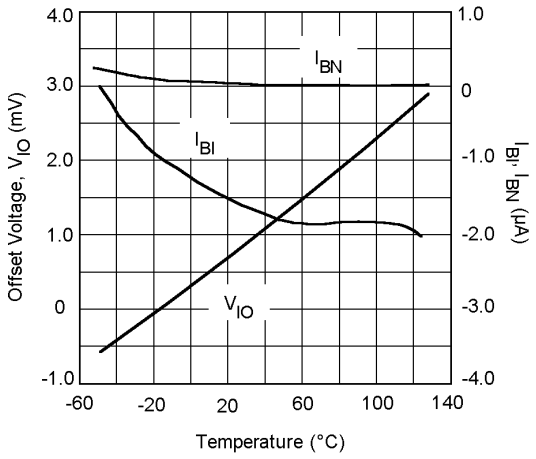
## Typical Performance Characteristics ($A_V$ = +2, $R_f$ = 348Ω: $V_{CC}$ = ±5V, $R_L$ = 100Ω Unless Specified). (Continued)

**$I_{BI}$, $I_{BN}$, $V_{IO}$ vs. Temperature**

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## Application Division

### Feedback Resistor

The feedback resistor, $R_f$, determines the loop gain and frequency response for a current feedback amplifier. Unless otherwise stated, the performance plots and data sheet specify CLC405 operation with $R_f$ of 348Ω at a gain of +2V/V. Optimize frequency response for different gains by changing $R_f$. Decrease to peak frequency response and extend bandwidth. Increase $R_f$ to roll off the frequency response and decrease bandwidth. Use a 2kΩ $R_f$ for unity gain, voltage follower circuits.

Use application note OA-13 to optimize your $R_f$ selection. The equations in this note are a good starting point for selecting $R_f$. The value for the inverting input impedance for OA-13 is approximately 182Ω.

### Enable/Disable Operation Using ±5V Supplies

The CLC405 has a TTL & CMOS logic compatible disable function. Apply a logic low (i.e. <0.8V) to pin 8, and the CLC405 is guaranteed disabled across its temperature range. Apply a logic high to pin 8, (i.e. >2.0V) and the CLC405 is guaranteed enabled. Voltage, not current, at pin 8 determines the enable/disable state of the CLC405.

Disable the CLC405 and its inputs and output become high impedances. While, disabled, the CLC405's quiescent power drops to 8mW.

Use the CLC405's disable to create analog switches or multiplexers. Implement a single analog switch with one CLC405 positioned between an input and output. Create an analog multiplexer with several CLC405s. Tie the outputs together and put a different signal on each CLC405 input.

Operate the CLC405 without connecting pin 8. An internal 20kΩ pull-up resistor guarantees the CLC405 is enabled when pin 8 is floating.

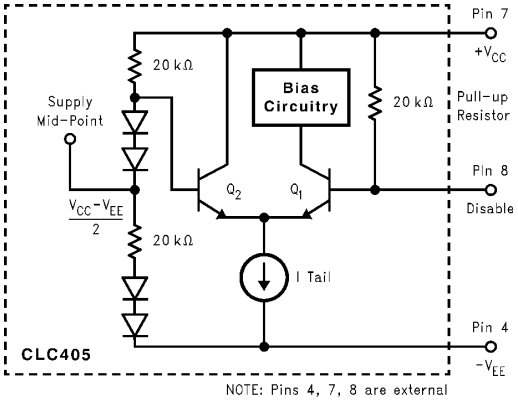


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**FIGURE 1. Enable/Disable Operation for Single or Unbalanced Supply Operation**

*Figure 1* illustrates the internal enable/disable operation of the CLC405. When pin 8 is left floating or is tied to $+V_{CC}$, Q1 is on and pulls tail current through the CLC405 bias circuitry. When pin 8 is less than 0.8V above the supply midpoint, Q1 stops tail current from flowing in the CLC405 circuitry. The CLC405 is now disabled.

### Disable Limitations

The feedback resistor, $R_f$, limits off isolation in inverting gain configurations. Do not apply voltages greater than $+V_{CC}$ or less than $-V_{EE}$ to pin 8 or any other pin.

### Input - Bias Current, Impedance, and Source Termination Considerations

The CLC405 has:

- a 6MΩ non-inverting input impedance.
- a 100nA non-inverting input bias current.

If a large source impedance application is considered, remove all parasitic capacitance around the non-inverting input source traces. Parasitic capacitances near the input and source act as a low-pass filter and reduce bandwidth

## Application Division (Continued)

Current feedback op amps have uncorrelated input bias currents. These uncorrelated bias currents prevent source impedance matching on each input from canceling offsets. Refer to application note OA-07 of the data book to find specific circuits to correct DC offsets.

**Layout Considerations**

Whenever questions about layout arise, USE THE EVALUATION BOARD AS A TEMPLATE.

Use the CLC730013 and CLC730027 evaluation boards for the DIP and SOIC respectively. These board layouts were optimized to produce the typical performance of the CLC405 shown in the data sheet. To reduce parasitic capacitances, the ground plane was removed near pins 2,3, and 6. To reduce series inductance, trace lengths of components and nodes were minimized.

Parasitics on traces degrade performance. Minimize coupling from traces to both power and ground planes. Use low inductive resistors for leaded components.

Do not use dip sockets for the CLC405 DIP amplifiers. These sockets can peak the frequency domain response or create overshoot in the time domain response. Use flush-mount socket pins when socketing is necessary. The 730013 circuit board device holes are sized for Cambion P/N 450-2598 socket pins or their functional equivalent.

Insert the back matching resistor ($R_{OUT}$) shown in *Figure 2* when driving coaxial cable or a capacitive load. Use the plot in the typical performance section labeled "Settling Time vs. Capacitive Load" to determine the optimum resistor value for $\mathbf{R_{OUT}}$ for different capacitive loads. This optimal resistance improves settling time for pulse-type applications and increases stability.

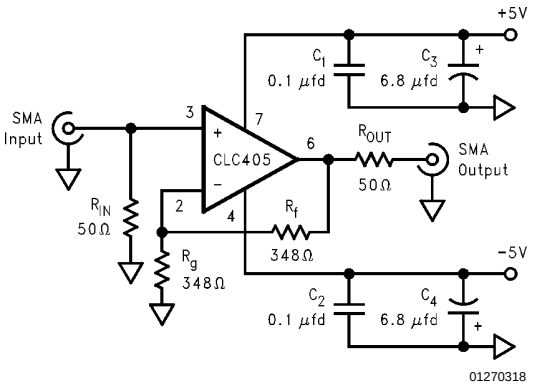
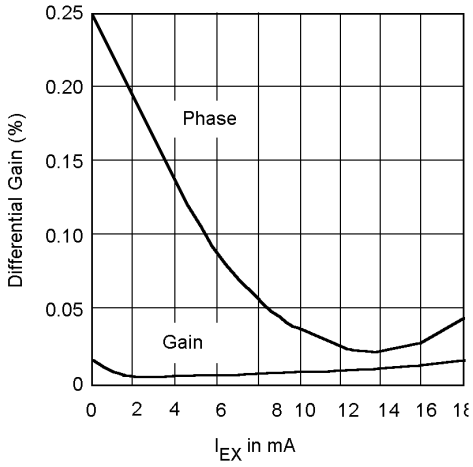



**FIGURE 2.**

Use power-supply bypassing capacitors when operating this amplifier. Choose quality 0.1µF ceramics for $C_1$ and $C_2$. Choose quality 6.8µF tantalum capacitors for $C_3$ and $C_4$. Place 0.1µF capacitors within 0.1 inches from the power pins. Place the 6.8µF capacitors within 3/4 inches from the power pins.

**Video Performance vs. $I_{EX}$**

Improve the video performance of the CLC405 by drawing extra current from the amplifier output stage. Using a single external resistor as shown in *Figure 3*, you can adjust the differential phase. Video performance vs. $I_{EX}$ is illustrated below in Graph 1. This graph represents positive video performance with negative synchronization pulses.




**Graph 1. Differential Gain & Phase vs. $I_{EX}$**

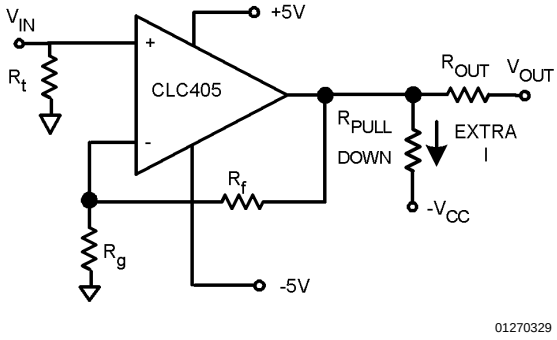



**FIGURE 3.**

The value for $R_{pd}$ in *Figure 3* is determined by:

$$R_{PD} = \frac{5}{I_{EX}}$$

at ±5V supplies.

**Wideband Digital PGA**

As shown on the front page, the CLC405 is easily configured as a digitally controlled programmable gain amplifier. Make a PGA by configuring several amplifiers at required gains. Keep $R_f$ near 348Ω and change $R_g$ for each different gain. Use a TTL decoder that has enough outputs to control the selection of different gains and the buffer stage. Connect the buffer stage like the buffer on the front page. The buffer isolates each gain stage from the load and can produce a gain of zero for a gain selection of zero. Use of an inverter (7404) on the buffer disable pin to keep the buffer operational at all gains except zero. Or float the buffer disable pin for a continuous enable state.

**Amplitude Equalization**

Sending signals over coaxial cable greater than 50 meters in length will attenuate high frequency signal components. Equalizers restore the attenuated components of this signal. The circuit in *Figure 4*, is an op amp equalizer. The RC networks peak the response of the CLC405 at higher fre-

## Application Division (Continued)

quencies. This peaking restores cable-attenuated frequencies. Graph 2 shows how the equalizer actually restores a digital word through 150 meters of coaxial cable.

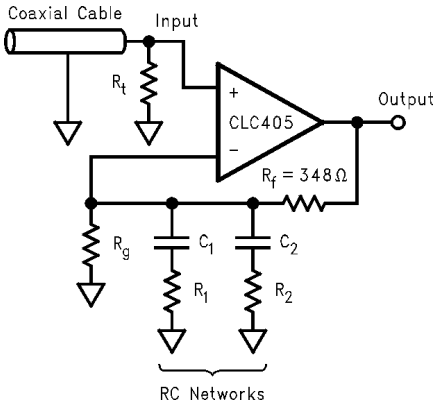
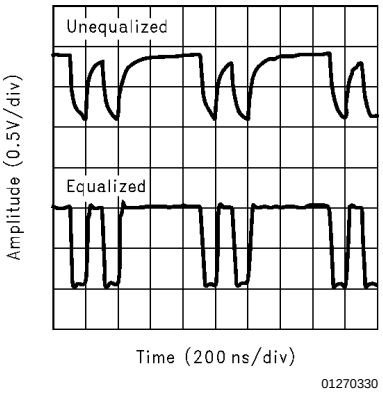



**FIGURE 4.**




**Graph 2. Digital Word Amplitude Equalization**

The values used to produce Graph 2 are:

$R_g$= 348Ω

$R_1$ = 450Ω

$C_1$ = 470pF

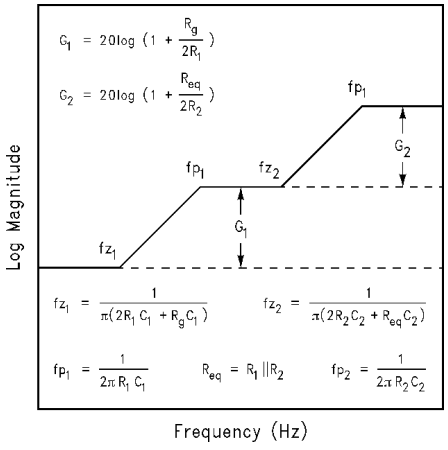
$R_2$ = 90Ω

$C_2$ = 70pF

**Amplitude Equalizer**

Place the first zero ($fz_1$) at some low frequency (540 khz for Graph 2). R1 & C1 produce a pole ($fp_1$ @ 750khz) that cancels $fz_1$. Place a second zero at a higher frequency ($fz_2$ @ 12Mhz). R2 & C2 provide a canceling pole (of $fp_2$ = 25Mhz).

Graph 3 shows the closed loop response of the op amp equalizer with equations for the poles, zeros, and gains.

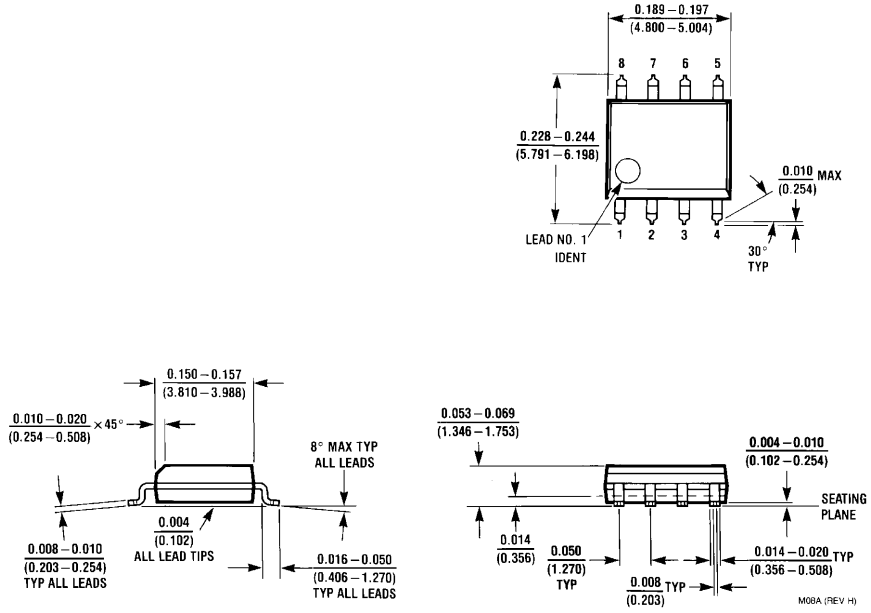



**Graph 3. Closed Loop Equalizer Frequency Response**

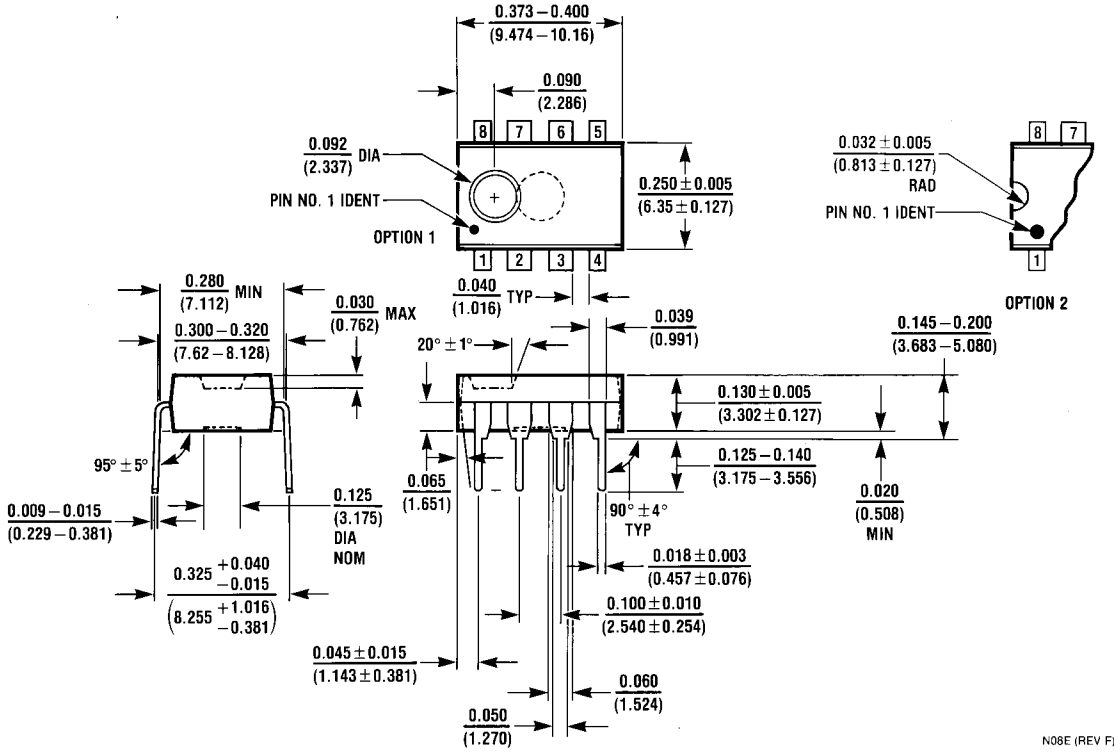
Note: For very high frequency equalization, us a higher bandwidth part (i.e., CLC44X).

## Physical Dimensions inches (millimeters)

unless otherwise noted




**8-Pin SOIC**
**NS Product Number M08A**




**8-Pin MDIP**
**NS Product Number N08E**

## Notes

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