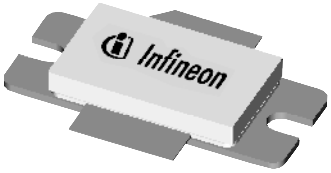
PTFA212401E
PTFA212401F

Thermally-Enhanced High Power RF LDMOS FETs
240 W, 2110 – 2170 MHz

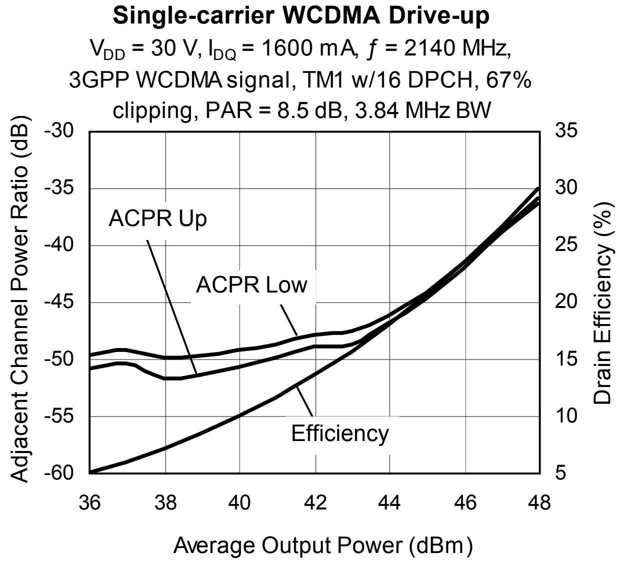
Description

The PTFA212401E and PTFA212401F are 240-watt LDMOS FETs designed for single- and two-carrier WCDMA power amplifier applications in the 2110 to 2170 MHz band. Features include input and output matching, and thermally-enhanced packages with slotted or earless flanges. Manufactured with Infineon's advanced LDMOS process, these devices provide excellent thermal performance and superior reliability.

PTFA212401E
Package H-36260-2



PTFA212401F
Package H-37260-2



Single-carrier WCDMA Drive-up
V_{DD} = 30 V, I_{DQ} = 1600 mA, f = 2140 MHz, 3GPP WCDMA signal, TM1 w/16 DPCH, 67% clipping, PAR = 8.5 dB, 3.84 MHz BW

Features

- Thermally-enhanced packages, Pb-free and RoHS compliant
- Broadband internal matching
- Typical two-carrier WCDMA performance at 2140 MHz, 30 V, 3GPP signal, PAR = 8 dB
  - Average output power = 47.0 dBm
  - Linear Gain = 15.8 dB
  - Efficiency = 28%
  - Intermodulation distortion = –35 dBc
  - Adjacent channel power = –40 dBc
- Typical single-carrier WCDMA performance at 2140 MHz, 30 V, 3GPP signal, PAR = 8.5 dB
  - Average output power = 49 dBm
  - Linear Gain = 15.8 dB
  - Efficiency = 34%
  - Adjacent channel power = –33 dBc
- Typical CW performance, 2140 MHz, 30 V
  - Output power at P–1dB = 240 W
  - Efficiency = 54%
- Integrated ESD protection: Human Body Model, Class 2 (minimum)
- Excellent thermal stability, low HCI drift
- Capable of handling 5:1 VSWR @ 30 V, 240 W (CW) output power

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics

Two-Carrier WCDMA Measurements (tested in Infineon test fixture)

V_{DD} = 30 V, I_{DQ} = 1.6 A, P_{OUT} = 50 W average
f_1 = 2135 MHz, f_2 = 2145 MHz, 3GPP signal, channel bandwidth = 3.84 MHz , peak/average = 8 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	14.8	15.8	—	dB
Drain Efficiency	η_D	26	28	—	%
Intermodulation Distortion	IMD	—	–35.0	–33	dBc

Two-tone Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)

V_{DD} = 30 V, I_{DQ} = 1.6 A, P_{OUT} = 220 W PEP, f_1 = 2140 MHz, f_2 = 2141 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	—	15.8	—	dB
Drain Efficiency	η_D	—	38.5	—	%
Intermodulation Distortion	IMD	—	–28	—	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 30 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	10.0	µA
On-State Resistance	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.03	—	Ω
Operating Gate Voltage	V_{DS} = 30 V, I_{DQ} = 1.6 A	V_{GS}	2.0	2.5	3.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA

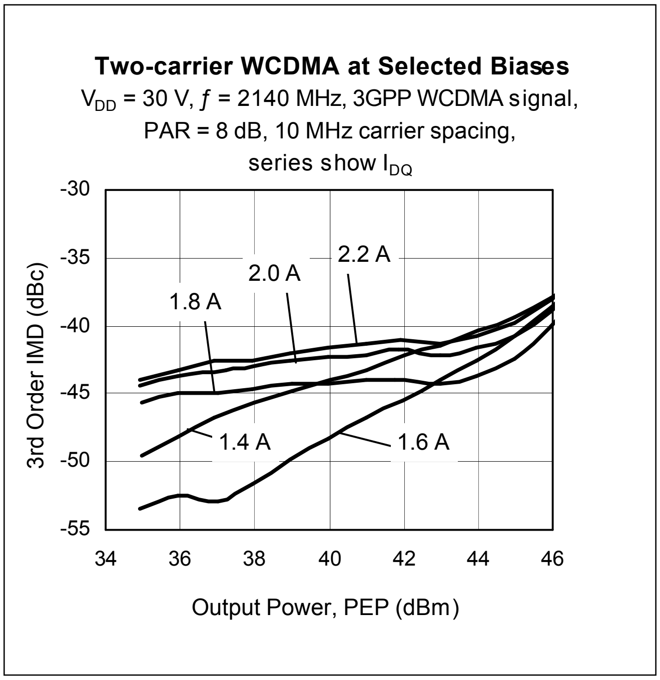
Maximum Ratings

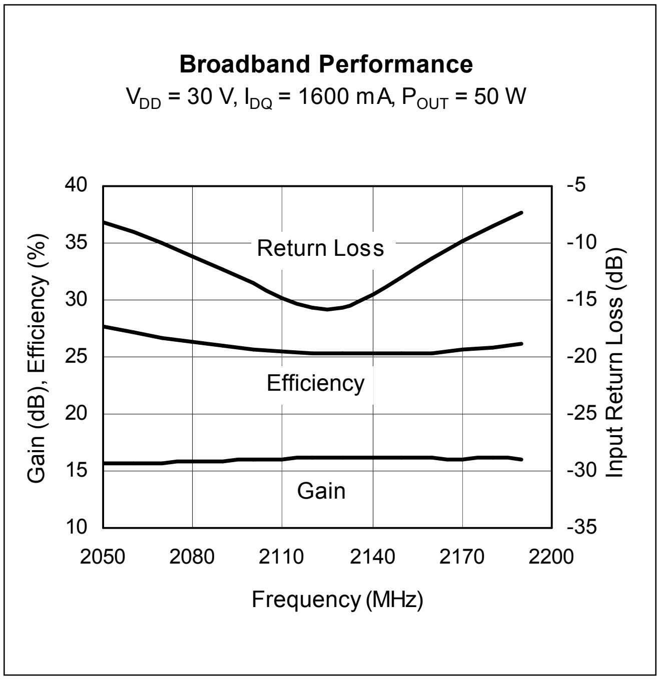
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	761	W
Above 25°C derate by		4.35	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C, 50 W Average WCDMA)	$R_{\theta JC}$	0.23	°C/W

Ordering Information

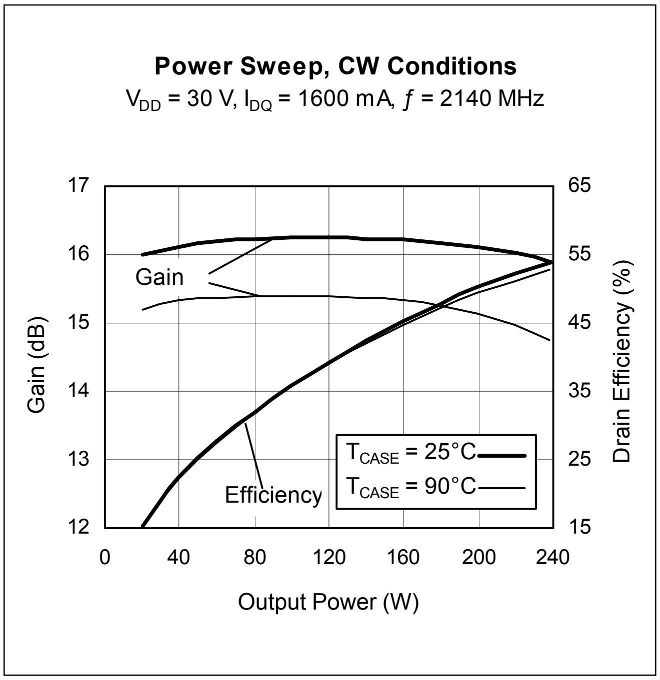
Type and Version	Package Outline	Package Description	Shipping
PTFA212401E V4	H-36260-2	Thermally-enhanced slotted flange, single-ended	Tray
PTFA212401F V4	H-37260-2	Thermally-enhanced earless flange, single-ended	Tray

Typical Performance (data taken in a production test fixture)

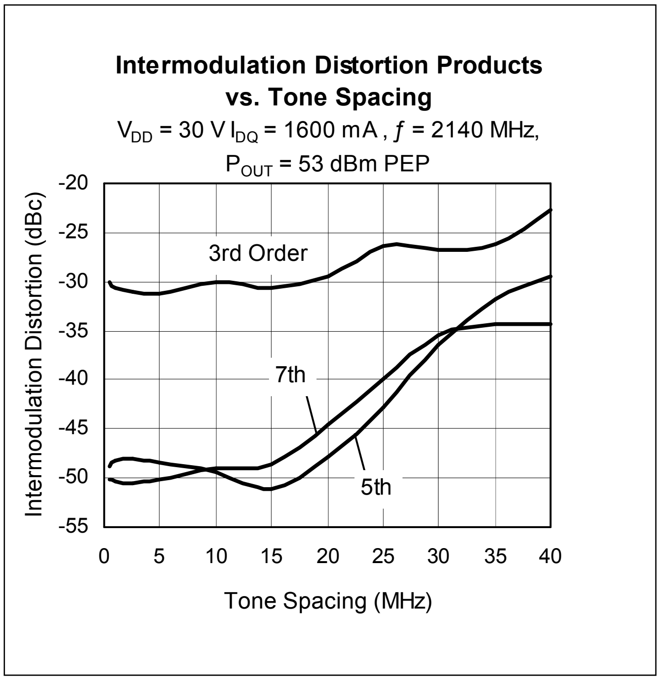




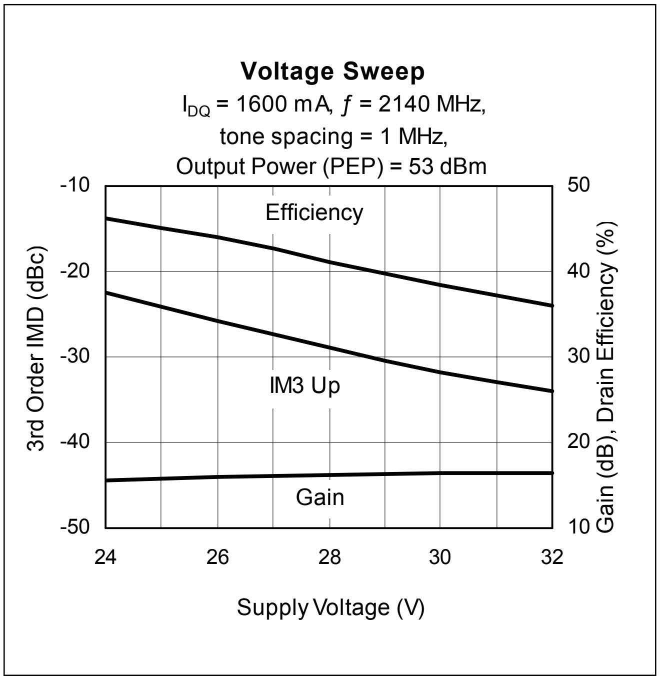
Typical Performance (cont.)



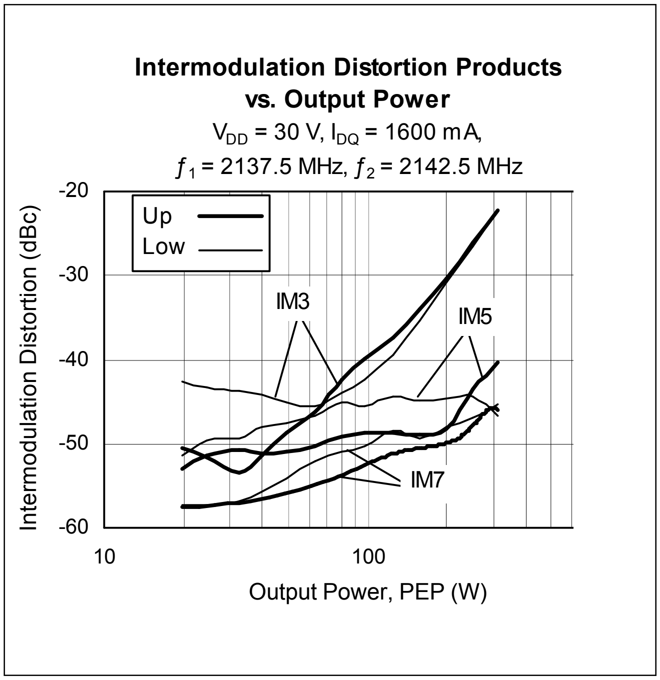
Power Sweep, CW Conditions
V_{DD} = 30 V, I_{DQ} = 1600 mA, ƒ = 2140 MHz



Intermodulation Distortion Products vs. Tone Spacing
V_{DD} = 30 V I_{DQ} = 1600 mA , ƒ = 2140 MHz,
P_{OUT} = 53 dBm PEP



Voltage Sweep
I_{DQ} = 1600 mA, ƒ = 2140 MHz,
tone spacing = 1 MHz,
Output Power (PEP) = 53 dBm

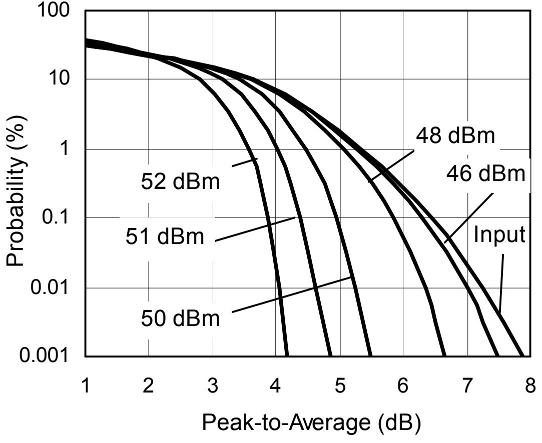


Intermodulation Distortion Products vs. Output Power
V_{DD} = 30 V, I_{DQ} = 1600 mA,
$ƒ_1$ = 2137.5 MHz, $ƒ_2$ = 2142.5 MHz

Typical Performance (cont.)

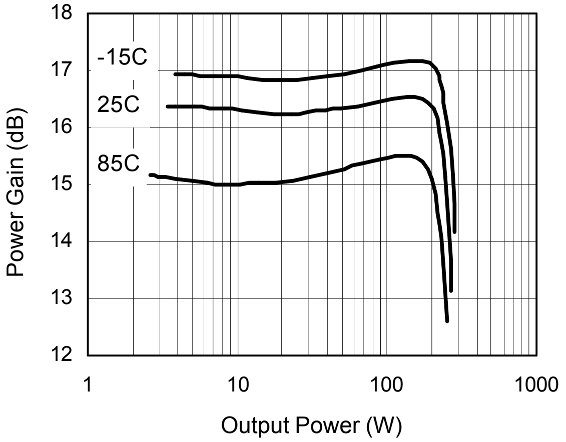
Output Peak-to-Average Ratio Compression (PARC) at various Power Levels

V_{DD} = 30 V, I_{DQ} = 1600 mA, f = 2170 MHz,
single-carrier WCDMA input PAR = 7.5 dB



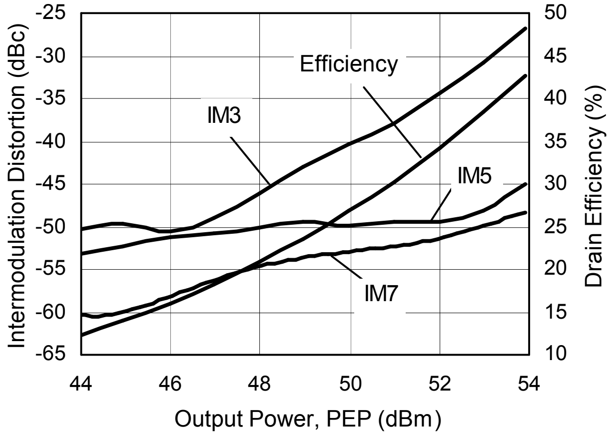
Power Gain vs. Power Sweep (CW) over Temperature

V_{DD} = 30 V, I_{DQ} = 1500 mA, f = 2140 MHz



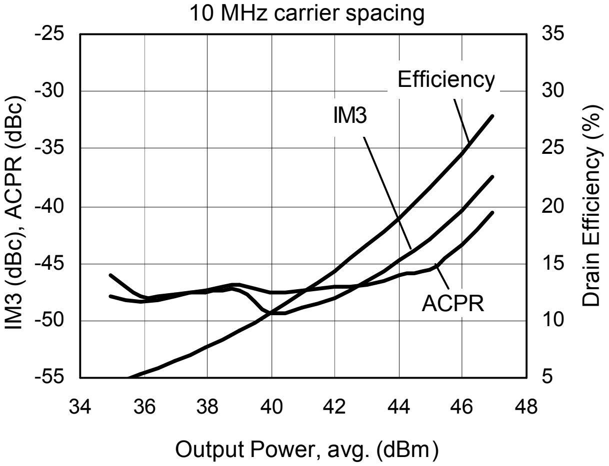
Two-tone Drive-up

V_{DD} = 30 V, I_{DQ} = 1600 mA,
f = 2140 MHz, tone spacing = 1 MHz

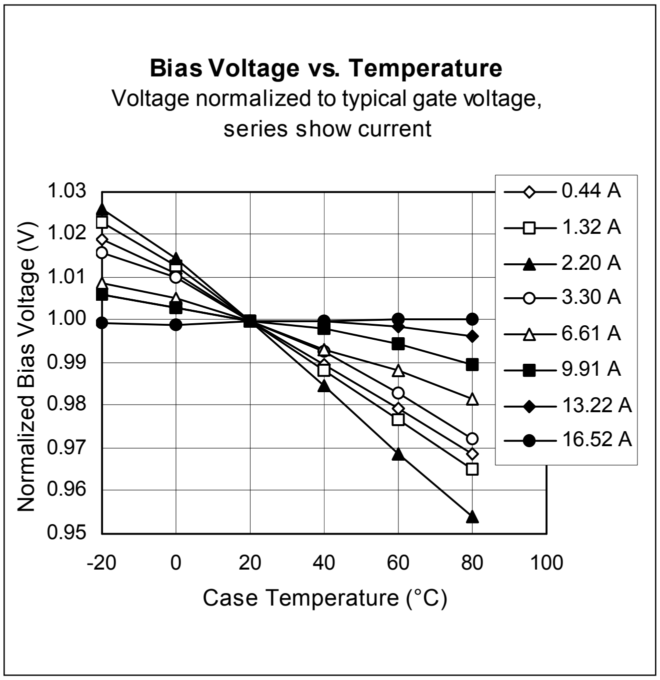


Two-carrier WCDMA Drive-up

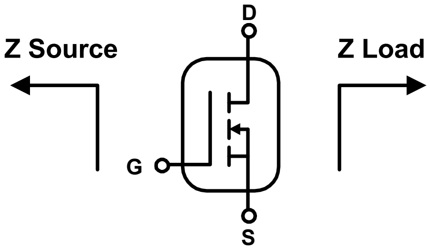
V_{DD} = 30 V, I_{DQ} = 1600 mA, f = 2140 MHz,
3GPP WCDMA signal, PAR = 8 dB,
10 MHz carrier spacing

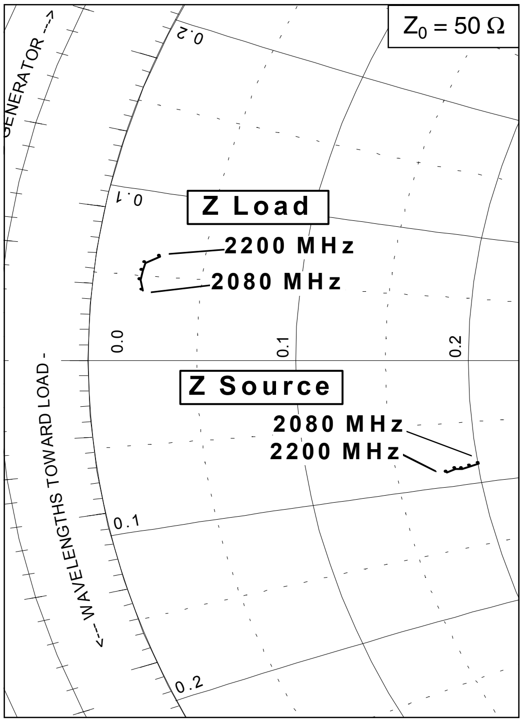


Typical Performance (cont.)



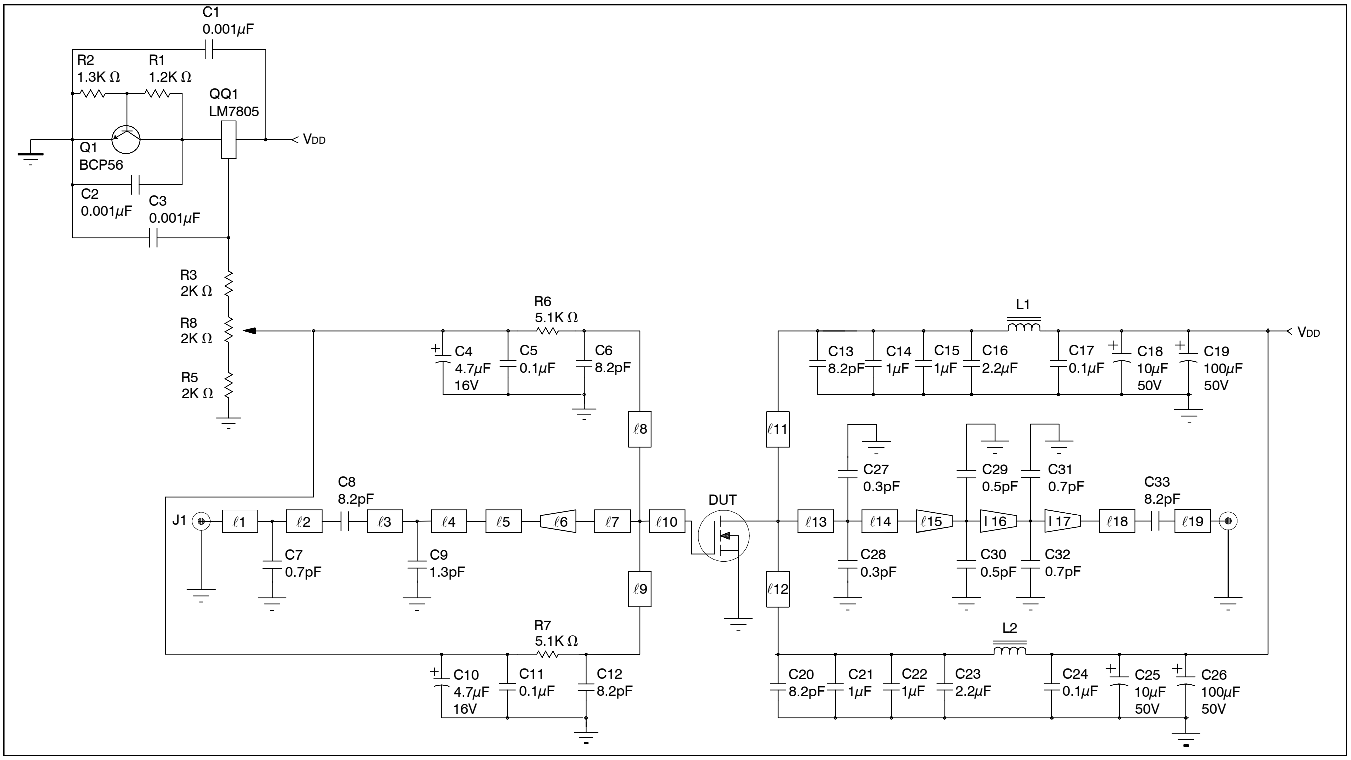
Broadband Circuit Impedance





Frequency	Z Source Ω		Z Load Ω	
MHz	R	jX	R	jX
2080	10.050	–4.250	1.140	2.07
2110	9.750	–4.320	1.080	2.38
2140	9.500	–4.380	1.090	2.65
2170	9.280	–4.350	1.130	2.89
2200	9.000	–4.460	1.450	3.11

Reference Circuit



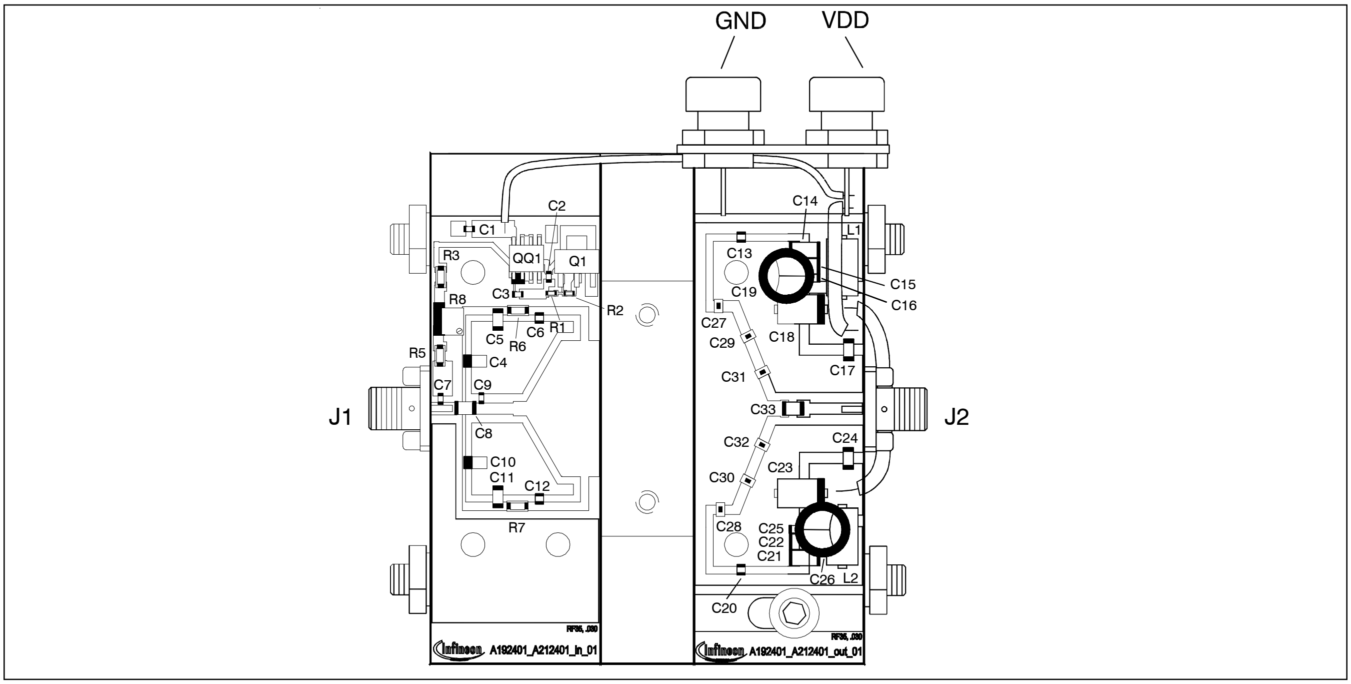
Reference circuit schematic for ƒ = 2140 MHz

Circuit Assembly Information

DUT	PTFA212401E or PTFA212401F	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, $\varepsilon_r = 3.5$	RF–35	1 oz. copper

Microstrip	Electrical Characteristics at 2140 MHz	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ1	0.018 λ, 49.9 Ω	1.55 x 1.70	0.061 x 0.067
ℓ2	0.022 λ, 49.9 Ω	1.91 x 1.70	0.075 x 0.067
ℓ3	0.047 λ, 49.9 Ω	3.99 x 1.70	0.157 x 0.067
ℓ4	0.034 λ, 49.9 Ω	2.90 x 1.70	0.114 x 0.067
ℓ5	0.024 λ, 42.8 Ω	2.01 x 2.16	0.079 x 0.085
ℓ6 (taper)	0.063 λ, 42.8 Ω / 6.9 Ω	5.28 x 2.16 / 20.32	0.208 x 0.085 / 0.800
ℓ7,	0.043 λ, 6.9 Ω	3.33 x 20.32	0.131 x 0.800
ℓ8, ℓ9	0.134 λ, 59.9 Ω	11.48 x 1.04	0.452 x 0.041
ℓ10	0.029 λ, 6.9 Ω	2.21 x 20.32	0.087 x 0.800
ℓ11, ℓ12	0.262 λ, 51.0 Ω	22.10 x 1.65	0.870 x 0.065
ℓ13	0.042 λ, 5.0 Ω	3.18 x 28.91	0.125 x 1.138
ℓ14	0.032 λ, 5.0 Ω	2.41 x 28.91	0.095 x 1.138
ℓ15 (taper)	0.014 λ, 5.0 Ω / 6.65 Ω	1.04 x 28.91 / 21.89	0.041 x 1.138 / 0.862
ℓ16 (taper)	0.026 λ, 6.65 Ω / 11.68 Ω	2.03 x 21.89 / 11.43	0.080 x 0.862 / 0.450
ℓ17 (taper)	0.025 λ, 11.68 Ω / 40.7 Ω	2.13 x 11.43 / 2.34	0.084 x 0.450 / 0.092
ℓ18	0.017 λ, 40.7 Ω	1.40 x 2.34	0.055 x 0.092
ℓ19	0.123 λ, 49.9 Ω	10.24 x 1.70	0.403 x 0.067

Reference Circuit (cont.)



Reference circuit assembly diagram (not to scale)*

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C2, C3	Capacitor, 0.001 µF	Digi-Key	PCC1772CT-ND
C4, C10	Capacitor, 4.7 µF, 16 V	Digi-Key	PCS3475CT-ND
C5, C11, C17, C24	Capacitor, 0.1 µF	Digi-Key	PCC104BCT-ND
C6, C12	Ceramic capacitor, 8.2 pF	ATC	100A 8R2
C7, C31, C32	Capacitor, 0.7 pF	AVX	08051J0R7BBTTR
C8, C33	Ceramic capacitor, 8.2 pF	ATC	100B 8R2
C9	Capacitor, 1.3 pF	ATC	600S1R3BT
C13, C20	Capacitor, 8.2 pF	AVX	100A 8R2
C14, C15, C21, C22	Ceramic capacitor, 1 µF	Digi-Key	445-1411-1-ND
C16, C23	Capacitor, 2.2 µF	Digi-Key	445-1447-2-ND
C18, C25	Tantalum capacitor, 10 µF, 50 V	Garrett Electronics	TPSE106K050R0400
C19, C26	Electrolytic capacitor, 100 µF, 50 V	Digi-Key	P5571-ND
C27, C28	Capacitor, 0.3 pF	AVX	08051J0R3BBTTR
C29, C30	Capacitor, 0.5 pF	AVX	08051J0R5BBTTR
L1, L2	Ferrite, 8.9 mm	Elna Magnetics	BDS 4.6/3/8.9-4S2
Q1	Transistor	Infineon Technologies	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Chip resistor 1.2 k-ohms	Digi-Key	P1.2KGCT-ND
R2	Chip resistor 1.3 k-ohms	Digi-Key	P1.3KGCT-ND
R3, R5	Chip resistor 2 k-ohms	Digi-Key	P2KECT-ND
R4	Chip resistor 10 ohms	Digi-Key	P10ECT-ND
R6, R7	Chip resistor 5.1 k-ohms	Digi-Key	P5.1KECT-ND
R8	Variable resistor 2 k-ohms	Digi-Key	3224W-202ETR-ND

Package Outline Specifications

Package H-36260-2

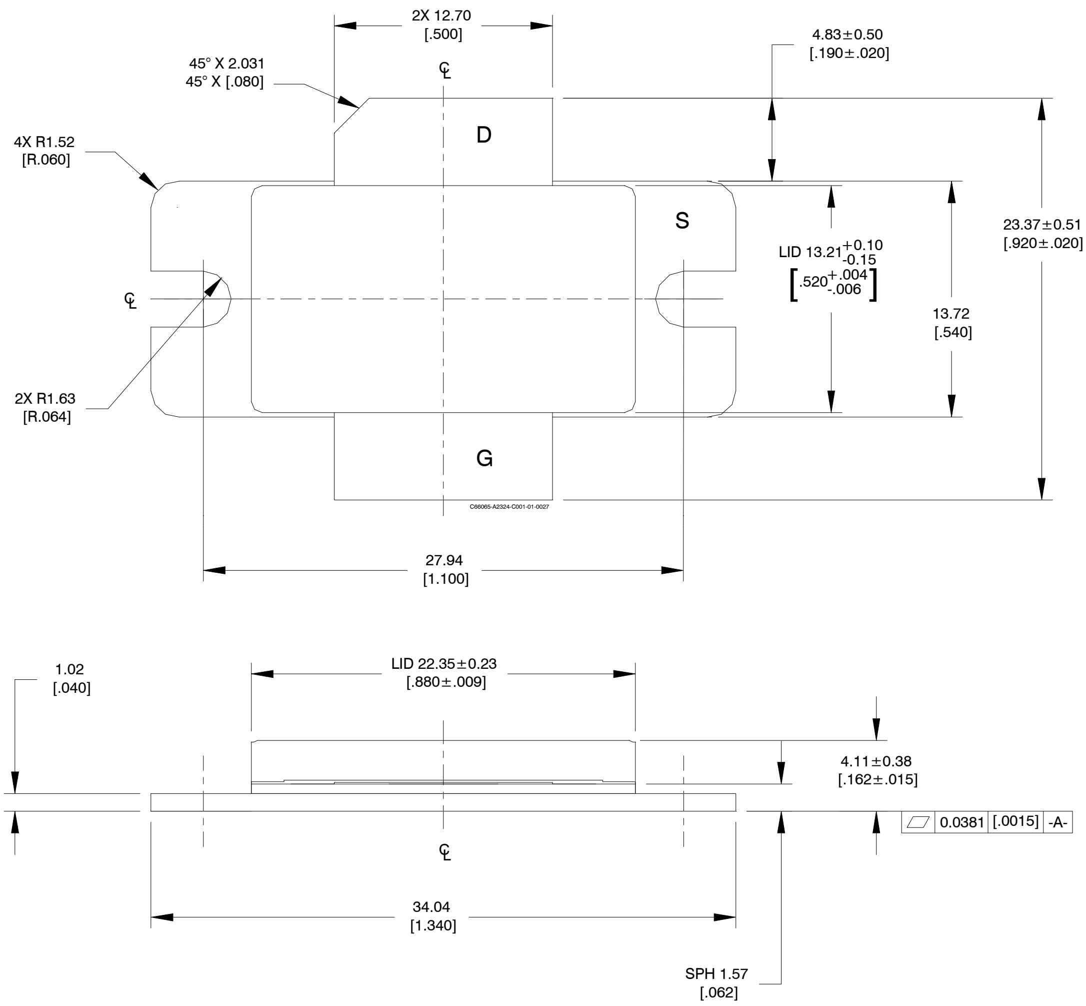
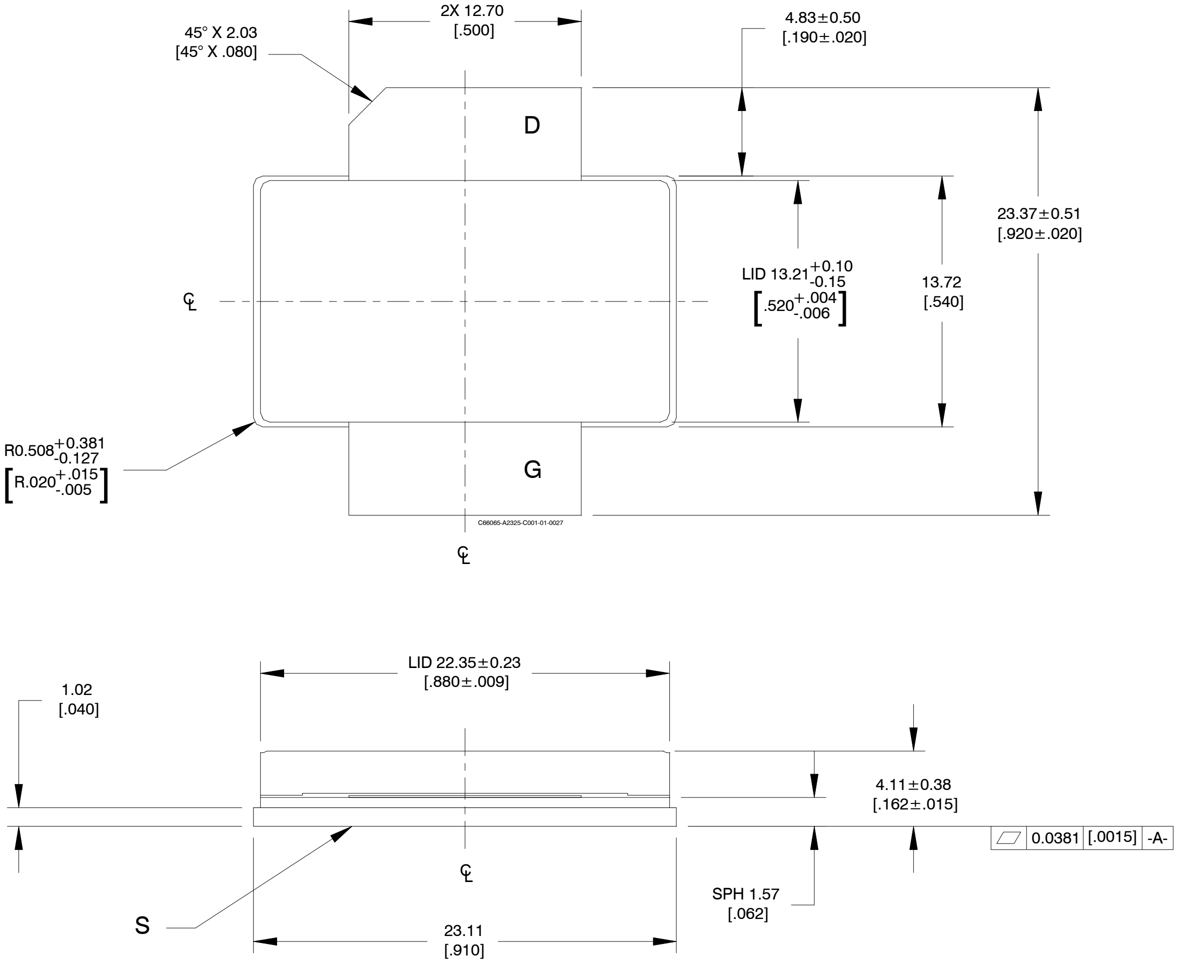


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. All tolerances ± 0.127 [.005] unless specified otherwise.
3. Primary dimensions are mm. Alternate dimensions are inches.
4. Pins: D = drain, S = source, G = gate.
5. Lead thickness: 0.10 +0.051/–0.025 [.004 +.002/–.001].
6. Gold plating thickness:
   S, D, G - flange & leads: 1.14 ± 0.38 micron [45 ± 15 microinch]

Package Outline Specifications (cont.)

Package H-37260-2



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Revision History: 2009-10-05 Data Sheet

Previous Version: 2009-04-01 Data Sheet

Page	**Subjects (major changes since last revision)**
2	Updated characteristics

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