36 V, 18 MHz, Low Noise, Fast Settling Single Supply, RRO, JFET Op Amp

Data Sheet

ADA4625-1

FEATURES

- Wide gain bandwidth product: 18 MHz typical
- High slew rate: 48 V/µs typical
- Low voltage noise density: 3.3 nV/√Hz typical at 1 kHz
- Low peak-to-peak noise: 0.15 µV p-p, 0.1 Hz to 10 Hz
- Low input bias current: ±15 pA typical at T_A = 25°C
- Low offset voltage: ±80 µV maximum at T_A = 25°C
- Offset voltage drift: ±1.2 µV/°C maximum at T_A = −40°C to 85°C
- Fast settling: 0.01% in 700 ns typical
- Wide range of operating voltages
  - Dual-supply operation: ±2.5 V to ±18 V
  - Single-supply operation: 5 V to 36 V
- Input voltage range includes V−
- Rail-to-rail output
- High capacitive load drive capability
- Output short-circuit current: ±46 mA
- No phase reversal
- Unity-gain stable

APPLICATIONS

- PLL filter amplifiers
- Transimpedance amplifiers
- Photodiode sensor interfaces
- Low noise charge amplifiers

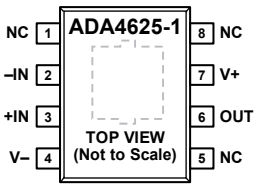
GENERAL DESCRIPTION

The ADA4625-1 builds upon Analog Devices, Inc., industry leading high voltage, single-supply, rail-to-rail output (RRO), precision junction field effect transistor (JFET) input op amps, taking that product type to a level of speed and low noise that has not been made available to the market previously.

The ADA4625-1 provides optimal performance in high voltage, high gain, and low noise applications. The input common-mode voltage range includes the negative supply, and the output swings rail to rail. This enables the user to maximize dynamic input range in low voltage, single supply applications without the need for a separate negative voltage power supply for ground sense.

The combination of wide bandwidth, low noise, and low input bias current makes the ADA4625-1 especially suitable for phase-locked loop (PLL), active filter amplifiers and for high tuning voltage (V_{TUNE}), voltage controlled oscillators (VCOs) and preamplifiers where low level signals require an amplifier that provides both high amplification and wide bandwidth.

PIN CONFIGURATION



NOTES
1. NC = NO CONNECTION. DO NOT CONNECT TO THIS PIN.
2. EXPOSED PAD. CONNECT THE EXPOSED PAD TO GND, V+ OR V– PLANE, OR LEAVE IT FLOATING.

15893-001

Figure 1.

The ADA4625-1 is unity-gain stable, and there is no phase reversal when input range exceeds either supply rail by 200 mV. The output is capable of driving loads up to 1000 pF and/or 600 Ω loads.

The ADA4625-1 is specified for operation over the extended industrial temperature range of −40°C to +125°C and operates from +5 V to +36 V (±2.5 V to ±18 V) with specifications at +5 V and ±18 V. The ADA4625-1 is available in 8-lead SOIC package with an exposed pad (EPAD).

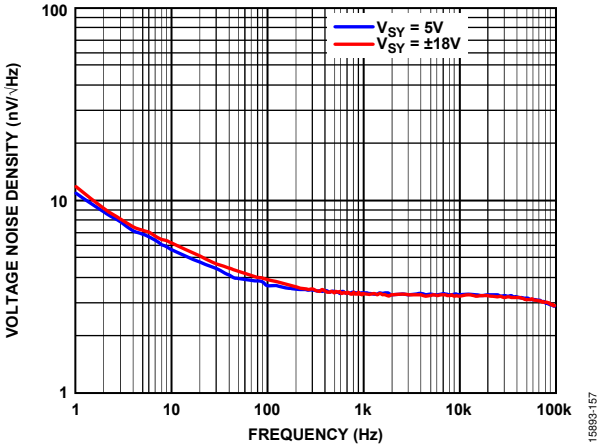


Figure 2. Voltage Noise Density vs. Frequency

Table 1. Related Precision JFET Operational Amplifiers

Single	Dual	Quad
Not applicable	AD823A	Not applicable
AD8510	AD8512	AD8513
AD8610	AD8620	Not applicable
ADA4610-1	ADA4610-2	ADA4610-4
ADA4622-1	ADA4622-2	ADA4622-4
ADA4627-1/ADA4637-1	Not applicable	Not applicable

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REVISION HISTORY

10/2017—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—±18 V OPERATION

Supply voltage (V_{SY}) = ±18 V, common-mode voltage (V_{CM}) = output voltage (V_{OUT}) = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			±15	±80	μV
		−40°C < T_A < +125°C			±250	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +85°C		±0.2	±1.2	μV/°C
		−40°C < T_A < +125°C		±0.5	±2.1	μV/°C
Input Bias Current	I_B			±15	±75	pA
		−40°C < T_A < +125°C			±5.5	nA
Input Offset Current	I_{OS}			±2	±50	pA
		−40°C < T_A < +125°C			±0.4	nA
Input Voltage Range	IVR		−18.2		+14.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −18.2 V to +14.5 V	97	115		dB
		−40°C < T_A < +125°C	94			dB
		V_{CM} = −18.2 V to +12 V	115	130		dB
		−40°C < T_A < +125°C	110			dB
Large Signal Voltage Gain	A_{VO}	Load resistance (R_L) = 2 kΩ, V_{OUT} = −17.5 V to +17.5 V	140	150		dB
		−40°C < T_A < +125°C	135			dB
		R_L = 600 Ω, V_{OUT} = −15 V to +15 V	130	135		dB
		−40°C < T_A < +125°C	115			dB
Input Capacitance	C_{DM}	Differential mode		8.6		pF
	C_{CM}	Common mode		11.3		pF
Input Resistance	R_{DM}	Differential mode		10^{12}		Ω
	R_{CM}	Common mode, V_{CM} from −18 V to +12 V		10^{12}		Ω
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ	17.65	17.72		V
		−40°C < T_A < +125°C	17.5			V
		R_L = 600 Ω	17.0	17.28		V
		−40°C < T_A < +125°C	16.75			V
Output Voltage Low	V_{OL}	R_L = 2 kΩ		−17.74	−17.70	V
		−40°C < T_A < +125°C			−17.5	V
		R_L = 600 Ω		−17.4	−17.0	V
		−40°C < T_A < +125°C			−16.85	V
Output Current	I_{OUT}	Dropout voltage ($V_{DROPOUT}$) < 1 V		±33		mA
Short-Circuit Current	I_{SC}			±46		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, closed-loop gain (A_V) = +1		2		Ω
		A_V = +10		18		Ω
		A_V = +100		29		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = ±5 V to ±18 V	105	120		dB
		−40°C < T_A < +125°C	102			dB
Supply Current per Amplifier	I_{SY}	V_{OUT} = 0 V		4.0	4.5	mA
		−40°C < T_A < +125°C			5	mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR	V_{OUT} = ±10 V, R_L = 2 kΩ, A_V = −1		48		V/µs
		V_{OUT} = ±10 V, R_L = 2 kΩ, A_V = −5		44		V/µs
Gain Bandwidth Product	GBP	A_V = 100		18		MHz
Unity-Gain Crossover	UGC	A_V = 1		12.4		MHz
−3 dB Bandwidth	−3 dB	A_V = 1		16		MHz
Phase Margin	ΦM			88		Degrees
Settling Time	t_S	To 0.1%, input voltage (V_{IN}) = 10V step, R_L = 2 kΩ, load capacitance (C_L) = 15 pF, A_V = −1		500		ns
		To 0.01%, V_{IN} = 10 V step, R_L = 2 kΩ, C_L = 15 pF, A_V = −1		700		ns
ELECTROMAGNETIC INTERFERENCE (EMI) REJECTION RATIO	EMIRR					
f = 1000 MHz				56		dB
f = 2400 MHz				93		dB
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_N p-p	0.1 Hz to 10 Hz		0.15		µV p-p
Voltage Noise Density	e_N	f = 10 Hz		5.5		nV/√Hz
		f = 100 Hz		3.6		nV/√Hz
		f = 1 kHz		3.3		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		4.5		fA/√Hz
Total Harmonic Distortion + Noise	THD + N	A_V = 1, f = 10 Hz to 20 kHz, R_L = 2 kΩ, V_{IN} = 6 V_{RMS} at 1 kHz				
Bandwidth = 80 kHz				0.0003		%
				−109		dB
Bandwidth = 500 kHz				0.0007		%
				−103		dB

ELECTRICAL CHARACTERISTICS—5 V OPERATION

V_{SY} = 5 V, V_{CM} = 1.5 V, V_{OUT} = V_{SY}/2, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			±0.1	±0.6	mV
		−40°C < T_A < +125°C			±1.0	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +85°C		±0.4	±2.6	µV/°C
		−40°C < T_A < +125°C		±0.7	±3.6	µV/°C
Input Bias Current	I_B			±15	±50	pA
		−40°C < T_A < +125°C			±3.5	nA
Input Offset Current	I_{OS}			±2	±50	pA
		−40°C < T_A < +125°C			±150	pA
Input Voltage Range	IVR		−0.2		+1.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 1.5 V	74	90		dB
		−40°C < T_A < +125°C	70			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ to V−, V_{OUT} = 0.35 V to 4.65 V	130	145		dB
		−40°C < T_A < +125°C	120			dB
		R_L = 600 Ω to V−, V_{OUT} = 0.5 V to 4.5 V	120	130		dB
		−40°C < T_A < +125°C	110			dB
Input Capacitance	C_{DM}	Differential mode		12.1		pF
	C_{CM}	Common mode		16.3		pF
Input Resistance	R_{DM}	Differential mode		10^{12}		Ω
	R_{CM}	Common mode, V_{CM} from 0 V to 1.5 V		10^{12}		Ω
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 2 kΩ to V−	4.75	4.82		V
		−40°C < T_A < +125°C	4.7			V
		R_L = 600 Ω to V−	4.65	4.74		V
		−40°C < T_A < +125°C	4.55			V
Output Voltage Low	V_{OL}	R_L = 2 kΩ to V+		0.17	0.22	V
		−40°C < T_A < +125°C			0.3	V
		R_L = 600 Ω to V+		0.25	0.3	V
		−40°C < T_A < +125°C			0.45	V
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1 V		±33		mA
Short-Circuit Current	I_{SC}			±46		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = +1		2		Ω
		A_V = +10		18		Ω
		A_V = +100		29		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 4.5 V to 10 V	80	97		dB
		−40°C < T_A < +125°C	75			dB
Supply Current per Amplifier	I_{SY}	V_{OUT} = 0 V		3.9	4.3	mA
		−40°C < T_A < +125°C			4.8	mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR	V_{OUT} = 0.5 V to 4.5 V, R_L = 2 kΩ, A_V = −1		32		V/µs
		V_{OUT} = 0.5 V to 4.5 V, R_L = 2 kΩ, A_V = −5		27		V/µs
Gain Bandwidth Product	GBP	A_V = 100		16		MHz
Unity-Gain Crossover	UGC	A_V = 1		11.2		MHz
−3 dB Bandwidth	−3 dB	A_V = 1		16		MHz
Phase Margin	ΦM			86		Degrees
Settling Time	t_S	To 0.1%, V_{IN} = 4 V step, R_L = 2 kΩ, C_L = 15 pF, A_V = −1		600		ns
		To 0.01%, V_{IN} = 4 V step, R_L = 2 kΩ, C_L = 15 pF, A_V = −1		950		ns
EMI REJECTION RATIO	EMIRR					
f = 1000 MHz				56		dB
f = 2400 MHz				87		dB
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_N p-p	0.1 Hz to 10 Hz		0.15		µV p-p
Voltage Noise Density	e_N	f = 10 Hz		5.5		nV/√Hz
		f = 100 Hz		3.6		nV/√Hz
		f = 1 kHz		3.3		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		4.5		fA/√Hz
Total Harmonic Distortion + Noise	THD + N	A_V = 1, f = 10 Hz to 20 kHz, R_L = 2 kΩ, V_{IN} = 0.6 V_{RMS} at 1 kHz				
Bandwidth = 80 kHz				0.0003		%
				−109		dB
Bandwidth = 500 kHz				0.0007		%
				−103		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	40 V
Input Voltage	(V–) – 0.2 V to (V+) + 0.2 V
Differential Input Voltage	(V–) – 0.2 V to (V+) + 0.2 V
Input Current[1]	±20 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature, Soldering (10 sec)	300°C
Electrostatic Discharge (ESD)	
Human Body Model (HBM)[2]	1.25 kV
Field Induced Charge Device Model (FICDM)[3]	1.25 kV

[1] The input pins have clamp diodes connected to the power supply pins. Limit the input current to 20 mA or less whenever input signals exceed the power supply rail by 0.3 V.
[2] ESDA/JEDEC JS-001-2011 applicable standard.
[3] JESD22-C101 (ESD FICDM standard of JEDEC) applicable standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 5. Thermal Resistance

Package Type[1, 2]	θ_{JA}[3]	θ_{JC}	Unit
RD-8-1	52.8	5.7	°C/W

[1] Values were obtained per JEDEC standard JESD-51.
[2] Although the exposed pad can be left floating, it must be connected to the GND, or the V+ or V– plane for proper thermal management.
[3] Board layout impacts thermal characteristics such as θ_{JA}. When proper thermal management techniques are used, a better θ_{JA} can be achieved. Refer to the Thermal Management section for additional information.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

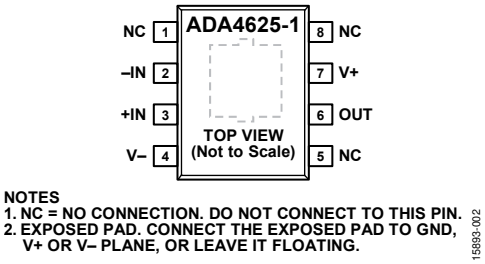

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5, 8	NC	No Connect. Do not connect to these pins.
2	–IN	Inverting Input.
3	+IN	Noninverting Input.
4	V–	Negative Supply Voltage.
6	OUT	Output.
7	V+	Positive Supply Voltage.
	EPAD	Exposed Pad. Connect the exposed pad to GND, V+ or V– plane, or leave it floating.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CM} = 0 V, unless otherwise noted.

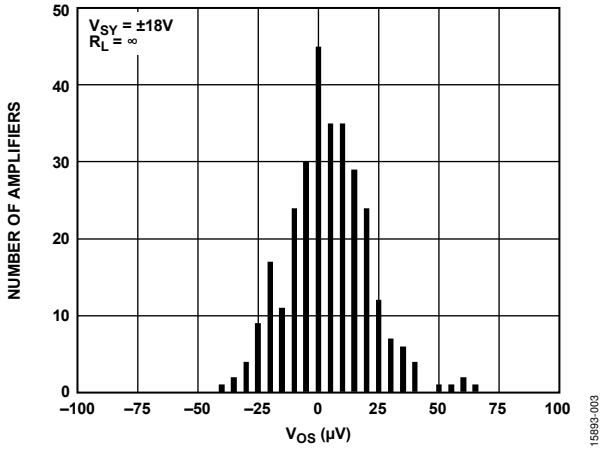

Figure 4. Input Offset Voltage (V_{OS}) Distribution, Supply Voltage (V_{SY}) = ±18 V

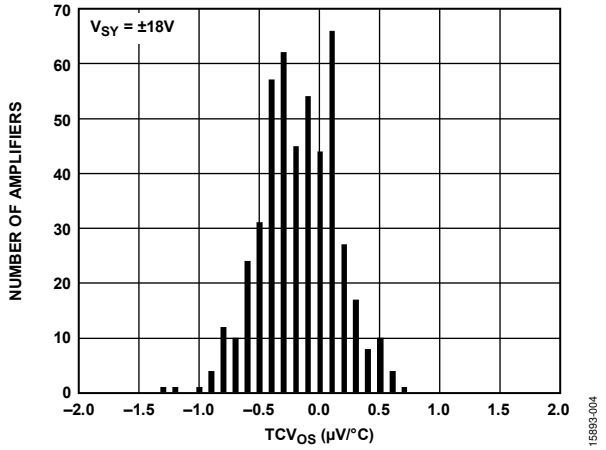

Figure 5. TCV_{OS} Distribution (−40°C to +125°C), V_{SY} = ±18 V

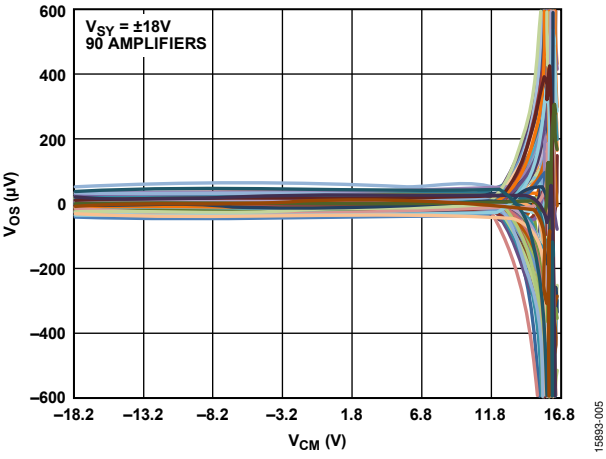

Figure 6. V_{OS} vs. Common-Mode Voltage (V_{CM}), V_{SY} = ±18 V

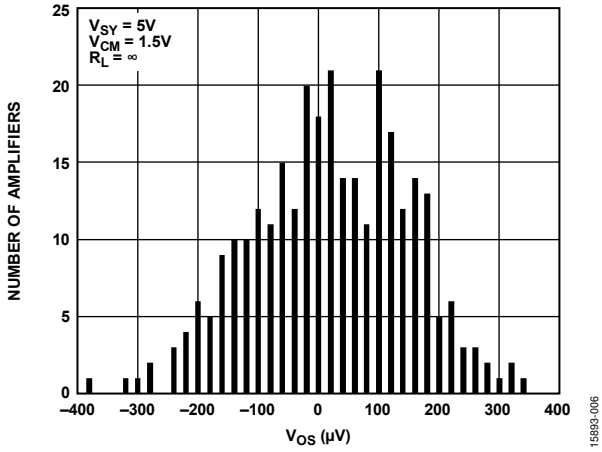

Figure 7. V_{OS} Distribution, V_{SY} = 5 V

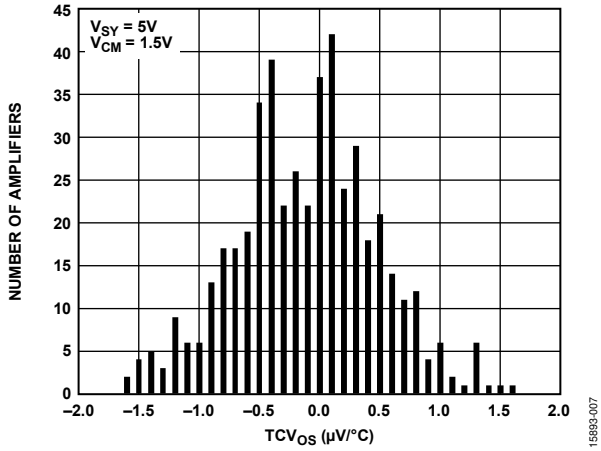

Figure 8. TCV_{OS} Distribution (−40°C to +125°C), V_{SY} = 5 V

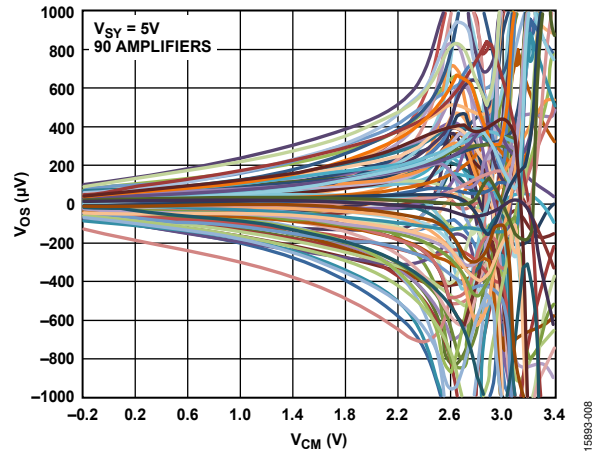

Figure 9. V_{OS} vs. V_{CM}, V_{SY} = 5 V

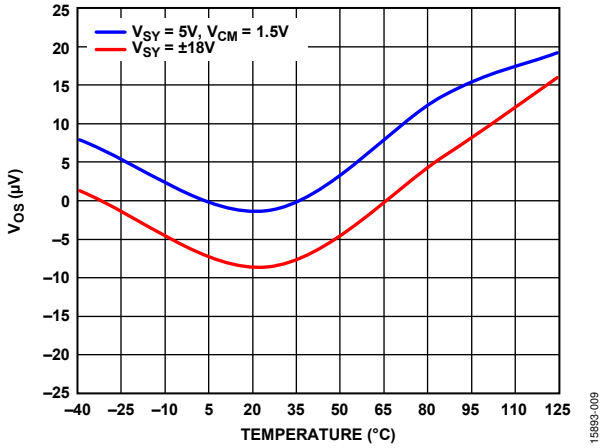

Figure 10. V_{OS} vs. Temperature

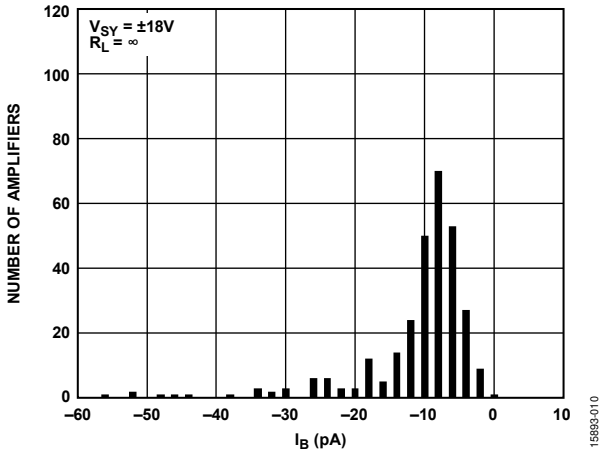

Figure 11. Input Bias Current (I_B) Distribution, V_{SY} = ±18 V

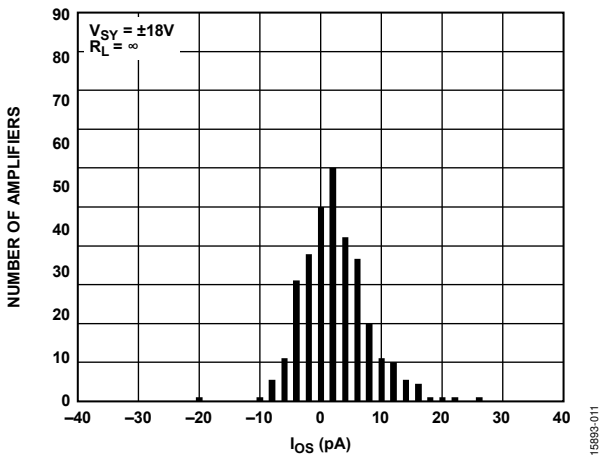

Figure 12. Input Offset Current (I_{OS}) Distribution, V_{SY} = ±18 V

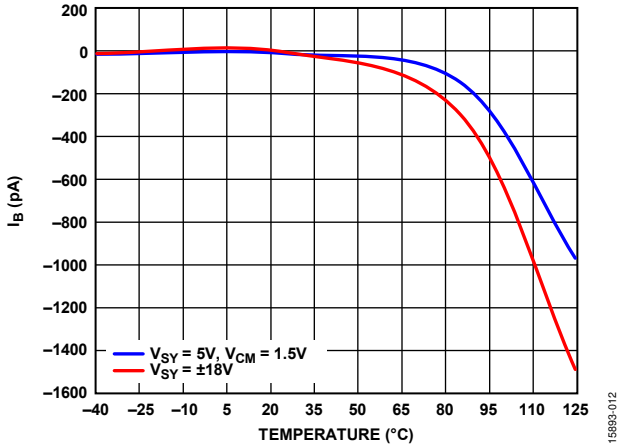

Figure 13. I_B vs. Temperature

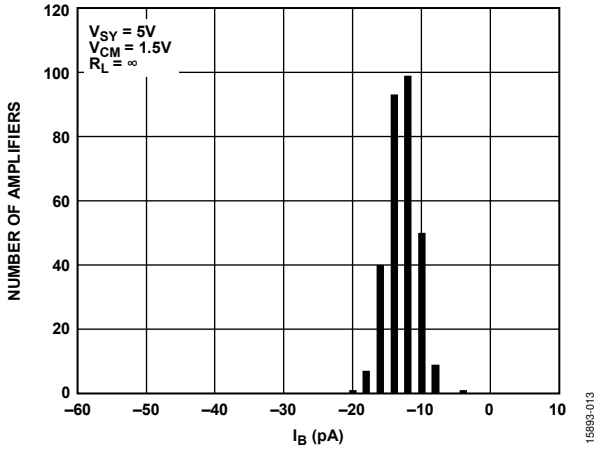

Figure 14. I_B Distribution, V_{SY} = 5 V

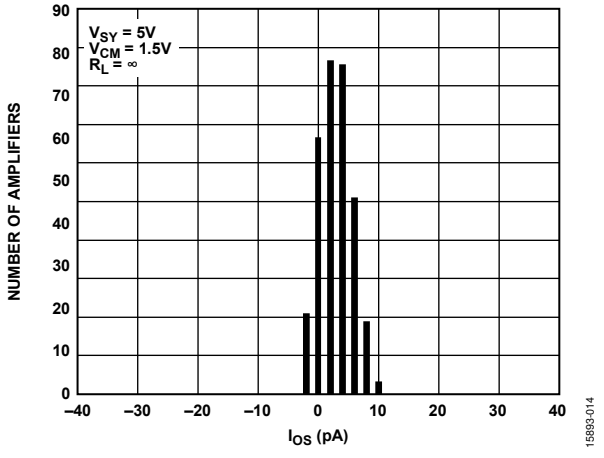

Figure 15. I_{OS} Distribution, V_{SY} = 5 V

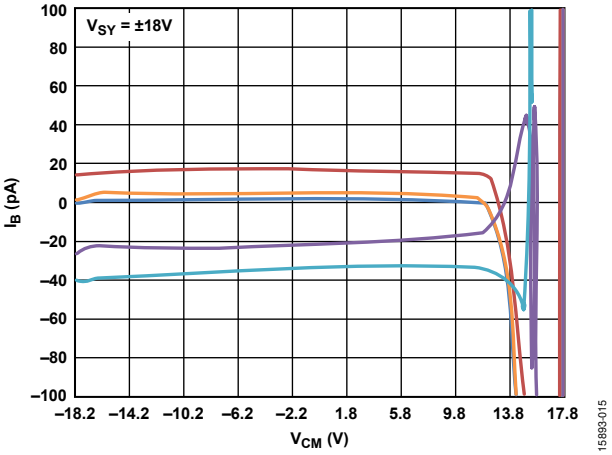

Figure 16. I_B vs. V_{CM}, V_{SY} = ±18 V

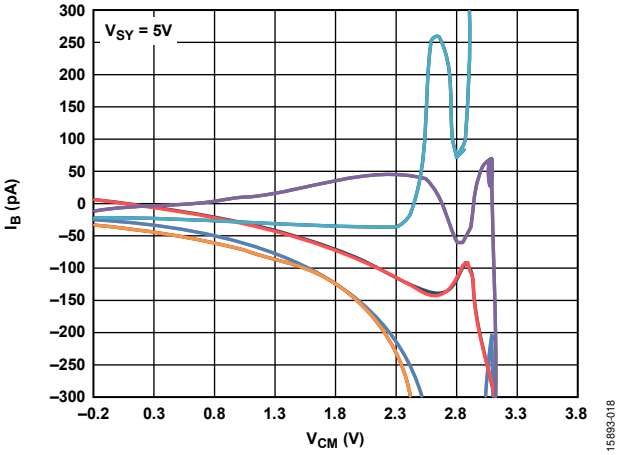

Figure 19. I_B vs. V_{CM}, V_{SY} = 5 V

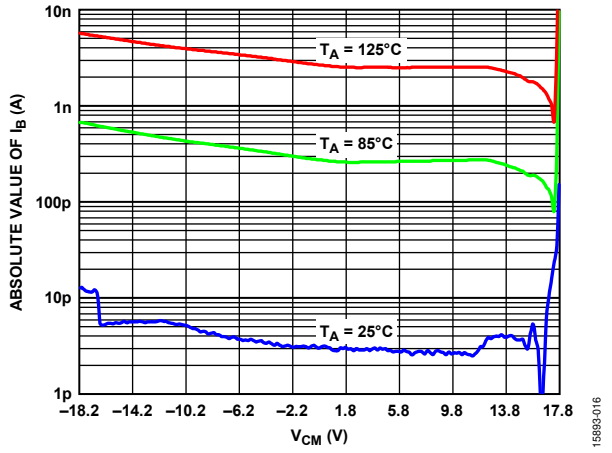

Figure 17. Absolute Value of I_B vs. V_{CM} for Various Temperatures, V_{SY} = ±18 V

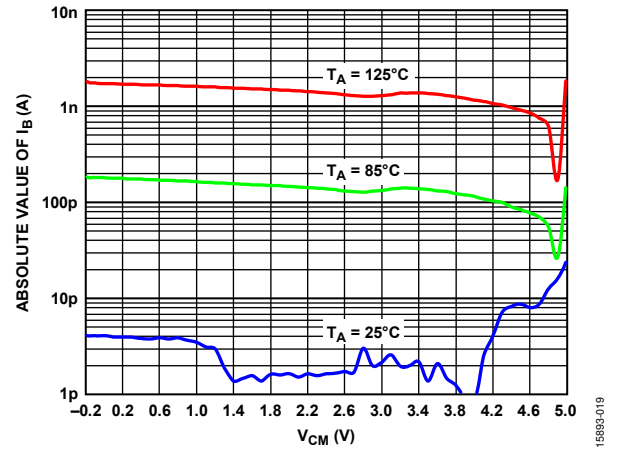

Figure 20. Absolute Value of I_B vs. V_{CM} for Various Temperature, V_{SY} = 5 V

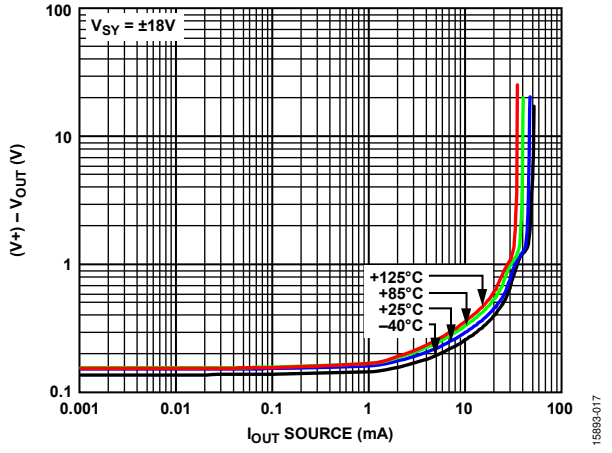

Figure 18. Dropout Voltage ((V+) – V_{OUT}) vs. Output Current (I_{OUT}) Source for Various Temperatures, V_{SY} = ±18 V

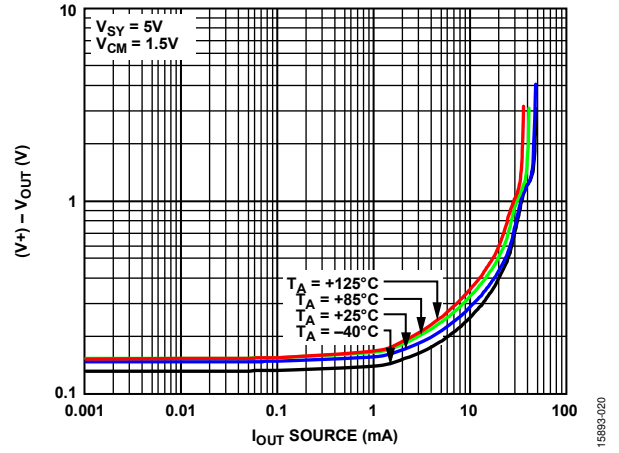

Figure 21. ((V+) – V_{OUT}) vs. I_{OUT} Source for Various Temperatures, V_{SY} = 5 V

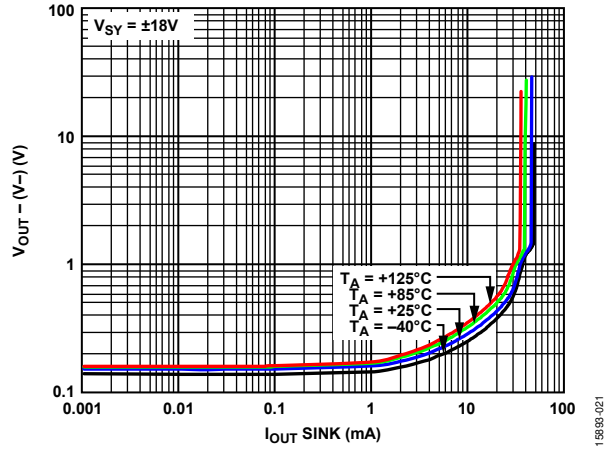

Figure 22. Dropout Voltage (V_{OUT} – (V–)) vs. I_{OUT} Sink for Various Temperatures, V_{SY} = ±18 V

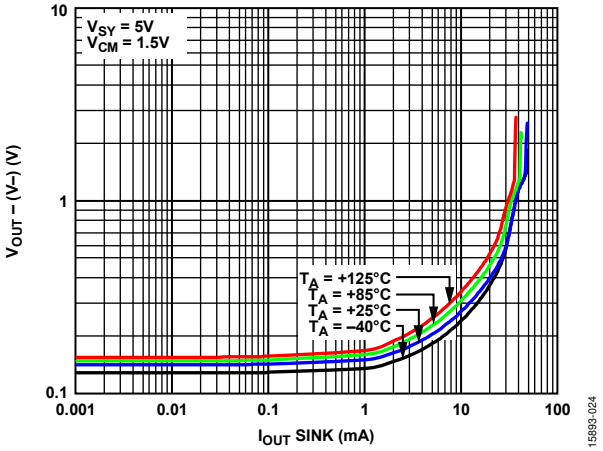

Figure 25. (V_{OUT} – (V–)) vs. I_{OUT} Sink for Various Temperatures, V_{SY} = 5 V

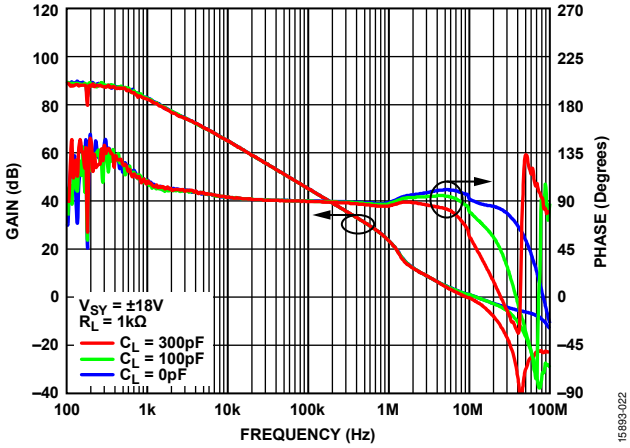

Figure 23. Open-Loop Gain and Phase vs. Frequency, V_{SY} = ±18 V

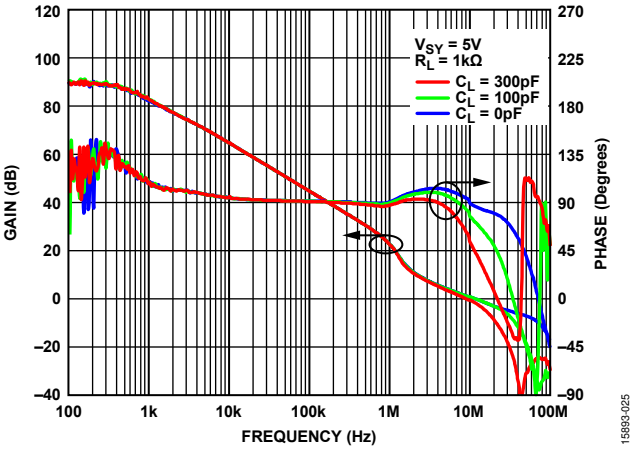

Figure 26. Open-Loop Gain and Phase vs. Frequency, V_{SY} = 5 V

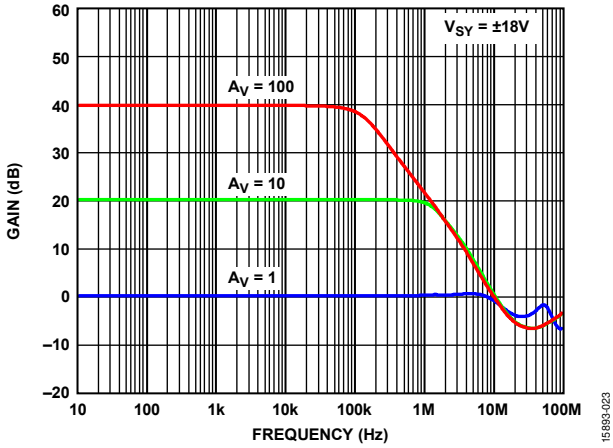

Figure 24. Gain vs. Frequency for Various Closed-Loop Gains, V_{SY} = ±18 V

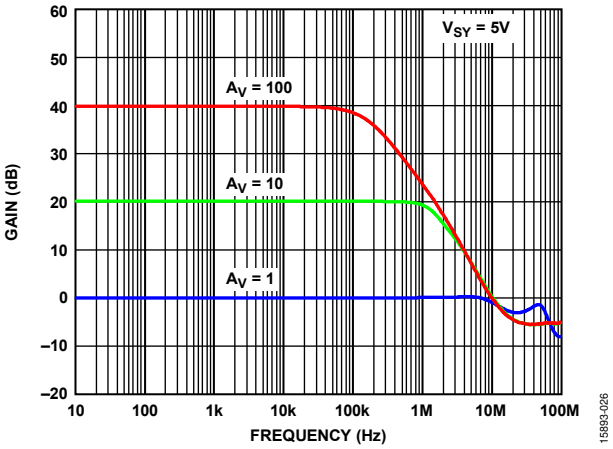

Figure 27. Gain vs. Frequency for Various Closed-Loop Gains, V_{SY} = 5 V

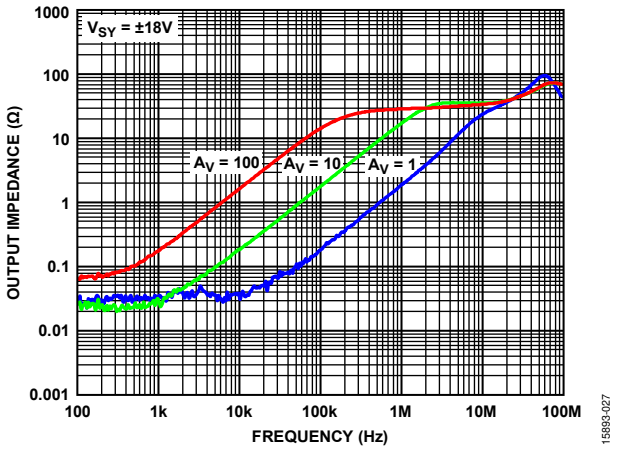

Figure 28. Output Impedance (Z_{OUT}) vs. Frequency, V_{SY} = ±18 V

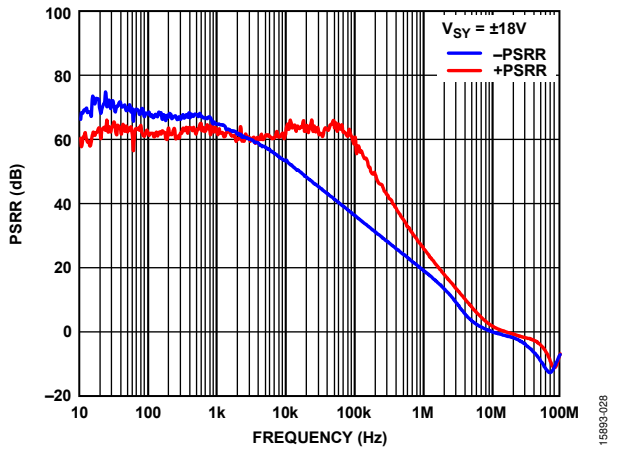

Figure 29. Power Supply Rejection Ration (PSRR) vs. Frequency, V_{SY} = ±18 V

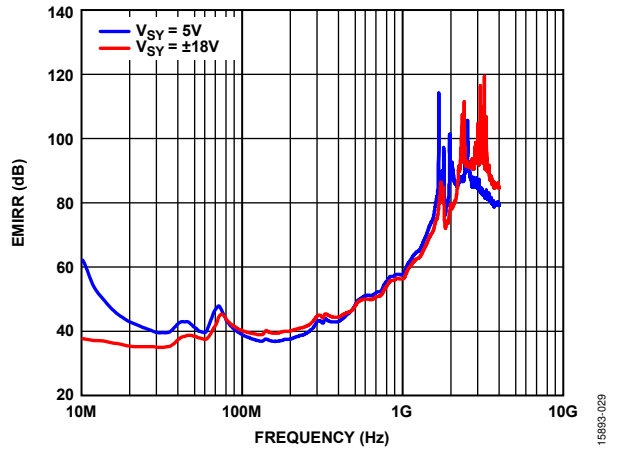

Figure 30. EMI Rejection Ratio (EMIRR) vs. Frequency

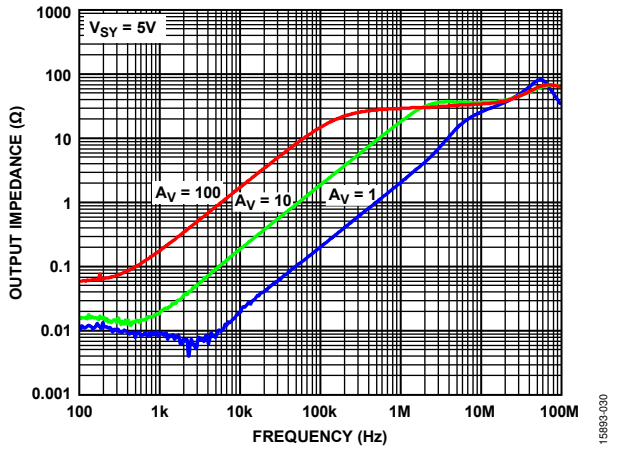

Figure 31. Z_{OUT} vs. Frequency, V_{SY} = 5 V

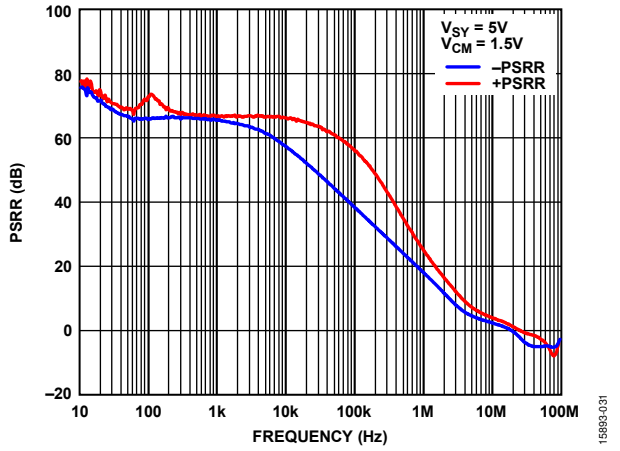

Figure 32. PSRR vs. Frequency, V_{SY} = 5 V

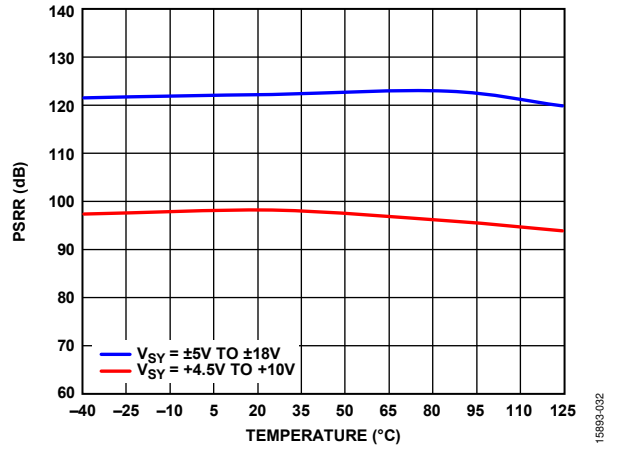

Figure 33. PSRR vs.Temperature

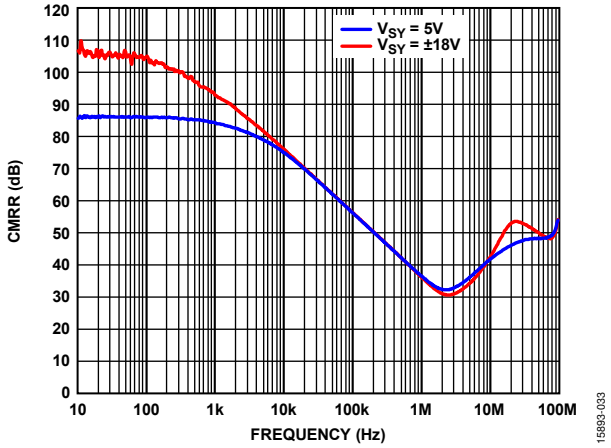

Figure 34. Common-Mode Rejection Ratio (CMRR) vs. Frequency

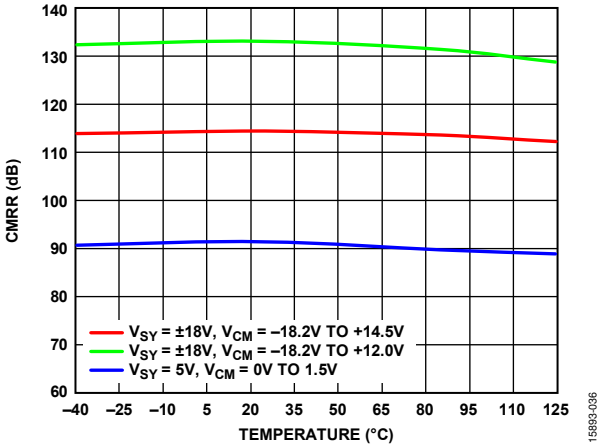

Figure 37. CMRR vs.Temperature

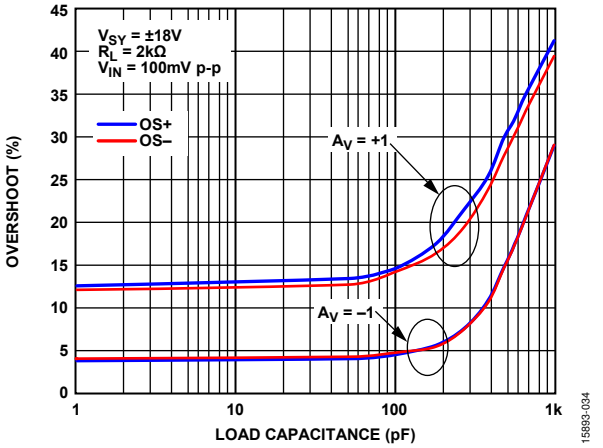

Figure 35. Small Signal Overshoot (OS±) vs. Load Capacitance, V_{SY} = ±18 V

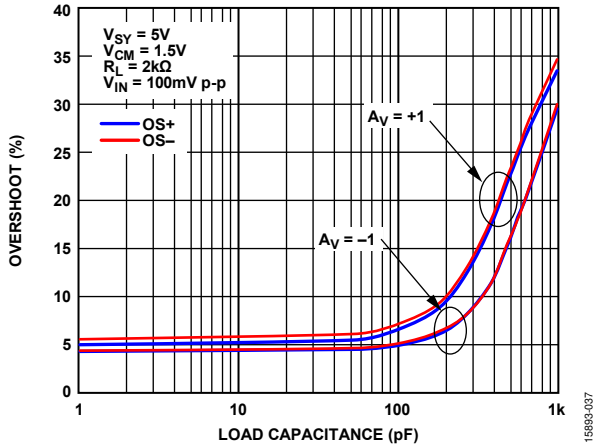

Figure 38. OS± vs. Load Capacitance, V_{SY} = 5 V

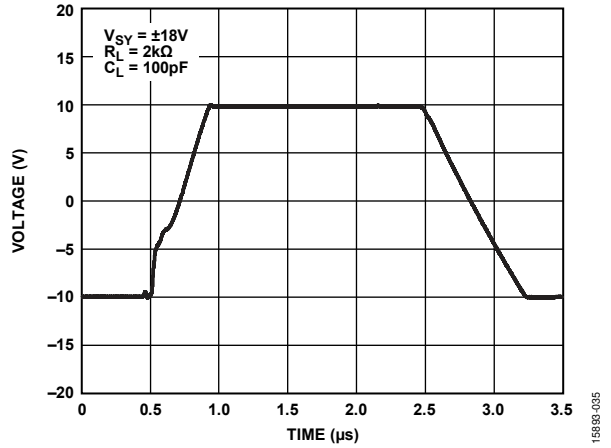

Figure 36. Large Signal Transient Response, A_V = +1, V_{SY} = ±18 V

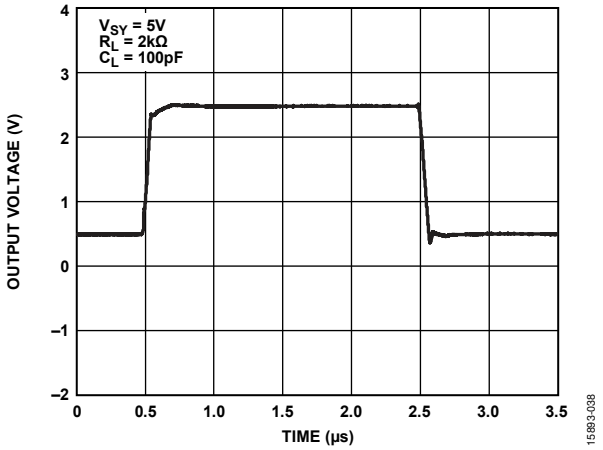

Figure 39. Large Signal Transient Response, A_V = +1, V_{SY} = 5 V

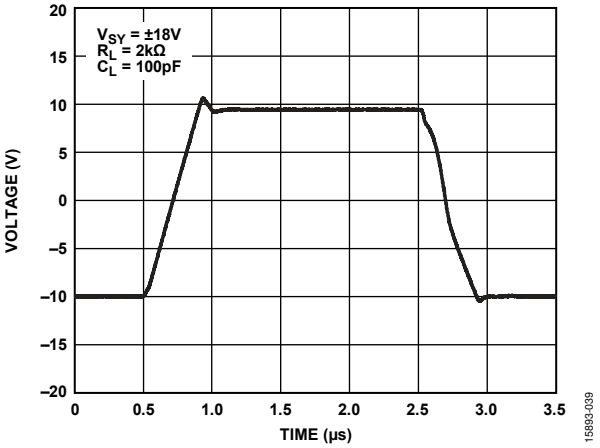

Figure 40. Large Signal Transient Response, A_V = −1, V_{SY} = ±18 V

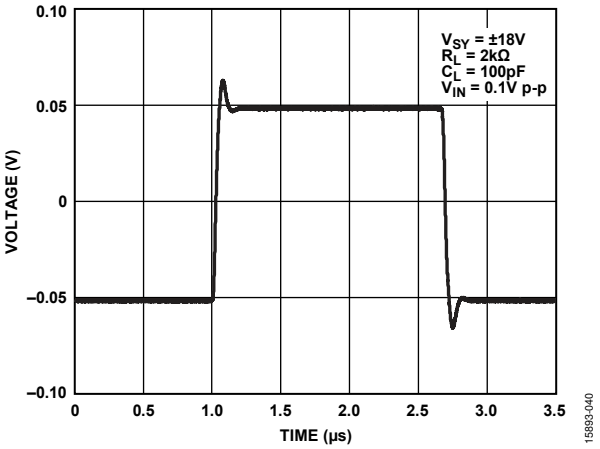

Figure 41. Small Signal Transient Response, A_V = 1, V_{SY} = ±18 V

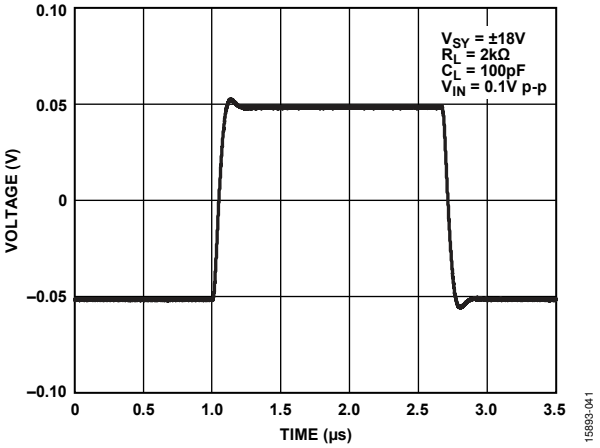

Figure 42. Small Signal Transient Response, A_V = −1, V_{SY} = ±18 V

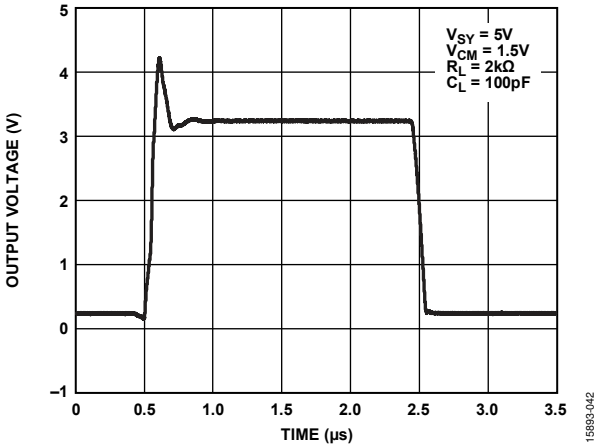

Figure 43. Large Signal Transient Response, A_V = -1, V_{SY} = 5 V

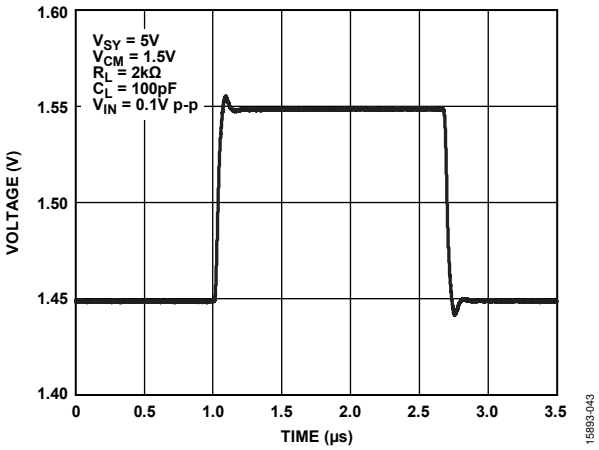

Figure 44. Small Signal Transient Response, A_V = 1, V_{SY} = 5 V

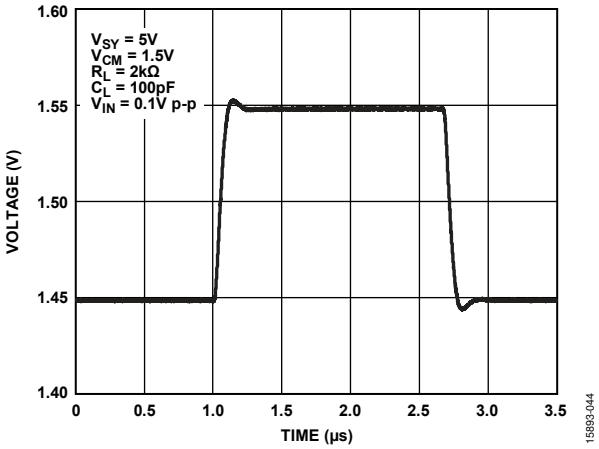

Figure 45. Small Signal Transient Response, A_V = −1, V_{SY} = 5 V

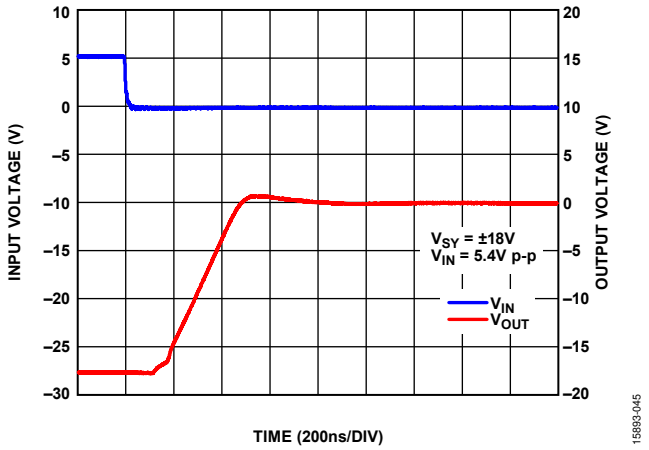

Figure 46. Negative Overload Recovery, $A_V = -10$, $V_{SY} = \pm 18$ V

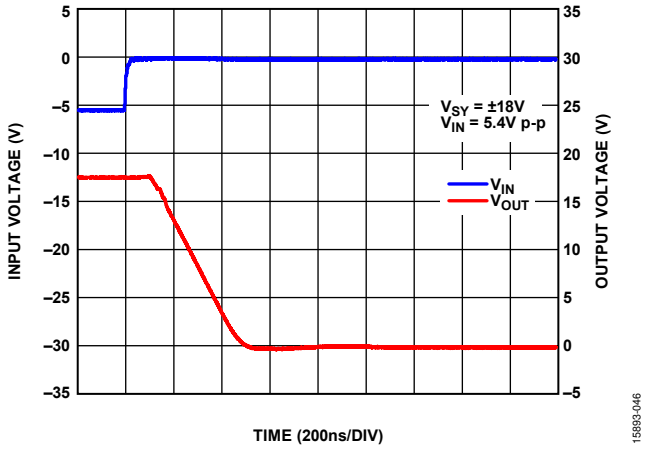

Figure 47. Positive Overload Recovery, $A_V = -10$, $V_{SY} = \pm 18$ V

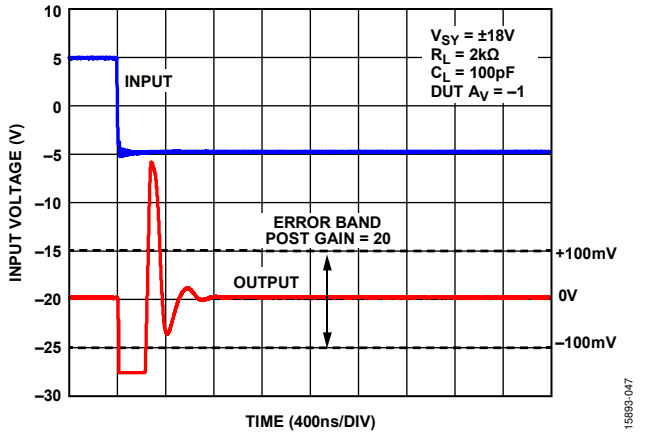

Figure 48. Negative Setting Time to 0.1%, $V_{SY} = \pm 18$ V

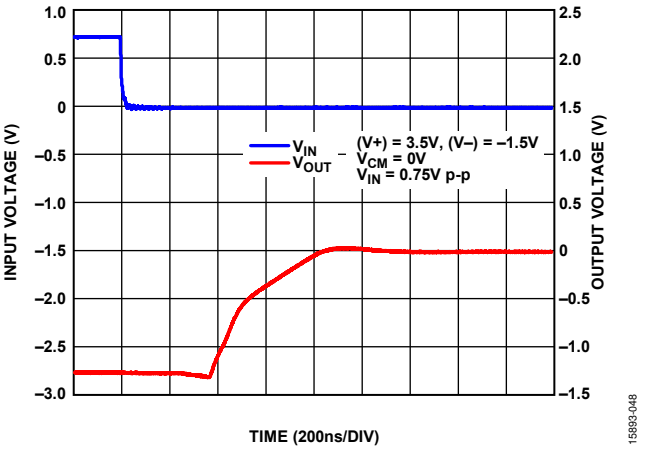

Figure 49. Negative Overload Recovery, $A_V = -10$, $V_{SY} = 5$ V

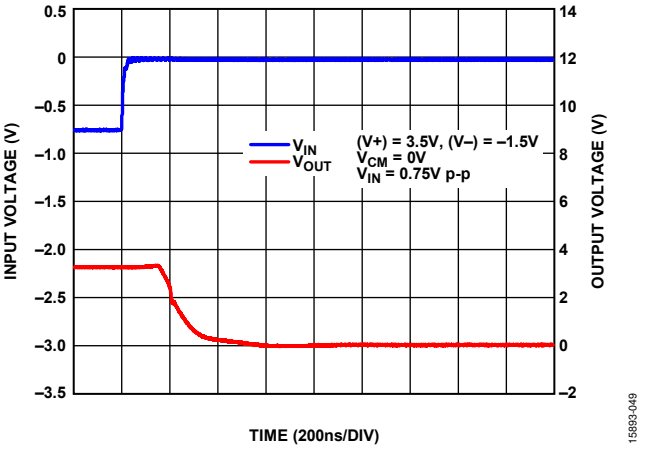

Figure 50. Positive Overload Recovery, $A_V = -10$, $V_{SY} = 5$ V

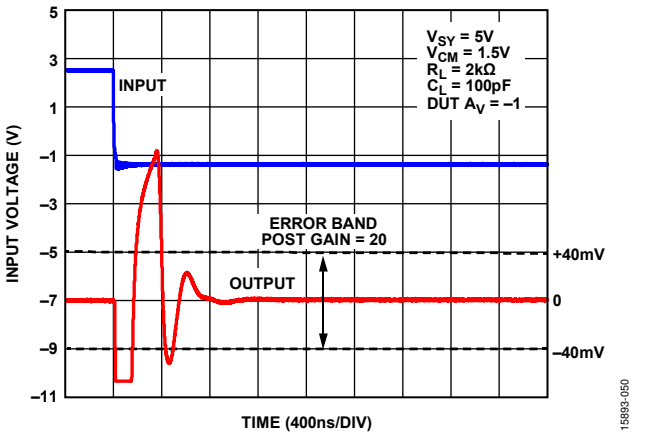

Figure 51. Negative Setting Time to 0.1%, $V_{SY} = 5$ V

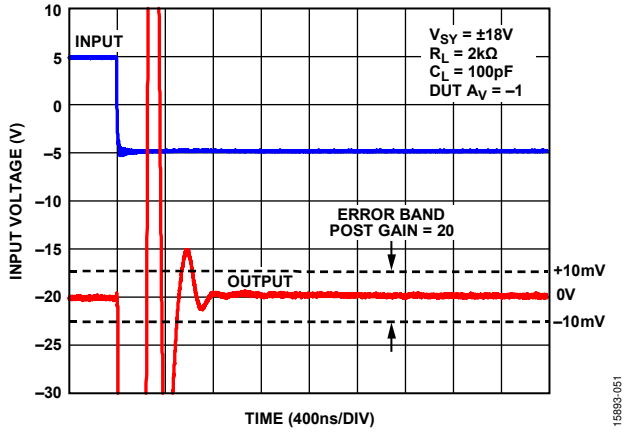

Figure 52. Negative Setting Time to 0.01%, V_{SY} = ±18 V

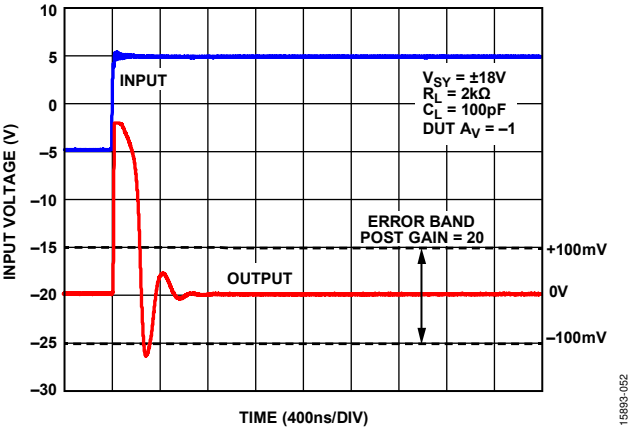

Figure 53. Positive Settling Time 0.1%, V_{SY} = ±18 V

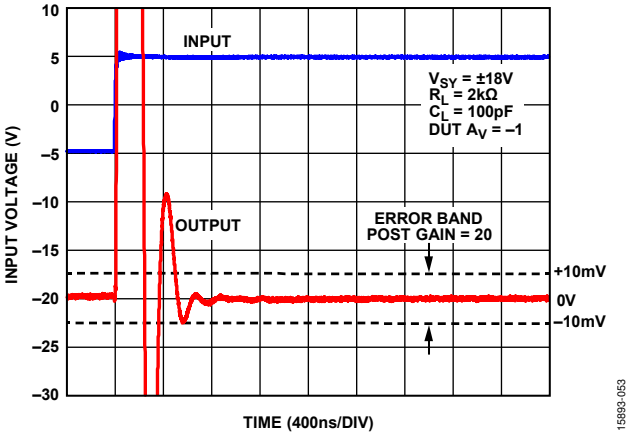

Figure 54. Positive Settling Time 0.01%, V_{SY} = ±18 V

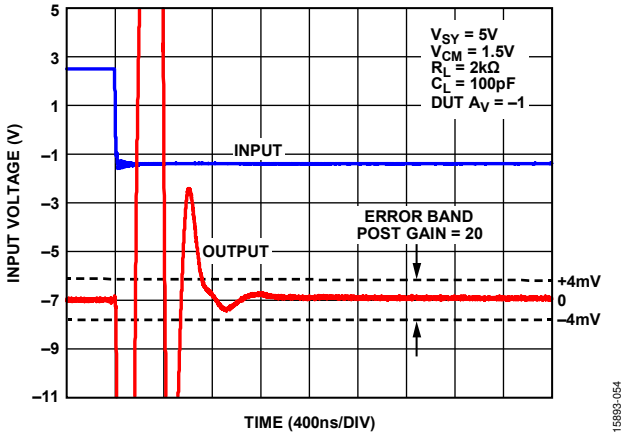

Figure 55. Negative Setting Time to 0.01%, V_{SY} = 5 V

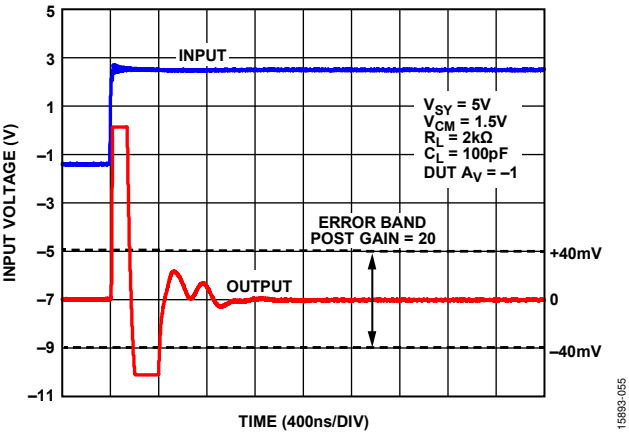

Figure 56. Positive Settling Time 0.1%, V_{SY} = 5 V

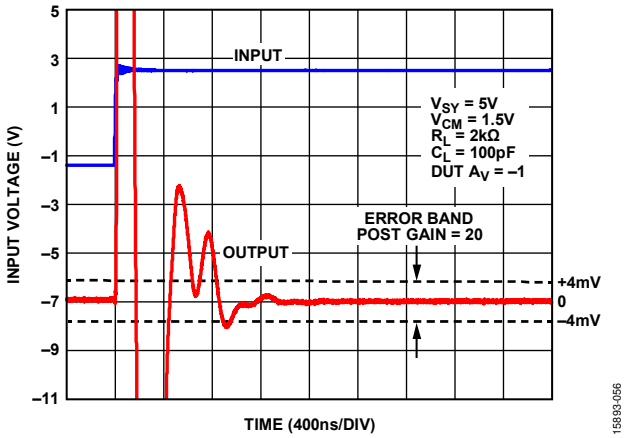

Figure 57. Positive Settling Time 0.01%, V_{SY} = 5 V

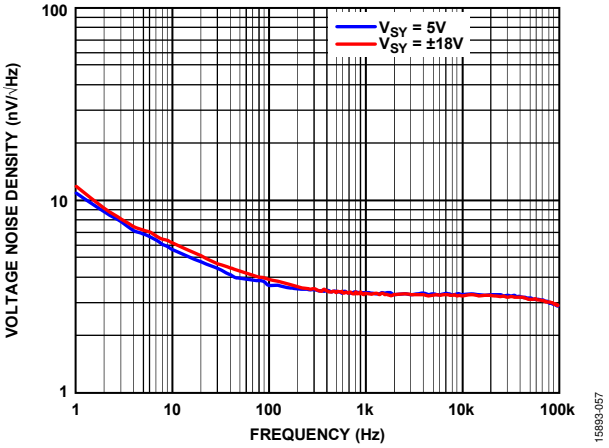

Figure 58. Voltage Noise Density vs. Frequency

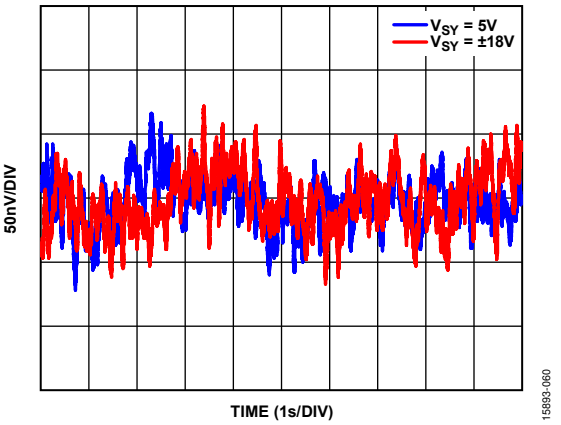

Figure 61. 0.1 Hz to 10 Hz Noise

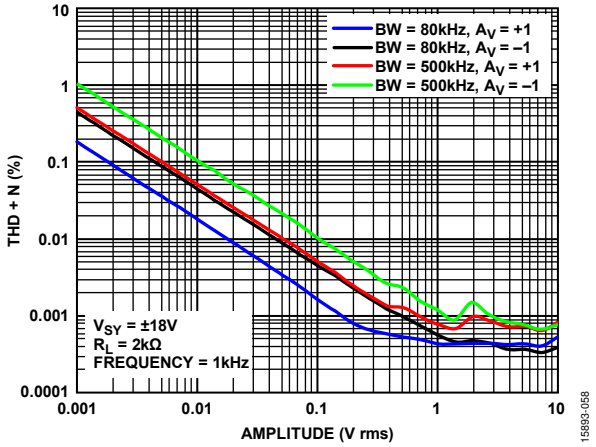

Figure 59. Total Harmonic Distortion + Noise (THD + N) vs. Amplitude, V_{SY} = ±18 V (BW Means Bandwidth)

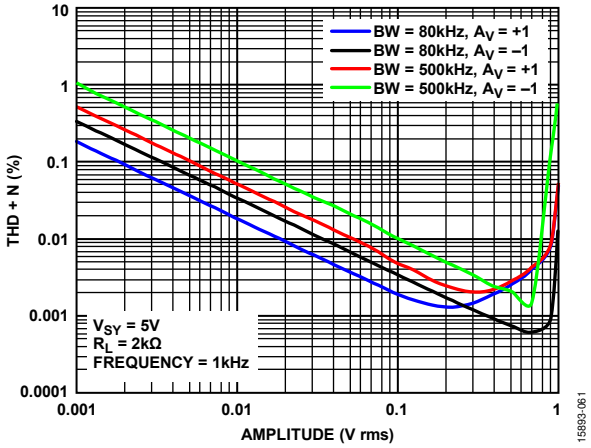

Figure 62. THD + N vs. Amplitude, V_{SY} = 5 V (BW Means Bandwidth)

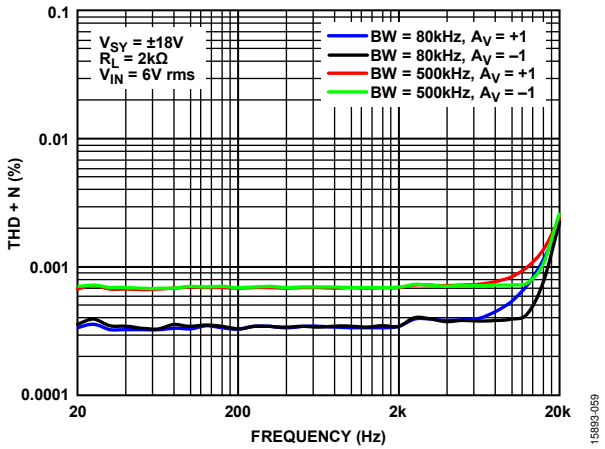

Figure 60. THD + N vs. Frequency, V_{SY} = ±18 V (BW Means Bandwidth)

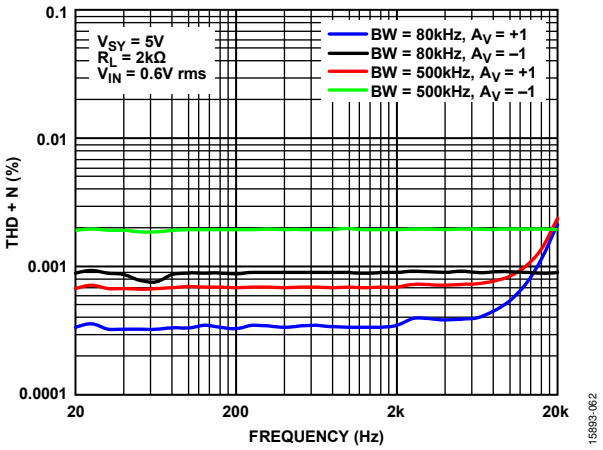

Figure 63. THD + N vs. Frequency, V_{SY} = 5 V (BW Means Bandwidth)

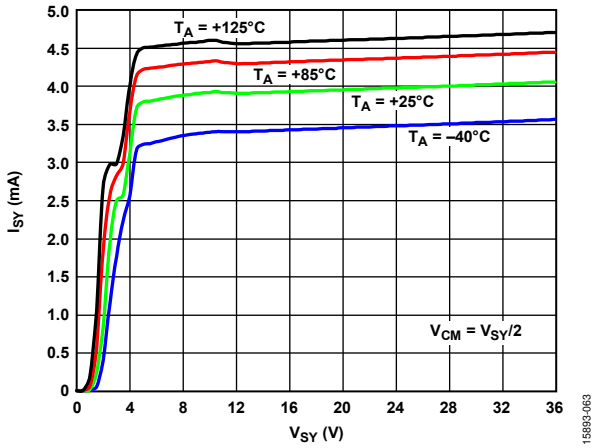

Figure 64. Supply Current (I_{SY}) vs. V_{SY} for Various Temperatures

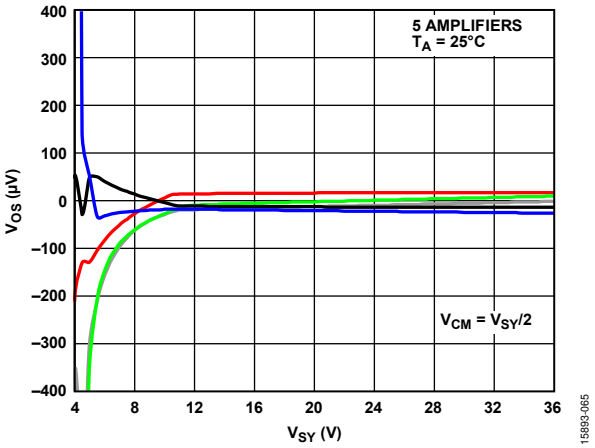

Figure 66. V_{OS} vs. V_{SY}

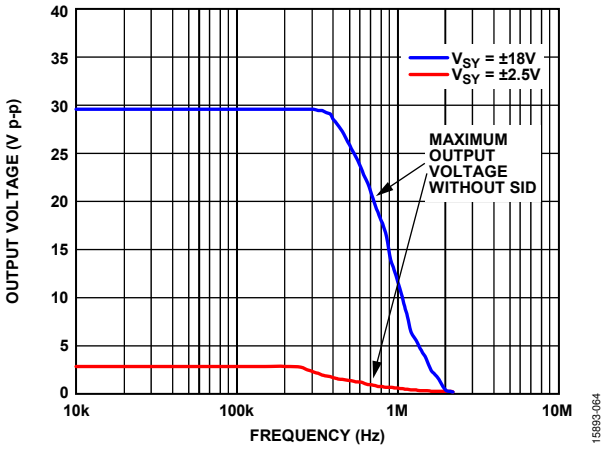

Figure 65. Maximum Peak-to-Peak Output Voltage Without Slew Rate Induced Distortion (SID) vs. Frequency

THEORY OF OPERATION

Figure 67 shows the simplified circuit diagram for the ADA4625-1. The JFET input stage architecture offers the advantages of low input bias current, high bandwidth, high gain, low noise, and no phase reversal when the applied input signal exceeds the common-mode voltage range. The output stage is rail to rail with high drive characteristics and low dropout voltage for both sinking and sourcing currents.

INPUT AND GAIN STAGES

To achieve high input impedance, low noise, low offset, and low offset drift, the ADA4625-1 uses large input N channel JFETs (M1 and M2). These JFETs operate with the S source at about 1.2 V above the G gate. In the worst case, the source is only 0.9 V above the gate. By design, the normal operation of the input tail current (I_{TAIL}) extends down to 0.6 V above V−, which gives the ADA4625-1 an input common-mode range down to 0.2 V below V− with margin. Resistive loads keep the noise low. The BUFF1 buffer drives the top of the input load resistors (R1 and R2), keeping the voltage drop across M1 and M2 nearly constant, making a virtual cascode. The differences of the input voltages of +IN and −IN steer I_{TAIL} through M1 and M2 to R1 and R2, generating a differential voltage. The first voltage to current gain block (GM1) translates that differential voltage into differential currents (I1 and I2) that drive the current mirror (Q1 and Q2), which generates a differential voltage between the reference node and gain node. JFET inputs of the second voltage to current gain block (GM2) maximizes the gain node impedance, giving the ADA4625-1 a high gain.

OUTPUT STAGE

The GM2 gain block generates two pairs of differential currents. One pair drives the bottom current mirror (Q3 and Q4) and the NPN output transistor (Q7), and the second pair drives the top current mirror (Q5 and Q6) and the output PNP transistor (Q8). The common emitter output transistors (Q7 and Q8) source and sink current rail to rail. GM2 also senses the base voltages of Q7 and Q8 and adjusts the I4 and I6 currents; with no output load, Q7 and Q8 collector currents are 0.6 mA. In addition, GM2 clamps the base voltages of Q7 and Q8 so neither completely turns off.

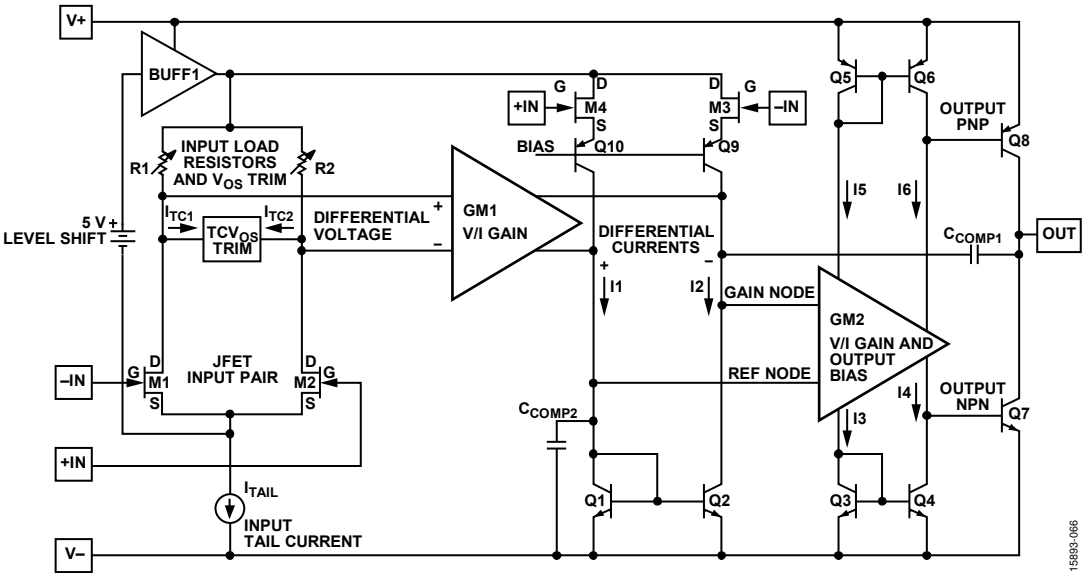

Figure 67. Simplified Circuit Diagram

NO PHASE INVERSION

Rail-to-rail output (RRO) amplifiers without rail-to-rail input (RRI) are prone to phase inversion because the output can drive the input outside of the normal common-mode range, causing the output to go in the wrong direction and latch up. To prevent phase inversion control the input at all times. Even though the RRO of the ADA4625-1 input stage (M1, M2, R1, and R2) operates correctly down to 0.2 V below V−, it does not operate correctly within 2.5 V of V+. The ADA4625-1 guarantees no phase inversion by implementing an input pair (M3 and M4) to extend the common-mode range to 0.2 V above V+, with reduced performance. M3 and M4 are not active in the normal common-mode range. Figure 68 shows that the input voltage exceeds both supplies by 200 mV with no phase inversion at the output.

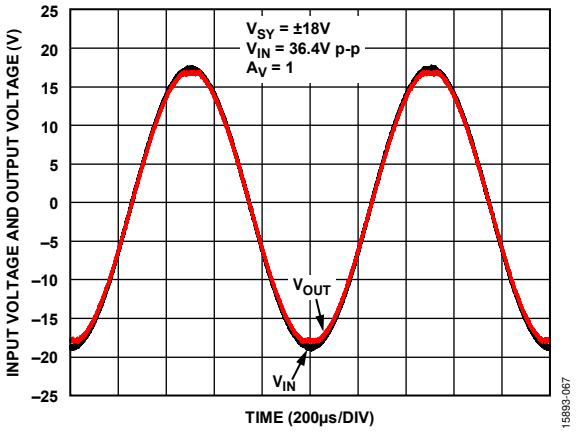

Figure 68. No Phase Reversal If the Input Range Exceeds the Power Supply by 200 mV

SUPPLY CURRENT

The supply current (I_{SY}) is the quiescent current drawn by the op amp with no load. Figure 69 and Figure 70 show that the quiescent current varies with the common-mode input voltage. The shape of I_{SY} vs. V_{CM} at higher V_{CM} shows saturation of BUFF1 and the turn off of I_{TAIL}.

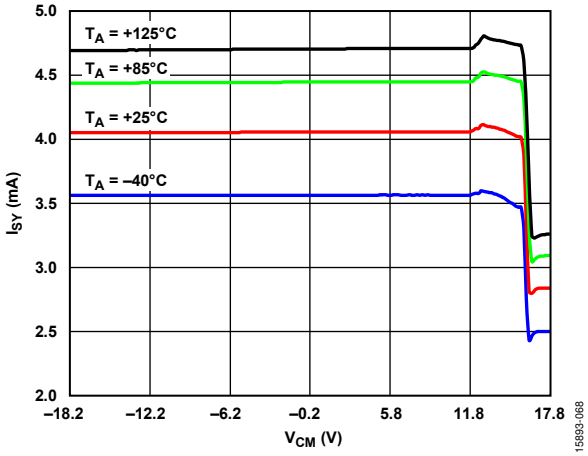

Figure 69. I_{SY} vs V_{CM}, V_{SY} = ±18 V

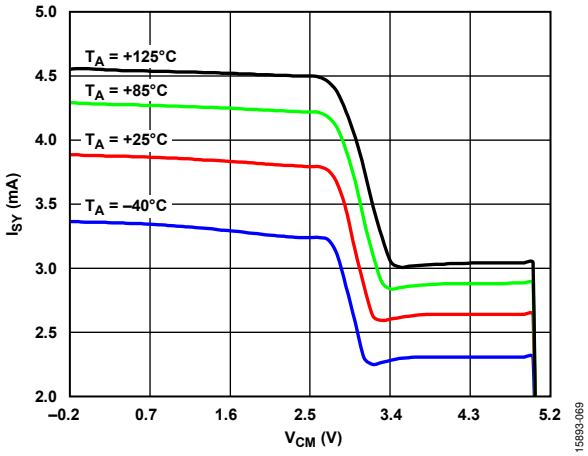

Figure 70. I_{SY} vs V_{CM}, V_{SY} = 5 V

APPLICATIONS INFORMATION

ACTIVE LOOP FILTER FOR PHASE-LOCKED LOOPS (PLLS)

PLL Basic

A PLL is a feedback system that combines a phase detector (PD), a loop filter, and a voltage controlled oscillator (VCO) that is so connected that the oscillator maintains a constant frequency (or phase angle) relative to the reference signal. The functional block diagram of a basic PLL is shown in Figure 71.

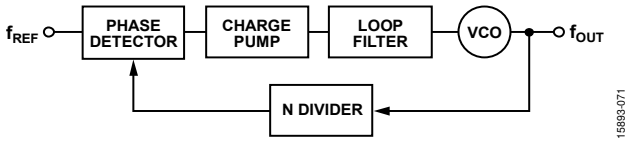

Figure 71. Basic PLL

The phase detector detects the phase difference between the input reference signal and the feedback signal. The resulting error signal is proportional to the relative phase of the input and the feedback signals. The charge pump converts the PD error signal into current pulses. A loop filter circuit is typically required to integrate and smooth the source and sink current pulses from the charge pump into a voltage, which in turn, drives the VCO. The VCO outputs a range of frequencies depending on the voltage level at its tuning port. By making the frequency N divider programmable, the VCO frequency can be tuned in either integer steps or fractional amounts characterizing the PLL as either an integer-N PLL or a fractional-N PLL. Because a PLL is a negative feedback loop, the output of the VCO adjusts as necessary until the frequency error signal is zero and the PLL is in lock. The output frequency is given by $f_{OUT} = N \times f_{REF}$.

Figure 72 shows the block diagram of the basic PLL model in the Laplace transform format, where f_{REF} is the frequency of the input signal, and f_{OUT} is the frequency of the VCO output signal. Because the phase difference is the integral of the frequency difference, there is a 1/s term in the PLL loop.

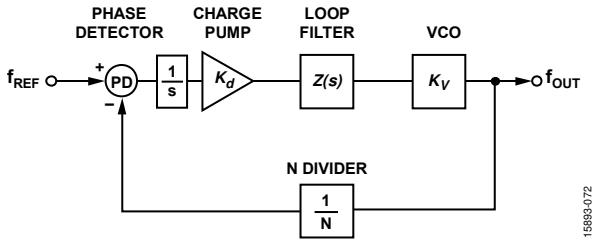

Figure 72. Basic PLL Model

Loop Filter

The loop filter, which smooths out the error signal, is a critical part of the system. For applications that require low phase noise and a wide tuning range, design the VCO with a low gain and a large input voltage range to satisfy these requirements. When the required VCO tuning voltage is higher than the maximum voltage the charge pump can supply, implement an active loop filter comprising of an op amp with gain to accommodate the higher tuning voltages. Figure 73 and Figure 74 illustrate the typical active loop filters in inverting and noninverting topologies, respectively, with prefiltering.

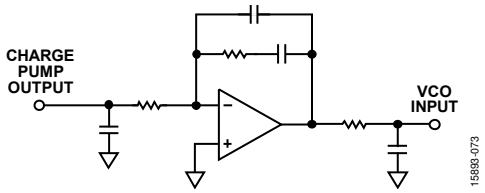

Figure 73. Typical Active Loop Filter—Inverting Topology

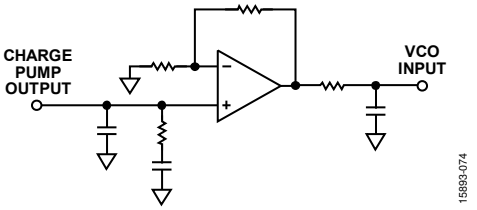

Figure 74. Typical Active Loop Filter—Noninverting Topology

The inverting topology has the advantage of biasing the charge pump output at a fixed voltage, typically one-half the charge pump voltage ($V_P/2$), which is optimal for spur performance. When using the inverting topology, ensure that the PLL IC allows the phase detector polarity to be inverted for the correct polarity voltage at the output of the op amp for driving the VCO.

ADA4625-1 ADVANTAGES AND DESIGN EXAMPLE

The op amp choice for an active filter affects the key performance parameters of the PLLs: frequency range, phase noise, spurious frequencies, and lock time. The output of the filter directly affects the generated frequency and phase. Low noise is essential because any voltage noise applied to the tuning port of the VCO is amplified by the VCO gain and translated into phase noise. Low input bias current is also recommended because the op amp bias current must be sourced from the PLL phase detector/ charge pump, and any mismatch or leakage at the output of the phase detector between the up and down currents causes ripples and reference spurs.

With 18 MHz gain bandwidth product (GBP), low input bias currents (±15 pA), low voltage noise density (3.3 nV/√Hz), ultralow current noise density, and low 1/f corner frequency, the ADA4625-1 is an ideal op amp for using in a PLL active loop filter. The ADA4625-1 does not require a negative voltage supply because of its ground sensing input. The rail-to-rail output stage is beneficial in terms of increasing the flexibility in biasing the op amp so that the output range of the PLL is mapped efficiently onto the input range of the VCO. In addition, the wide 5 V to 36 V operating supply range makes the ADA4625-1 a versatile choice for the design of a wide variety of active loop filters.

Figure 76 shows the ADA4625-1 as the loop filter for the ADF4159, a 13 GHz fractional-N synthesizer. The phase detector polarity of the ADF4159 is programmed to negative because the ADA4625-1 is used in an inverting active loop filter configuration. The VCO is set up to feedback the VCO/2 output to the ADF4159. The loop filter has a 900 kHz loop bandwidth (LBW) and a phase margin of 58° with 2.5 mA charge pump current. Lowering the bandwidth further improves phase noise at the expense of increased PLL lock time.

Figure 75 shows the PLL loop filter transfer function. Capacitor C1 and Resistor R1 change the phase detector current pulses into a continuous time voltage waveform. At frequencies lower than the R2C2 zero, the amplifier and R1C2 form an integrator. Between the R2C2 zero and the R2C3 pole, the gain is constant at the value set by R2/R1. Above the R2C3 pole, the amplifier is an integrator until R1C3 becomes a feedforward noninverting zero path around the amplifier. Resistor R3 and Capacitor C4 add an additional pole in the loop filter signal path. Setting the R3C4 pole below the R2C3 pole reduces the effect of the R1C3 feedforward zero.

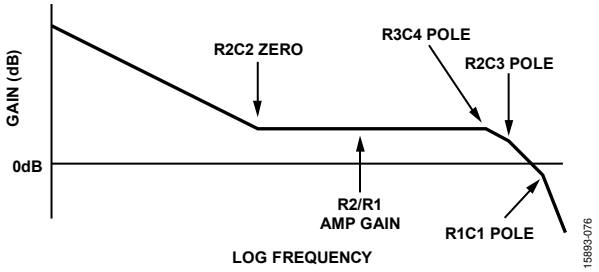

Figure 75. PLL Loop Filter Transfer Function

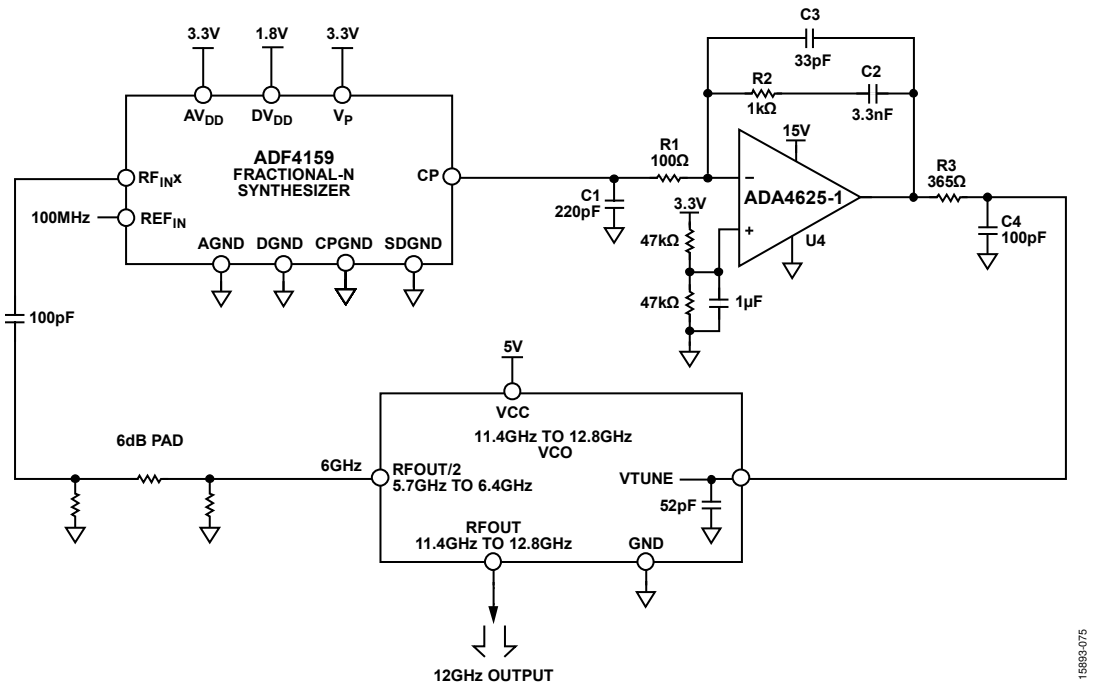

Figure 76. Block Diagram of ADA4625-1 Active Loop Filter for ADF4159

PLLs in which the loop gain passes through 0 dB above the R2C2 zero and below the R2C3 pole and R3C4 pole are stable. At low charge pump currents, the loop gain passes through zero above R2C2 zero. At high charge pump currents, the loop gain passes through zero below the R2C3 pole and R3C4 pole (see Figure 77).

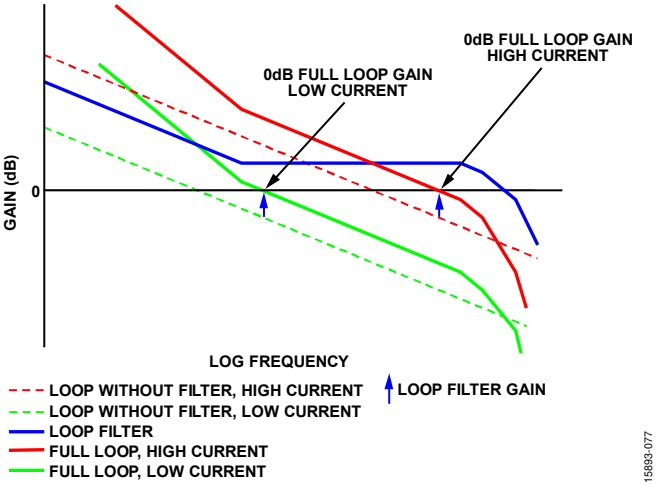

Figure 77. Gain vs. Frequency of PLL and Loop Filter

Figure 78 shows the measured phase noise vs. frequency offset from 12 GHz carrier for different charge pump currents (I_{CP}). Generally, most operations have a charge pump current of 2.5 mA and below. Refer to the UG-383 User Guide for details on running these tests and setting up the software required.

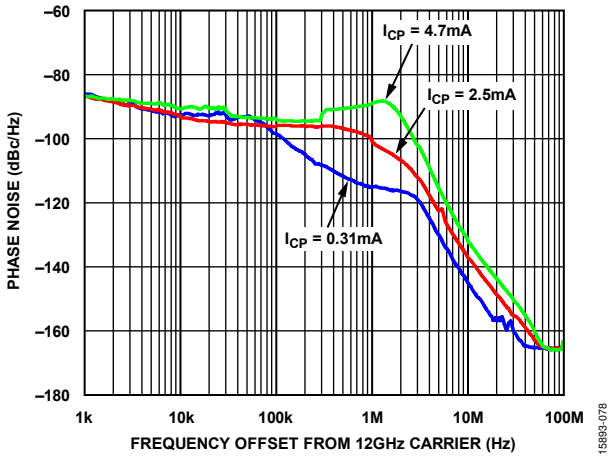

Figure 78. Phase Noise vs. Frequency Offset from 12 GHz Carrier for Different Charge Pump Currents (I_{CP})

The Analog Devices simulation tool, ADIsimPLL, allows the design and simulation of PLL loop filter topologies and has a library of Analog Devices op amps built in. The simulation tool accurately predicts PLL closed-loop phase noise and is able to model the effect of op amp noise along with the noise of the other PLL loop components. For more information about the ADIsimPLL design tools, refer to www.analog.com/ADIsimPLL.

TRANSIMPEDANCE AMPLIFIER

The ADA4625-1 is an excellent choice for low noise transimpedance amplifier (TIA) applications. While its low voltage and current noise maximize signal-to-noise ratio (SNR), its low voltage offset and input bias current minimize the dc error at the amplifier output. Having a true ground sense capability, the ADA4625-1 is ideal for single-supply operation. In addition, its rail-to-rail output swing allows the detection and amplification of a wide range of input current signals. Figure 79 shows the ADA4625-1 as a current to voltage (I-V) converter with an electrical model of a photodiode.

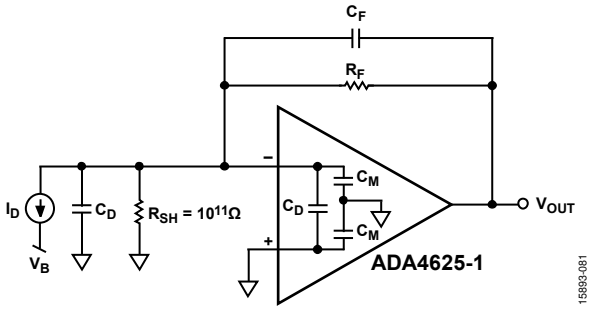

Figure 79. Equivalent TIA Circuit

Photodiodes can operate in either photovoltaic mode (zero bias) or photoconductive mode (with an applied reverse-bias across the diode). Mode selection depends on the speed and dark current requirements of the application and the choice of photodiode. In photovoltaic mode, the dark current is at a minimum and is preferred for low frequency and/or low light level applications (that is, PN photodiodes). Photoconductive mode is better for applications that required faster and linear responses (that is, PIN photodiodes); however, the tradeoffs include increases in dark and noise currents.

The following transfer function describes the transimpedance gain of Figure 79:

$$V_{OUT} = \frac{I_D R_F}{1 + sC_F R_F} \quad (1)$$

where:
V_{OUT} is the desired output dc voltage of the op amp.
I_D is the output current of the photodiode.
R_F and C_F are the feedback resistor and capacitor. The parallel combination of R_F and C_F sets the signal bandwidth.
s is the s plane.

Set R_F such that the maximum attainable output voltage corresponds to the maximum diode output current. Because signal levels increase directly with R_F, while the noise due to R_F increases with the square root of the resistor value, employing the full output swing maximizes the SNR.

It is important to distinguish between the signal gain and the noise gain (NG) because the noise gain characteristics determine the net circuit stability. The noise gain has the same transfer function as the noninverting signal gain, which follows:

$$NG = \left(1 + \frac{R_F}{R_{SH}}\right) \times \frac{1 + s(R_F // R_{SH})(C_{IN} + C_F)}{1 + sR_F C_F} \quad (2)$$

where:
R_{SH} is the diode shunt resistance.
C_{IN} is the total input capacitance consisting of the sum of the diode shunt capacitance (C_D), the input capacitance of the amplifier ($C_{DM} + C_{CM}$), and the external stray capacitance.
C_{IN} and R_F produce a zero in the noise gain transfer function and the zero frequency (f_Z) is as follows:

$$f_Z = \frac{1}{2\pi (R_F // R_{SH})(C_{IN} + C_F)} \quad (3)$$

Because the photodiode shunt resistance $R_{SH} >> R_F$, the circuit behavior is not impacted by the effect of the junction resistance, and f_Z simplifies to

$$f_Z = \frac{1}{2\pi R_F (C_{IN} + C_F)} \quad (4)$$

Figure 80 shows the TIA noise gain superimposed upon the open loop gain of the amplifier. For the system to be stable, the noise gain curve must intersect with the open loop response with a net slope of less than 20 dB/decade. In Figure 80, the dotted line shows an uncompensated noise gain (C_F = 0 pF) intersecting with the open loop gain at the frequency (f_X) with a slope of 20 dB/decade, indicating an unstable condition.

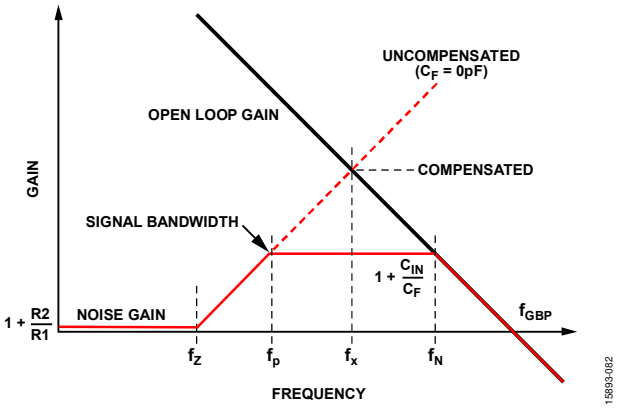

Figure 80. Generalized TIA Noise Gain and Transfer Function

The instability caused by C_{IN} can be compensated by adding C_F to introduce a pole at a frequency equal to or lower than f_X. The pole frequency is as follows:

$$f_P = \frac{1}{2\pi R_F C_F} \quad (5)$$

Setting the pole at the f_X frequency maximizes the signal bandwidth with a 45° phase margin but is marginal for stability, as indicated by the dashed line. Because f_X is the geometric mean of f_Z and the gain bandwidth product frequency (f_{GBP}) of the amplifier, calculate f_X by

$$f_X = \sqrt{f_Z f_{GBP}} \quad (6)$$

Substituting Equation 4 and Equation 5 into Equation 6, the C_F value that produces f_X is

$$C_F = \frac{1 + \sqrt{1 + 8\pi R_F C_{IN} f_{GBP}}}{4\pi R_F f_{GBP}} \quad (7)$$

If $8\pi \times R_F \times C_{IN} \times f_{GBP} >> 1$, Equation 7 simplifies to

$$C_F = \sqrt{\frac{C_{IN}}{2\pi R_F f_{GBP}}} \quad (8)$$

Adding C_F also sets the signal bandwidth at f_P. Substitute Equation 8 into Equation 5 and rearrange the equation for the signal bandwidth in terms of f_{GBP}, R_F, and C_{IN}:

$$f_P = \sqrt{\frac{f_{GBP}}{2\pi R_F C_{IN}}} \quad (9)$$

Notice the attainable signal bandwidth is a function of the time constant $R_F C_{IN}$ and the f_{GBP} of the amplifier. To maximize the signal bandwidth, choose an op amp with high bandwidth and low input capacitance, and operate the photodiode in reverse bias to reduce its junction capacitance.

Because the input current noise of the FET input op amp is negligible, and the shot noise of the photodiode is negligible due to the filtering effect of the shunt capacitance, the dominant sources of output noise in the wideband photodiode TIA circuit are the input voltage noise of the amplifier e_N and the thermal noise generated by R_F.

At low frequencies, the circuit noise gain is $1 + R_F/R_{SH}$. At frequencies equal to or greater than f_Z, the noise gain begins to increase and plateau when the gain is $1 + C_{IN}/C_F$ (see Figure 80). In addition, the noise bandwidth frequency, f_N (where the compensated noise gain intersecting the open loop gain), can be estimated by

$$f_N = \frac{C_F}{(C_{IN} + C_F)} f_{GBP} \quad (10)$$

Design Example

As a design example, Figure 81 shows the ADA4625-1 configured as a TIA amplifier in a photodiode preamp application. Assuming the photodiode has a C_D of 5 pF and an I_D of 200 µA, and the desired full-scale V_{OUT} is 10 V, and using Equation 1, R_F is 50 kΩ.

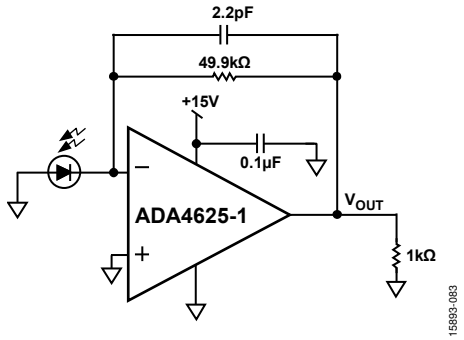

Figure 81. Single-Supply TIA Circuit Using the ADA4625-1

The ADA4625-1 input capacitance (C_{CM} + C_{DM}) is 19.9 pF; therefore, the total input capacitance (C_{IN}) is 24.9 pF. By substituting C_{IN} = 24.9 pF, R_F = 50 kΩ, and f_{GBP} = 18 MHz into Equation 7 and Equation 9, the resulting feedback capacitor value (C_F) and the −3 dB signal bandwidth (f_P) are 2.2 pF and 1.45 MHz, respectively.

Figure 82 and Figure 83 show the compensations of the TIA circuit. The system has a bandwidth of 1.45 MHz when it is maximized for a signal bandwidth with C_F = 2.2 pF. Increasing C_F to 3.9 pF reduces the bandwidth to 0.82 MHz; however, it greatly reduces the overshoot (see Figure 84). In practice, an optimum C_F value is determined experimentally by varying it slightly to optimize the output pulse response.

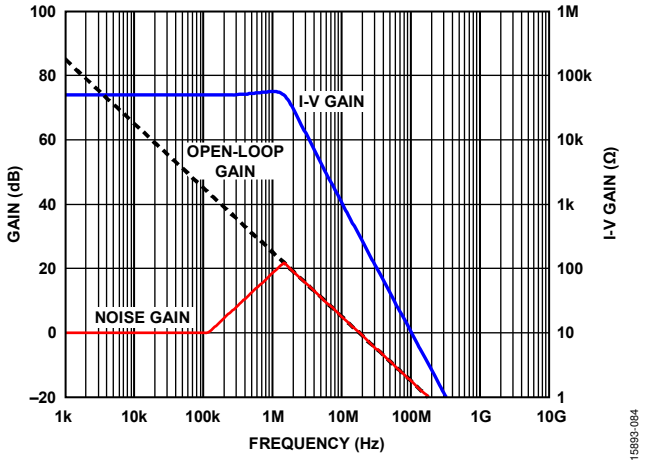

Figure 82. Compensating the TIA, C_F = 2.2pF

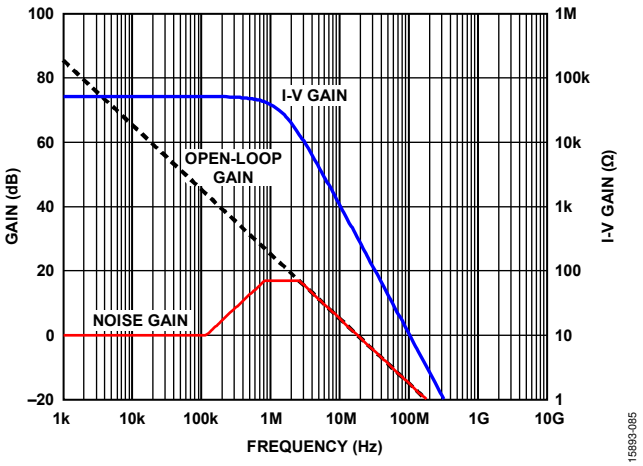

Figure 83. Compensating the TIA, C_F = 3.9 pF

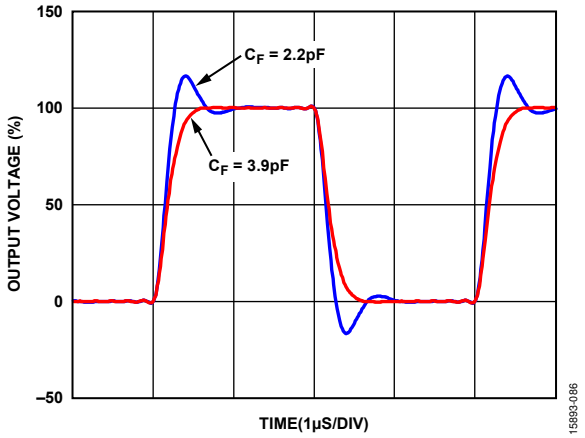

Figure 84. Pulse Response vs. C_F

Table 7 shows the noise sources and estimated total output noise for the photodiode amplifier with C_F = 2.2 pF and C_F =3.9 pF, respectively.

Use the Analog Devices Analog Photodiode Wizard to design a transimpedance amplifier circuit to interface with a photodiode.

Table 7. RMS Noise Contributions of the Photodiode Preamplifier

Noise Contributor	Expression	RMS Noise (μV)[1]	
		C_F = 2.2 pF	**C_F = 3.9 pF**
R_F	$\sqrt{4kTR_F\left(\frac{\pi}{2}f_P\right)}$ where: *k* is Boltzmann's constant (1.38 × 10^{-23} J/K). *T* is the temperature in Kelvin (K).	43.2	32.5
Current Noise, $V_{ni, AMP}$	$i_N R_F \sqrt{\frac{\pi}{2}f_p}$	0.34	0.25
Voltage Noise, $V_{nv, AMP}$	$e_N\sqrt{\left(1+\frac{C_{IN}}{C_F}\right)\frac{\pi}{2}f_{GBP}}$	61.6	47.7
Total Noise	$\sqrt{V_{nv, AMP}{}^2 + V_{nv, AMP}{}^2 + V_{R_F}{}^2}$	75.2	57.7

[1] RMS noise with R_F = 49.9 kΩ, $C_{IN} = C_{CM} + C_{DM}$ = 19.9 pF, C_D = 5 pF, i_N = 4.5 fA/√Hz, and e_N =3.3 nV/√Hz.

RECOMMENDED POWER SOLUTION

Analog Devices has a wide range of power management products to meet the requirements of most high performance signal chains.

For a dual-supply application, the ADA4625-1 typically needs a ±15 V supply. Low dropout (LDO) linear regulators such as the ADP7118 or the ADP7142 for the positive supply and the ADP7182 for the negative supply help improve the PSRR at high frequency and generate a low noise power rail. In addition, if a negative supply is not available, the ADP5070 can generate the negative supply from a positive supply. Figure 85 shows an example of this power solution configuration for the ADA4625-1.

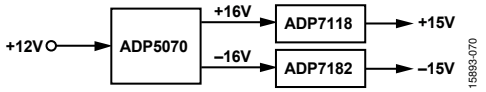

Figure 85. Power Solution Configuration for the ADA4625-1

Table 8. Recommended Power Management Devices

Product	Description
ADP5070	DC-to-dc switching regulator with independent positive and negative outputs
ADP7118	20 V, 200 mA, low noise, CMOS LDO linear regulator
ADP7142	40 V, 200 mA, low noise, CMOS LDO linear regulator
ADP7182	−28 V, −200 mA, low noise, linear regulator

It is recommended to use a low ESR, 0.1 µF bypass capacitor close to each power supply pins of the ADA4625-1 and ground to reduce errors coupling in from the power supplies. For noisy power supplies, place an additional 10 µF capacitor in parallel with the 0.1 µF for better performance.

INPUT OVERVOLTAGE PROTECTION

The ADA4625-1 has internal protective circuitry that allows voltages as high as 0.2 V beyond the supplies to be applied at the input of either terminal without causing damage. For higher input voltages, a series resistor is necessary to limit the input current. Determine the resistor value by

$$(V_{IN} - V_S)/R_S \leq 20 \text{ mA}$$

where:
V_{IN} is the input voltage.
V_S is the voltage of either V+ or V−.
R_S is the series resistor.

With a very low bias current of <5.5 nA up to 125°C, higher resistor values can be used in series with the inputs. A 500 Ω resistor protects the inputs from voltages as high as 10 V beyond the supplies and adds less than 2.75 µV to the offset. However, note that the added series resistor (R_S) may increase the overall noise and lower the bandwidth due to the addition of a pole introduced by R_S and the input capacitor of the amplifier.

DRIVING CAPACITIVE LOADS

The inherent output resistance of the op amp combined with a capacitive load forms an additional pole in the transfer function of the amplifier. Adding capacitance to the output of any op amp results in additional phase lag. This lag reduces stability and leads to overshoot or oscillation, which is a common situation when an amplifier is used to drive the input of switched capacitor analog-to-digital converters (ADCs).

The ADA4625-1 has a high phase margin and low output impedance and is capable of directly driving a capacitive load up to 1 nF with no external compensation at unity-gain without oscillation.

For other considerations and various circuit solutions, see the *Ask the Applications Engineer-25, Op Amps Driving Capacitive Loads* Analog Dialogue article.

THERMAL MANAGEMENT

The ADA4625-1 can operate with up to a 36 V supply voltage with a typical 4 mA quiescent current. Heavy loads increase power dissipation and raise the chip junction temperature.

The maximum safe power dissipation for the ADA4625-1 is limited by the associated rise in junction temperature (T_J) on the die. Two conditions affect T_J: power dissipation (P_D) of the device and ambient temperature (T_A) surrounding the package. This relationship is shown in Equation 11.

$$T_J = P_D \times \theta_{JA} + T_A \quad (11)$$

where θ_{JA} is the thermal resistance between the die and the ambient environment. The total power dissipation in the amplifier is the sum of the power dissipated in the output stage plus the quiescent power. Power dissipation for the sourcing current is shown in Equation 12, where V_{SY} is the total supply voltage $(V+) - (V-)$.

$$P_D = V_{SY} \times I_{SY} + ((V+) - V_{OUT})I_{OUT} \quad (12)$$

Replace $((V+) - V_{OUT})$ in Equation 12 with $((V-) - V_{OUT})$ when sinking current.

For symmetrical supplies with a ground referenced load, use the following equation to calculate the average power for the amplifier processing sine signal.

$$P_{AVG,SINE} = (V_{SY} \times I_{SY}) + \left(\frac{2}{\pi} \times \frac{(V+) \times V_{PEAK}}{R_L}\right) - \left(\frac{V_{PEAK}^2}{2 \times R_L}\right) \quad (13)$$

where V_{PEAK} is the peak value of a sine wave output voltage.

The specified thermal resistance θ_{JA} of the ADA4625-1 is 52.8°C/W. A good PCB layout and an external heat sink can improve thermal performance by reducing junction to ambient temperature.

The ADA4625-1 features an exposed pad that floats internally to provide the maximum flexibility and ease of use. Solder the exposed pad to the PCB board GND, or the V+ or V− plane for best thermal transfer. Where thermal heating is not an issue, the exposed pad can be left floating.

Incorporate the use of thermal vias or heat pipes into the design of the mounting pad for the exposed pad to lower the overall θ_{JA}.

OUTLINE DIMENSIONS

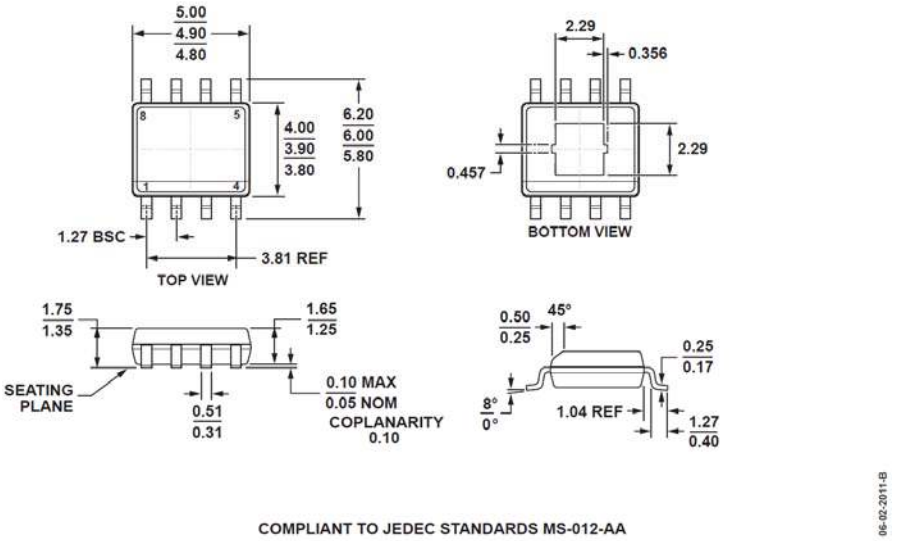

Figure 86. 8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]
Narrow Body
(RD-8-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADA4625-1ARDZ	−40°C to +125°C	8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]	RD-8-1
ADA4625-1ARDZ-R7	−40°C to +125°C	8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]	RD-8-1
ADA4625-1ARDZ-RL	−40°C to +125°C	8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]	RD-8-1
EVAL-ADA4625-1ARDZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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