19-2098; Rev 2; 7/04

MAXIM

Dual-Rate, 1Gbps/2Gbps Fibre Channel Quad-Port Bypass ICs with Repeater

General Description

The MAX3754/MAX3755 quad-port bypass circuits (PBCs) are designed for use in Fibre Channel Arbitrated Loop applications. Each consists of four serially connected port bypass circuits and a repeater that provides clock and data recovery. The quad-PBC allows connection of up to four Fibre Channel L-ports; each can be enabled or bypassed by individual logic inputs. To reduce the external parts count, all signal inputs and outputs have internal termination resistors. The MAX3754/MAX3755 comply with Fibre Channel jitter tolerance requirements and can recover data signals with up to 0.7 unit intervals (UIs) of high-frequency jitter. These devices operate from a single +3.3V supply.

Applications

1.0625Gbps/2.125Gbps Dual-Rate Fibre Channel

Fibre Channel Data Storage Systems

Storage Area Networks

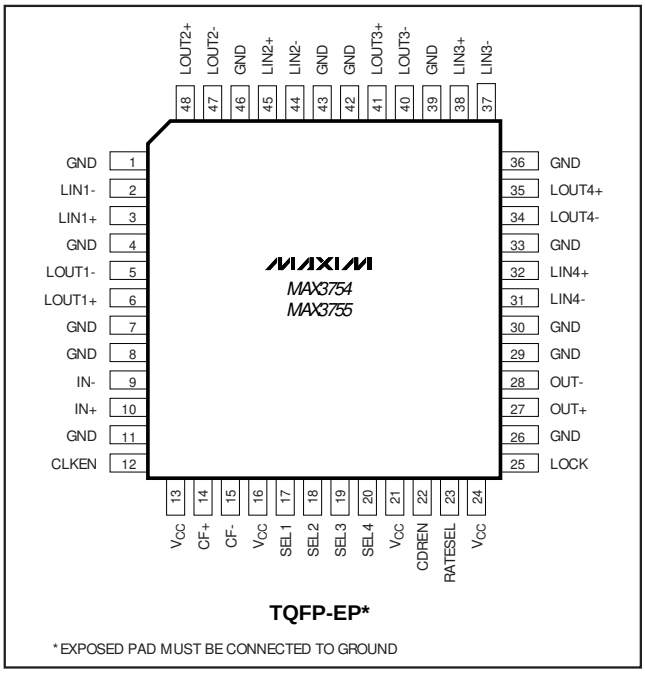
Fibre Channel Hubs

Typical Operating Circuit appears at end of data sheet.

Features

- **Pin Selectable 1.0625Gbps/2.125Gbps Dual-Rate Operation**
- **Meets Fibre Channel Jitter Tolerance**
- **1400mV Typical Differential Output Swing**
- **3.0V to 3.6V Operation**
- **No Reference Clock Required**
- **Frequency Lock Indication**
- **1W Power Consumption (MAX3754) at +3.3V**
- **150Ω or 100Ω Differential L-Port Impedance Available**

Pin Configuration



TQFP-EP*

*EXPOSED PAD MUST BE CONNECTED TO GROUND

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	DIFFERENTIAL LIN AND LOUT TERMINATION	DIFFERENTIAL IN AND OUT TERMINATION
MAX3754CCM	0°C to +70°C	48 TQFP-EP*	150Ω	100Ω
MAX3755CCM	0°C to +70°C	48 TQFP-EP*	100Ω	100Ω
MAX3755CCM+	0°C to +70°C	48 TQFP-EP*	100Ω	100Ω

*EP = Exposed pad.

+Denotes lead-free package.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Dual-Rate, 1Gbps/2Gbps Fibre Channel Quad-Port Bypass ICs with Repeater

ABSOLUTE MAXIMUM RATINGS

V_{CC} .....-0.5V to +5V
Current into OUT±, LOUT1±, LOUT2±, LOUT3±, LOUT4± 22mA
Voltage at OUT±, LOUT1±, LOUT2±, LOUT3±, LOUT4± .....(V_{CC} - 1.65V) to (V_{CC} + 0.5V)
Voltage at IN±, LIN1±, LIN2±, LIN3±, LIN4± .....-0.5V to (V_{CC} + 0.5V)
Voltage at CLKEN, CF+, CF-, CDREN, RATESEL, SEL_, LOCK.....-0.5V to (V_{CC} + 0.5V)
Current into LOCK.....-1mA to +10mA
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFP-EP (derate 30.0mW/°C above +70°C) 2W
Operating Junction Temperature Range.....-55°C to +150°C
Operating Temperature Range .....-55°C to +110°C
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, CLKEN = GND, 8B/10B data coding, C_F = 0.047µF, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current (Note 1)	CDREN = GND	MAX3754		245	285	mA
		MAX3755		285	334	
	CDREN = V_{CC}	MAX3754		308	362	
		MAX3755		349	411	
Input Data Rate Range	1.0625Gbps operation, RATESEL = GND		-100		+100	ppm
	2.125Gbps operation, RATESEL = V_{CC}		-100		+100	
Differential Input Voltage Swing			200		2200	mV_{P-P}
Input Common-Mode Voltage				V_{CC} - 0.45		V
Differential Output Voltage Swing	R_{LOAD} = R_{SOURCE}		1000	1400	1800	mV_{P-P}
Differential L-Port Input Resistance		MAX3754	118	150	182	Ω
		MAX3755	78	100	122	
Differential L-Port Output Resistance		MAX3754	118	150	182	Ω
		MAX3755	78	100	122	
Differential Input Resistance at IN±			78	100	122	Ω
Differential Output Resistance at OUT±			78	100	122	Ω
TTL Low Input Voltage					0.8	V
TTL High Input Voltage			2			V
TTL Input Current	0 ≤ TTL input voltages ≤ V_{CC}		-50		50	µA
LOCK Output Low Voltage	I_{OL} = +1mA (sinking)				0.4	V
LOCK Output High Voltage	I_{OH} = -100µA (sourcing)		2.4			V
Differential Voltage across CF±					V_{CC}	V
Data Propagation Delay	IN± to OUT±, SEL_ = GND, CDREN = V_{CC}				3	ns
	LIN(n)± to LOUT(n+1)±, LIN4± to OUT±				1	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, CLKEN = GND, 8B/10B data coding, C_F = 0.047µF, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Channel Select Delay to Data Valid	SEL(n)± to LOUT(n+1)± , SEL4 to OUT±			9		ns
Data Transition Time	20% to 80%		65	110	160	ps
Supply Noise Tolerance (Note 2)	10Hz ≤ f < 100Hz			100		mV_{P-P}
	100Hz ≤ f < 1MHz			40		
	1MHz ≤ f < 2.5GHz			10		
CDR Lock Time				530		µs
OPERATION AT 2.125Gbps (Note 3)						
Random Jitter at OUT±, L-Port Outputs±	Pattern = K28.7, CDREN = GND (Note 4)			1.6		ps_{RMS}
	Pattern = K28.7, CDREN = V_{CC}			4.1		
	Pattern = CRPAT, CDREN = V_{CC} (Notes 5, 6)			3		
Deterministic Jitter at OUT±, L-Port Outputs±	Pattern = K28.5±, CDREN = GND (Note 7)			29	60	ps_{P-P}
	Pattern = K28.5±, CDREN = V_{CC}			19	50	
	Pattern = RPAT, CDREN = V_{CC} (Notes 6, 8, 9)			28	50	
Total Jitter at OUT±, LOUT_±	Pattern = RPAT, CDREN = V_{CC} (Notes 6, 8, 9)				105	ps_{P-P}
Sinusoidal Component of Jitter Tolerance (BER = 10^{-12})	Pattern = CJTPAT (Notes 6, 10)	f = 85kHz sine wave	1.5			UI
		f = 1.27MHz sine wave	0.1			
		f = 10MHz sine wave	0.1			
Deterministic Jitter Tolerance	CJTPAT (Note 10)		0.4			UI
Total High-Frequency Jitter Tolerance	Pattern = CJTPAT (Notes 6, 10, 11)		0.7			UI
Jitter Transfer Bandwidth				6	10	MHz
Jitter Transfer Peaking	(Note 12)				0.05	dB
OPERATION AT 1.0625Gbps (Note 3)						
Random Jitter at OUT±, L-Port Outputs±	Pattern = K28.7, CDREN = GND (Note 4)			1.7		ps_{RMS}
	Pattern = K28.7, CDREN = V_{CC}			5.4		
	Pattern = CRPAT, CDREN = V_{CC} (Notes 5, 6)			3.8		
Deterministic Jitter at OUT±, L-Port Outputs±	Pattern = K28.5±, CDREN = GND (Note 7)			27	60	ps_{P-P}
	Pattern = K28.5±, CDREN = V_{CC}			19	50	
	Pattern = RPAT, CDREN = V_{CC} (Notes 6, 8, 9)			37	75	
Total Jitter at OUT±, LOUT_±	Pattern = RPAT, CDREN = V_{CC} (Notes 6, 8, 9)				135	ps_{P-P}
Sinusoidal Component of Jitter Tolerance (BER = 10^{-12})	Pattern = CJTPAT (Notes 6, 10)	f = 42.5kHz sine wave	1.5			UI
		f = 635kHz sine wave	0.1			
		f = 5MHz sine wave	0.1			

Dual-Rate, 1Gbps/2Gbps Fibre Channel Quad-Port Bypass ICs with Repeater

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, CLKEN = GND, 8B/10B data coding, C_F = 0.047µF, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Deterministic Jitter Tolerance	CJTPAT (Note 10)	0.4			UI
Total High-Frequency Jitter Tolerance	Pattern = CJTPAT (Notes 6, 10, 11)	0.7			UI
Jitter Transfer Bandwidth			3	5	MHz
Jitter Transfer Peaking	(Note 12)			0.05	dB

Note 1: Includes output currents.

Note 2: Meets jitter output specifications with noise applied.

Note 3: AC characteristics are guaranteed by design and characterization.

Note 4: K28.7 Pattern: 00 1111 1000

Note 5: Compliant Random Pattern in hex (CRPAT):

Pattern Sequence:	Repetitions:
3E AA 2A AA AA	6
3E AA A6 A5 A9	1
86 BA 6C64 75 D0 E8 DC A8 B4 79 49 EA A6 65	16
72 31 9A 95 AB	1
C1 6A AA 9A A6	1

Note 6: Parameter measured with 0.40UI deterministic and 0.20UI random jitter (BER = 10^{-12}) applied to the input. All ports are bypassed, SEL_ = TTL low. Jitter is in compliance with the inter-enclosure, Fibre Channel jitter tolerance (at compliance point α_R) and jitter output (at compliance point α_T) specifications (FC-PI rev 10.0). Output jitter is specified as an output total given a non-zero jitter input.

Note 7: K28.5± Pattern: 00 1111 1010 11 0000 0101

Note 8: Random Pattern in Hex (RPAT): 3EB0 5C67 85D3 172C A856 D84B B6A6 65

Note 9: Using differential drive over the entire input amplitude range. The input signal bandwidth is limited to 0.75 × (bit-rate) by a 4th-order Bessel-Thompson filter or equivalent. Total jitter (TJ) is the range of the eye pattern where the bit error rate exceeds 10^{-12}. TJ can be estimated as TJ = DJ + (14 × RJ). DJ is deterministic jitter. RJ is one sigma distribution (RMS) of random jitter.

Note 10: Compliant Jitter Tolerance Pattern in Hex (CJTPAT):

Pattern Sequence:	Repetitions:
3E AA 2A AA AA	6
3E AA A6 A5 A9	1
87 1E 38 71 E3	41
87 1E 38 70 BC 78 F4 AA AA AA	1
AA AA AA AA AA	12
AA A1 55 55 E3 87 1E 38 71 E1	1
AB 9C 96 86 E6	1
C1 6A AA 9A A6	1

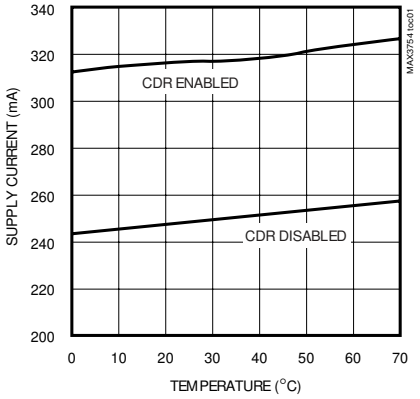
Note 11: Parameter measured with 0.1UI sinusoidal jitter at 10MHz for 2.125Gbps data rate, or 5MHz for 1.0625Gbps.

Note 12: Simulation shows peaking of 0.01dBm max. Characterization results limited by test equipment.

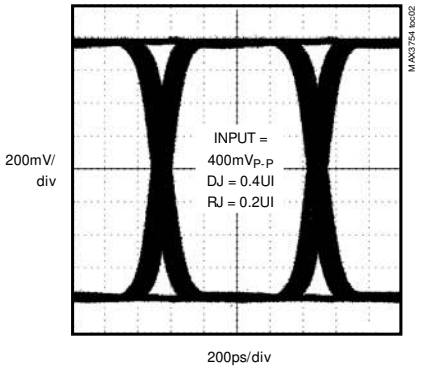
Typical Operating Characteristics

(V_{CC} = +3.3V, C_F = 0.047µF, T_A = +25°C, unless otherwise noted.)

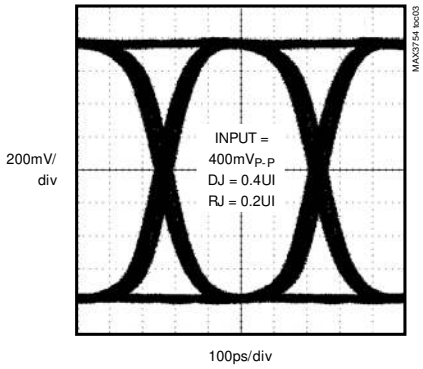
SUPPLY CURRENT vs. TEMPERTURE (MAX3754)



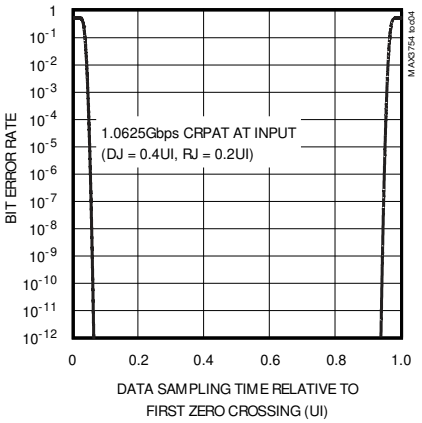
OUTPUT EYE DIAGRAM AT OUT± (1.0625Gbps CRPAT, CDR ENABLED)



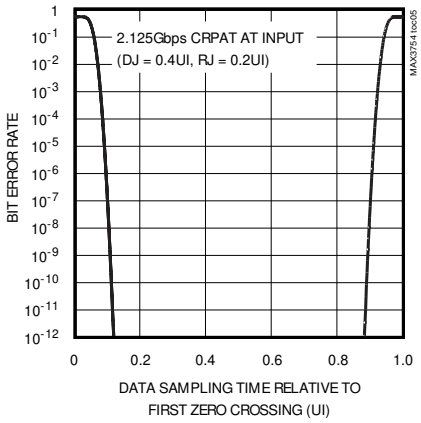
OUTPUT EYE DIAGRAM AT OUT± (2.125Gbps CRPAT, CDR ENABLED)



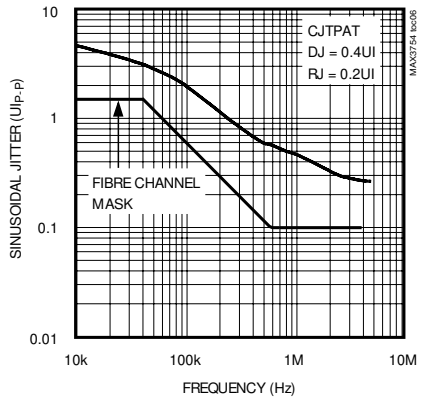
OUTPUT JITTER BATHTUB PLOT (1.0625Gbps)



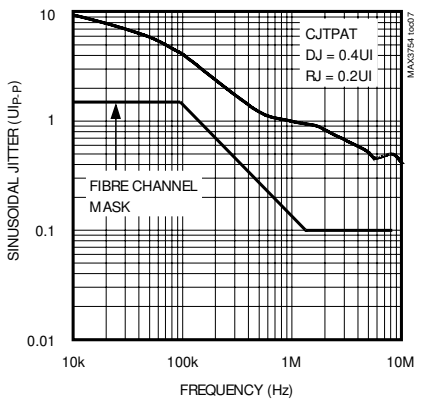
OUTPUT JITTER BATHTUB PLOT (2.125Gbps)



JITTER TOLERANCE 1.0625Gbps



JITTER TOLERANCE 2.125Gbps



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Pin Description

PIN	NAME	DESCRIPTION
1, 4, 7, 8, 11, 26, 29, 30, 33, 36, 39, 42, 43, 46	GND	Electrical Ground
2	LIN1-	Inverted Data Input for L-Port 1
3	LIN1+	Noninverted Data Input for L-Port 1
5	LOUT1-	Inverted Data Output for L-Port 1
6	LOUT1+	Noninverted Data Output for L-Port 1
9	IN-	Inverted Data Input
10	IN+	Noninverted Data Input
12	CLKEN	Clock Enable. A TTL high level enables clock output at L-Port 1.
13, 16, 21, 24	V_{CC}	Supply Voltage
14	CF+	CDR Filter Capacitor Positive Connection. C_F = 0.047µF.
15	CF-	CDR Filter Capacitor Negative Connection. C_F = 0.047µF.
17	SEL1	Select 1. A TTL low on SEL1 selects data from IN. TTL high on SEL1 selects data from LIN1.
18	SEL2	Select 2. A TTL low on SEL2 selects data from the previous port bypass circuit. A TTL high on SEL2 selects data from LIN2.
19	SEL3	Select 3. A TTL low on SEL3 selects data from the previous port bypass circuit. A TTL high on SEL3 selects data from LIN3.
20	SEL4	Select 4. A TTL low on SEL4 selects data from the previous port bypass circuit. A TTL high on SEL4 selects data from LIN4.
22	CDREN	CDR Enable Input (TTL). A high input enables the CDR for data recovery. A low input disables the CDR (no data recovery).
23	RATESEL	Rate Select Pin. TTL low selects 1.0625Gbps operation. TTL high selects 2.125Gbps operation.
25	LOCK	Frequency Lock Indicator. When data is present, a high level indicates the PLL is frequency-locked. The output of the LOCK pin may chatter when large jitter is applied to the input.
27	OUT+	Noninverted Data Output
28	OUT-	Inverted Data Output
31	LIN4-	Inverted Data Input for L-Port 4
32	LIN4+	Noninverted Data Input for L-Port 4
34	LOUT4-	Inverted Data Output for L-Port 4
35	LOUT4+	Noninverted Data Output for L-Port 4
37	LIN3-	Inverted Data Input for L-Port 3
38	LIN3+	Noninverted Data Input for L-Port 3
40	LOUT3-	Inverted Data Output for L-Port 3
41	LOUT3+	Noninverted Data Output for L-Port 3
44	LIN2-	Inverted Data Input for L-Port 2
45	LIN2+	Noninverted Data Input for L-Port 2
47	LOUT2-	Inverted Data Output for L-Port 2
48	LOUT2+	Noninverted Data Output for L-Port 2
EP	Exposed Pad	The exposed pad must be soldered to the circuit board ground for proper thermal performance.

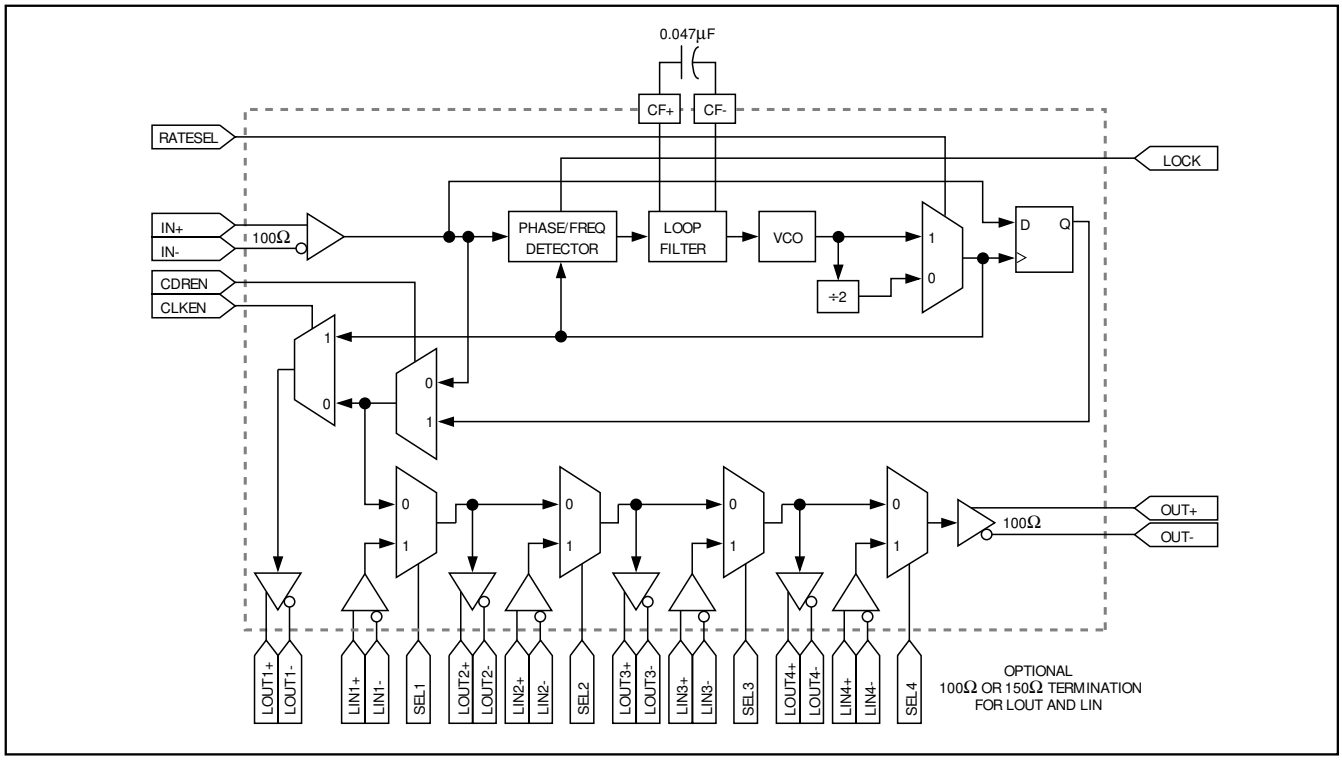

Figure 1. MAX3754/MAX3755 Functional Diagram

Detailed Description

The MAX3754/MAX3755 quad port bypass circuits (PBCs) consist of an input buffer, a rate-selectable clock and data recovery (CDR) circuit (for optional jitter attenuation), four serially connected port bypass circuits, and an output buffer (Figure 1). The circuit design is optimized for both 1.0625Gbps and 2.125Gbps operation at 3.3V.

Input Buffer

The input buffer provides line termination and level conversion. It accepts a differential input voltage of 200mV to 2200mV at IN±. Internal resistors terminate the inputs to 100Ω differentially eliminating the need for external resistors.

Clock and Data Recovery

The purpose of the CDR is to improve jitter transfer performance by attenuating jitter that may be present in the input data. The CDR can recover 1.0625Gpbs or 2.125Gbps data signals that are corrupted by up to 0.7UI of high-frequency jitter (BER = 10^{-12}). When jitter attenuation is not needed, the CDR may be disabled in order to save power.

The input buffer drives the CDR circuit, as well as one input of a 2:1 multiplexer. A TTL high on CDREN enables the CDR and connects the CDR data output to the port bypass circuits. The recovered clock signal is available for test purposes at LOUT1 when CLKEN is asserted high. A TTL low on CDREN disables the CDR and connects the output of the input buffer directly to the port bypass circuits. A RATESEL pin is included to switch the CDR between data rates. The VCO output has a divide-by-2 block that is switched into the PLL when RATESEL is TTL low for 1.0625Gbps operation (see Figure 1).

Phase and Frequency Detector

The frequency difference between the VCO clock and the received data is derived by sampling the in-phase and quadrature VCO outputs on the edges of the input data signal. The frequency detector drives the VCO until the frequency difference is reduced to zero. Once frequency acquisition is complete, the phase detector produces a voltage proportional to the phase difference between the incoming data and the internal clock. The PLL drives this error voltage to zero, aligning the recovered clock to the center of the incoming eye.

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Loop Filter, VCO, and Latch

The phase detector and frequency detector outputs are summed into a loop filter. An external capacitor (between CF+ and CF-) is required to set the PLL damping factor. The fully integrated VCO contains an internal current reference and filter circuitry to minimize the influence of V_{CC} noise. The VCO creates a clock output with frequency proportional to the control voltage applied by the loop filter. Data recovery is accomplished by using the recovered clock signal to latch the incoming data to the CML output buffers, significantly reducing output jitter.

LOCK Output

An active high LOCK output monitor derived from the frequency detector indicates that the PLL is frequency locked onto the input data. Without input data, the LOCK signal may settle at TTL High or TTL Low. The use of a low-pass RC filter is recommended to reduce the effects of chatter that could be caused by a high input jitter content.

RATESEL Input

The RATESEL input is used to select between input data rates of 2.125Gbps and 1.0625Gbps. This function allows the repeater to sample data at the correct data rate by selecting an optional a divide-by-2 network. RATESEL selects between the VCO tuned frequency and half that frequency, allowing maximum jitter tolerance at both data rates. The loop bandwidth of the repeater scales with the selected frequency; i.e., the loop-bandwidth at an input rate of 1.0625Gbps is half that at the input rate of 2.125Gbps.

Port Bypass Circuits

The output of the 2:1 input multiplexer drives a cascaded series of four PBCs. Each PBC consists of a differential output buffer, a differential input buffer, and a 2:1 multiplexer. The multiplexer select input (SEL_) controls whether a port is included in the loop. A TTL low on a multiplexer select pin routes the data signal from the previous stage to the multiplexer output (port bypass mode). A TTL high on the multiplexer select pin routes the data signal from the input buffer to the multiplexer output (port enable mode). The output of the last PBC drives the output buffer.

The MAX3754 has 150Ω differential termination on the inputs and 75Ω single-ended terminations to V_{CC} on the outputs (see *Input/Output Structures* for specifics) of the L-ports to match Fibre Channel Arbitrated Loop specifications. The MAX3755 is terminated with 100Ω and 50Ω, respectively. Testing a MAX3754 using standard 50Ω test equipment requires an impedance matching network

Output Buffer

The output signal of the last PBC drives the differential high-power output buffer. The output buffer drives the output port (OUT±). Internal resistors terminate each output with 50Ω to V_{CC} (100Ω differentially), eliminating the need for external termination resistors. The output buffer produces a differential peak-to-peak output voltage of 1V to 1.8V when driving a differential load.

Applications Information

The MAX3754/MAX3755 quad-PBC is designed for hard-disk array applications using the Fibre Channel Arbitrated Loop network protocol. In applications where data storage reliability is critical, it may be desirable to create a disk array where the data is stored redundantly on more than one physical drive.

The Fibre Channel Arbitrated Loop protocol enables multiple physical drives to be connected in a loop topology. Each physical drive is connected to the Fibre Channel loop through an L-port that may be individually addressed and controlled to create an array of logical drives. Data is transmitted over the loop as an encoded serial bit stream. Using the Fibre Channel Arbitrated Loop protocol, the configuration of the disk array can be rearranged under software control to achieve desired objectives (such as data reliability or fast access).

The port bypass circuit allows any L-port to be enabled (connected to the loop) or bypassed (disconnected from the loop) while the loop is operating. This enables hot swapping of physical drives (inserting or removing physical drives while the loop is operating) so that drives may be replaced with minimal disruption to the disk array system. Figure 2 shows a disk array.

Filter Capacitor Requirements

The MAX3754/MAX3755 phase lock loop's (PLL) filter capacitor is required to be supplied in a port bypass design. This capacitor sets the damping factor of the device. It also determines how fast the PLL can acquire initial lock. This device is specified and tested with the recommended filter capacitor value of 0.047µF that limits transfer peaking.

Input/Output Structures

Figures 3 and 4 show models for the MAX3754/MAX3755 inputs and outputs, modeling package parasitics, and ESD diodes.

Cascading Port Bypass Circuits

Two or more MAX3754/MAX3755 quad-PBCs can be cascaded by directly connecting the OUT± pins of one quad-PBC to the IN± pins of the next quad-PBC. See

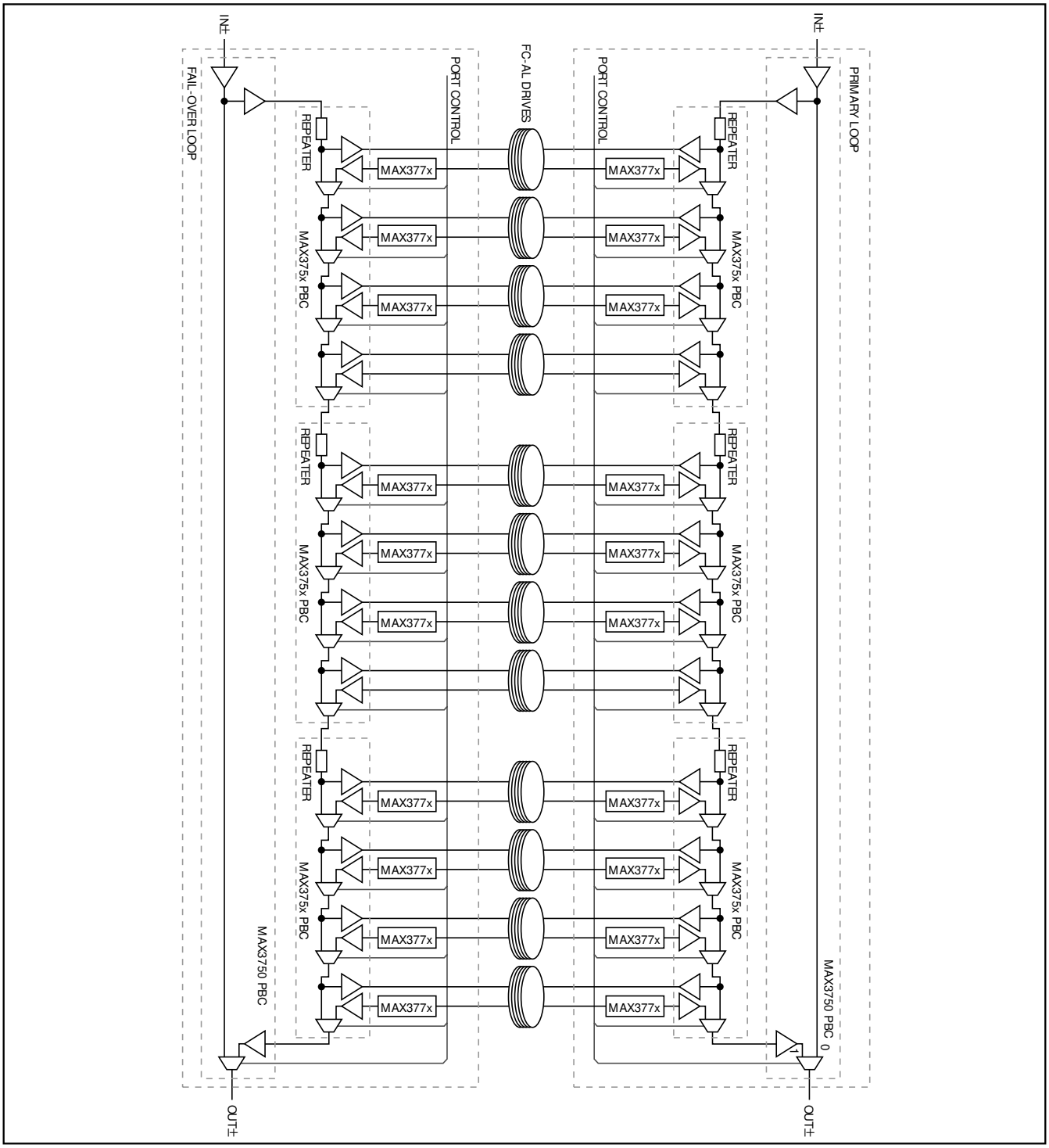


Figure 2. Disk Array Implemented with Port Bypass Circuits

Dual-Rate, 1Gbps/2Gbps Fibre Channel Quad-Port Bypass ICs with Repeater

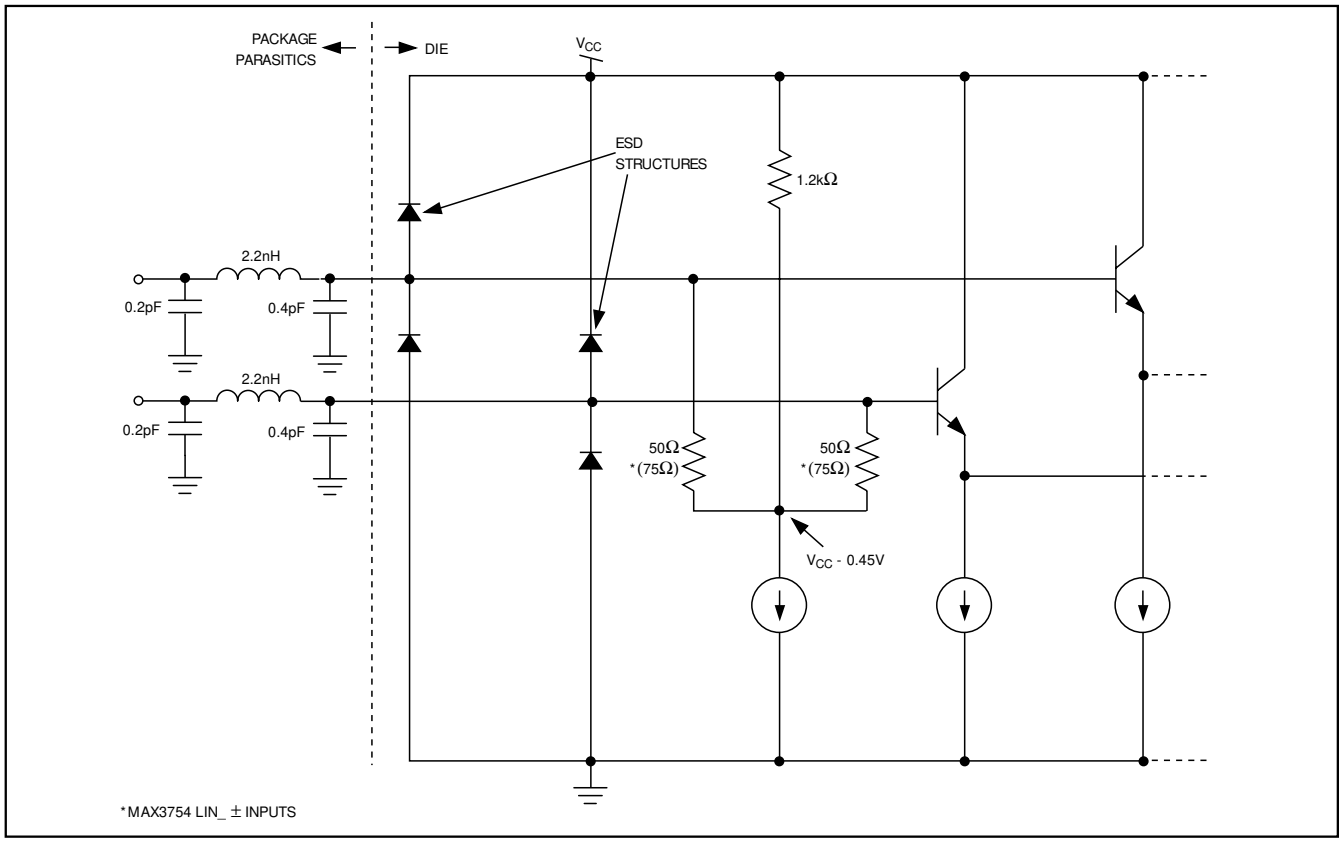


Figure 3. MAX3754/MAX3755 Input Structure

quad-PBC to the IN± pins of the next quad-PBC. See *Typical Operating Circuit*.

Layout Considerations

For best performance, carefully lay out the PC board using high-frequency techniques. Filter voltage supplies, keep ground connections short with multiple vias where possible. Use controlled impedance transmission lines to interface with the MAX3754/MAX3755 high-speed inputs and outputs. Power-supply decoupling capacitors should be placed very close to V_{CC} pins. Isolate the input signals from the output signals as much as possible.

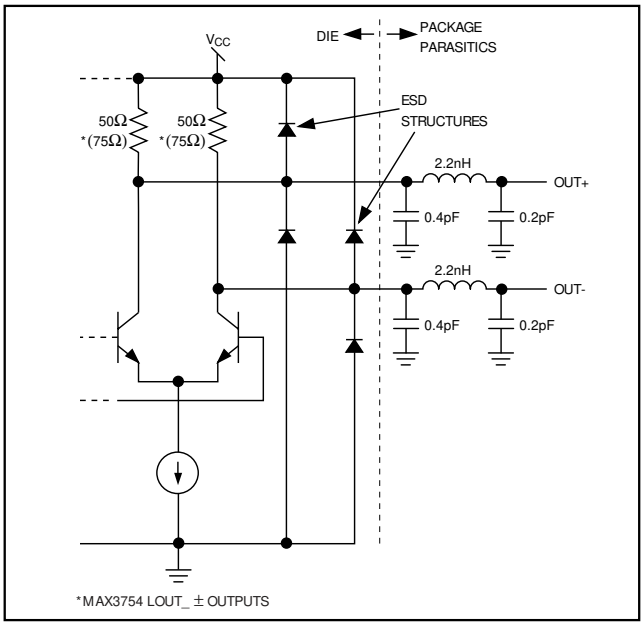
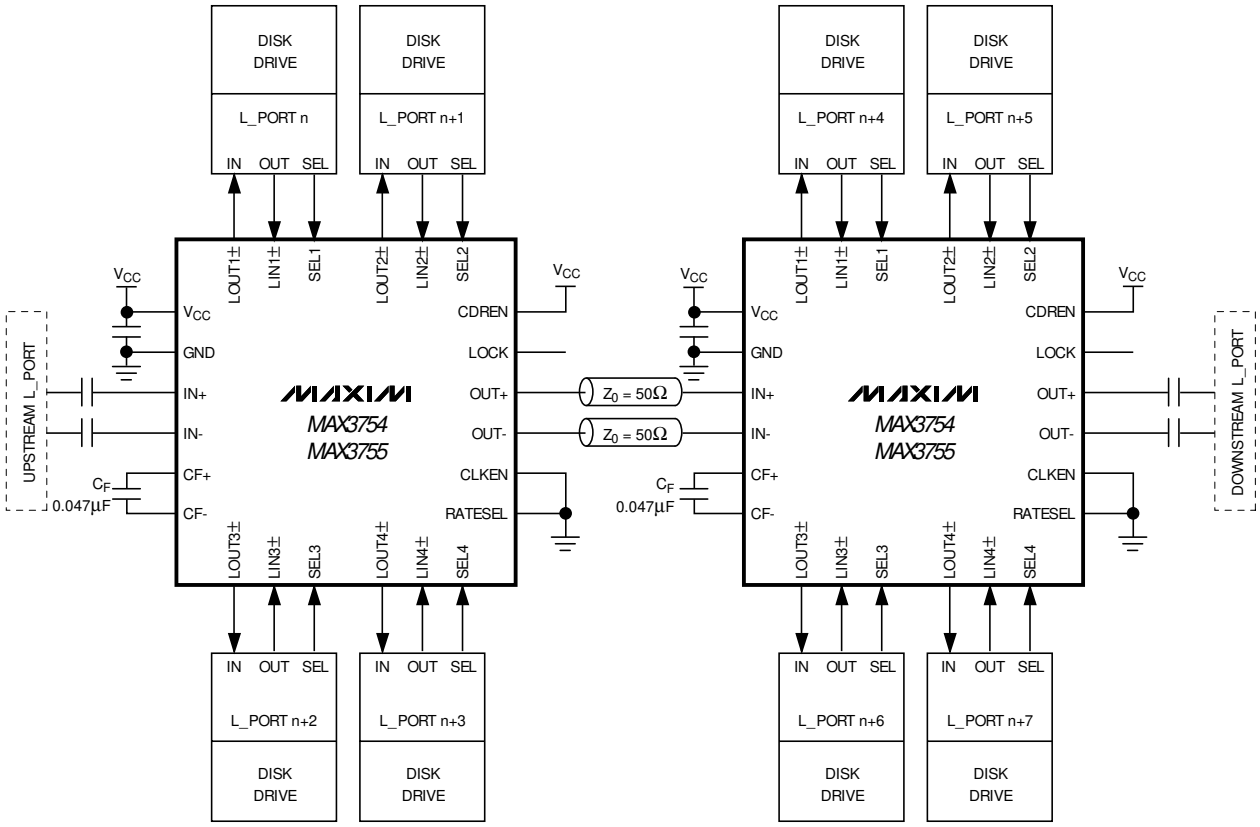


Figure 4. MAX3754/MAX3755 Output Structure

Typical Operating Circuit



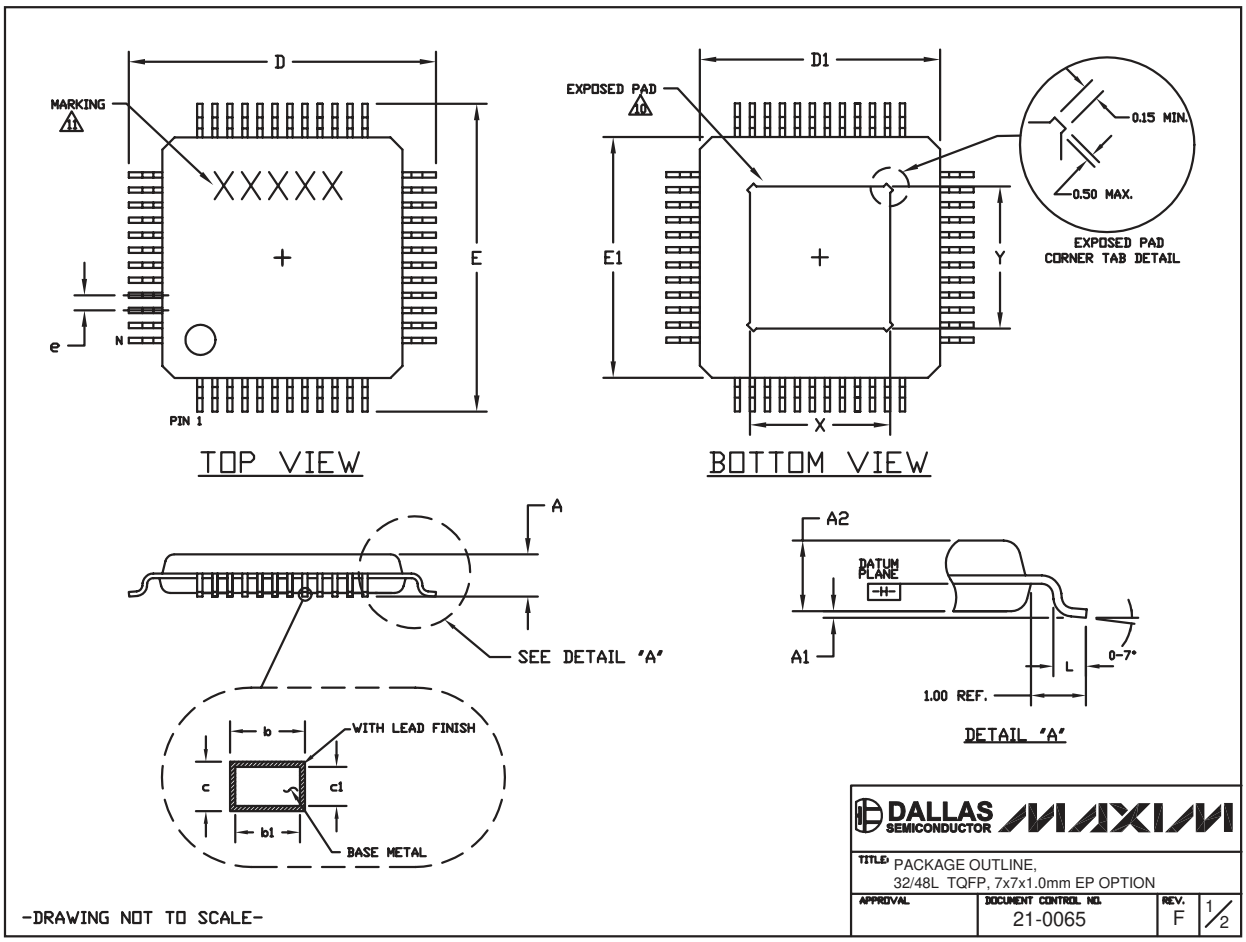
NOTE: ALL HIGH-SPEED INPUTS AND OUTPUTS (IN±, OUT±, LIN±, AND LOUT±) SHOULD BE CONNECTED USING CONTROLLED-IMPEDANCE TRANSMISSION LINES. AC-COUPLING MAY ALSO BE REQUIRED. ALL CAPACITORS ARE 0.1µF UNLESS OTHERWISE INDICATED. FIGURE SHOWS 1.0625Gbps OPERATION. FOR 2.125Gbps OPERATION, CONNECT RATESEL TO V_{CC}.

Dual-Rate, 1Gbps/2Gbps Fibre Channel Quad-Port Bypass ICs with Repeater

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

48L, TQFP.EPS



Dual-Rate, 1Gbps/2Gbps Fibre Channel Quad-Port Bypass ICs with Repeater

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:
1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE [-H-] IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026, VARIATIONS ABA-HD AND ABC-HD.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X & Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS					
	ABA-HD			ABC-HD		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	~~	~~	1.20	~~	~~	1.20
A_1	0.05	0.10	0.15	0.05	0.10	0.15
A_2	0.95	1.00	1.05	0.95	1.00	1.05
D	8.90	9.00	9.10	8.90	9.00	9.10
D_1	6.90	7.00	7.10	6.90	7.00	7.10
E	8.90	9.00	9.10	8.90	9.00	9.10
E_1	6.90	7.00	7.10	6.90	7.00	7.10
L	0.45	0.60	0.75	0.45	0.60	0.75
N	32			48		
e	0.80 BSC.			0.50 BSC.		
b	0.30	0.37	0.45	0.17	0.22	0.27
b1	0.30	0.35	0.40	0.17	0.20	0.23
c	0.09	--	0.20	0.09	--	0.20
c1	0.09	--	0.16	0.09	--	0.16
X	3.20	3.50	3.80	3.70	4.00	4.30
Y	3.20	3.50	3.80	3.70	4.00	4.30

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 32/48L TQFP, 7x7x1.0mm EP OPTION

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