BLC9H10XS-60P

Power LDMOS transistor

Rev. 2 — 29 May 2018

AMPLEON

Product data sheet

1. Product profile

1.1 General description

60 W LDMOS packaged symmetric power transistor for base station applications at frequencies from 400 MHz to 1000 MHz.

Table 1. Typical performance 940 MHz

Typical RF performance at T_{case} = 25 °C in a class-AB demo circuit. V_{DS} = 50 V; I_{Dq} = 115 mA (per section).

Test signal	f	V_{DS}	P_L	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	925 to 960	50	35	16.5	13	–47 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01% probability on CCDF.

Table 2. Typical performance 859 MHz

Typical RF performance at T_{case} = 25 °C in a class-AB demo circuit. V_{DS} = 48 V; I_{Dq} = 125 mA (per section).

Test signal	f	V_{DS}	P_L	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	785 to 960	48	35	16.1	11.9	–46.6 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01% probability on CCDF.

1.2 Features and benefits

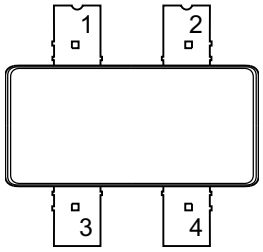
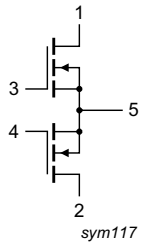
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (400 MHz to 1000 MHz)
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

RF power amplifiers for base stations and multi carrier applications in the 400 MHz to 1000 MHz frequency range

2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
BLC9H10XS-60P	-	air cavity plastic earless flanged package; 4 leads	SOT1273-1

4. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	105	V
V_{GS}	gate-source voltage		–6	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature	operating [1]	–40	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 50 V; I_{Dq} = 115 mA (per section); T_{case} = 80 °C; P_L = 3.16 W	0.8	K/W

6. Characteristics

Table 7. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.22 mA	105	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 22 mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 110 mA	-	2.2	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	3.6	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 1.1 A	-	1.5	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 0.77 A	-	1070	1328	mΩ

Table 8. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 929.5 MHz; f_2 = 954.5 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 110 mA; T_{case} = 25 °C; unless otherwise specified; in a class AB production test circuit at frequencies from 927 MHz to 957 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 3.2 W	15.3	16.3	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 3.2 W	-	–24	–17	dB
η_D	drain efficiency	$P_{L(AV)}$ = 3.2 W	11.5	12.5	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 3.2 W	-	–49	–44	dBc

Table 9. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f = 929.5 MHz; RF performance at V_{DS} = 50V; I_{Dq} = 110 mA; T_{case} = 25 °C; unless otherwise specified; in a class AB production test circuit at frequencies from 927 MHz to 957 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_O	output peak-to-average ratio	$P_{L(AV)}$ = 17.4 W	6.1	6.8	-	dB
$P_{L(M)}$	peak output power	$P_{L(AV)}$ = 17.4 W	70	102	-	W

7. Test information

7.1 Ruggedness in class-AB operation

The BLC9H10XS-60P is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:

- V_{DS} = 52 V; I_{Dq} = 115 mA (per section); f = 925 MHz; P_L = 19 W; 1T-W-CDMA
- V_{DS} = 52 V; I_{Dq} = 115 mA (per section); f = 925 MHz; P_L = 60 W; pulsed CW (t_p = 100 μs; δ = 10 %)

7.2 Impedance information

Table 10. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 110 mA (per section); V_{DS} = 50 V; pulsed CW (t_p = 100 µs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
600	4.81 + j13.6	21.86 – j0.92	55.1	62.9	16.8
698	4.97 + j11.1	13.94 + j3.05	46.8	55.7	15.3
720	4.93 + j10.6	14.52 + j5.94	49.2	62.9	15.9
746	4.93 + j10.1	13.04 + j7.01	49.3	64.3	15.8
757	4.97 + j9.96	10.67 + j6.38	50.9	62.0	15.2
769	4.98 + j9.75	11.88 + j5.04	52.0	61.6	15.0
790	4.95 + j9.32	16.62 + j4.46	51.8	63.4	15.1
800	4.96 + j9.11	16.68 + j4.43	51.5	63.1	14.9
820	4.86 + j8.73	15.09 + j5.39	49.7	62.7	14.9
869	4.83 + j7.86	15.02 + j4.25	48.0	58.8	14.0
880	4.76 + j7.64	17.58 + j5.87	47.8	60.5	14.3
894	4.76 + j7.41	15.40 + j4.05	46.6	57.2	13.8
925	4.64 + j6.90	14.04 + j6.92	45.5	60.2	14.1
942	4.59 + j6.55	14.94 + j6.98	45.4	59.8	13.9
960	4.55 + j6.23	11.33 + j6.56	45.8	59.7	13.6
1000	4.46 + j5.57	11.26 + j6.49	46.6	60.8	13.3
Maximum drain efficiency load					
600	4.78 + j13.50	25.42 + j5.49	51.0	68.5	17.9
698	4.89 + j10.98	21.35 + j17.90	34.0	66.5	17.9
720	4.85 + j10.57	17.70 + j13.04	39.6	67.5	17.2
746	4.80 + j10.02	14.55 + j15.59	34.5	68.6	17.6
757	4.78 + j9.79	12.05 + j15.07	34.6	70.0	17.5
769	4.74 + j9.57	12.02 + j15.05	35.0	70.5	17.6
800	4.72 + j9.14	11.18 + j14.21	35.9	71.4	17.2
805	4.71 + j8.92	11.20 + j14.23	35.3	71.0	17.1
820	4.64 + j8.56	11.08 + j14.07	34.3	68.5	17.0
869	4.52 + j7.57	7.82 + j16.59	24.0	68.2	17.5
880	4.51 + j7.45	8.69 + j13.51	33.1	68.1	16.5
894	4.47 + j7.17	8.51 + j14.09	31.4	68.0	16.6
925	4.41 + j6.71	8.50 + j14.03	32.6	69.0	16.4
942	4.36 + j6.34	8.44 + j14.04	32.3	68.5	16.2
960	4.27 + j6.01	7.19 + j13.36	31.9	69.4	16.2
1000	4.17 + j5.32	7.17 + j13.26	31.7	69.9	16.1

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

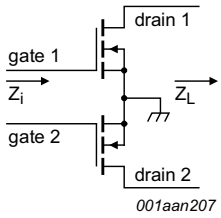
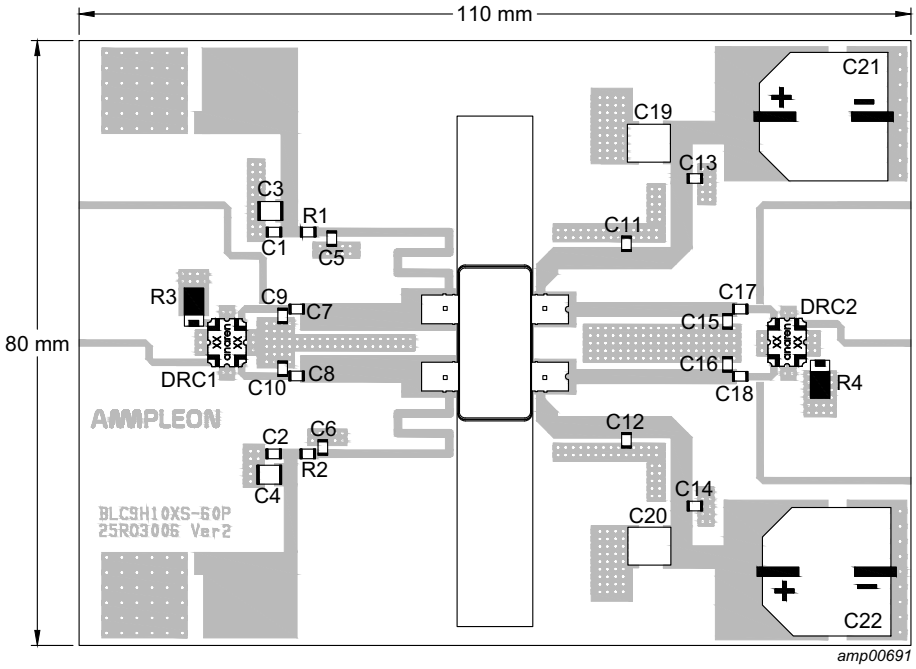


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): RO3006: ε_r = 6.15; thickness = 0.635 mm; thickness copper plating = 35 μm. See Table 11 for a list of components.

Fig 2. Component layout

Table 11. List of components

See Figure 2 for component layout.

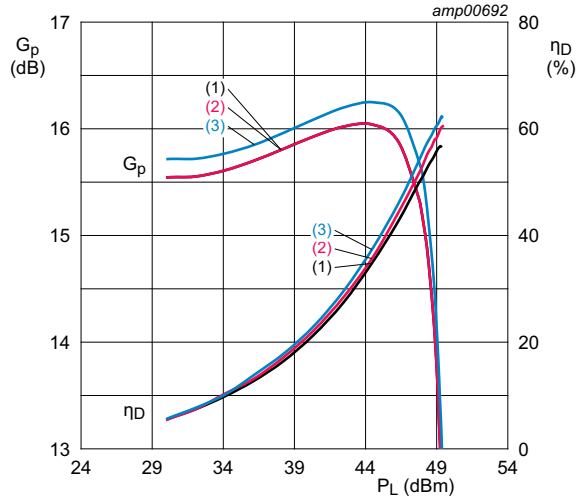
Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	10 nF, 50 V	Murata: Hi-Q SMD 0805
C3, C4	multilayer ceramic chip capacitor	4.7 μF, 50 V	Murata: Hi-Q SMD 1210
C5, C6, C7, C8, C13, C14, C17, C18	multilayer ceramic chip capacitor	82 pF, 250 V	Murata: Hi-Q SMD 0805
C9, C10	multilayer ceramic chip capacitor	9.1 pF, 250 V	Murata: Hi-Q SMD 0805
C11, C12	multilayer ceramic chip capacitor	2 pF, 250 V	Murata: Hi-Q SMD 0805
C15, C16	multilayer ceramic chip capacitor	4.3 pF, 250 V	Murata: Hi-Q SMD 0805
C19, C20	multilayer ceramic chip capacitor	4.7 μF, 100V	Murata: Hi-Q SMD 2220

Table 11. List of components *...continued*
See Figure 2 for component layout.

Component	Description	Value	Remarks
C21, C22	electrolytic capacitor	470 μF, 100 V	Panasonic: FK series
R1, R2	resistor	5.6 Ω, 1/6 W	SMD 0805
R3, R4	resistor	50 Ω, 16 W	Anaren: C16A50Z4
DRC1, DRC2	hybrid coupler	3 dB, 90°	Anaren: X3C09F1-03S

7.4 Graphical data

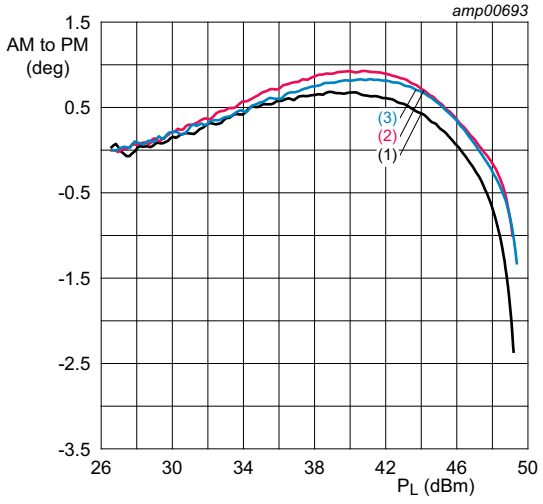
7.4.1 Pulsed CW



V_{DS} = 50 V; I_{Dq} = 115 mA; t_p = 100 μs; δ = 10 %.

(1) f = 925 MHz
(2) f = 942.5 MHz
(3) f = 960 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



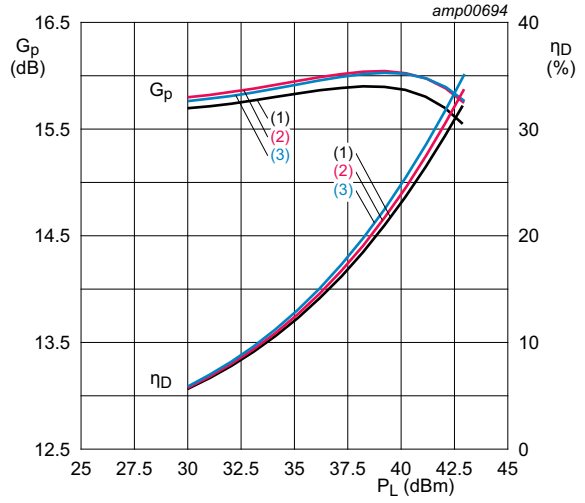
V_{DS} = 50 V; I_{Dq} = 115 mA.

(1) f = 925 MHz
(2) f = 942.5 MHz
(3) f = 960 MHz

Fig 4. Normalized AM to PM as a function of output power; typical values

7.4.2 1-Carrier W-CDMA

Test signal: 3GPP test model 1; 1 to 64 DPCH (100 % clipping): PAR = 9.9 dB per carrier at 0.01 % probability on CCDF per carrier.



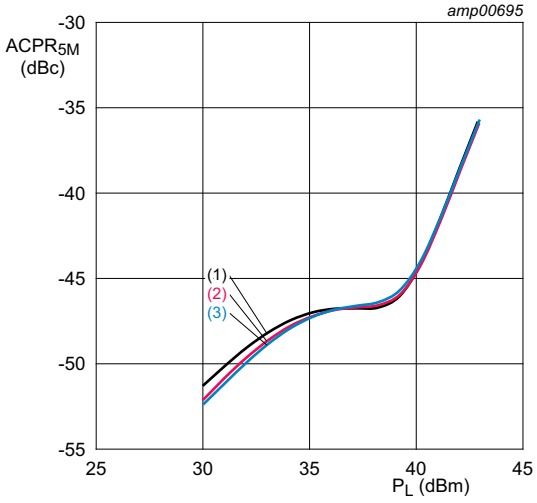
V_{DS} = 50 V; I_{Dq} = 115 mA.

(1) f = 925 MHz

(2) f = 942.5 MHz

(3) f = 960 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



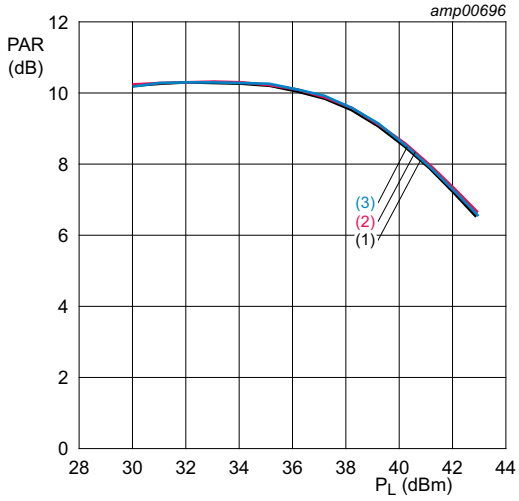
V_{DS} = 50 V; I_{Dq} = 115 mA.

(1) f = 925 MHz

(2) f = 942.5 MHz

(3) f = 960 MHz

Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 115 mA.

(1) f = 925 MHz

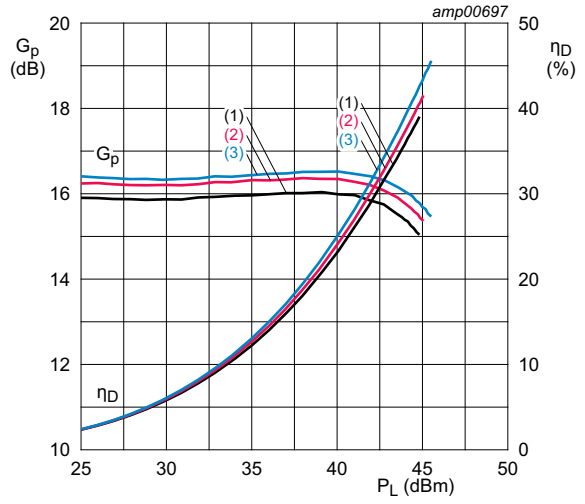
(2) f = 942.5 MHz

(3) f = 960 MHz

Fig 7. Peak-to-average power ratio as a function of output power; typical values

7.4.3 2-Carrier W-CDMA

Test signal: 3GPP test model 1; 1 to 64 DPCH (46 % clipping, 5 MHz spacing).



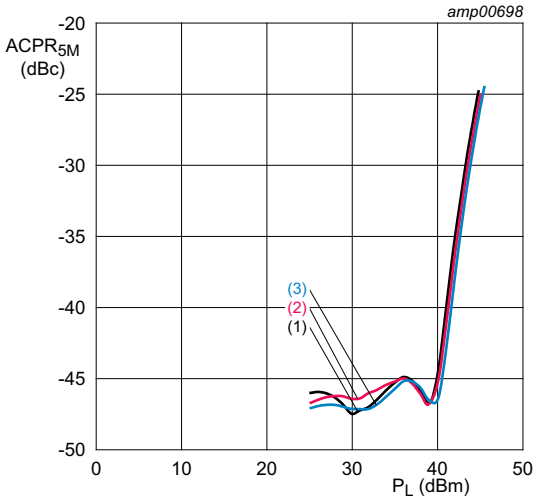
V_{DS} = 50 V; I_{Dq} = 115 mA.

(1) f = 925 MHz

(2) f = 942.5 MHz

(3) f = 960 MHz

Fig 8. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 115 mA.

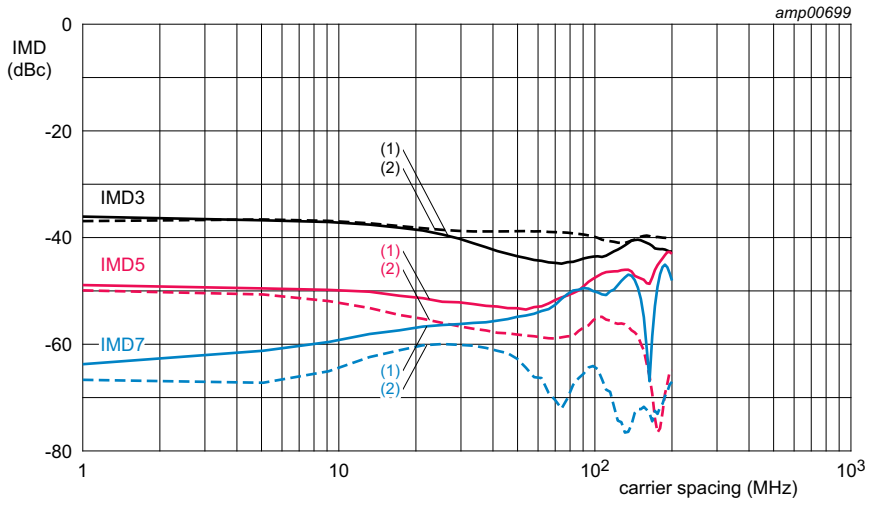
(1) f = 925 MHz

(2) f = 942.5 MHz

(3) f = 960 MHz

Fig 9. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

7.4.4 2-Tone VBW



V_{DS} = 50 V; I_{Dq} = 115 mA.

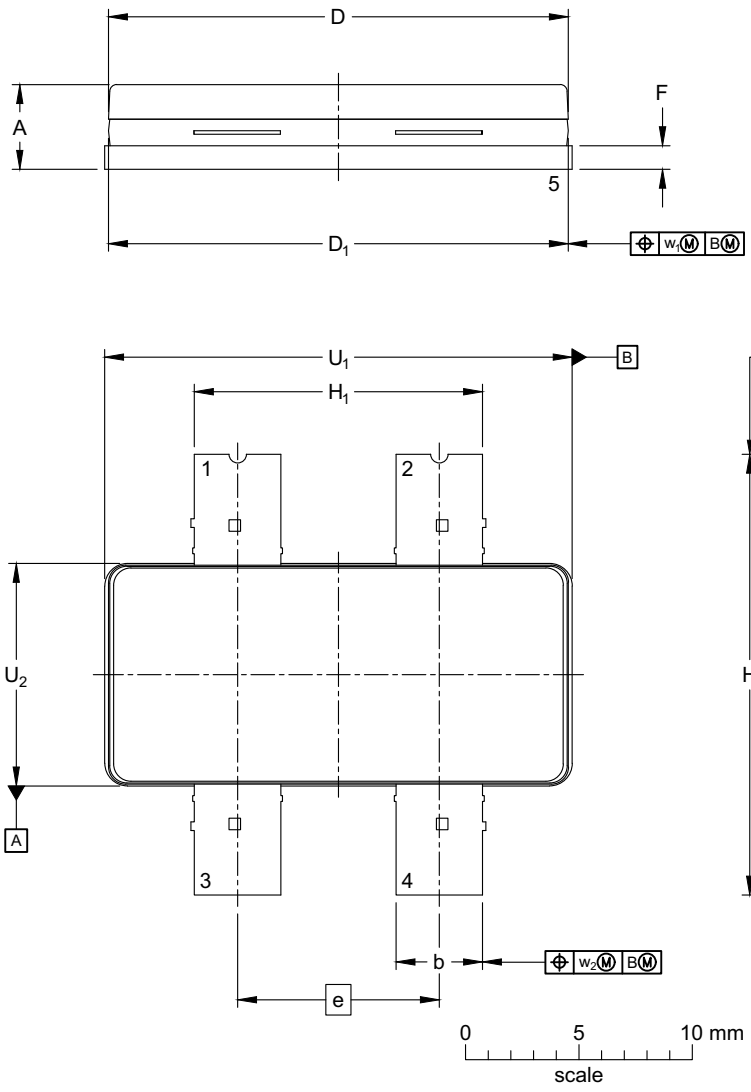
(1) IMD low

(2) IMD high

Fig 10. VBW capability

8. Package outline

Air cavity plastic earless flanged package; 4 leads SOT1273-1



Dimensions

Unit		A	b	c	D	D_1	E	E_1	e	F	H	H_1	$Q^{(1)}$	U_1	U_2	v	w_1	w_2	y
mm	max	4.01	3.91	0.18	20.42	20.37	9.80	9.75		1.14	19.53	12.83	1.68	20.70	9.91	0.50	0.50	0.50	0.10
	nom								8.89										
	min	3.40	3.71	0.13	20.12	20.17	9.50	9.55		0.94	19.33	12.57	1.45	20.50	9.70				

Note:
1. Dimension Q is measured at 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1273-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1273-1						17-01-12

Fig 11. Package outline SOT1273-1

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 12. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C3 is granted to any part that passes after exposure to an ESD pulse of ≥ 1000 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 13. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC9H10XS-60P v.2	20180529	Product data sheet	-	BLC9H10XS-60P v.1
Modifications	• Table 1 on page 1: updated table note • Table 2 on page 1: updated table • Section 7.1 on page 3: updated first list item • Section 7.4.2 on page 7: updated first paragraph • removed section 7.4.5. Group delay • Table 12 on page 10: updated table			
BLC9H10XS-60P v.1	20180501	Preliminary data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

12.2 Definitions

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13. Contact information

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