MPQ3428A

19A, 600kHz, 20V Wide Input Range, Synchronous Boost Converter with Input Disconnect Function, AEC-Q100 Qualified

DESCRIPTION

The MPQ3428A is an Automotive AECQ application device with 600kHz, fixed-frequency, high-efficiency, wide input range, current mode boost converter, optional input disconnect and an input average current limit function. The input disconnect feature provides additional protection by isolating the input from the output during output short or shutdown.

With a programmable input average current limit, the MPQ3428A supports a wide range of applications, including eCall, Smart latch, Telematics and infotainment. The MPQ3428A features a 18mΩ, 24V power switch and a synchronous gate driver for high efficiency. An external compensation pin allows flexibility in setting loop dynamics and obtaining optimal transient performance under all conditions.

The MPQ3428A includes under-voltage lockout, switching current limiting, and thermal shutdown to prevent damage in the event of an output overload. The MPQ3428A is available in a low-profile QFN-22 (3mmx4mm) package.

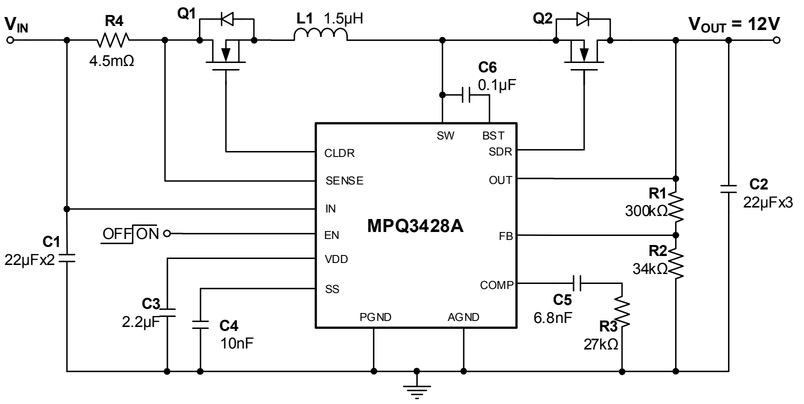
FEATURES

- Guaranteed Industrial/Automotive Temp
- 3V to 20V Wide Input Range
- Integrated 18mΩ Low-Side Power FET
- SDR Driver for Synchronous Solution
- 19A Internal Switch Current Limit or External Programmable Input Current Limit
- Input Disconnect and Output SCP
- External Soft Start and Compensation for Higher Flexibility
- Programmable UVLO and Hysteresis
- <1μA Shutdown Current
- Thermal Shutdown at 150°C
- Available in a QFN-22 (3mmx4mm) Package
- Available in AEC-Q100 Grade 1

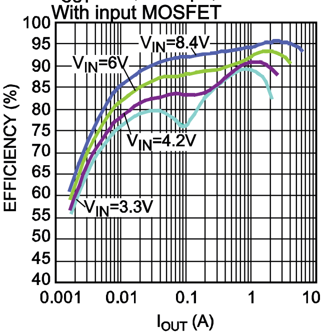
APPLICATIONS

- Industrial Automotive Applications
- eCall
- Smart latch
- Telematics
- Infotainment

TYPICAL APPLICATION



Efficiency vs. Output Current
V_{OUT}=12V, L=1.5μH,
With input MOSFET



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ3428AGL	QFN-22 (3mmx4mm)	*See Below*	1
MPQ3428AGL-AEC1			

* For Tape & Reel, add suffix –Z (e.g. MPQ3428AGL–Z).

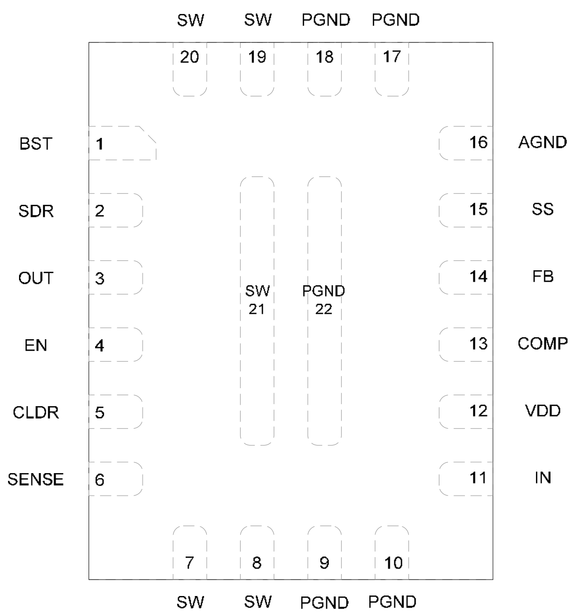
TOP MARKING

MPYW
3428
ALLL

MP: MPS prefix
Y: Year code
W: Week code
3428A: First five digits of the part number
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-22 (3mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	BST	**Bootstrap.** BST powers the SDR driver.
2	SDR	**Synchronous gate driver for the output rectifier.**
3	OUT	**Samples the output voltage and charges the BST capacitor.** VDD is powered from OUT when V_{OUT} exceeds V_{IN}.
4	EN	**Regulator on/off control input.** EN high turns on the internal regulator circuit. EN low turns off the regulator circuit. An input higher than the EN turn-on threshold enables the IC to start switching. If not used, connect EN to the input source (through a 100kΩ pull-up resistor if V_{IN} > 5.5V) for automatic start-up. EN can also program V_{IN} UVLO. Do not leave EN floating.
5	CLDR	**Driver for the input disconnect MOSFET.** If connected to the gate of the input MOSFET or floating, an external current-sense resistor is needed. Connect CLDR to GND to use the internal current-sense circuit. Do not pull CLDR down to GND through a resistor.
6	SENSE	**Voltage sense.** Voltage sensed between SENSE and IN determines the external current-sense signal. Connect SENSE to IN if the internal current-sense solution is selected.
7, 8, 19, 20, 21	SW	**Power switch output.** SW is the drain of the internal power MOSFET. Connect the power inductor and output rectifier to SW.
9, 10, 17, 18, 22	PGND	**Power ground.**
11	IN	**Input supply.** IN must be bypassed locally.
12	VDD	**Internal bias supply.** Decouple with a 2.2µF ceramic capacitor as close to VDD as possible.
13	COMP	**Compensation.** Connect a capacitor and resistor in series to analog ground for loop stability.
14	FB	**Feedback input.** The reference voltage is 1.225V. Connect a resistor divider from V_{OUT} to FB.
15	SS	**Soft-start control.** Connect a soft-start capacitor to SS. The soft-start capacitor is charged with a constant current. Leave SS disconnected if soft start is not used.
16	AGND	**Analog ground.**

ABSOLUTE MAXIMUM RATINGS (1)

SW.......................-0.3V to +24V (28V for <10ns)
IN, SENSE, OUT........................... -0.3V to +24V
CLDR....................................-0.3V to VIN +5.5V
BST, SDR..............................-0.3V to V_{SW} +5.5V
All other pins ....-0.3V to +5.5V
EN bias current 0.5mA (2)
Junction temperature .... 150°C
Lead temperature..................................... 260°C
Storage temperature..................-65°C to +150°C
Continuous power dissipation (T_A = 25°C) (3)
.... 2.6W

ESD Rating

Human-body model (HBM)..................... Class 2
Charged-device model (CDM)......................C4B

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) .... 3V to 20V
Output voltage (V_{OUT}) ....V_{IN} to 22V
EN bias current.....................0mA to 0.3mA (2)
Operating junction temp (T_J) .... -40°C to +125°C

***Thermal Resistance* (5)**	θ_{JA}	θ_{JC}	
QFN-22 (3mmx4mm)	48	11	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) See the Enable and Programmable UVLO section on page 15.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, T_J = -40°C to +125°C, typical value is tested at 25°C, unless otherwise noted.

Parameter	Symbol	Condition		Min	Typ	Max	Units
Operating input voltage	V_{IN}			3		20	V
Input UVLO	IN_{UVLO-R}	V_{IN} rising		2.58	2.68	2.78	V
Input UVLO hysteresis	$IN_{UVLO-HYS}$				250		mV
Operating VDD voltage	V_{DD}	V_{IN} = 12V			5		V
Shutdown current	I_{SD}	V_{EN} = 0V, measured on IN	T_J = 25°C			1	µA
			T_J = -40°C to +125°C			5	
Quiescent current	I_{Q-OUT}	V_{FB} = 1.35V, V_{IN} = 3.3V, V_{OUT} = 12V, no switching, measured on OUT	T_J = 25°C		650	750	µA
			T_J = -40°C to +125°C			900	
	I_{Q-IN}	V_{FB} = 1.35V, V_{IN} = 3.3V, V_{OUT} = 12V, no switching, measured on IN	T_J = 25°C		110	150	
			T_J = -40°C to +125°C			200	
Switching frequency	f_{SW}	T_J = 25°C		510	600	690	kHz
		T_J = -40°C to +125°C		480		720	
Minimum off time (6)	$t_{MIN-OFF}$	V_{FB} = 0V			200		ns
Minimum on time (6)	t_{MIN-ON}				120		ns
EN turn-on threshold	V_{EN-ON}	V_{EN} rising (switching)		1.27	1.33	1.39	V
EN high threshold	V_{EN-H}	V_{EN} rising (micro power)				1.0	V
EN low threshold	V_{EN-L}	V_{EN} falling (micro power)		0.36			V
EN turn-on hysteresis current	I_{EN-HYS}	1.0V < EN < 1.4V		3	4.5	6	µA
EN input bias current	I_{EN}	V_{EN} = 0V, 3.3V			0		µA
Soft-start charge current	I_{SS}			4.5	7	9	µA
FB reference voltage	V_{FB}	T_J = 25°C		1.212	1.225	1.238	V
		T_J = -40°C to +125°C		1.2		1.25	
FB input/bias current	I_{FB}	V_{FB} = 1V		-100			nA
SDR rise time (6)	$t_{SDR-Rise}$	C_{Load} = 2.7nF, test from 10% to 90%			20		ns
SDR fall time (6)	$t_{SDR-Fall}$	C_{Load} = 2.7nF, test from 90% to 10%			30		ns
Error amp voltage gain (7)	A_{V-EA}				300		V/V
Error amp transconductance	G_{EA}				160		µA/V
Error amp max output current		V_{FB} = 1V or 1.5V			22		µA
Current to COMP gain	Gcs	V_{CLDR} = GND			27		A/V
Sense to COMP gain	Gxcs	CLDR float, ΔV_{SENSE} / ΔV_{COMP}			103		mV/V
Comp threshold for switching (6)	V_{PSM}				0.5		V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.3V, T_J = -40°C to +125°C, typical value is tested at 25°C, unless otherwise noted.

Parameter	Symbol	Condition		Min	Typ	Max	Units
Comp high clamp					2		V
SW on resistance	R_{ON}					18	mΩ
SW current limit	I_{LIMT}	V_{CLDR} = GND, duty cycle = 40%	T_J = 25°C	19	25	29	A
			T_J = -40°C to +125°C	16	25	29	
External sense average current limit	V_{CL}	CLDR float		45	54	63	mV
Linear charge start-up SCP blanking time	t_{CL}	CLDR float			0.5		ms
Thermal shutdown (6)	T_{SD}				150		°C
Thermal shutdown hysteresis (6)	T_{SD-HYS}				25		°C

Notes:

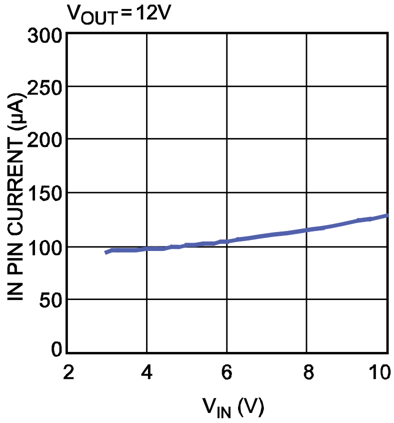
6) Guaranteed by characterization, not tested in production.
7) Guaranteed by design.

TYPICAL ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

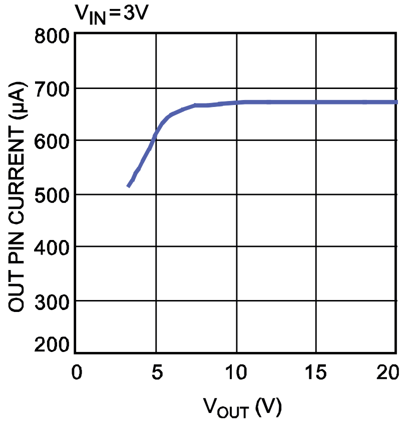
IN Quiescent Current vs. Input Voltage

V_{OUT}=12V



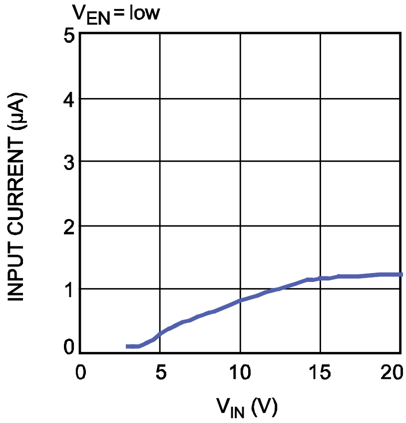
OUT Quiescent Current vs. Output Voltage

V_{IN}=3V

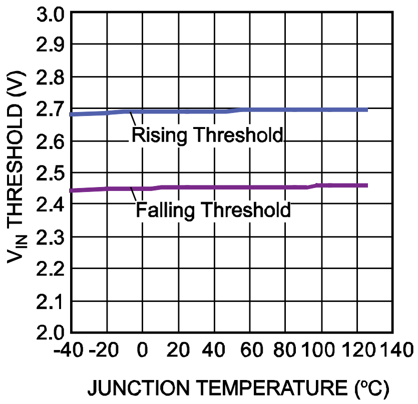


Shutdown Current vs. Input Voltage

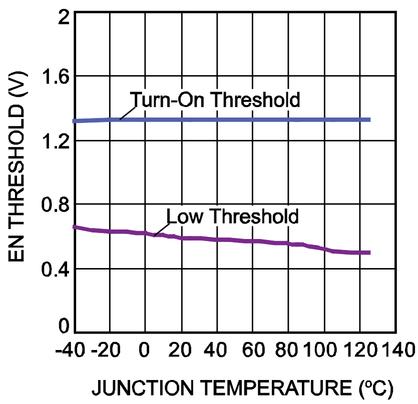
V_{EN}=low



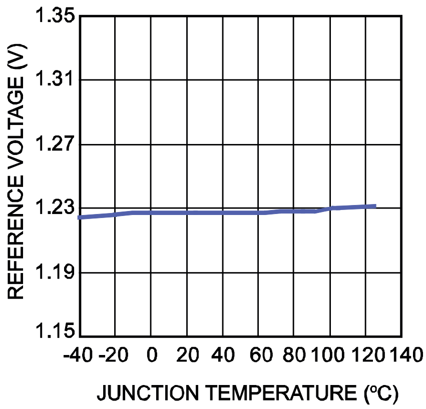
VIN UVLO Threshold vs. Temperature



EN Threshold vs. Temperature

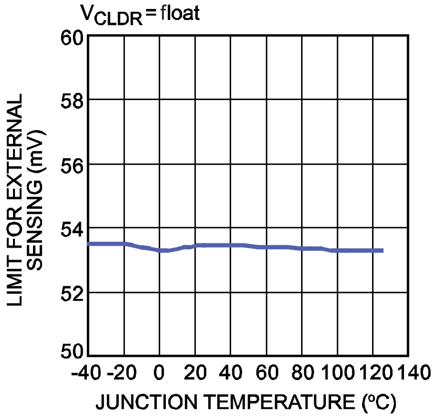


FB Reference Voltage vs. Temperature

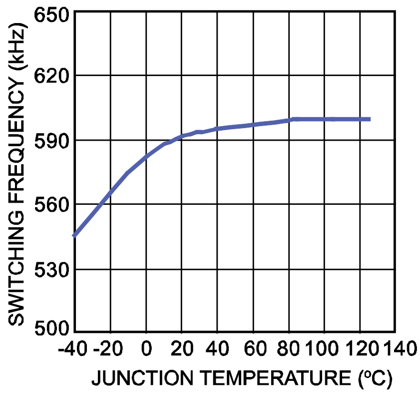


External Sense Average Current Limit vs. Temperature

V_{CLDR}=float

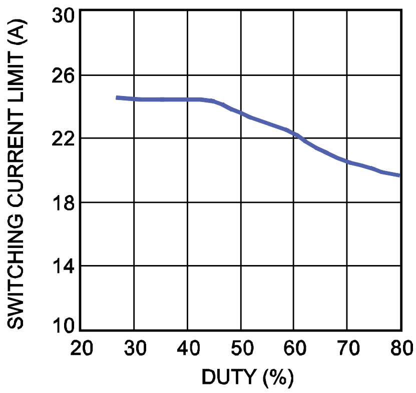


Switching Frequency vs. Temperature



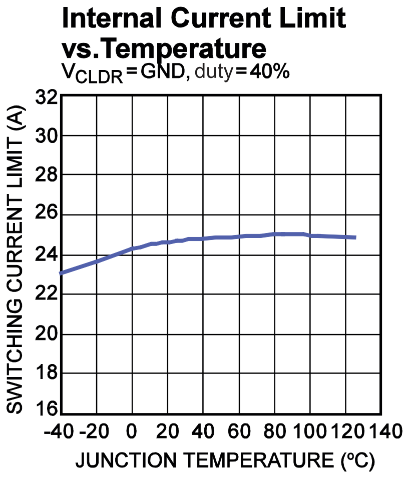
Internal Current Limit vs. Duty

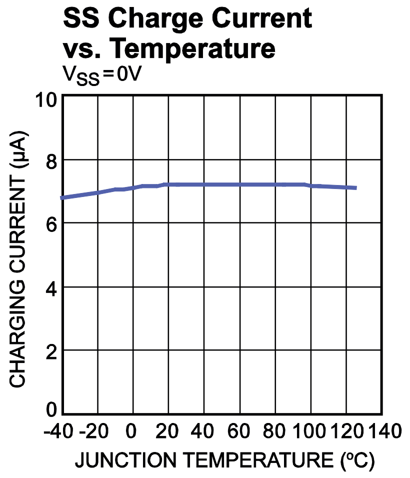
V_{CLDR}=GND



TYPICAL ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

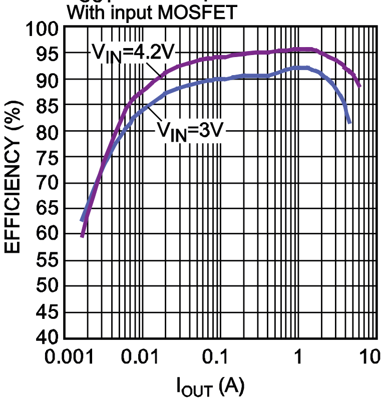




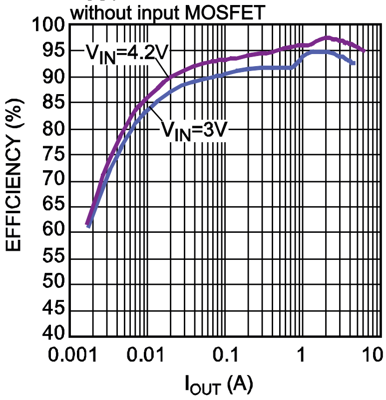
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 2A, C_{OUT} = 22µFx3, R_{SENSE} = 4.5mΩ, add input disconnect and output SCP MOSFET, tested on 4-layer board, T_A = 25°C, unless otherwise noted.

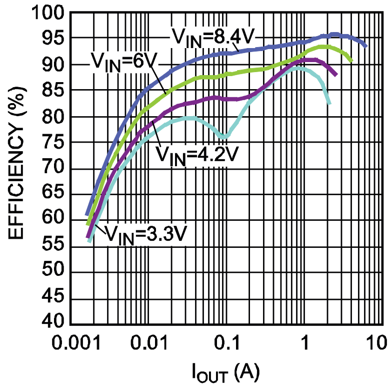
Efficiency vs. Output Current
V_{OUT}=5V, L=1µH, With input MOSFET



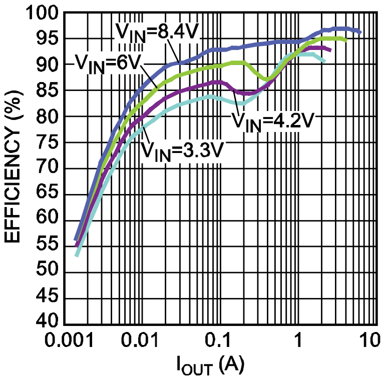
Efficiency vs. Output Current
V_{OUT}=5V, L=1µH, CLDR=GND, without input MOSFET



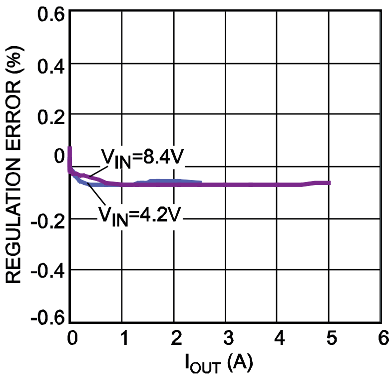
Efficiency vs. Output Current
With input MOSFET



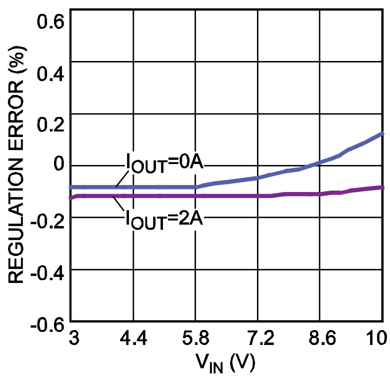
Efficiency vs. Output Current
without input MOSFET



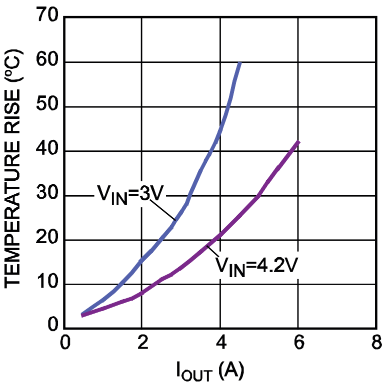
Load Regulation



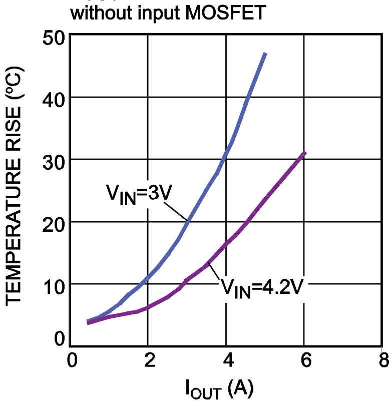
Line Regulation



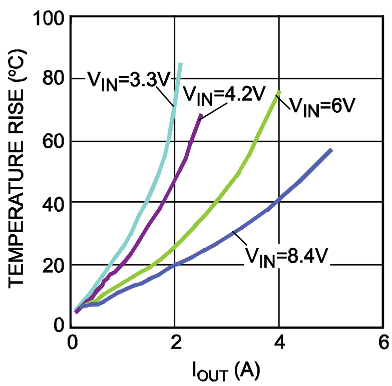
Case Temperature Rise
V_{OUT}=5V, With input MOSFET



Case Temperature Rise
V_{OUT}=5V, CLDR=GND, without input MOSFET



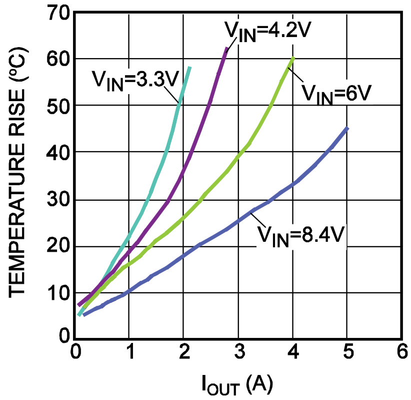
Case Temperature Rise
With input MOSFET



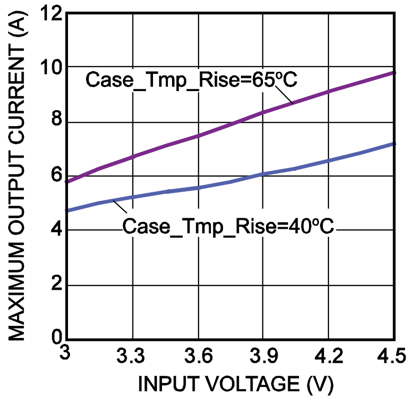
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5μH, I_{OUT} = 2A, C_{OUT} = 22μFx3, R_{SENSE} = 4.5mΩ, add input disconnect and output SCP MOSFET, tested on 4-layer board, T_A = 25°C, unless otherwise noted.

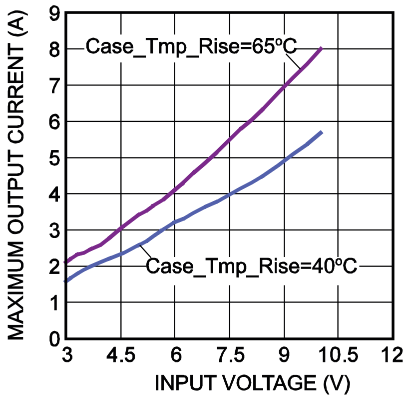
Case Temperature Rise
CLDR=GND,
without input MOSFET



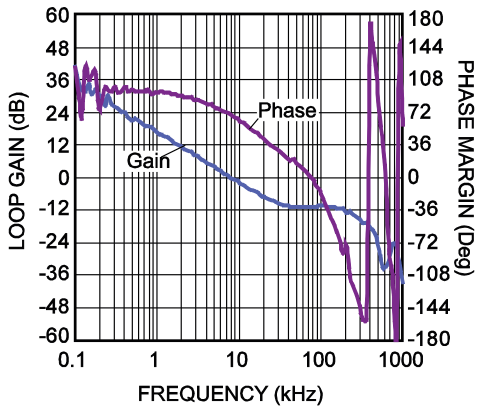
Load Capability
V_{OUT}=5V, CLDR=GND,
without input MOSFET



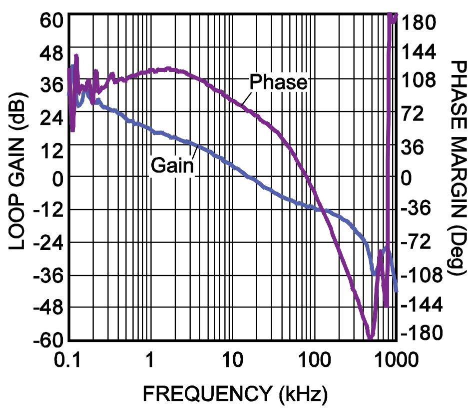
Load Capability
CLDR=GND,
without input MOSFET



Bode Plot
V_{IN}=3.3V



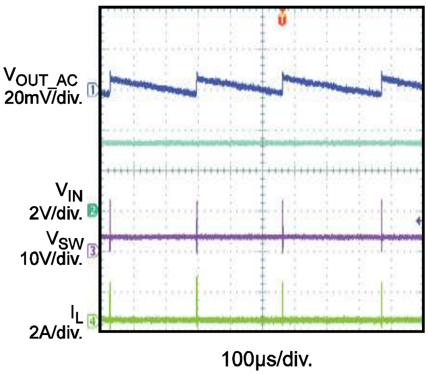
Bode Plot
V_{IN}=6V, I_{OUT}=4A



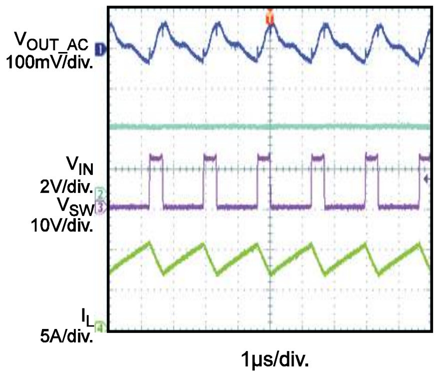
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 2A, C_{OUT} = 22µFx3, R_{SENSE} = 4.5mΩ, add input disconnect and output SCP MOSFET, T_A = 25°C, unless otherwise noted.

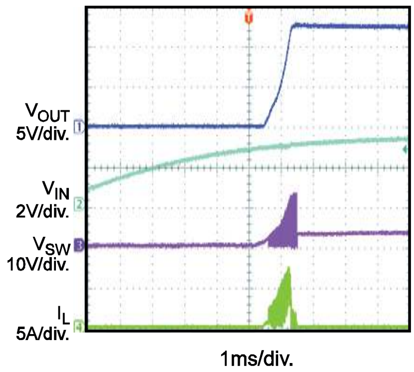
Steady State
I_{OUT}=0A



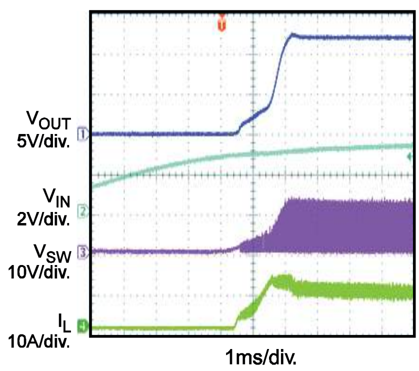
Steady State



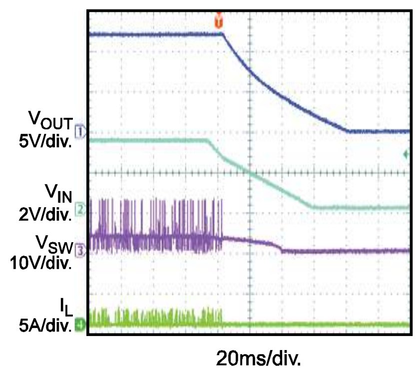
V_{IN} Start-Up
I_{OUT}=0A



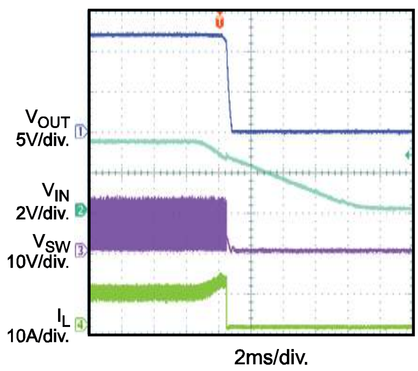
V_{IN} Start-Up



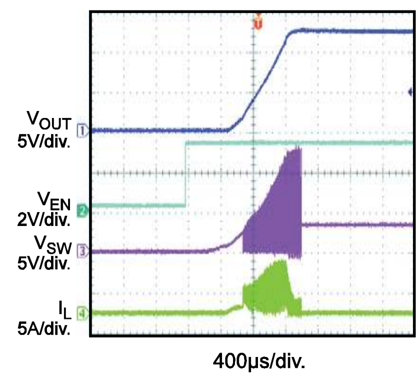
V_{IN} Shutdown
I_{OUT}=0.01A



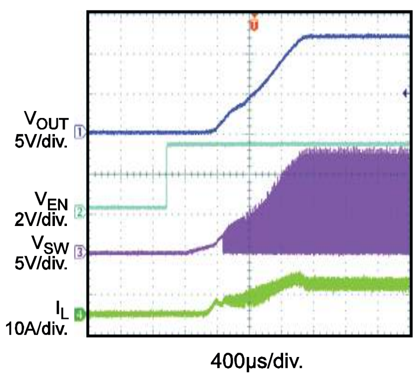
V_{IN} Shutdown



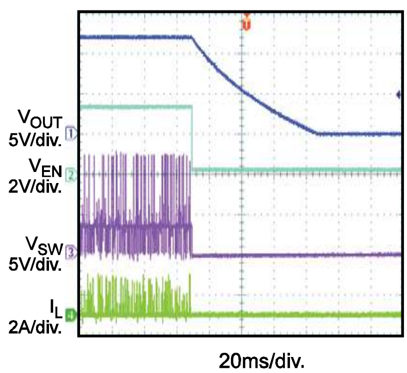
EN Start-Up
I_{OUT}=0A



EN Start-Up



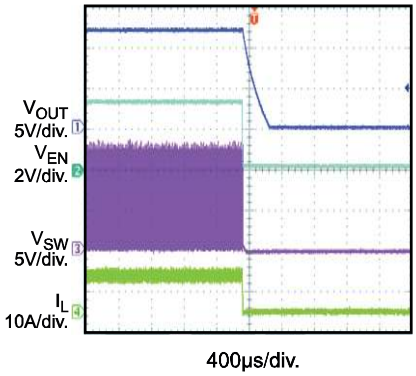
EN Shutdown
I_{OUT}=0.01A



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

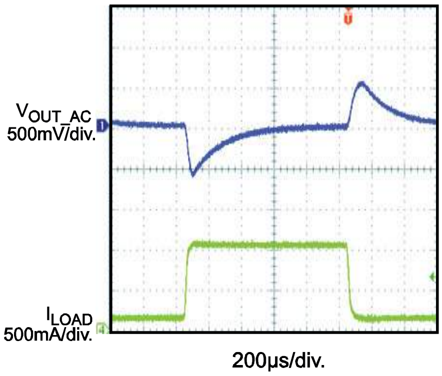
V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 2A, C_{OUT} = 22µFx3, R_{SENSE} = 4.5mΩ, add input disconnect and output SCP MOSFET, T_A = 25°C, unless otherwise noted.

EN Shutdown



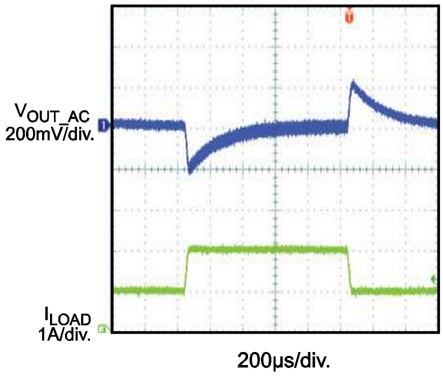
Response to Transient Load

V_{IN}=6V, I_{OUT}=0.1A to 1A@25mA/µs

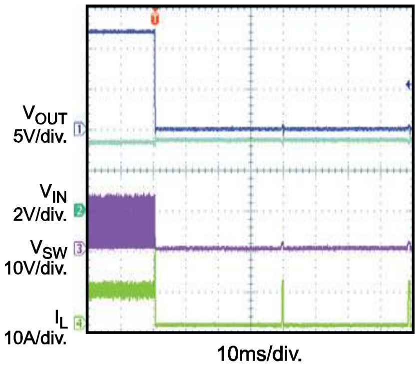


Response to Transient Load

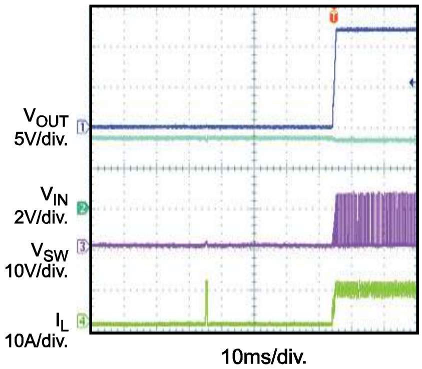
V_{IN}=6V, I_{OUT}=1A to 2A@25mA/µs



Response to Output Short



Recovery from Output Short



FUNCTIONAL BLOCK DIAGRAM

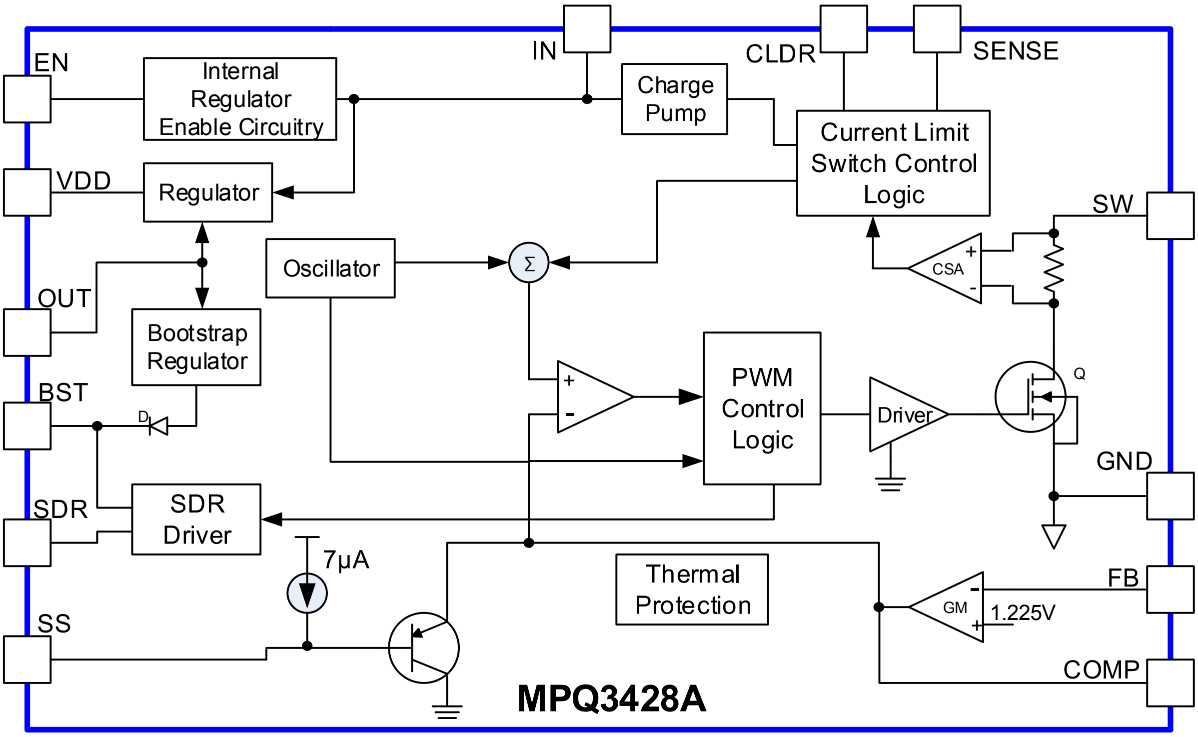


Figure 1: Functional Block Diagram

OPERATION

Boost Function

The MPQ3428A uses a constant-frequency, peak current mode, boost regulation architecture to regulate the output voltage.

At the beginning of each cycle, the N-channel MOSFET switch Q is turned on, forcing the inductor current to rise. The current flowing through switch Q is measured externally (or measured internally when CLDR is connected to GND) and converted to a voltage by the current amplifier. That voltage is compared with the error voltage on the internal COMP, which is a buffer voltage from the external COMP pin during normal operation. The voltage on the external COMP pin is an amplified version of the difference between the 1.225V reference voltage and the feedback voltage. When the sensed voltage is equal to the buffered COMP voltage, the PWM comparator turns off switch Q, forcing the inductor current into the output capacitor through the external rectifier. This causes the inductor current to decrease. The peak inductor current is controlled by the COMP voltage, which is in turn controlled by the output voltage. Thus, the output voltage is regulated by the inductor current to satisfy the load. Current mode regulation improves transient response and control loop stability.

VDD Power

The MPQ3428A's internal circuit is powered by VDD. A ceramic capacitor (no lower than 2.2µF) is required to decouple VDD. During start-up, VDD power is regulated from IN. Once the output voltage exceeds the input voltage, VDD is powered from V_{OUT} instead of V_{IN}. This allows the MPQ3428A to maintain low R_{ON} and high efficiency even with a low input voltage.

Soft Start (SS)

The MPQ3428A uses one external capacitor on SS to control the switching frequency during start-up. The operation frequency is initially 1/4 of the normal frequency. As the SS capacitor is charged (charging happens after the MPQ3428A runs in boost operation), the frequency increases continually. When the voltage on SS exceeds 0.65V, the frequency switches to a normal frequency. In addition, the COMP voltage is clamped within V_{SS} + 0.7V. During start-up, the COMP voltage reaches 0.7V quickly and then rises at the same rate of V_{SS}. These two mechanisms protect the input power supply from high inrush current.

SDR and BST Function

The MPQ3428A generates a synchronous gate driver, which is complementary to the gate driver of the internal low-side MOSFET. The SDR driver is powered from BST (typically 5V). A low Q_G, N-channel MOSFET with a gate threshold voltage below 2.5V is preferred for synchronous rectification. In high-power applications, using a synchronous rectifier switch improves the overall converting efficiency. If a synchronous rectifier switch is not used, float SDR.

The 5V BST voltage is powered from OUT. If the output voltage is low or the duty cycle is too low, the BST voltage may not be regulated to 5V, triggering a BST_UVLO. If this condition occurs, a Schottky diode from an external 5V source to BST is recommended. Otherwise the SDR driver signal may be lost.

Current-Sensing Configuration

The MPQ3428A offers the option of using an internal circuit or an external resistor to sense the inductor current. When using an internal current-sense circuit, the CLDR must be connected directly to GND before powering on. Meanwhile, SENSE should be connected to IN. In this condition, the internally sensed current is compared to both the COMP voltage and the peak inductor current limit to generate the duty cycle.

When CLDR is connected to the gate of the input MOSFET or left floating before powering on, the inductor current is sensed by an external resistor between IN and SENSE. Under this configuration, the externally sensed current is compared with COMP for low-side switch on/off control. The overload protection, or disconnect function, is achieved by monitoring the average input current through the external sensing resistor (see the Protection and Input Disconnect Function section on page 14 for details).

Protection and Input Disconnect Function

The MPQ3428A features excellent OCP and SCP.

During start-up, the MPQ3428A monitors the voltage on CLDR to determine whether to use internal or external current sensing. Connecting CLDR to the gate of an external MOSFET or leaving it floating selects an external sensing resistor; connecting CLDR directly to GND selects an internal sensing circuit.

If internal current sensing is selected, OCP is achieved by limiting the peak inductor current in every switching cycle (without hiccup in OCP) unless V_{OUT} is pulled below V_{IN}. After the SS voltage exceeds about 0.7V, the MPQ3428A may run in hiccup mode if it detects that the output voltage is below the input voltage. This prevents the MPQ3428A from damage even if there is not an input disconnecting the MOSFET during a heavy-load condition.

If external current sensing is selected, CLDR is charged by a current (typically 13μA) from the internal charge pump. Once the voltage on CLDR reaches the MOSFET's threshold, the input current is generated, charging up the output capacitors, and the output voltage follows the CLDR voltage with a MOSFET (V_{TH}) threshold difference. The MPQ3428A has a current feedback loop to control the CLDR and COMP voltages so the input current will not exceed V_{CL} (mV) / R_{SENSE} (mΩ).

During start-up with external current sensing (if V_{CLDR} is below V_{IN} + 1.6V), the linear charge current limit works with the V_{CL} / R_{SENSE} limitation (V_{CLDR} is regulated to limit the current). The MPQ3428A shuts down if the linear charge current limit is triggered for more than 0.5ms by pulling CLDR down to GND. The MPQ3428A waits for about 20ms to 70ms (the hiccup time depends on V_{IN} and V_{OUT}) to restart if it is not reset by V_{IN} or EN. A normal load will not lead to hiccup protection during start-up.

If V_{CLDR} exceeds V_{IN} + 1.6V, boost switching is enabled. SS is charged and the power MOSFET turns on/off periodically to regulate V_{OUT} following the SS signal. When the MPQ3428A starts switching and V_{OUT} is below V_{IN}, both the linear charge current limit (regulated CLDR voltage) and the boost input average current limit (regulated COMP voltage) begin to work; both the control loops work with the limit of V_{CL} / R_{SENSE}.

After V_{OUT} is charged above V_{IN} in boost mode, only the boost input average current limit works (regulated COMP voltage). The MPQ3428A will not trigger hiccup OCP unless the SS voltage exceeds 0.7V, and V_{OUT} drops below V_{IN}. If hiccup protection is triggered in switching mode, switching stops and CLDR is pulled low. It restarts after about 20ms to 70ms, depending on V_{IN} and V_{OUT}. The recovery process is the same as the start-up process.

Table 1 shows the detailed OCP mode when using an external current-sense resistor.

If the inductor current ramps quickly and the inductor peak current exceeds 100mV / R_{SENSE} (mΩ), the MPQ3428A shuts down immediately, entering SCP hiccup mode. This fast protection allows the MPQ3428A to survive all SCP events.

When the MPQ3428A is shut down by EN or V_{IN}, CLDR is pulled down to GND, and the output and input are isolated by the input MOSFET. This is the V_{IN}-to-V_{OUT} disconnect function.

Light-Load Operation

To optimize efficiency at light load, the MPQ3428A employs a foldback frequency and a pulse-skipping mechanism. When the load becomes lighter, the COMP voltage decreases, causing the MPQ3428A to enter foldback operation (the lighter the load, the lower the frequency). However, if the load becomes exceedingly low, the MPQ3428A enters PSM. PSM operation is optimized so that only one switching pulse is launched in every burst cycle.

Table 1: MPQ3428A OCP Mode when Using an External Current-Sense Resistor

Condition	Work Mode	OCP Action
$V_{CLDR} < V_{IN} + 1.6V$	Linear charge mode, no boost switching	The linear charge current limit works: • V_{CLDR} is regulated down to keep the input current at V_{CL} / R_{SENSE}. • If the linear charge OCP lasts 0.5ms, the MPQ3428A triggers hiccup protection. The boost input average current limit does not work.
$V_{CLDR} \geq V_{IN} + 1.6V$ (8) $V_{OUT} \leq V_{IN}$ $V_{SS} \leq 0.7V$	Boost switching	The linear charge current limit works: • V_{CLDR} is regulated down to keep the input current at V_{CL} / R_{SENSE}. • If the linear charge OCP lasts 0.5ms, the MPQ3428A triggers hiccup protection. The boost input average current limit works: • The COMP voltage is regulated to keep the input average current at V_{CL} / R_{SENSE}.
$V_{CLDR} \geq V_{IN} + 1.6V$ (8) $V_{OUT} \leq V_{IN}$ $V_{SS} > 0.7V$	Boost switching	Runs into hiccup protection without delay.
$V_{CLDR} \geq V_{IN} + 1.6V$ (8) $V_{OUT} > V_{IN}$	Boost switching	The linear charge current limit does not work. V_{CLDR} remains high. The boost input average current limit works. • The COMP voltage is regulated to keep the input average current at V_{CL} / R_{SENSE}, no hiccup.

Note:

8) After start-up, the $V_{CLDR} \geq V_{IN} + 1.6V$ condition is registered if V_{CLDR} exceeds $V_{IN} + 1.6V$ one time. This means the MPQ3428A treats the condition as $V_{CLDR} \geq V_{IN} + 1.6V$ even if V_{CLDR} falls below $V_{IN} + 1.6V$ again in protection mode (unless it is turned off by the hiccup protection or by the power recycle).

Enable (EN) and Programmable UVLO

EN enables and disables the MPQ3428A. When a voltage greater than V_{EN_H} (1V) is applied, the MPQ3428A starts up some of the internal circuits (micro-power mode). If the EN voltage continues to increase above V_{EN_ON} (1.33V), the MPQ3428A enables all functions and begins boost operation. Boost operation is disabled if the EN voltage is below V_{EN_ON} (1.33V). To shut down the MPQ3428A completely, a voltage less than V_{EN_L} (0.36V) is required on EN. After shutdown, the MPQ3428A sinks a current less than 1μA from the input power.

The maximum recommended voltage on EN is 5.5V. If the EN control signal comes from a voltage greater than 5.5V, a resistor should be added between EN and the control source. An internal Zener diode on EN clamps the EN voltage to prevent runaway. Ensure the Zener clamped current flowing into EN is less than 0.3mA. EN can be used to program V_{IN}'s UVLO. See the UVLO Hysteresis section on page 16 for details.

Output Over-Voltage Protection

Except for controlling the COMP signal to regulate the output voltage, the MPQ3428A also provides over-voltage protection. If the FB voltage exceeds 108% of the reference voltage, boost switching stops. When the FB voltage drops below 104% of the reference voltage, the device resumes switching automatically.

Thermal Shutdown

The device has an internal temperature monitor. If the die temperature exceeds 150°C, the converter shuts down. Once the temperature drops below 125°C, the converter turns on again.

APPLICATION INFORMATION

Components referred to below apply to the typical application circuit (Figure 6) on page 20.

Selecting the Current Limit Resistor

The MPQ3428A features an average current limit when the external sensing resistor is used. The resistor (R_{SENSE}) connected between IN and SENSE sets the current limit (I_{CL}). Calculate I_{CL} with Equation (1):

$$I_{CL} = V_{CL} / R_{SENSE} \quad (1)$$

Where V_{CL} is typically 54mV, I_{CL} is in A, and R_{SENSE} is in mΩ.

Considering the parasitic inductance on the sense resistor, a small-sized resistor (e.g. 0805) is recommended. Add several parallel resistors if the power rating is lower than recommended. To reduce the effect of parasitic resistance and noise, a sense resistor with resistance greater than 4mΩ is recommended.

UVLO Hysteresis

The MPQ3428A features a programmable UVLO hysteresis. When powering up, EN sinks a 4.5μA current from the upper resistor, R_{TOP} (see Figure 2).

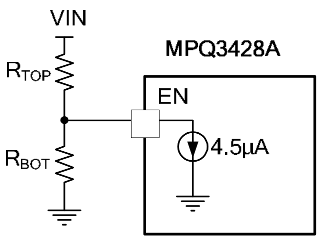


Figure 2: V_{IN} UVLO Program

VIN must increase in voltage to overcome the current sink. Calculate the VIN start-up threshold with Equation (2):

$$V_{IN-ON} = V_{EN-ON} \times (1 + \frac{R_{TOP}}{R_{BOT}}) + 4.5\mu A \times R_{TOP} \quad (2)$$

Where V_{EN-ON} is the EN voltage turn-on threshold (typically 1.33V).

Once the EN voltage reaches V_{EN-ON}, the 4.5μA sink current turns off to create a reverse hysteresis for the VIN falling threshold. Calculate $V_{IN-UVLO-HYS}$ with Equation (3):

$$V_{IN-UVLO-HYS} = 4.5\mu A \times R_{TOP} \quad (3)$$

Selecting the Soft-Start Capacitor

The MPQ3428A includes a soft-start circuit that limits the voltage on COMP during start-up to prevent excessive input current. This prevents premature termination of the source voltage at start-up due to input current overshoot. When power is applied to the MPQ3428A and EN is asserted, a 7μA internal current source charges the external capacitor at SS.

The SS voltage clamps the COMP voltage (and the inductor peak current) until the output is close to regulation or until COMP reaches 2V. For most applications, a 10nF SS capacitor is sufficient. If the output capacitance is large or the front power supply cannot withstand the huge inrush current, SS capacitors can be increased accordingly.

Setting the Output Voltage

The output voltage is fed back through two sense resistors in series. The feedback reference voltage is typically 1.225V. The output voltage is determined with Equation (4):

$$V_{OUT} = V_{REF} \times (1 + \frac{R1}{R2}) \quad (4)$$

Where R1 is the top feedback resistor, R2 is the bottom feedback resistor, and V_{REF} is the reference voltage (typically 1.225V).

Choose the feedback resistors to be about 10kΩ (or higher) for good efficiency.

Selecting the Input Capacitor

An input capacitor is required to supply the AC ripple current to the inductor while limiting noise at the input source. A low-ESR capacitor is required to minimize noise. Ceramic capacitors are recommended, but tantalum or low-ESR electrolytic capacitors will suffice.

At least two 22μF capacitors are recommended for loop stability in high-power applications. The capacitor can be electrolytic, tantalum, or ceramic. Since the capacitor absorbs the input switching current, it requires an adequate ripple current rating. Use a capacitor with an RMS current rating greater than the inductor ripple current. See the Selecting the Inductor section on page 17 to determine the inductor ripple current.

To ensure stable operation, place the input capacitor as close to the IC as possible. Alternately, a smaller, high-quality 0.1µF ceramic capacitor may be placed closer to the IC and the larger capacitor placed farther away. If using this technique, a larger electrolytic or tantalum capacitor is recommended. All ceramic capacitors should be placed close to the MPQ3428A input.

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Low-ESR capacitors are preferred to minimize the output voltage ripple. The characteristics of the output capacitor affect the stability of the regulation control system. Ceramic, tantalum, or low-ESR electrolytic capacitors are recommended. If using ceramic capacitors, the capacitance dominates the impedance at the switching frequency, so the output voltage ripple is independent of the ESR. Estimate the output voltage ripple with Equation (5):

$$V_{RIPPLE} = \frac{(1-\frac{V_{IN}}{V_{OUT}}) \times I_{LOAD}}{C_{OUT} \times f_{SW}} \tag{5}$$

Where V_{RIPPLE} is the output ripple voltage, V_{IN} and V_{OUT} are the DC input and output voltages respectively, I_{LOAD} is the load current, f_{SW} is the 600kHz fixed switching frequency, and C_{OUT} is the capacitance of the output capacitor.

If using tantalum or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency. Estimate the output ripple using Equation (6):

$$V_{RIPPLE} = \frac{(1-\frac{V_{IN}}{V_{OUT}}) \times I_{LOAD}}{C_{OUT} \times f_{SW}} + \frac{I_{LOAD} \times R_{ESR} \times V_{OUT}}{V_{IN}} \tag{6}$$

Where R_{ESR} is the equivalent series resistance of the output capacitors.

Choose an output capacitor to satisfy the output ripple and load transient requirements of the design. Capacitance derating should be taken into consideration when designing high output voltage applications. Three 22µF ceramic capacitors are suitable for most applications.

Selecting the Inductor

The inductor is required to force the higher output voltage while being driven by the input voltage. A higher-value inductor has less ripple current, resulting in lower peak inductor current. This reduces stress on the internal N-channel switch and enhances efficiency. However, the higher-value inductor also has a larger physical size, higher series resistance, and lower saturation current.

A good rule of thumb is to allow the peak-to-peak ripple current to be approximately 30% to 40% of the maximum input current. Ensure that the peak inductor current is below 75% of the current limit at the operating duty cycle to prevent loss of regulation due to the current limit. In addition, be sure that the inductor does not saturate under the worst-case load transient and start-up conditions. Calculate the required inductance value with Equation (7) and Equation (8):

$$L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I} \tag{7}$$

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{LOAD(MAX)}}{V_{IN} \times \eta} \tag{8}$$

Where $I_{LOAD(MAX)}$ is the maximum load current, ΔI is the peak-to-peak inductor ripple current, ΔI = (30% to 40%) x $I_{IN\ (MAX)}$, and η is the efficiency.

Selecting the Output Rectifier

The MPQ3428A features an SDR gate driver. Instead of a Schottky diode, an N-channel MOSFET can be used to freewheel the inductor current when the internal MOSFET is off. The SDR gate driver voltage has a high 5V voltage, so choose an N-channel MOSFET compatible with a 5V gate voltage rating. The minimum high level is about 3V. Therefore, the MOSFET's turn-on threshold is recommended to be below 2.5V.

In some low-output applications, such as a 5V output, the voltage across the BST capacitor may be insufficient. In this case, a Schottky diode should be connected from the output port to BST, conducting the current into the BST capacitor when SW goes low (see Figure 3).

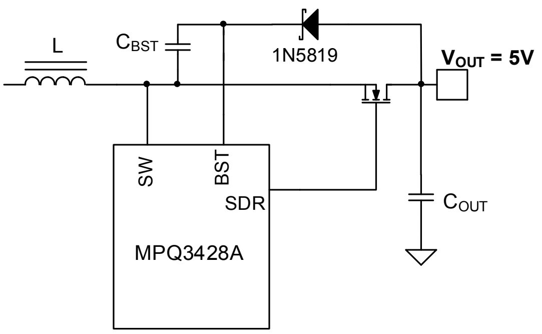


Figure 3: BST Charger for Low-Output Application

The MOSFET voltage rating should be equal to or greater than the output voltage. The average current rating must exceed the maximum load current, and the peak current rating must exceed the peak inductor current. If a Schottky diode is used as the output rectifier, the same specifications should be considered.

Selecting the Input MOSFET

The MPQ3428A integrates one CLDR pin to drive an external N-channel MOSFET to disconnect the input power or limit the input current. The following key factors should be considered when selecting the input disconnecting MOSFET:

1. Drain-to-source voltage rating: This value should be greater than V_{IN} + V_{TH} of the input MOSFET.
2. Drain-to-source current rating: The maximum current through the input disconnecting MOSFET is the maximum input current. This occurs when the input voltage is at a minimum and the load power is at a maximum.
3. SOA: The MOSFET should survive when conducting a current pulse that has a high level of V_{CL} (mV) / R_{SENSE} (mΩ) and lasts for C_{SS} (nF) x 0.7 (V) / 7 (μA) + 0.5ms.
4. Gate-to-source voltage rating: The positive gate-to-source voltage rating should be greater than 5.5V, while the negative voltage rating should be greater than the value of the output voltage. If the output voltage is too high and the MOSFET gate-to-source rating cannot meet the requirement, a diode from the source to the gate of the disconnecting MOSFET is recommended (see Figure 4).
5. Gate-to-source threshold voltage: The threshold should be below 1.5V. A 1V to 1.2V overall temperature range is preferred.
6. On resistance (R_{DS_ON}): The on resistance should be small for high conversion efficiency.
7. Low leakage current: The leakage current should be low for better isolation.

In addition, size and thermal temperature should be taken into consideration.

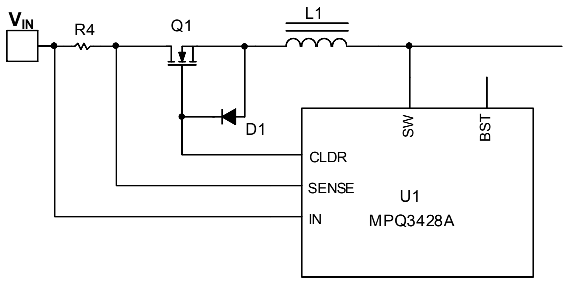


Figure 4: Gate Protection Diode for High Output Voltage Condition

Compensation

The output of the transconductance error amplifier (COMP) is used to compensate the regulation control system. The system uses two poles and one zero to stabilize the control loop.

The poles are f_{P1} (set by the output capacitor, C_{OUT}, and the load resistance), and f_{P2} (start from origin). The zero f_{Z1} is set by the compensation capacitor (C_{COMP}) and the compensation resistor (R_{COMP}). Calculate f_{P2} and f_{Z1} with Equation (9) and Equation (10):

$$f_{P1} = \frac{1}{2 \times \pi \times R_{LOAD} \times C_{OUT}} (Hz) \tag{9}$$

$$f_{Z1} = \frac{1}{2 \times \pi \times R_{COMP} \times C_{COMP}} (Hz) \tag{10}$$

Where R_{LOAD} is the load resistance.

Calculate the DC loop gain using Equation (11):

$$A_{VDC} = \frac{A_{VEA} \times V_{IN} \times R_{LOAD} \times V_{FB} \times G_{CS} x\ R_{COMP}}{2 \times V_{OUT}^2} (V/V) \tag{11}$$

Where G_{CS} is the compensation voltage to the inductor current gain, A_{VEA} is the error amplifier voltage gain, and V_{FB} is the feedback regulation threshold.

There is a right-half-plane zero (f_{RHPZ}) that exists in continuous conduction mode (the inductor current does not drop to zero in each cycle). The frequency of the right-half-plane zero is determined with Equation (12):

$$f_{RHPZ} = \frac{R_{LOAD}}{2 \times \pi \times L} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2 (Hz) \tag{12}$$

The right-half-plane zero increases the gain and reduces the phase simultaneously, which results in a smaller phase and gain margin. The worst-case condition occurs when the input voltage is at its minimum and the output power is at its maximum.

Compensation recommendations are listed in the Typical Application Circuits section on page 20.

Design Example

Below is a design example following the application guidelines for the specifications:

Table 2: Design Example

V_{IN}	3.3V to 10V
V_{OUT}	12V
I_{OUT}	0A to 2A [9]

Note:

9) The maximum load capability may be limited by the permitted temperature rising.

The maximum output current is determined by the permitted temperature rising, current limit, and input voltage. The detailed application schematic is shown in Figure 6. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section on page 8. For more device applications, refer to the related evaluation board datasheets.

PCB Layout Guidelines

High-frequency switching regulators require very careful layout for stable operation and low noise. All components should be placed as close to the IC as possible, and a 4-layer PCB is recommended for high-power applications. For best results, refer to Figure 5 and follow the guidelines below:

1. Keep the output loop (SW, PGND, Q2, and C2) as small as possible.
2. Place the FB divider R1 and R2 as close as possible to FB.
3. Route the sensing traces (SENSE and IN) in parallel closely with a small closed area. A 0805 package is recommended for the sensing resistor (R4) to reduce parasitic inductance.
4. Connect FB and OUT feedback from the output capacitor (C2).
5. Connect the compensation components and SS capacitor to AGND with a short loop.
6. Connect the VDD capacitor to AGND with a short loop.
7. Do not connect to the PGND net before connecting to the IC and AGND.
8. Keep the input loop (C1, R4, Q1, L1, SW, and PGND) as small as possible.
9. Make the BST and SDR path as short as possible.
10. Place enough GND vias close to the MPQ3428A for good thermal dissipation.
11. Do not place vias on the SW net.
12. Place wide copper pours and vias associated with the input MOSFET's drain pin for thermal dissipation.

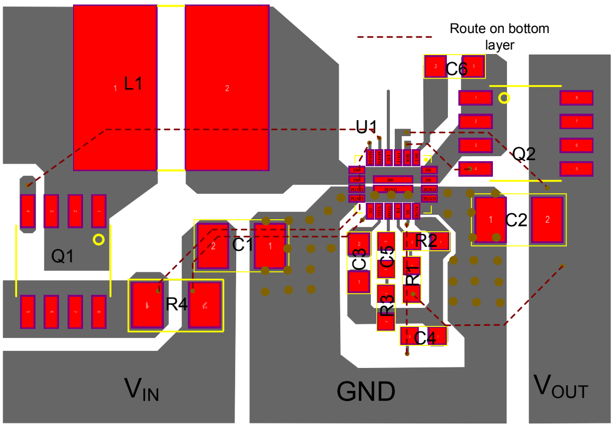


Figure 5: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

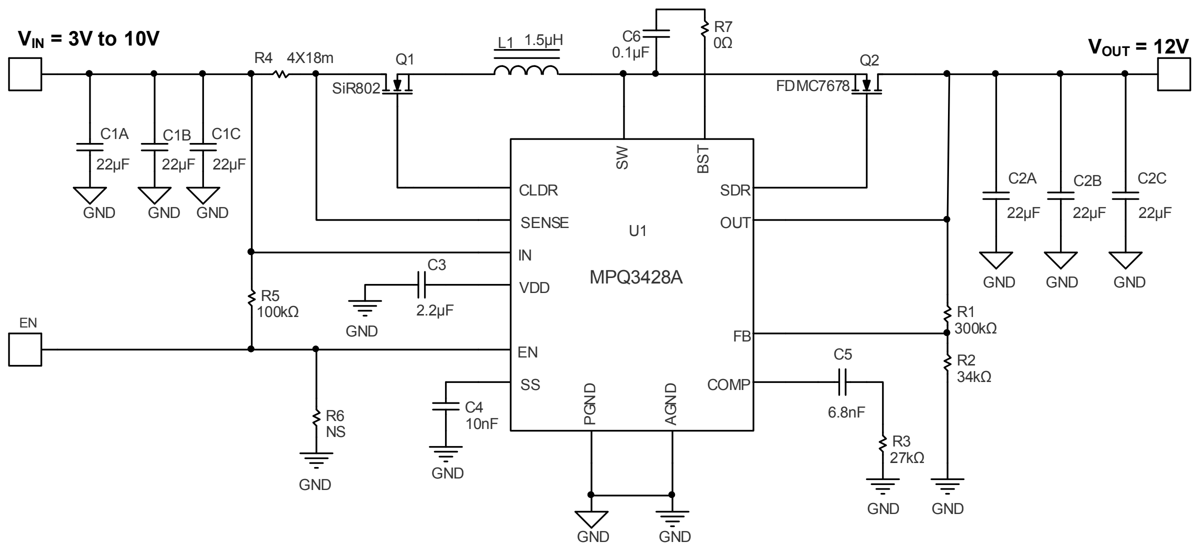


Figure 6: 12V Output Synchronous Solution with Input Disconnect Function

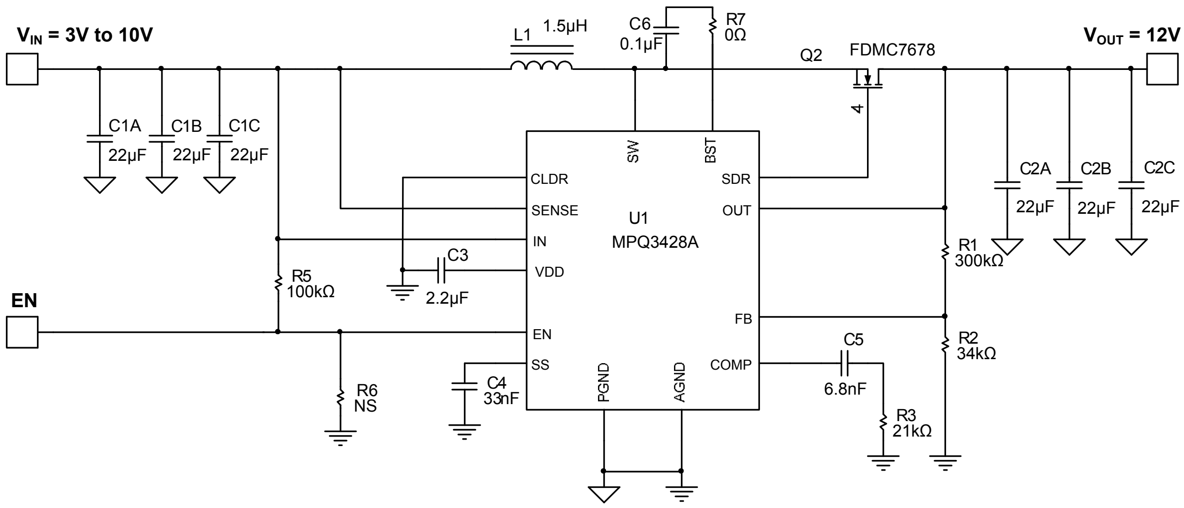


Figure 7: 12V Output Synchronous Solution Using an Internal Current-Sensing Circuit

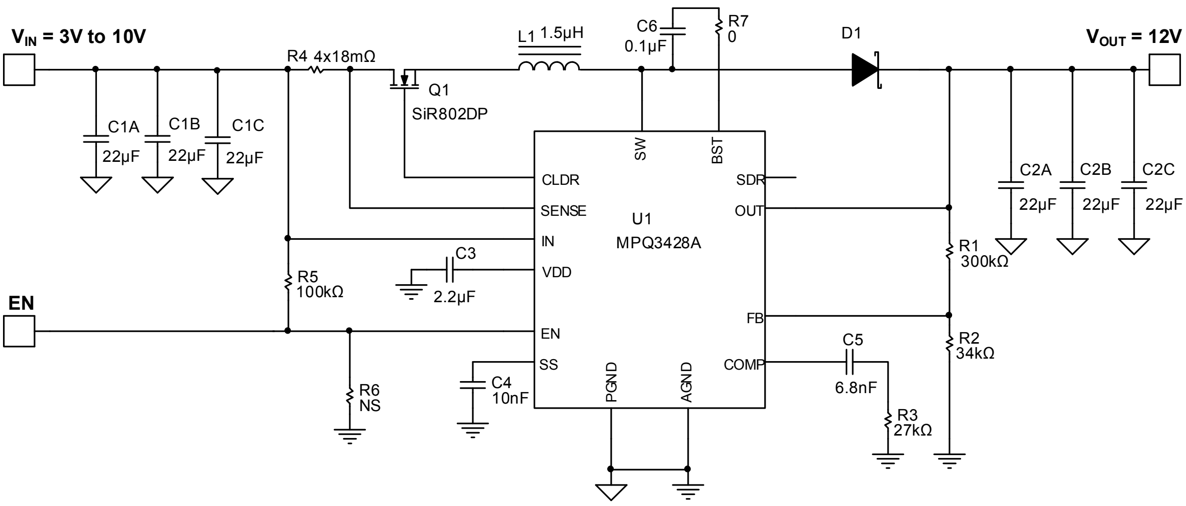


Figure 8: 12V Output Non-Synchronous Solution with Input Disconnect Function

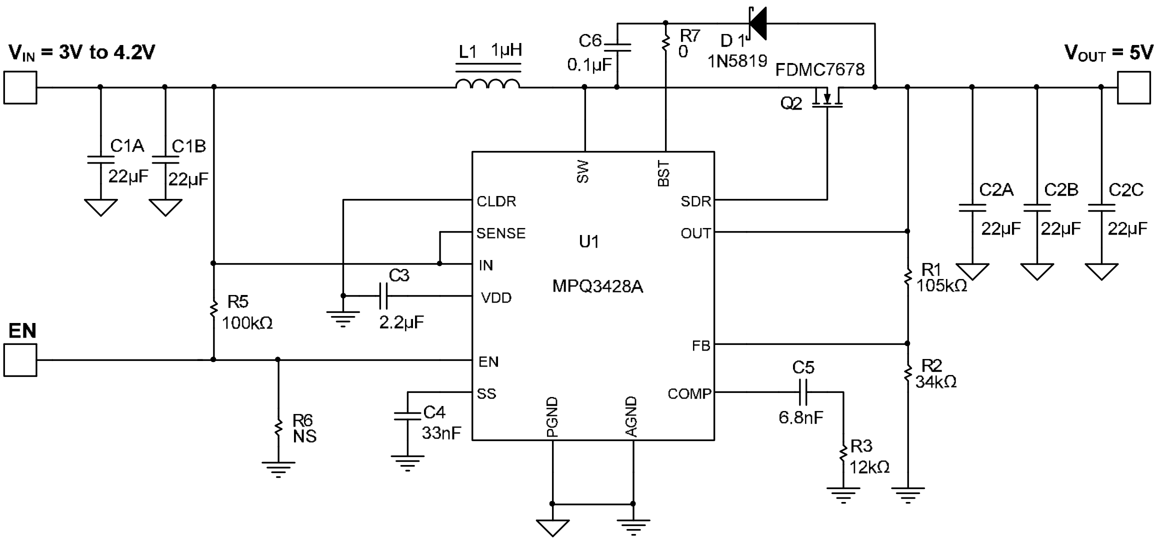
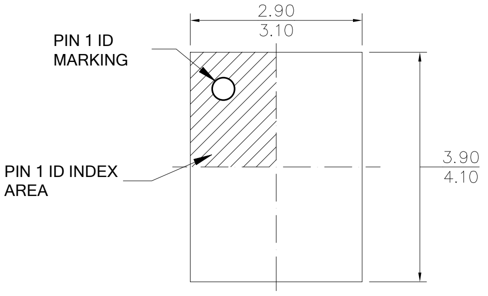


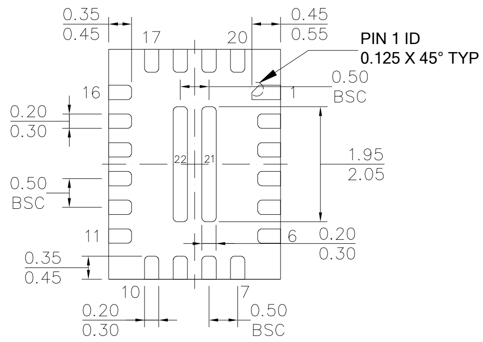
Figure 9: 5V Output Synchronous Solution Using Internal Current-Sensing Circuit

PACKAGE INFORMATION

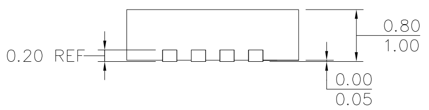
QFN-22 (3mmx4mm)



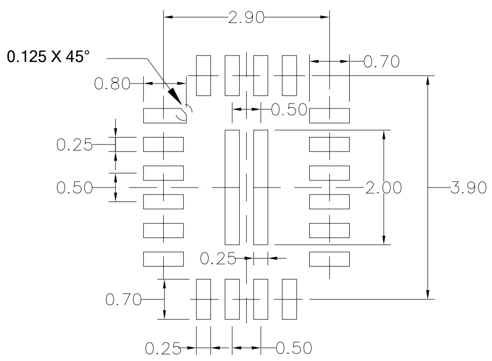
TOP VIEW



BOTTOM VIEW



SIDE VIEW

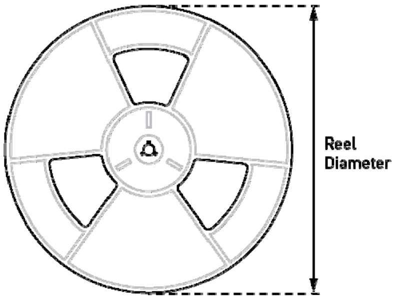


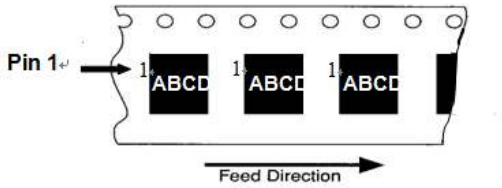
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/Reel	Quantity/Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ3428AGL–Z	QFN 3x4	5000	N/A	13 in.	12mm	8mm