FAIRCHILD

SEMICONDUCTOR®

February 2007

FAN7382
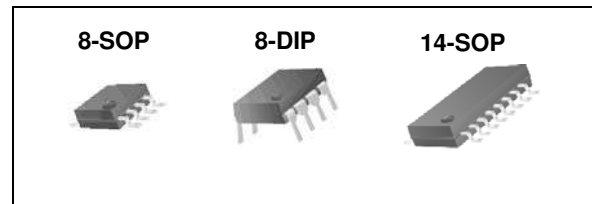# High- and Low-Side Gate Driver

Features

- Floating Channels Designed for Bootstrap Operation to +600V
- Typically 350mA/650mA Sourcing/Sinking Current Driving Capability for Both Channels
- Common-Mode dv/dt Noise Canceling Circuit
- Extended Allowable Negative V_S Swing to -9.8V for Signal Propagation at $V_{CC}=V_{BS}=15V$
- V_{CC} & V_{BS} Supply Range from 10V to 20V
- UVLO Functions for Both Channels
- TTL Compatible Input Logic Threshold Levels
- Matched Propagation Delay Below 50nsec
- Output In-phase with Input Signal

Applications

- PDP Scan Driver
- Fluorescent Lamp Ballast
- SMPS
- Motor Driver

Description

The FAN7382, a monolithic high and low side gate-drive IC, can drive MOSFETs and IGBTs that operate up to +600V. Fairchild's high-voltage process and common-mode noise canceling technique provides stable operation of the high-side driver under high-dv/dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to V_S=-9.8V (typical) for V_{BS}=15V. The input logic level is compatible with standard TTL-series logic gates. UVLO circuits for both channels prevent malfunction when V_{CC} or V_{BS} is lower than the specified threshold voltage. Output drivers typically source/sink 350mA/650mA, respectively, which is suitable for fluorescent lamp ballasts, PDP scan drivers, motor controls, etc.

8-SOP	8-DIP	14-SOP

Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Packing Method
FAN7382N	8-DIP			Tube
FAN7382M[1]	8-SOP			Tube
FAN7382MX[1]		Yes	-40°C ~ 125°C	Tape & Reel
FAN7382M1[1]	14-SOP			Tube
FAN7382M1X[1]				Tape & Reel

Note:

1. These devices passed wave soldering test by JESD22A-111.

Typical Application Circuit

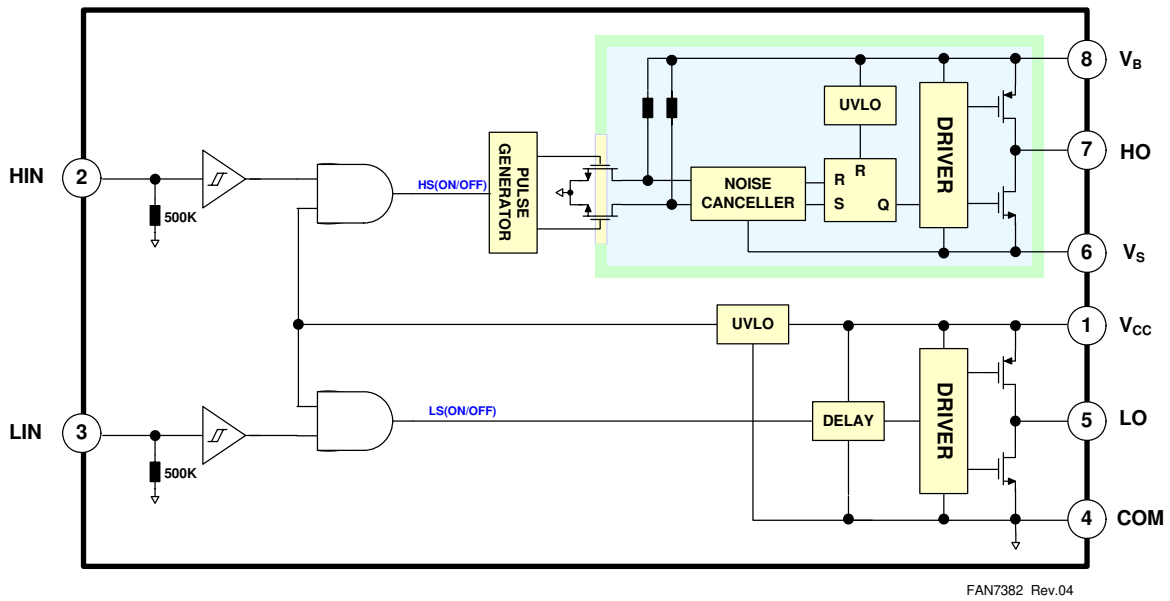FAN7382 Rev.05
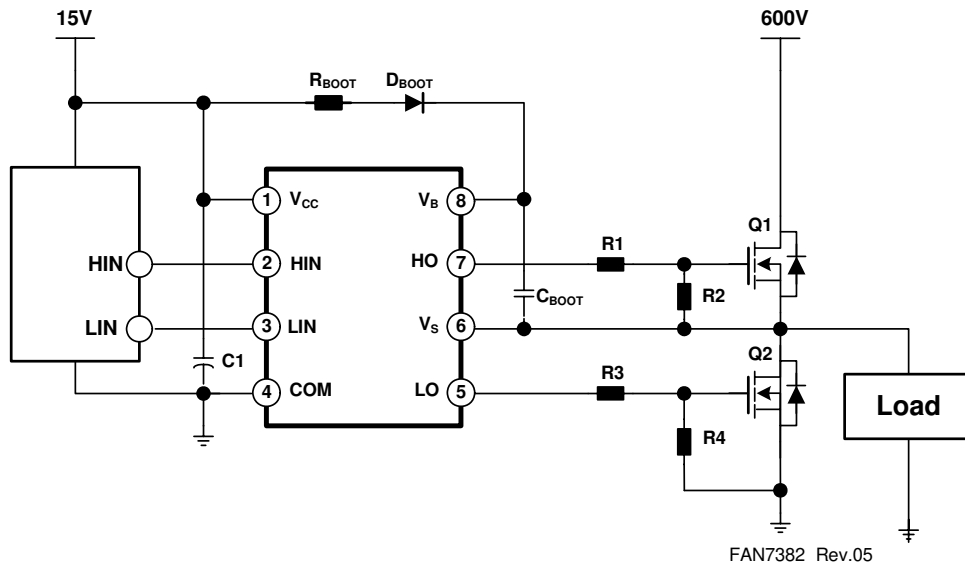
Figure 1. Application Circuit for Half-Bridge

Internal Block Diagram

FAN7382 Rev.04

Figure 2. Functional Block Diagram

Pin Assignments

FAN7382N
FAN7382M

V_{CC}	1		8	V_B
HIN	2		7	HO
LIN	3		6	V_S
COM	4		5	LO

FAN7382 Rev.05

FAN7382M1

V_{CC}	1		14	NC
HIN	2		13	V_B
LIN	3		12	HO
NC	4		11	V_S
NC	5		10	NC
COM	6		9	NC
LO	7		8	NC

FAN7382 Rev.01
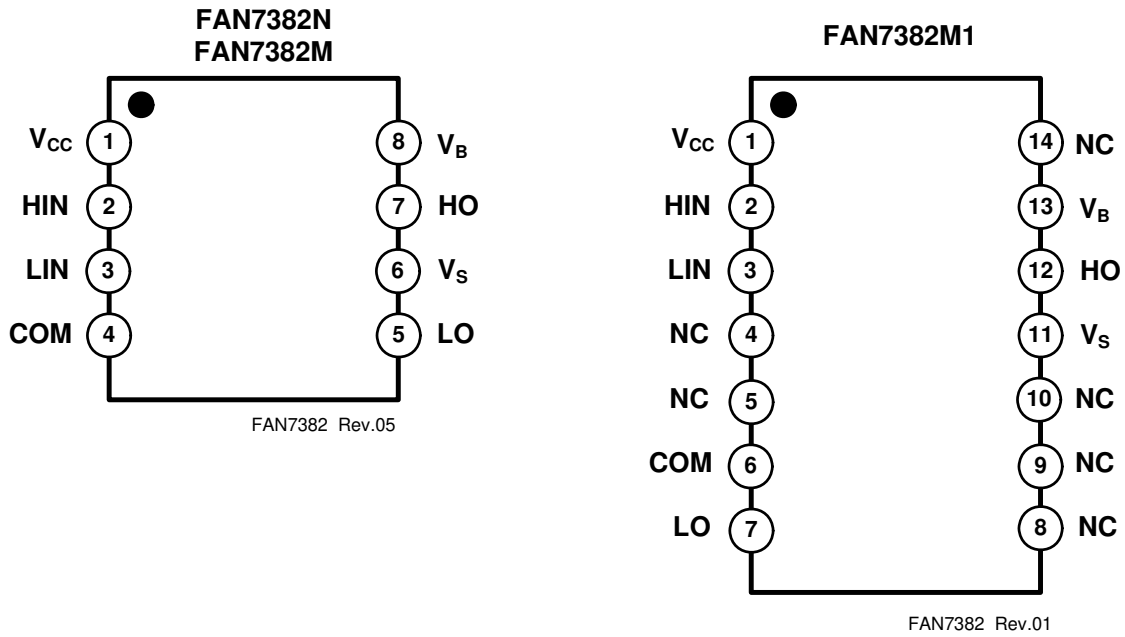
Figure 3. Pin Configuration (Top View)

Pin Definitions

Name	Description
V_{CC}	Low-Side Supply Voltage
HIN	Logic Input for High-Side Gate Driver Output
LIN	Logic Input for Low-Side Gate Driver Output
COM	Logic Ground and Low-Side Driver Return
LO	Low-Side Driver Output
V_S	High-Voltage Floating Supply Return
HO	High-Side Driver Output
V_B	High-Side Floating Supply

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Characteristics	Min.	Max.	Unit
V_S	High-side offset voltage	V_B-25	V_B+0.3	
V_B	High-side floating supply voltage	-0.3	625	
V_{HO}	High-side floating output voltage HO	V_S-0.3	V_B+0.3	
V_{CC}	Low-side and logic fixed supply voltage	-0.3	25	V
V_{LO}	Low-side output voltage LO	-0.3	V_{CC}+0.3	
V_{IN}	Logic input voltage (HIN, LIN)	-0.3	V_{CC}+0.3	
COM	Logic ground	V_{CC}-25	V_{CC}+0.3	
dV_S/dt	Allowable offset voltage slew rate		50	V/ns
P_D[2][3][4]	Power dissipation	8-SOP	0.625	W
		14-SOP	1.0	
		8-DIP	1.2	
θ_{JA}	Thermal resistance, junction-to-ambient	8-SOP	200	°C/W
		14-SOP	110	
		8-DIP	100	
T_J	Junction temperature		150	°C
T_{STG}	Storage temperature		150	°C

Notes:

2. Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).

3. Refer to the following standards:

   JESD51-2: Integral circuits thermal test method environmental conditions - natural convection

   JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages

4. Do not exceed P_D under any circumstances.

Recommended Operating Ratings

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_B	High-side floating supply voltage	V_S+10	V_S+20	
V_S	High-side floating supply offset voltage	6-V_{CC}	600	
V_{HO}	High-side (HO) output voltage	V_S	V_B	V
V_{LO}	Low-side (LO) output voltage	COM	V_{CC}	
V_{IN}	Logic input voltage (HIN, LIN)	COM	V_{CC}	
V_{CC}	Low-side supply voltage	10	20	
T_A	Ambient temperature	-40	125	°C

Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS})=15.0V, T_A = 25°C, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S and COM and are applicable to the respective outputs HO and LO.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply under-voltage positive going threshold		8.2	9.2	10.0	V
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply under-voltage negative going threshold		7.6	8.7	9.6	
V_{CCUVH} V_{BSUVH}	V_{CC} supply under-voltage lockout hysteresis			0.6		
I_{LK}	Offset supply leakage current	$V_B=V_S$=600V			50	
I_{QBS}	Quiescent V_{BS} supply current	V_{IN}=0V or 5V		45	120	µA
I_{QCC}	Quiescent V_{CC} supply current	V_{IN}=0V or 5V		70	180	
I_{PBS}	Operating V_{BS} supply current	f_{IN}=20kHz,rms value			600	µA
I_{PCC}	Operating V_{CC} supply current	f_{IN}=20kHz,rms value			600	
V_{IH}	Logic "1" input voltage		2.9			V
V_{IL}	Logic "0" input voltage				0.8	
V_{OH}	High-level output voltage, V_{BIAS}-V_O	I_O=20mA			1.0	
V_{OL}	Low-level output voltage, V_O				0.6	
I_{IN+}	Logic "1" input bias current	V_{IN}=5V		10	20	µA
I_{IN-}	Logic "0" input bias current	V_{IN}=0V		1.0	2.0	
I_{O+}	Output high short-circuit pulsed current	V_O=0V, V_{IN}=5V with PW<10µs	250	350		mA
I_{O-}	Output low short-circuit pulsed current	V_O=15V, V_{IN}=0V with PW<10µs	500	650		
V_S	Allowable negative V_S pin voltage for HIN signal propagation to HO			-9.8	-7.0	V

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS})=15.0V, V_S=COM, C_L=1000pF and, T_A = 25°C, unless otherwise specified.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	V_S=0V	100	170	300	ns
t_{off}	Turn-off propagation delay	V_S=0V or 600V[5]	100	200	300	
t_r	Turn-on rise time		20	60	140	
t_f	Turn-off fall time			30	80	
MT	Delay matching, HS & LS turn-on/off				50	

Note:

5. This parameter guaranteed by design.

Typical Characteristics
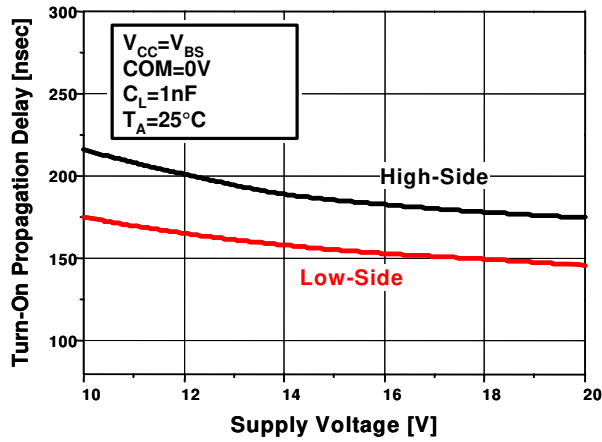
Figure 4. Turn-On Propagation Delay vs. Supply Voltage
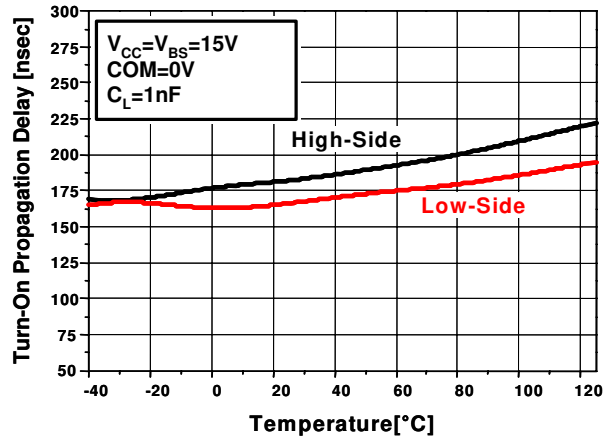

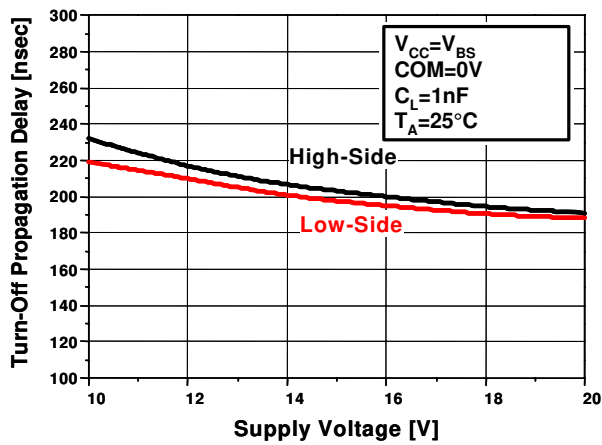Figure 5. Turn-On Propagation Delay vs. Temp.

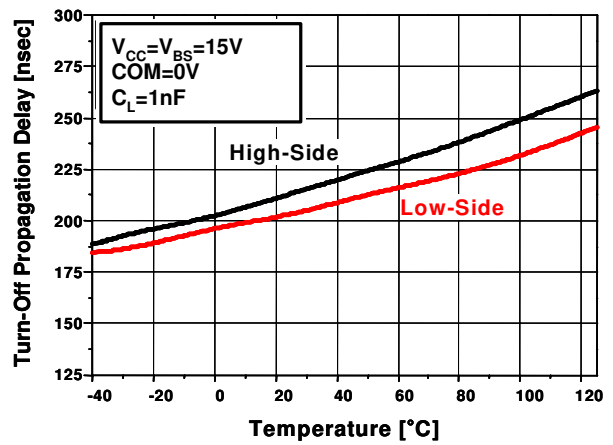Figure 6. Turn-Off Propagation Delay vs. Supply Voltage
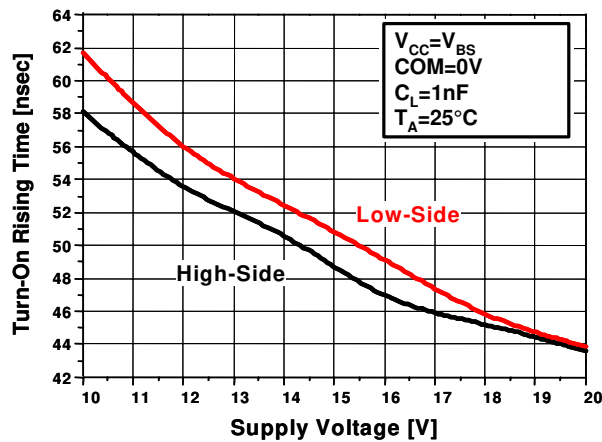

Figure 7. Turn-Off Propagation Delay vs. Temp.
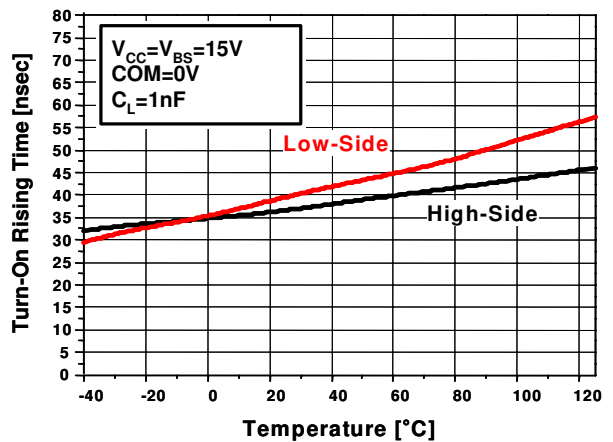

Figure 8. Turn-On Rising Time vs. Supply Voltage
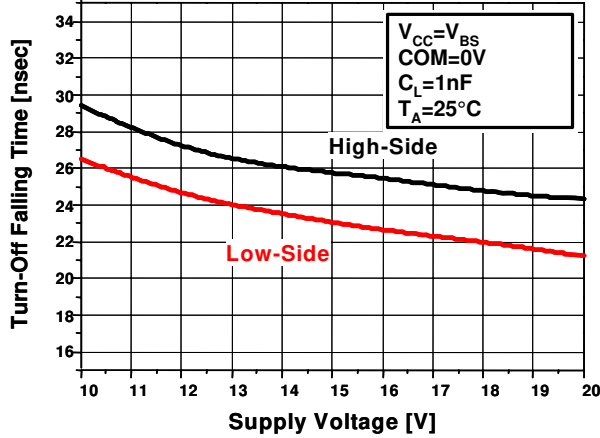

Figure 9. Turn-On Rising Time vs. Temp.

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Typical Characteristics (Continued)

Figure 10. Turn-Off Falling Time vs. Supply Voltage
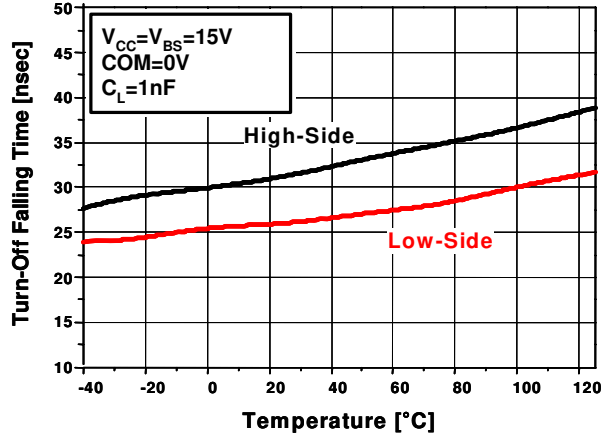
Figure 11. Turn-Off Falling Time vs. Temp.
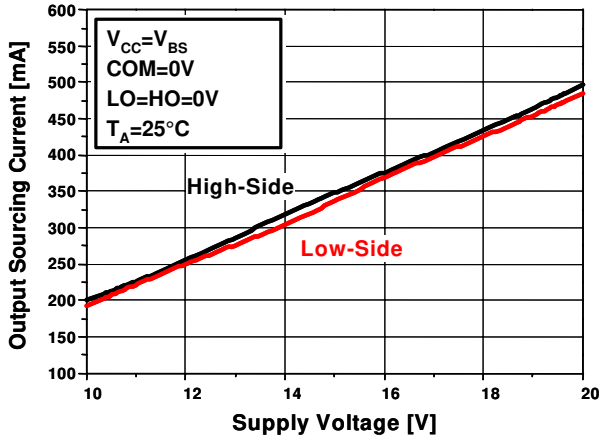
Figure 12. Output Sourcing Current vs. Supply Voltage
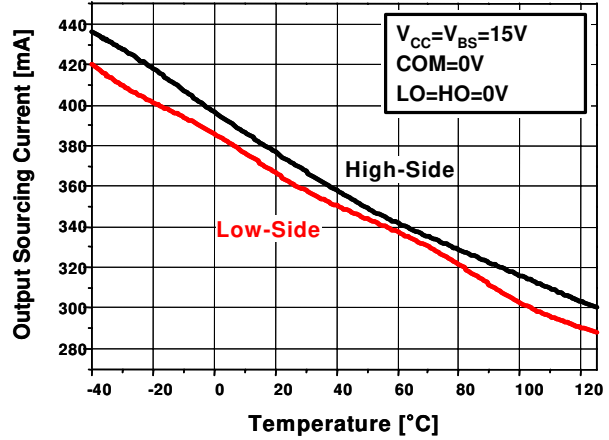
Figure 13. Output Sourcing Current vs. Temp
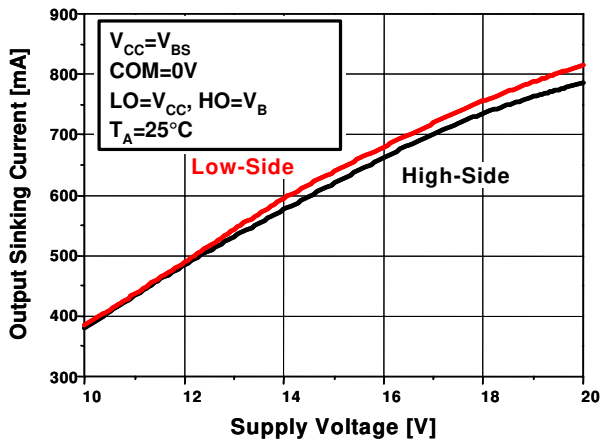
Figure 14. Output Sinking Current vs. Supply Voltage
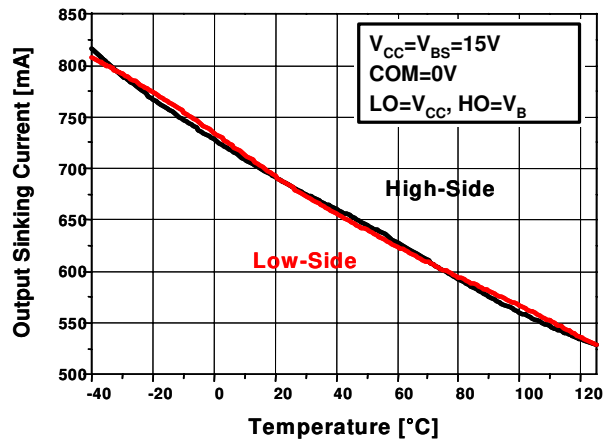
Figure 15. Output Sinking Current vs. Temp.

Typical Characteristics (Continued)
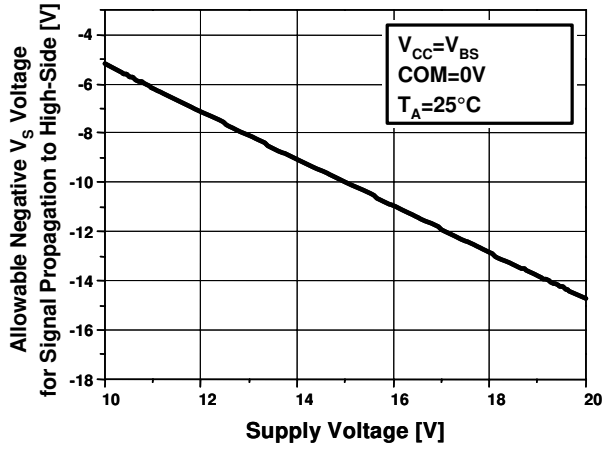
Figure 16. Allowable Negative V$_S$ Voltage for Signal Propagation to High Side vs. Supply Voltage
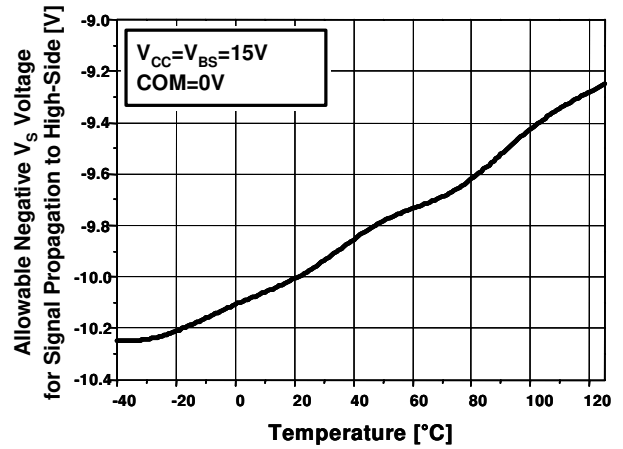
Figure 17. Allowable Negative V$_S$ Voltage for Signal Propagation to High Side vs. Temp.
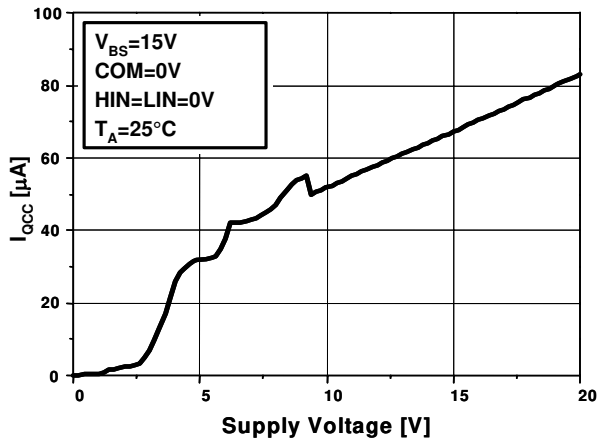
Figure 18. I$_{QCC}$ vs. Supply Voltage
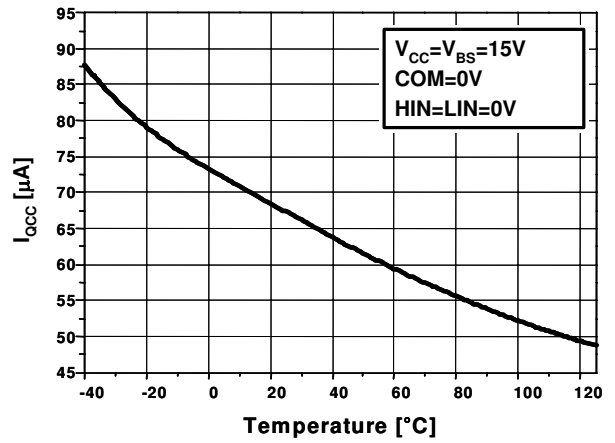
Figure 19. I$_{QCC}$ vs. Temp.
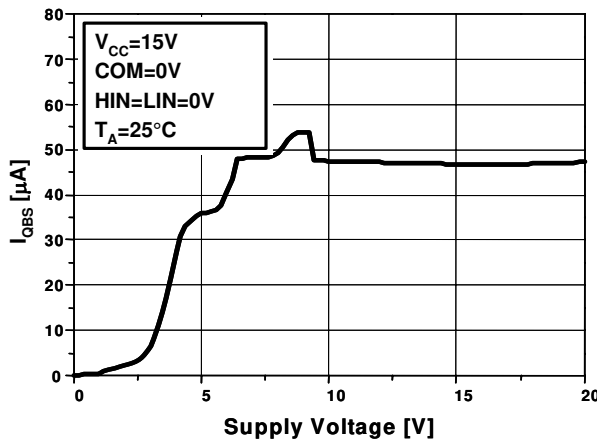
Figure 20. I$_{QBS}$ vs. Supply Voltage
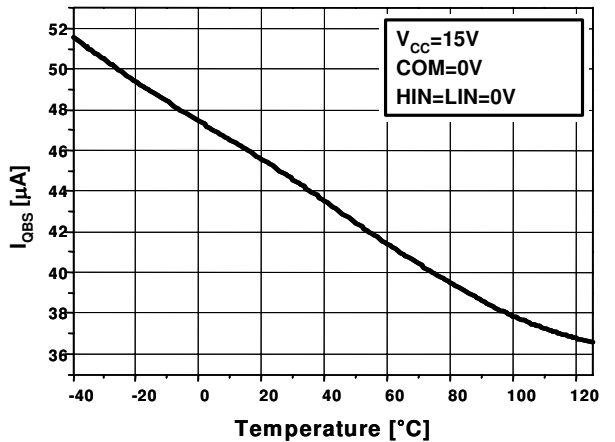
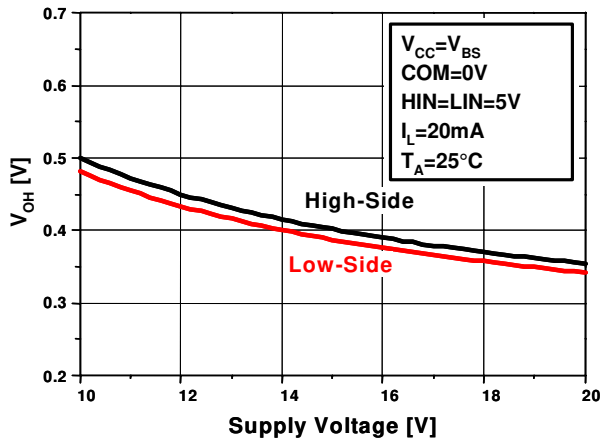Figure 21. I$_{QBS}$ vs. Temp.

Typical Characteristics (Continued)

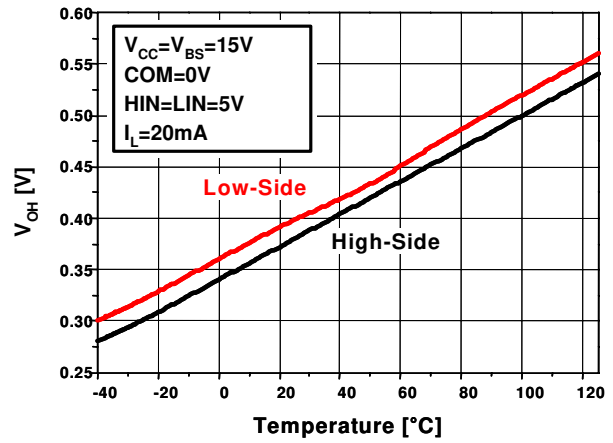**Figure 22. High-Level Output Voltage vs. Supply Voltage**

$V_{CC}=V_{BS}$
COM=0V
HIN=LIN=5V
I_L=20mA
T_A=25°C

High-Side
Low-Side

Figure 23. High-Level Output Voltage vs. Temp.

$V_{CC}=V_{BS}$=15V
COM=0V
HIN=LIN=5V
I_L=20mA

Low-Side
High-Side
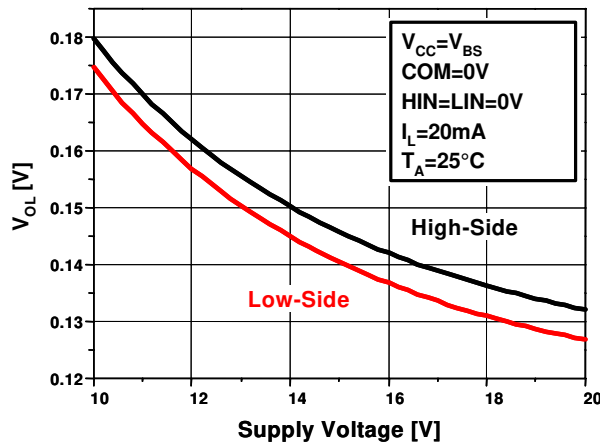
Figure 24. Low-Level Output Voltage vs. Supply Voltage

$V_{CC}=V_{BS}$
COM=0V
HIN=LIN=0V
I_L=20mA
T_A=25°C

High-Side
Low-Side
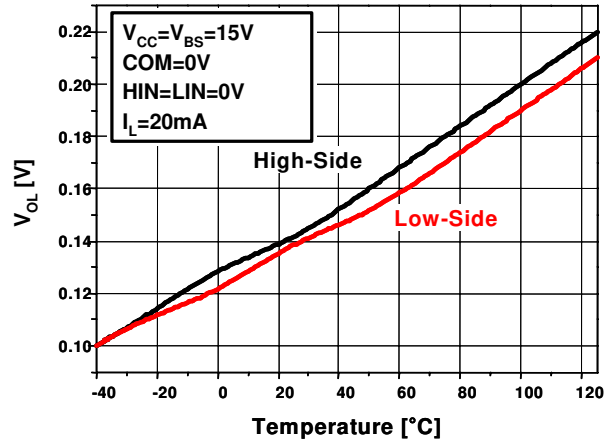
Figure 25. Low-Level Output Voltage vs. Temp.

$V_{CC}=V_{BS}$=15V
COM=0V
HIN=LIN=0V
I_L=20mA

High-Side
Low-Side
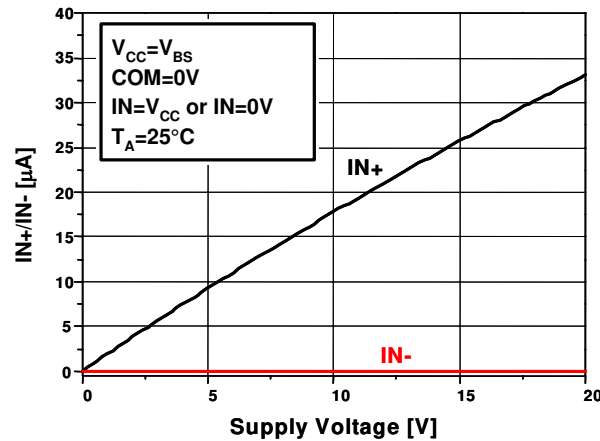
Figure 26. Input Bias Current vs. Supply Voltage

$V_{CC}=V_{BS}$
COM=0V
IN=V_{CC} or IN=0V
T_A=25°C

IN+
IN-

Figure 27. Input Bias Current vs. Temp.

HIN=LIN=5V

LIN
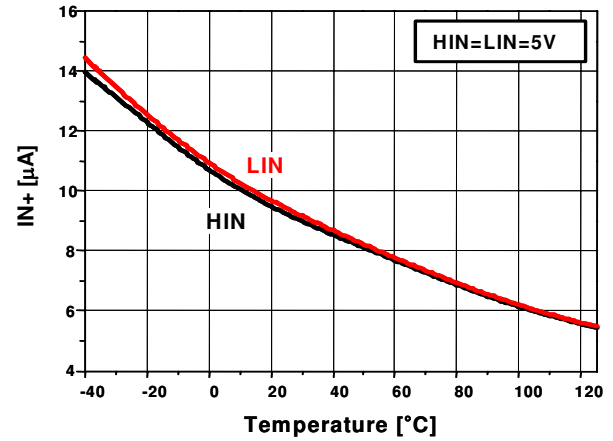HIN

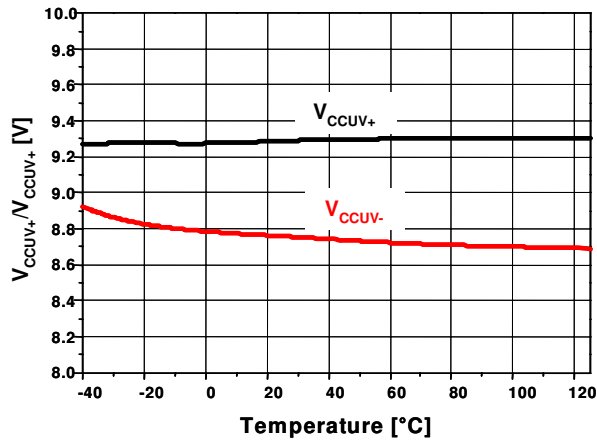## Typical Characteristics (Continued)

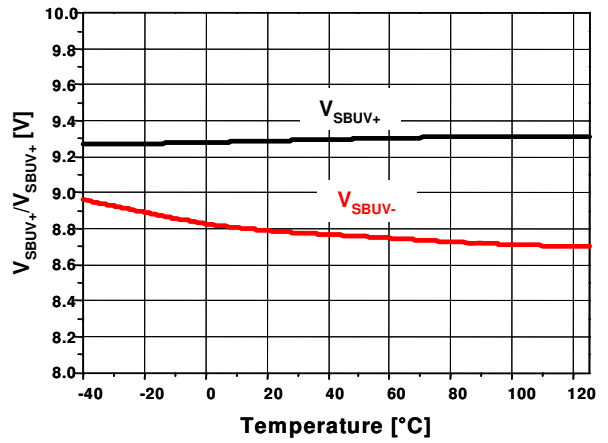Figure 28. V$_{CC}$ UVLO Threshold Voltage vs. Temp.
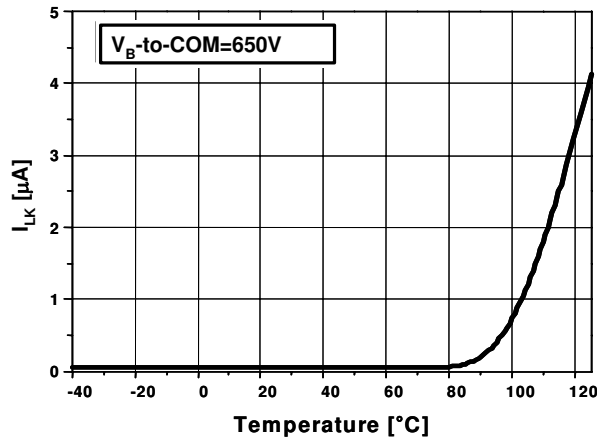

Figure 29. V$_{BS}$ UVLO Threshold Voltage vs. Temp.
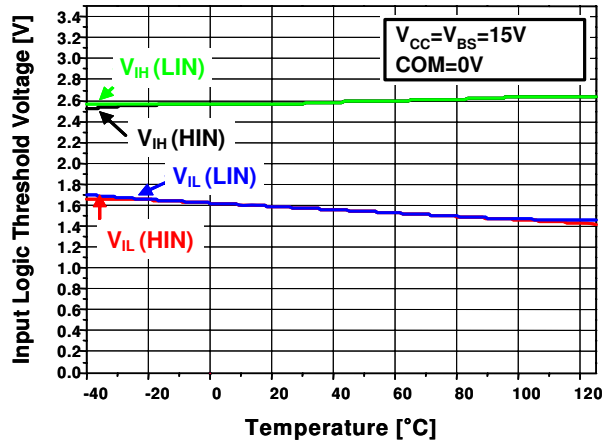

Figure 30. V$_B$ to COM Leakage Current vs. Temp.

Figure 31. Input Logic Threshold Voltage vs. Temp.
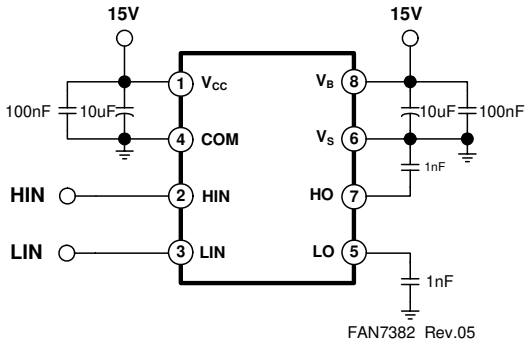
Typical Characteristics (Continued)
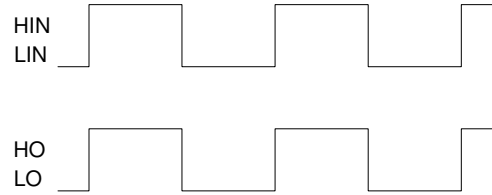

FAN7382 Rev.05

Figure 32. Switching Time Test Circuit

FAN7382 Rev.03

Figure 33. Input / Output Timing Diagram

t_{on} : Turn-on Delay Time
t_{off} : Turn-off Delay Time
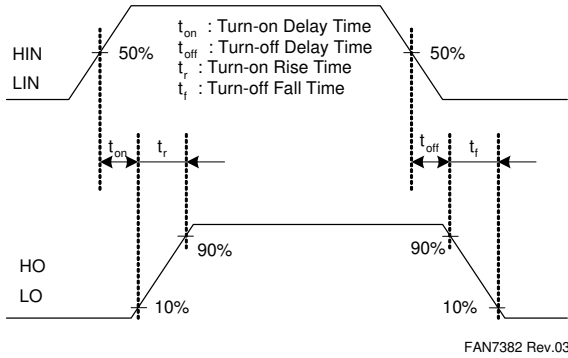t_r : Turn-on Rise Time
t_f : Turn-off Fall Time

FAN7382 Rev.03

Figure 34. Switching Time Waveform Definition

FAN7382 Rev.03
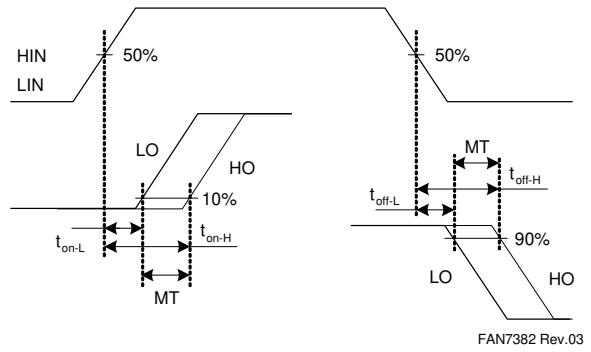
Figure 35. Delay Matching Waveform Definition

9.83
9.00

8

5

6.670
6.096

1

4

TOP VIEW

(0.56)

1.65
1.27

5.08 MAX

3.683
3.200

0.33 MIN

3.60
3.00

2.54

0.560
0.355

7.62

FRONT VIEW

8.255
7.610

7.62

0.356
0.200

15°
0°

9.957
7.870

SIDE VIEW
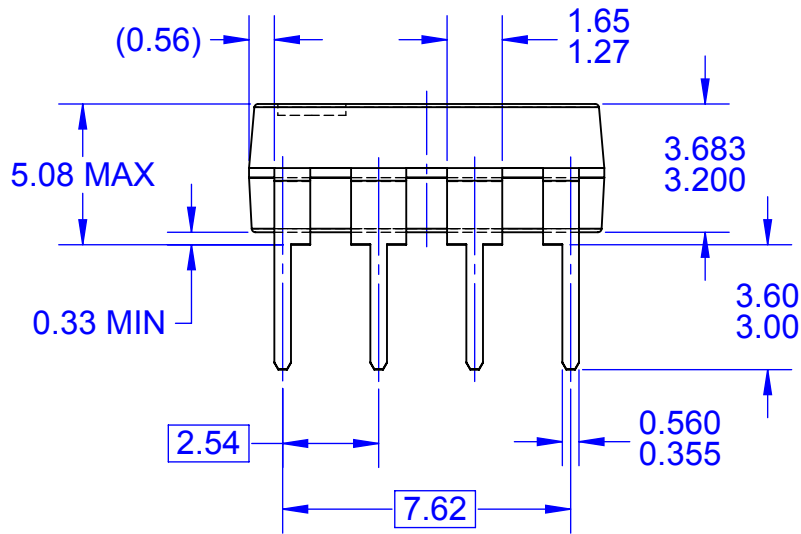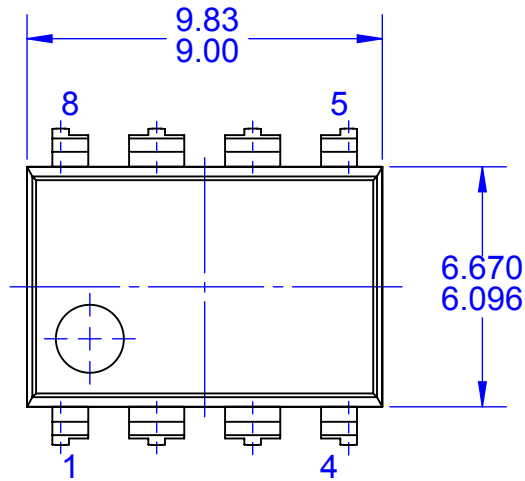
NOTES:
A. CONFORMS TO JEDEC MS-001, VARIATION BA
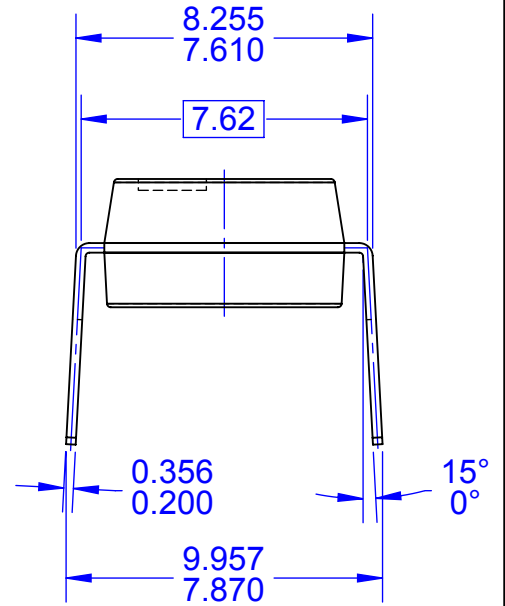B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS,
   MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONS AND TOLERANCES PER ASME
   Y14.5M-2009
E. DRAWING FILENAME: MKT-N08Frev3

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TOP VIEW

$\overset{C}{\triangle}$ $\overset{5.12}{4.72}$ [A]
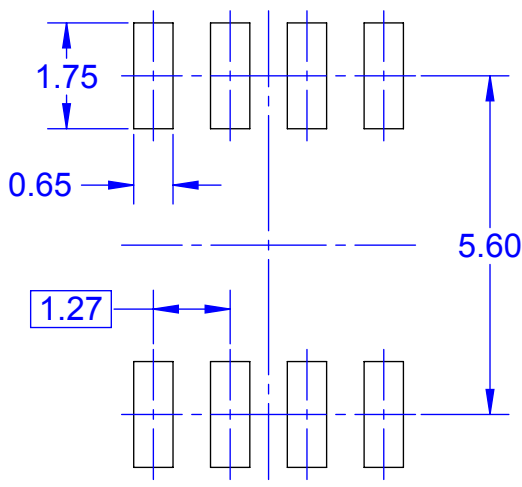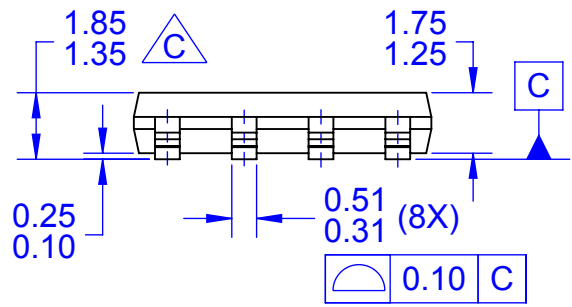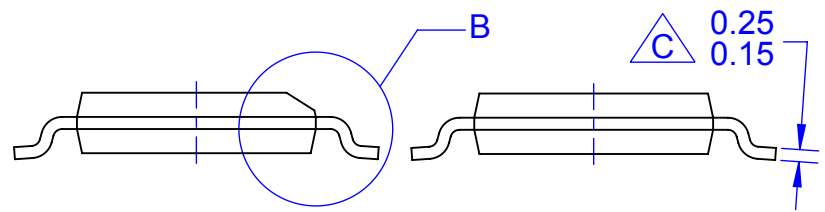
(0.35)

8   5   [B]

$\overset{6.30}{5.70}$ $\overset{4.15}{3.75}$

1   4

PIN #1 ID

1.27

$\oplus$ | 0.25 Ⓜ | C | B | A
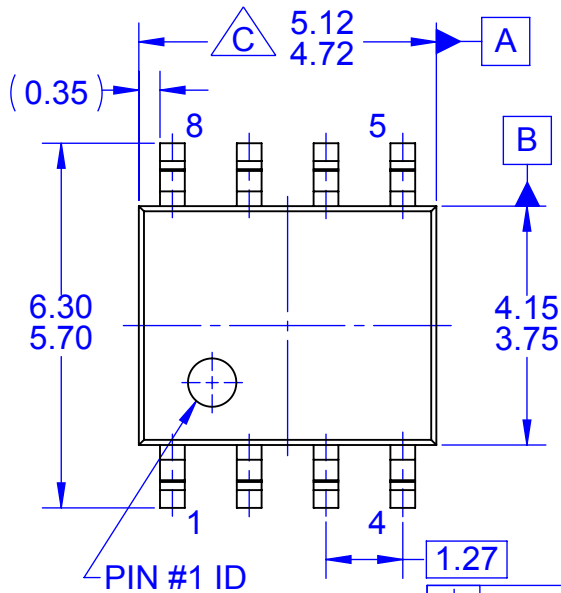
LAND PATTERN RECOMMENDATION

1.75

0.65

1.27

5.60

FRONT VIEW

$\overset{1.85}{1.35}$ $\overset{C}{\triangle}$ $\overset{1.75}{1.25}$ [C]

$\overset{0.25}{0.10}$ $\overset{0.51}{0.31}$ (8X)

$\cap$ | 0.10 | C

SIDE VIEW

B

$\overset{C}{\triangle}$ $\overset{0.25}{0.15}$

OPTION A
BEVEL EDGE

OPTION B
NON-BEVEL EDGE

DETAIL "B"
SCALE 2:1

GAGE
PLANE   BEVEL   R0.10

0.25

8°
4°

SEATING
PLANE

0.80
0.30

(1.04)

NOTES: UNLESS OTHERWISED SPECIFIED

A.   THIS PACKAGE CONFORMS TO JEDEC
       MS-012 VARIATION A EXCEPT WHERE NOTED.
B.   ALL DIMENSIONS ARE IN MILLIMETERS

$\overset{C}{\triangle}$ OUT OF JEDEC STANDARD VALUE

D.   DIMENSIONS ARE EXCLUSIVE OF BURRS,
       MOLD FLASH AND TIE BAR EXTRUSIONS.
E.   LAND PATTERN AS PER IPC
       SOIC127P600X175-8M
F.   DRAWING FILENAME: MKT-M08Brev2

FAIRCHILD ™

TOP VIEW

8.76
8.36

7.62

0.65

1.70

1.27

5.60

A

B

6.00

4.20
3.75

1.27

PIN #1 ID

14

8

1

7

(0.27)

SIDE VIEW

E
1.80 MAX

C

0.25
0.05

E

0.10 C

ALL LEAD TIPS

1.65
1.25

0.51
0.36

0.20 Ⓜ C A B

END VIEW

CHAMFER OPTIONAL

A

0.30
0.15

E

DETAIL "A"
SCALE 2:1

GAUGE
PLANE

SEATING
PLANE

0.36

0°~5°

0.90
0.45

(1.04)
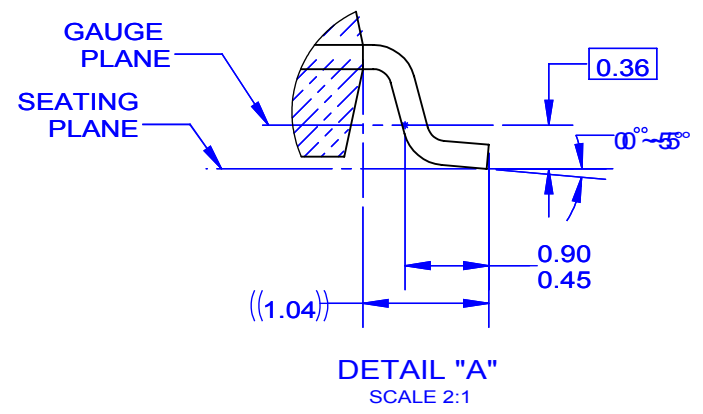
NOTES: UNLESS OTHERWISE SPECIFIED

A. THIS PACKAGE REFERENCE TO JEDEC MS-012
   VARIATION AB.
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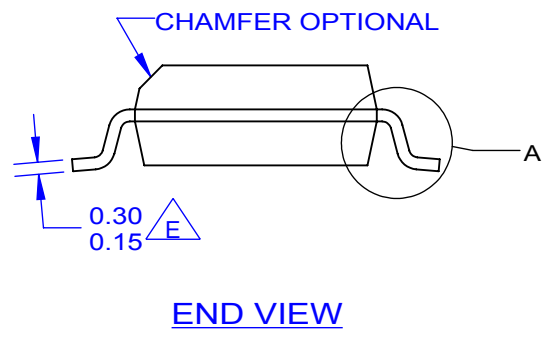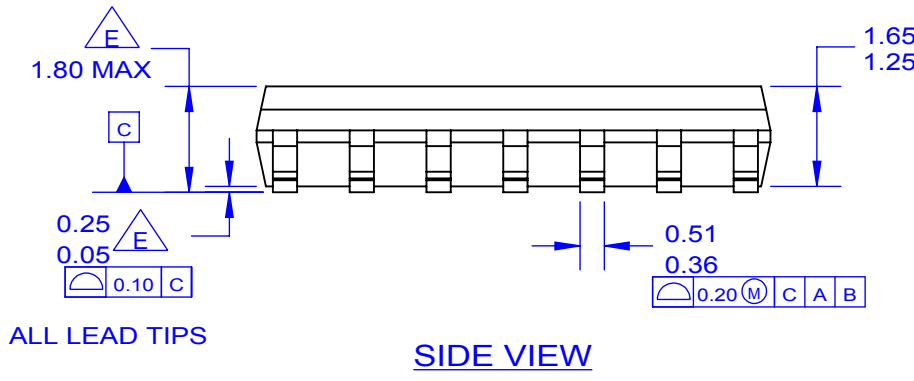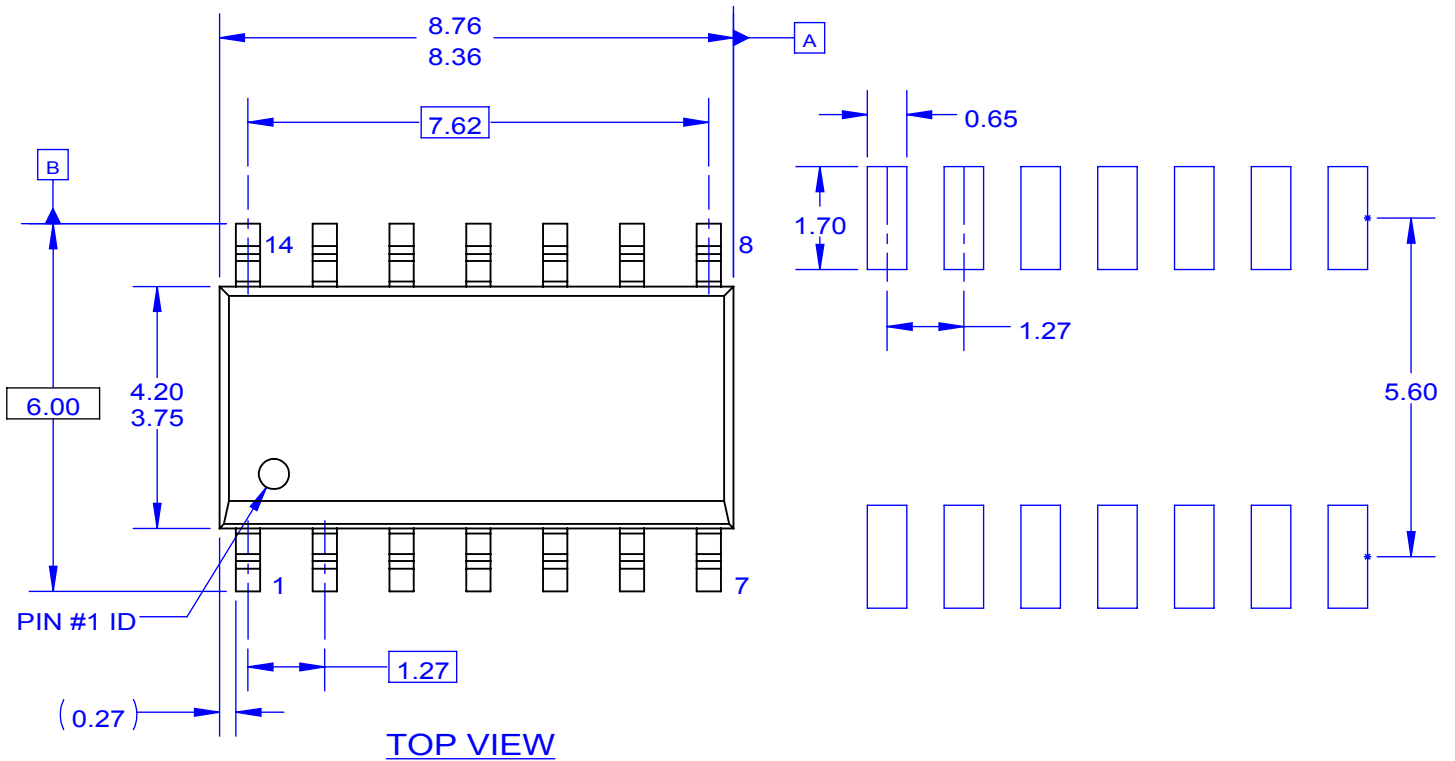E. OUT OF JEDEC STANDARD VALUE.
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G. FILE NAME: MKT-M14C REV2

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