Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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COMPOUND FIELD EFFECT POWER TRANSISTOR μ PA1556A

N-CHANNEL POWER MOS FET ARRAY SWITCHING TYPE

DESCRIPTION

The $\mu PA1556A$ is N-channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

FEATURES

- 4 V driving is possible
- Large Current and Low On-state Resistance

 $ID(pulse) = \pm 20 A$

RDS(on) = 0.20Ω TYP. (Vgs = 10 V)

RDS(on) = 0.25Ω TYP. (Vgs = 4 V)

- Low Capacitance Ciss = 700 pF TYP.
- Gate Protecter built in.
- 2.54 mm Pitch (0.1 inch)

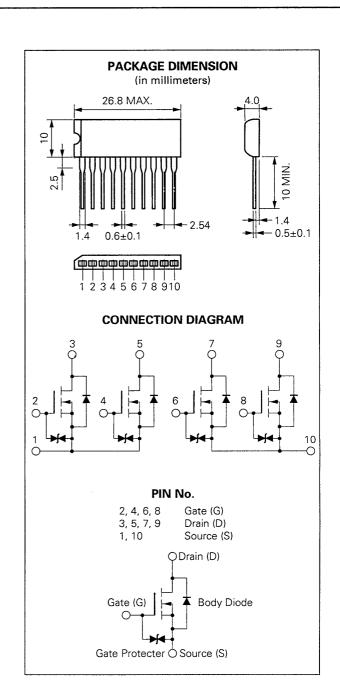
ORDERING INFORMATION

Part Number	Package	Quality Grade		
μPA1556AH	10 Pin SIP	Standard		

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

	Drain to Source Voltage	Voss	100	V
	Gate to Source Voltage (AC)	Vgss	±20	V
	Gate to Source Voltage (DC)	Vgss	+20,-10	V
	Drain Current (DC)	ID(DC)	±5.0	A/unit
	Drain Current (pulse)	ID(pulse)	* ±20	A/unit
	Total Power Dissipation (4 circ	uits)		
	<tc 25="" =="" °c=""></tc>	PT1	28	W
	Total Power Dissipation (4 circ	uits)		
	<Ta = 25 °C $>$	P _{T2}	3.5	W
	Storage Temperature	T _{stg}	-55 to +150) °C
	Junction Temperature	T_j	150	°C
*	PW ≤ 10 μ s, Duty Cycle ≤ 1 %			



ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Drain Leakage Current	loss			10	μΑ	V _{DS} = 100 V, V _{GS} = 0	
Gate to Source Leakage Current	lgss			±10	μΑ	V _G S = ±20 V, V _D S = 0	
Gate to Source Cutoff Voltage	V _{GS(off)}	1.0		2.5	٧	Vps = 10 V, lp = 1 mA	
Forward Transfer Admittance	yfs	4.0			S	Vps = 10 V, Ip = 3 A	
Drain to Source On-state Resistance	RDS(on)1		0.20	0.25	Ω	Vgs = 10 V, ID = 3 A	
Drain to Source On-state Resistance	RDS(on)2		0.25	0.33	Ω	Vgs = 4 V, ID = 3 A	
Input Capacitance	Ciss		700		pF	V _{DS} = 10 V V _{GS} = 0 f = 1.0 MHz	
Output Capacitance	Coss		200		pF		
Reverse Transfer Capacitance	Crss		30		pF		
Turn-On Delay Time	td(on)		35		ns	Io = 3 A	
Rise Time	tr		60		ns	$V_{GS} = 10 \text{ V}$ $V_{CC} = 50 \text{ V}$ $R_L = 17 \Omega$, $R_{in} = 10 \Omega$ See Fig. 1	
Turn-Off Delay Time	td(off)		800		ns		
Fall Time	tf		200		ns		
Total Gate Charge	QG		17		nC	Vgs = 10 V lb = 5 A Vbb = 80 V See Fig. 2	
Gate to Source Charge	Qgs		2.5		nC		
Gate to Drain Charge	Qgp		4		nC		
Diode Forward Voltage	VF(S-D)		1.0		V	IF = 5 A, VGS = 0	
Reverse Recovery Time	trr		120		ns	lr = 5 A, Vgs = 0 di/dt = 50 A/µs	
Reverse Recovery Charge	Qrr		230		nC		

Fig. 1 Switching Time Test Circuit

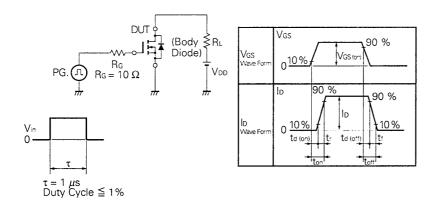
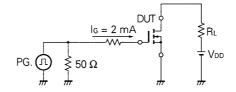
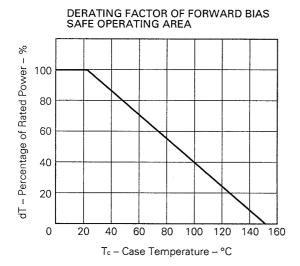
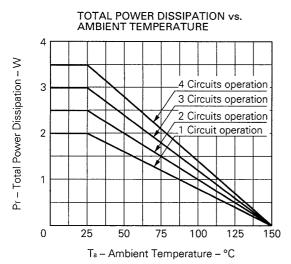


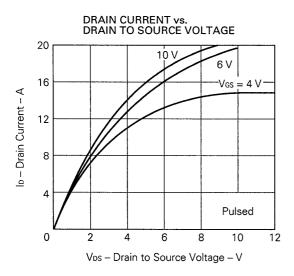
Fig. 2 Gate Charge Test Circuit

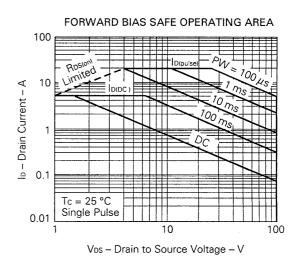


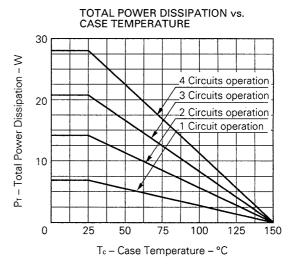
TYPICAL CHARACTERISTICS (Ta = 25 °C)

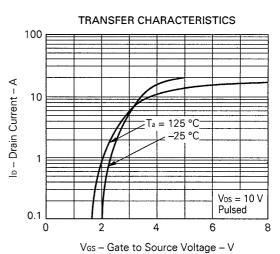


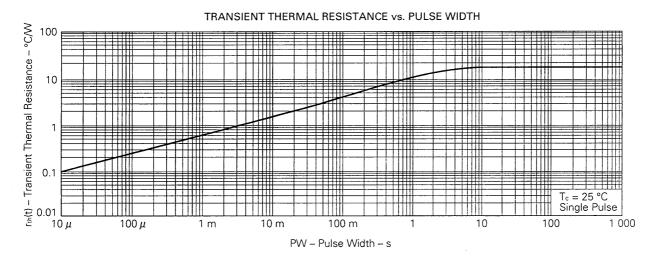


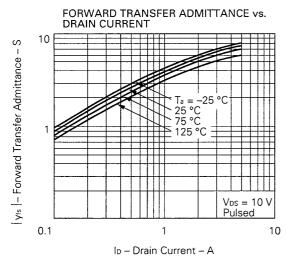


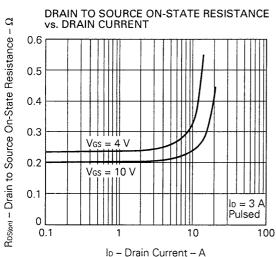


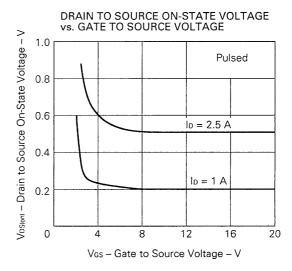


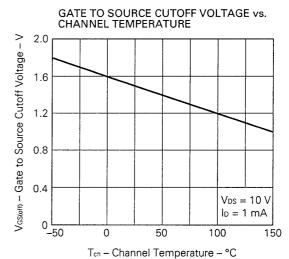


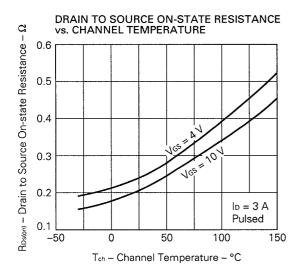


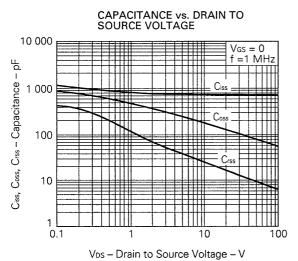


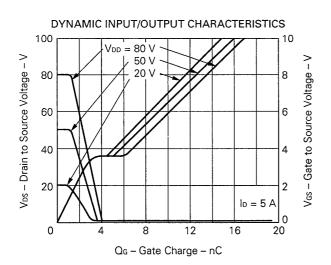


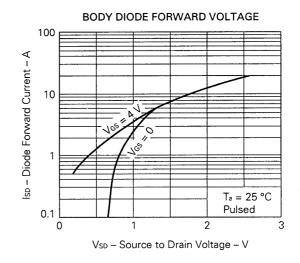


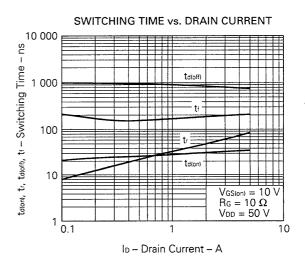


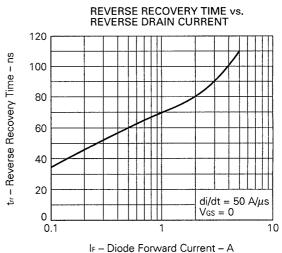














Reference

Document name	Document No.
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207
Safe operating area of Power MOS FET	TEA-1034
Appication circuit using Power MOS FET	TEA-1035

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