

Complete Data Sheet available via web, Harris' home page: <http://www.semi.harris.com> or via Harris AnswerFAX, see Section 17

CMOS, 10-Bit, A/D Converters with Internal Track and Hold

August 1997

Features

- CMOS Low Power (Typ).....15mW
- Single Supply Voltage3V to 6V
- Conversion Time13 μ s
- Built-In Track and Hold
- Rail-to-Rail Input Range
- Latched Three-state Output Drivers
- Microprocessor-Compatible Control Lines
- Internal or External Clock

Applications

- Fast, No-Droop, Sample and Hold
- Voice Grade Digital Audio
- DSP Modems
- Remote Low Power Data Acquisition Systems
- μ P Controlled Systems

Description

The Harris CA3310 is a fast, low power, 10-bit successive approximation analog-to-digital converter, with microprocessor-compatible outputs. It uses only a single 3V to 6V supply and typically draws just 3mA when operating at 5V. It can accept full rail-to-rail input signals, and features a built-in track and hold. The track and hold will follow high bandwidth input signals, as it has only a 100ns (typical) input time constant.

The ten data outputs feature full high-speed CMOS three-state bus driver capability, and are latched and held through a full conversion cycle. Separate 8 MSB and 2 LSB enables, a data ready flag, and conversion start and ready reset inputs complete the microprocessor interface.

An internal, adjustable clock is provided and is available as an output. The clock may also be driven from an external source.

Ordering Information

PART NUMBER	LINEARITY (INL, DNL)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3310E	± 0.75 LSB	-40 to 85	24 Ld PDIP	E24.6
CA3310AE	± 0.5 LSB	-40 to 85	24 Ld PDIP	E24.6
CA3310M	± 0.75 LSB	-40 to 85	24 Ld SOIC	M24.3
CA3310AM	± 0.5 LSB	-40 to 85	24 Ld SOIC	M24.3
CA3310D	± 0.75 LSB	-55 to 125	24 Ld SBDIP	D24.6
CA3310AD	± 0.5 LSB	-55 to 125	24 Ld SBDIP	D24.6

Pinout

CA3310, CA3310A
(PDIP, SBDIP, SOIC)
TOP VIEW

