HARRIS
SEMICONDUCTOR

HSP45256

Binary Correlator

Features

- **Reconfigurable 256 Stage Binary Correlator**
- **1-Bit Reference x 1, 2, 4, or 8-Bit Data**
- **Separate Control and Reference Interfaces**
- **25.6, 33MHz Versions**
- **Configurable for 1-D and 2-D Operation**
- **Double Buffered Mask and Reference**
- **Programmable Output Delay**
- **Cascadable**
- **Standard Microprocessor Interface**

Applications

- **Radar/Sonar**
- **Spread Spectrum Communications**
- **Pattern/Character Recognition**
- **Error Correction Coding**

Ordering Information

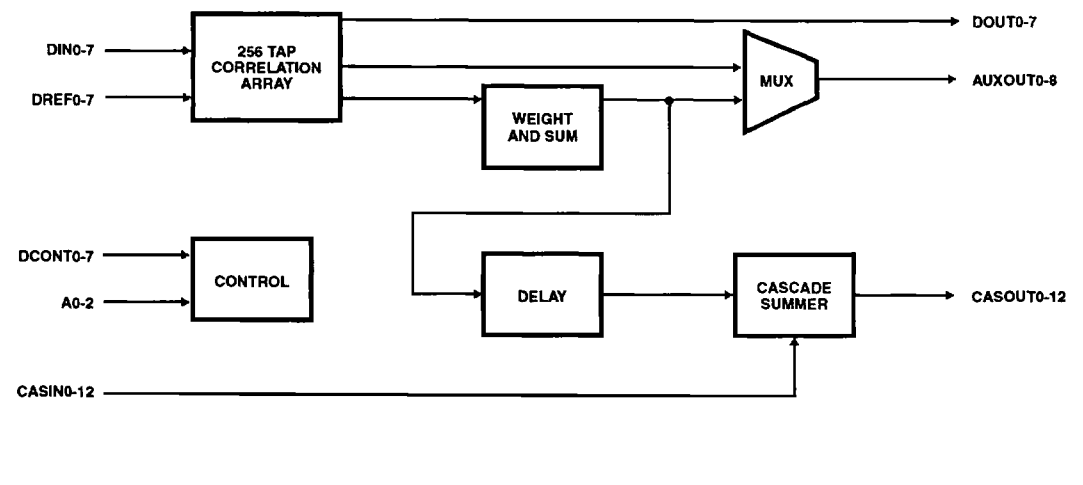| PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP45256JC-25	0°C to +70°C	84 Lead PLCC
HSP45256JC-33	0°C to +70°C	84 Lead PLCC
HSP45256GC-25	0°C to +70°C	85 Lead PGA
HSP45256GC-33	0°C to +70°C	85 Lead PGA

Description

The Harris HSP45256 is a high-speed, 256 tap binary correlator. It can be configured to perform one- or two-dimensional correlations of selectable data precision and length. Multiple HSP45256's can be cascaded for increased correlation length. Unused taps can be masked out for reduced correlation length.

The correlation array consists of eight 32-tap stages. These may be cascaded internally to compare 1, 2, 4 or 8-bit input data with a 1-bit reference. Depending on the number of bits in the input data, the length of the correlation can be up to 256, 128, 64, or 32 taps. The HSP45256 can also be configured as two separate correlators with window sizes from 4 by 32 to 1 by 128 each. The mask register can be used to prevent any subset of the 256 bits from contributing to the correlation score.

The output of the correlation array (correlation score) feeds the weight and sum logic, which gives added flexibility to the data format. In addition, an offset register is provided so that a preprogrammed value can be added to the correlation score. This result is then passed through a user programmable delay stage to the cascade summer. The delay stage simplifies the cascading of multiple correlators by compensating for the latency of previous correlators.

The Binary Correlator is configured by writing a set of control registers via a standard microprocessor interface. To simplify operation, both the control and reference registers are double buffered. This allows the user to load new mask and reference data while the current correlation is in progress.

7

SPECIAL FUNCTION

Block Diagram

File Number **2814.3**

Pinouts

85 PIN PGA — BOTTOM VIEW

85 PIN PGA — TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11
A	CASIN2	CASIN4	CASIN5	CASIN7	CASIN10	CASIN11	CASOUT0	CASOUT3	CASOUT5	GND	CASOUT8
B	GND	CASIN1	CASIN3	CASIN6	CASIN9	CASOUT2	CASOUT1	CASOUT4	CASOUT6	CASOUT7	CASOUT10
C	CLK	CASIN0	INDEX PIN		CASIN8	CASIN12	OEC#		CASOUT9		CASOUT11
D	DIN7	VCC								GND	CASOUT12
E	DIN4	DIN5	DIN6						DOUT0	DOUT1	DOUT2
F	DREF6	DIN3	DIN2						DOUT4	DOUT7	DOUT3
G	DIN0	DREF7	DIN1						VCC	DOUT6	DOUT5
H	DREF5	DREF4								AUXOUT1	AUXOUT0
J	DREF3	DREF1			A1	DCONT5	DCONT4			GND	AUXOUT2
K	DREF2	VCC	RLOAD#	CLOAD#	A0	DCONT6	DCONT2	OEA#	AUXOUT6	AUXOUT4	AUXOUT3
L	DREF0	GND	TXFR#	A2	DCONT7	DCONT1	DCONT3	DCONT0	AUXOUT8	AUXOUT7	AUXOUT5

84 PIN PLCC — TOP VIEW

Top edge (pins 11–1, then 84–75): CASIN2 (11), CASIN3 (10), CASIN4 (9), CASIN5 (8), CASIN6 (7), CASIN7 (6), CASIN8 (5), CASIN9 (4), CASIN10 (3), CASIN11 (2), CASIN12 (1), OEC# (84), CASOUT0 (83), CASOUT1 (82), CASOUT2 (81), CASOUT3 (80), CASOUT4 (79), CASOUT5 (78), GND (77), CASOUT6 (76), CASOUT7 (75)

Left edge:
Pin	Signal
12	CASIN1
13	CASIN0
14	GND
15	CLK
16	VCC
17	DIN7
18	DIN6
19	DIN5
20	DIN4
21	DIN3
22	DIN2
23	DIN1
24	DIN0
25	DREF7
26	DREF6
27	DREF5
28	DREF4
29	DREF3
30	DREF2
31	DREF1
32	DREF0

Right edge:
Pin	Signal
74	CASOUT8
73	CASOUT9
72	CASOUT10
71	CASOUT11
70	GND
69	CASOUT12
68	DOUT0
67	DOUT1
66	DOUT2
65	DOUT3
64	DOUT4
63	VCC
62	DOUT5
61	DOUT6
60	DOUT7
59	AUXOUT0
58	AUXOUT1
57	AUXOUT2
56	AUXOUT3
55	GND
54	AUXOUT4

Bottom edge (pins 33–53): VCC (33), RLOAD# (34), GND (35), TXFR# (36), CLOAD# (37), A2 (38), A1 (39), A0 (40), DCONT7 (41), DCONT6 (42), DCONT5 (43), DCONT4 (44), DCONT3 (45), DCONT2 (46), DCONT1 (47), DCONT0 (48), OEA# (49), AUXOUT8 (50), AUXOUT7 (51), AUXOUT6 (52), AUXOUT5 (53)

Pin Description

SYMBOL	PLCC PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	16, 33, 63		The +5V power supply pin.
GND	14, 35, 55, 70, 77		Ground.
DIN0-7	17-24	I	The DIN0-7 bus consists of eight single data input pins. The assignment of the active pins is determined by the configuration. Data is loaded synchronous to the rising edge of CLK. DIN0 is the LSB.
DOUT0-7	60-62, 64-68	O	The DOUT0-7 bus is the data output of the correlation array. The format of the output is dependent on the window configuration and bit weighting. DOUT0 is the LSB.
CLK	15	I	System clock. Positive edge triggered.
CASIN0-12	1-13	I	CASIN0-12 allows multiple correlators to be cascaded by connecting CASOUT0-12 of one correlator to CASIN0-12 of another. The CASIN bus is added internally to the correlation score to form CASOUT. CASIN0 is the LSB.
CASOUT0-12	69, 71-76, 78-83	O	CASOUT0-12 is the output correlation score. This value is the delayed sum of all the 256 taps of one chip and CASIN0-12. When the part is configured to act as two independent correlators, CASOUT0-8 represents the correlation score for the first correlator while the second correlation score is available on the AUXOUT0-8 bus. In this configuration, the cascading feature is no longer an option. CASOUT0 is the LSB.
OEC#	84	I	OEC# is the output enable for CASOUT0-12. When OEC# is high, the output is three-stated. Processing is not interrupted by this pin. (Active low.)
TXFR#	36	I	TXFR# is a synchronous clock enable signal that allows the loading of the reference and mask inputs from the preload register to the correlation array. Data is transferred on the rising edge of CLK while TXFR# is low. (Active low.)
DREF0-7	25-32	I	DREF0-7 is an 8-bit wide data reference input. This is the input data bus used to load the reference data. RLOAD# going active initiates the loading of the reference registers. This input bus is used to load the reference registers of the correlation array. The manner in which the reference data is loaded is determined by the window configuration. If the window configuration is 1 x 256, the reference bits are loaded one at a time over DREF7. When the HSP45256 is configured as an 8 x 32 array, the data is loaded into all stages in parallel. In this case, DREF7 is the reference data for the first stage and DREF0 is the reference data for the eighth stage. The contents of the reference data registers are not affected by changing the window configuration. DREF0 is the LSB.
RLOAD#	34	I	RLOAD# enables loading of the reference registers. Data on DREF0-7 is loaded into the preload registers on the rising edge of RLOAD#. This data is transferred into the correlation array by TXFR#. (Active low.)
DCONT0-7	41-48	I	DCONT0-7 is the control data input, which is used to load the mask bit for each tap as well as the configuration registers. The mask data is sequentially loaded into the eight stages in the same manner as the reference data. DCONT0 is the LSB.
CLOAD#	37	I	CLOAD# enables the loading of the data on DCONT0-7. The destination of this data is controlled by A0-2. (Active low.)
A0-2	38-40	I	A0-2 is a 3-bit address that determines what function will be performed when CLOAD# is active. This address bus is set up with respect to the rising edge of the load signal, CLOAD#. A0 is the LSB.
AUXOUT0-8	50-54, 56-59	O	AUXOUT0-8 is a 9-bit bus that provides either the data reference output or the 9-bit correlation score of the second correlator, depending on the configuration. When the user programs the chip to be two separate correlators, the score of the second correlator is output on this bus. When the user has programmed the chip to be one correlator, AUXOUT0-7 represents the reference data out, with the state of AUXOUT0-8 undefined. AUXOUT0 is the LSB.
OEA#	49	I	The OEA# signal is the output enable for the AUXOUT0-8 output. When OEA# is high, the output is disabled. Processing is not interrupted by this pin. (Active low.)

7

SPECIAL
FUNCTION

Functional Description

The correlation array consists of eight 32-bit stages. The first stage receives data directly from input pin DIN7. The other seven stages receive input data from either an external data pin, DIN0-6, or from the shift register output of the previous stage, as determined by the Configuration Register. When the part is configured as a single correlator the sum of correlation score, offset register and cascade input appears on CASOUT0-12. Delayed versions of the data and reference inputs appear on DOUT0-7 and AUXOUT0-7, respectively. The input and output multiplexers of the correlation array are controlled together; for example, in a 1 x 256 correlation, the input data is loaded into DIN7 and the output appears on DOUT7. The configuration of the data bits, the length of the correlation (and in the two- dimensional data, the number of rows), is commonly called the correlation window.

Correlator Array

The core of the HSP45256 is the correlation array, which consists of eight 32-tap stages. A single correlator cell consists of an XNOR gate for the individual bit comparison; i.e., if the data and reference bits are either both high or both low, the output of the correlator cell is high. In addition, two latches, one for the reference and one for the control data path are contained in this cell. These latches are loaded from the preload registers on the rising edge of CLK when TXFR# is low so that the reference and mask values are updated without interrupting data processing.

The mask function is implemented with an AND gate. When a mask bit is a logic low, the corresponding correlator cell output is low.

The function performed by one correlation cell is:

$$(D_{i,n} \text{ XNOR } R_{i,n}) \text{ AND } M_{i,n}$$

where:

$D_{i,n}$ = Bit i of data register n

$R_{i,n}$ = Bit i of reference register n

$M_{i,n}$ = Bit i of mask register n

The reference and mask bits are loaded sequentially, N bits at a time, where N depends on the current configuration (See Table 3). New reference data is loaded on the rising edge of RLOAD# and new mask data is loaded on the rising edge of CLOAD#. The mask and reference bits are stored internally in shift registers, so that the mask and reference information that was loaded most recently will be used to process the newest data. When new information is loaded in, the previous contents of the mask and reference bits are shifted over by one sample, and the oldest information is lost. There are no registers in the multiplexer array (Figure 1), so the data on DOUT0-7 corresponds to the data in the last element of the correlation array. When monitoring DOUT0-7, AUXOUT0-8, and REFOUT0-7, only those bits listed in Table 3 are valid.

Weight and Sum Logic

The Weight and Sum Logic provides the bit weighting and final correlator score from the eight stages of the correlation array. For a 1 x 256 1-D configuration, the outputs of each of the stages are given a weight of 1 and then added together. In a 8 x 32 (8-bit data) configuration, the output of each stage will be shifted so that the output data represents an 8-bit word, with stage seven being the MSB.

The 13-bit offset register is loaded from the control data bus. Its output is added to the correlation score obtained from the correlator array. This sum then goes to the programmable delay register data input.

When the chip is configured as dual correlators, the user has the capability of loading two different offset values for the two correlators.

The Programmable Delay Register sets the number of pipeline stages between the output of the weight and sum logic and the input of the Cascade Summer. This delay register is used to align the output of multiple correlators in cascaded configurations (See Applications). The number of delays is programmable from 1 to 16, allowing for up to 16 correlators to be cascaded. When the HSP45256 is configured as dual correlators, the delay must be set to 0000, which specifies a delay of 1.
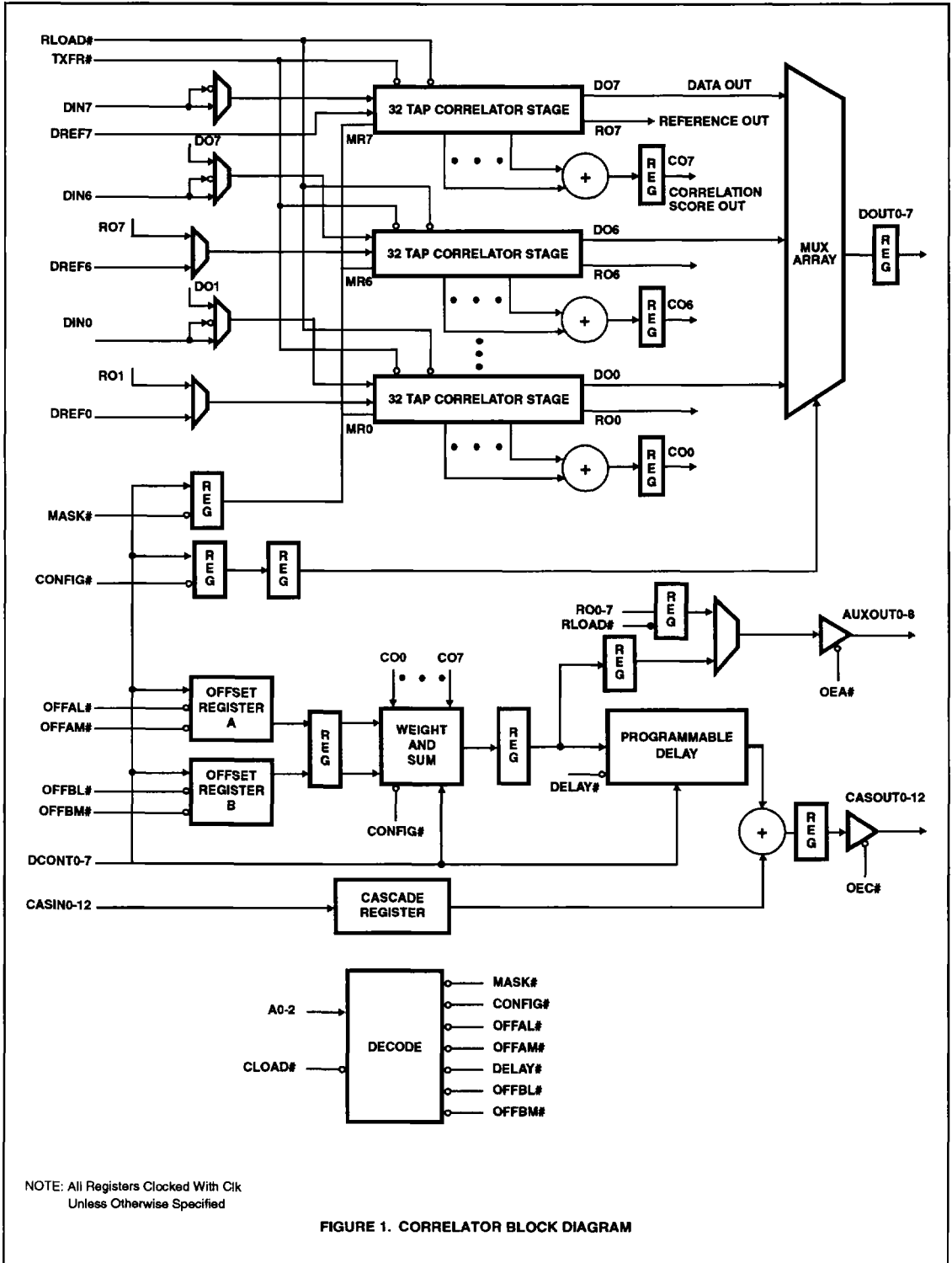
Cascade Summer

This is used for cascading several correlators together. This value on this bus represents the correlation score from the previous HSP45256 that will be summed with the current score to provide the final correlation score. When several correlators are cascaded, the CASOUT0-12 of each of the other correlators is connected to the CASIN0-12 of the next correlator in the chain. The CASIN0-12 of the first chip is tied low. The following function represents the correlation score seen on CASOUT0-12 of each correlator:

$$\begin{aligned}
CASOUT(n) = \;&(W7 \times CO7)(n\text{-Delay}) + (W6 \times CO6)(n\text{-Delay}) + \\
&(W5 \times CO5)(n\text{-Delay}) + (W4 \times CO4)(n\text{-Delay}) + \\
&(W3 \times CO3)(n\text{-Delay}) + (W2 \times CO2)(n\text{-Delay}) + \\
&(W1 \times CO1)(n\text{-Delay}) + (W0 \times CO0)(n\text{-Delay}) + \\
&\text{Offset } (n\text{-Delay}) + CASIN.
\end{aligned}$$

where:

CO0-CO7 are the correlation score outputs out of the correlation stages; W0-W7 is the weight given to each stage; n-Delay represents the delay on the weighted and summed correlation score through the Programmable Delay Register; Offset is the value programmed into the Offset register; CASIN is the cascade input.

FIGURE 1. CORRELATOR BLOCK DIAGRAM

NOTE: All Registers Clocked With Clk
Unless Otherwise Specified

7

SPECIAL
FUNCTION

Control Registers

The 3-bit address value, A0-2, is used to determine which internal register will be loaded with the data on DCONT0-7. The function is initiated when CLOAD# is brought low, and the register is loaded on the rising edge of CLOAD#. Table 1 indicates the function associated with each address. Table 2 shows the function of the bits in each of the registers.

TABLE 1. ADDRESS MAPPING

A2	A1	A0	DESTINATION
0	0	0	Mask Register
0	0	1	Configuration Register
0	1	0	Offset Register A-Most Significant Bits
0	1	1	Offset Register A-Least Significant Bits
1	0	0	Programmable Delay Register
1	0	1	Offset Register B-Most Significant Bits
1	1	0	Offset Register B-Least Significant Bits
1	1	1	Reserved

TABLE 2. CONTROL REGISTER BITS

A0-2 = 000 Mask Register

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0

MR0-7: Mask Register. When mask register bit N = 1, the corresponding reference register bit is enabled. Mask register data is loaded from the DCONT0-7 bus into a holding register on the rising edge of CLOAD# and is written to the mask register on the rising edge of TXFR#.

A0-2 = 001 Configuration Register

-	-	TC	CONFIG4	CONFIG3	CONFIG2	CONFIG1	CONFIG0

TC: Configures correlator for two's complement input. Inverts the MSB of the input data, where the position of the MSB depends on the current configuration.

CONFIG4: The state of CONFIG4 sets up the HSP45256 as either one or two correlators. When CONFIG4 = 0, the HSP45256 is configured as one correlator with the correlation score available on CASOUT0-12. When CONFIG4 = 1, the HSP45256 is configured as dual correlators with the first correlator's score available on CASOUT0-8 and the second score available on AUXOUT0-8. When the chip is configured as dual correlators, the Programmable Delay must be set to 0000 for a delay of 1.

CONFIG2-3: Control the number of data bits to be correlated. See Table 3.

CONFIG0-1: CONFIG1 and CONFIG0 represent the length of the correlation window as indicated in Table 3.

A0-2 = 010 MS Offset Register A

-	-	-	OFFA12	OFFA11	OFFA10	OFFA9	OFFA8

OFFA8-12: Most significant bits of Offset Register A. This is the register used in single correlator mode.

A0-2 = 011 LS Offset Register A

OFFA7	OFFA6	OFFA5	OFFA4	OFFA3	OFFA2	OFFA1	OFFA0

OFFA0-7: Least significant bits of Offset Register A.

A0-2 = 100 Programmable Delay

-	-	-	-	PDELAY3	PDELAY2	PDELAY1	PDELAY0

PDELAY0-3: Controls amount of delay from the weight and sum logic to the cascade summer. The number of delays is 1-16, with PDELAY = 0000 corresponding to a delay of 1 and PDELAY = 1111 corresponding to a delay of 16.

A0-2 = 101 MS Offset Register B

-	-	-	-	-	-	-	OFFSETB8

OFFB8: Most significant bit of Offset Register B. In dual correlator mode, this register is used for the correlator whose output appears on the AUXOUT pins.

A0-2 = 110 LS Offset Register B

OFFB7	OFFB6	OFFB5	OFFB4	OFFB3	OFFB2	OFFB1	OFFB0

OFFB0-7: Least significant bits of Offset Register B.

TABLE 3. CONFIGURATION SETUP

4	3	2	1	0	NO. OF CORRE-LATORS	DATA BITS	ROWS	LENGTH	CORRE-LATOR	DIN	DREF	DOUT	AUXOUT	CASOUT	CO7	CO6	CO5	CO4	CO3	CO2	CO1	CO0
0	0	0	0	0	1	1	1	256	-	7	7	7	7	12-0	1	1	1	1	1	1	1	1
0	0	0	0	1	1	1	2	128	-	7,3	7,3	7,3	7,3	12-0	1	1	1	1	1	1	1	1
0	0	0	1	0	1	1	4	64	-	7,5,3,1	7,5,3,1	7,5,3,1	7,5,3,1	12-0	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	8	32	-	7-0	7-0	7-0	7-0	12-0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	2	1	128	-	7,3	7	7,3	7,3	12-0	2	2	2	2	1	1	1	1
0	0	1	1	0	1	2	2	64	-	7,5,3,1	7,5	7,5,3,1	7,5,3,1	12-0	2	2	2	2	1	1	1	1
0	0	1	1	1	1	2	4	32	-	7-0	7,6,5,4	7-0	7-0	12-0	2	2	2	2	1	1	1	1
0	1	0	1	0	1	4	1	64	-	7,5,3,1	7	7,5,3,1	7,5,3,1	12-0	8	8	2	2	4	4	1	1
0	1	0	1	1	1	4	2	32	-	7-0	7,6	7-0	7-0	12-0	8	8	2	2	4	4	1	1
0	1	1	1	1	1	8	1	32	-	7-0	7	7-0	7-0	12-0	128	8	32	4	64	2	16	1
1	0	0	0	1	2	1	1	128	A	7	7	7	-	12-0	1	1	1	1	-	-	-	-
									B	3	3	3	8-0	-	-	-	-	-	1	1	1	1
1	0	0	1	0	2	1	2	64	A	7,5 3,1	7,5 3,1	7,5 3,1	-	12-0	1	1	1	1	-	-	-	-
									B				8-0	-	-	-	-	-	1	1	1	1
1	0	0	1	1	2	1	4	32	A	7-4 3-0	7-4 3-0	7-4 3-0	-	12-0	1	1	1	1	-	-	-	-
									B				8-0	-	-	-	-	-	1	1	1	1
1	0	1	1	0	2	2	1	64	A	7,5 3,1	7	7,5 3,1	-	12-0	2	2	1	1	-	-	-	-
									B		3		8-0	-	-	-	-	-	2	2	1	1
1	0	1	1	1	2	2	2	32	A	7-4 3-0	7,6	7-4 3-0	-	12-0	2	2	1	1	-	-	-	-
									B		3,2		8-0	-	-	-	-	-	2	2	1	1
1	1	0	1	1	2	4	1	32	A	7-4 3-0	7	7-4 3-0	-	12-0	8	2	4	1	-	-	-	-
									B		3		8-0	-	-	-	-	-	8	2	4	1

During reference register loading, the 8-bits, DREF0-7 are used as reference data inputs. The falling edge of RLOAD# initiates reference data loading; when RLOAD# returns high, the data on DREF0-7 is latched into the selected correlation stages. The active bits on DREF0-7 are controlled by the current configuration.

The window configuration is determined by the state of control signals upon programming the control register. Table 3 represents the programming information required for each window configuration. In Table 3, note that the data listed for Output Weighting refers to the weights given to each of the Correlation Sum Outputs (CO0-7 in Figure 1).

During initialization, the loading configuration for the reference data is set by the user. Table 3 shows the loading options. These load controls specify whether the reference data for a given stage comes from the shift register output of the previous stage or from an external data pin.

Applications

Single HSP45256 – 1-Bit Data, 256 Samples

A 1 x 256 (1-D configuration) correlation requires only 1 HSP45256. To initialize the correlator, all the reference bits, control bits, the delay value of the variable delay, and the window configuration must be specified.

TABLE 4. REGISTER CONTENTS FOR 1 X 256 CORRELATOR WITH EQUAL WEIGHTING

A0-2	DCONT0-7	NOTES
001	00000000	1 256-tap correlator: 1 x 256 window configuration, reference loaded from DREF7, eight stages weighted equally, DIN 7 and DOUT7 are the data input and output, respectively.
010	00000000	Offset Register A = 0
011	00000000	
100	00000000	Programmable Delay = 0
101	00000000	Offset Register B = 0 (Loading of this register optional in this mode.)
110	00000000	

The loading of the reference and mask registers may be done simultaneously by setting A0-2 = 000, setting the DREF and DCONT inputs to their proper values and pulsing RLOAD# and CLOAD# low. In this configuration, DREF7 loads the reference data and DCONT7 loads the mask information; both sets of data are loaded serially. It will take 256 load pulses (RLOAD#) to load the reference array, and 256 CLOAD# pulses to load the mask array. Upon completion of the mask and register loading, TXFR# is pulsed low, which transfers the reference and control data from the preload registers to the reference and mask registers, updating the data that will be used in the correlation. Reference and mask data can be loaded more quickly by configuring the correlator as an 8 row by 32 sample array, loading the bits eight at a time, then changing the configuration back to 1 x 256 to perform the correlation.

Single HSP45256 – 8-Bit Data, 32 Samples

An 8 x 32 correlation also requires only 1 HSP45256. To initialize the correlator, all the reference bits, control bits, the value of the programmable delay, and the window configuration must be specified.

Again, the loading of the reference and mask registers can be done simultaneously. Due to the programming initialization, DREF0-7 are used to load the reference data 8-bits at a time. It will take 32 load pulses each of RLOAD# and CLOAD# to load both arrays. Upon completion of the mask and register loading, TXFR# is pulsed low, which transfers the reference and control data from the preload registers to the registers that store the active data.

TABLE 5. REGISTER LOADING FOR 8 X 32 CORRELATOR WITH BINARY WEIGHTING

A0-2	DCONT0-7	NOTES
001	00001111	1 256-tap correlator; 8 x 32 window configuration, 8-bit data stream; reference register is loaded from DREF7 for all stages. Correlator score = $(128 \times CO7) + (64 \times CO3) + (32 \times CO5) + (16 \times CO1) + (8 \times CO6) + (4 \times CO4) + (2 \times CO2) + CO0$
010	00000000	Offset Register A = 0000000010000
011	00010000	
100	00000000	Programmable Delay = 0
101	00000000	Offset Register B = 0 (Loading optional in this mode.)
110	00000000	

This configuration performs correlation of an 8-bit number with a 1-bit reference. Each byte out of the correlation array gives an 8-bit level of confidence that the data corresponds to the reference. The correlation score is the sum of these confidence levels.

Single HSP45256 – Dual Correlators, 2-Bit Data, 64 Samples

Dual 2 x 64 correlators require only one HSP45256. To initialize the correlator, all the reference bits, control bits, the delay value of the variable delay, and the window configuration must be specified.

In this example, each of the dual correlators compares 2-bit data to a 1-bit reference. It will take 64 load pulses (RLOAD#/CLOAD#) to completely load the reference and mask registers in the array. The programmable delay must be set to 0 for the output of the two correlators to be aligned.

TABLE 6. REGISTER LOADING FOR DUAL 2 X 64 CORRELATORS WITH EQUAL WEIGHTING

AO-2	DCONT0-7	NOTES
001	00010010	Dual correlators: each 2 bit data, 64 taps; reference register for correlation A is loaded from DREF7 and DREF5, the reference register for correlator B is loaded from DREF3 and DREF1. Correlator #1 = 2x CO7 + 2 x CO6 + CO5 + CO4, correlator #2 = 2 x CO3 + 2x CO2 + CO1 + CO0.
010	00000000	Offset Register A = 0000000010000
011	00010000	
100	00000000	Programmable Delay = 0
101	00000000	Offset Register B = 0
110	00000000	

Cascading Correlators

Correlators can be cascaded in either a serial or parallel fashion. Longer correlations can be achieved by connecting several correlators together as shown in Figure 2. Each correlator is in a one data bit, one row, 256 tap configuration. The number of bits of significance at the CASOUT output of each correlator builds up from one correlation to the next,

that is, the maximum score out of the first correlator is 256, the maximum output of the second correlator is 512, etc. In this configuration, the maximum length of the correlation is 4096. This would be implemented with 16 HSP45256's. The programmable delay register in the first correlator would be set for one delay, the second would be set for two, and so on, with the final HSP45256 being set for a delay of 16.

Correlations of more bits can be calculated by connecting CASOUT of each chip to the CASIN of the following chip (Figure 3). The data on the CASOUT lines accumulates in a similar manner as in the 1 x 256 mode, except that the maximum output of the first correlator is decimal 960, (hexadecimal 3C0); in the general case, the maximum number of correlators that can be cascaded in this manner is eight, since the maximum output of the last one would be 1E00, which nearly uses up the 13-bit range of the cascade summer. More parts could be cascaded together if some bits are to be masked out or if the user has a prior knowledge of the maximum value of the correlation score. As before, the delay in the first correlator would be set to one, the second correlator would be set for a delay of two, and so on.

Multiple HSP45256's can be cascaded for two dimensional one bit data (Figure 4). The maximum output for each chip is the same as in the 1 x 256 case; the only difference is in the manner in which the correlators are connected. The programmable delay registers would be set as before.
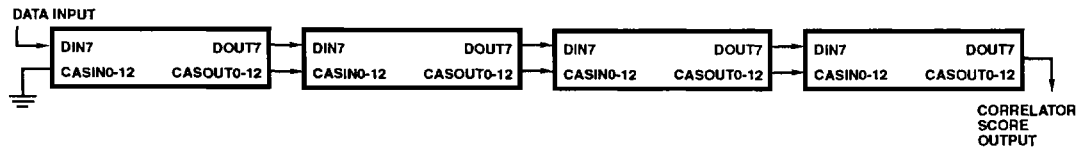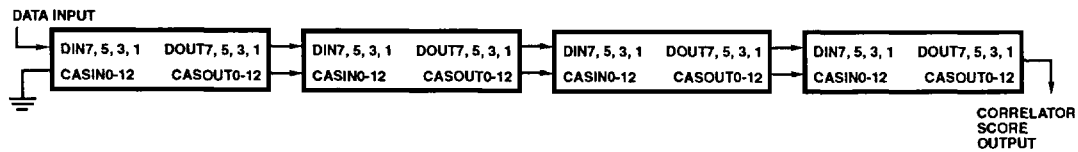

FIGURE 2. 1 BIT, 1024 SAMPLE CONFIGURATION

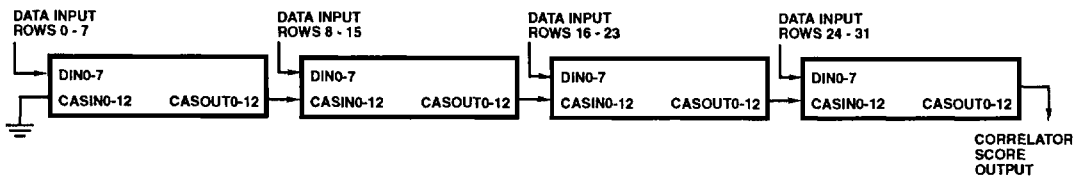FIGURE 3. 4 BIT, 256 SAMPLE CONFIGURATION

FIGURE 4. 1 BIT, 32 X 32 WINDOW CONFIGURATION

Reloading Data During Operation

RLOAD# and CLOAD# are asynchronous signals that are designed to be driven by the memory interface signals of a microprocessor. TXFR# is synchronized to CLK so that the mask or reference data is updated on a specific clock cycle. In the normal mode of operation, the user loads the reference and mask memories, then pulses TXFR# to use that data. The correlator uses the new mask or reference information immediately. Loading of the reference and mask data remains asynchronous as long as there is at least one cycle of CLK between the rising edge of RLOAD# or CLOAD# and the TXFR# pulse.

If the system timing makes it necessary for TXFR# and RLOAD# and/or CLOAD# to be active during the same clock cycle, then they must be treated as synchronous signals; the timing for this case is shown in Figure 5 and given in the AC Timing Specifications (T_{THCL} and T_{CLLH}). In this example, data is loaded during clock cycle 1 and transferred on the rising edge of CLK that occurs in clock cycle two. Another set of data is loaded during clock cycle 2, which will be transferred by a later TXFR# pulse. The sequence of events is as follows:

1. In clock cycle 1, TXFR# becomes active at least T_{TH} nanoseconds after the rising edge of CLK.

2. RLOAD and/or CLOAD# pulses low; the timing is not critical as long as its rising edge occurs before the end of clock cycle 1. If this condition is not met, it is undetermined whether the data loaded by this pulse will be transferred by the current TXFR# pulse.

3. The rising edge of TXFR# occurs while CLK is high during clock cycle 2. The margin between the rising edge of TXFR# and the falling edge of CLK is defined by T_{THCL}.

4. RLOAD# and/or CLOAD# pulses low. The rising edge of RLOAD# and CLOAD# must occur after the falling edge of CLK. The margin between the two is defined by T_{CLLH}.

The time from the rising edge of TXFR# to the falling edge of CLK must be greater than T_{THCL}, and the time from the falling edge of CLK to the rising edge of RLOAD# or CLOAD# must be greater than T_s. If this timing is violated, the data being transferred by the TXFR# pulse shown may or may not include the data loaded in clock cycle 2.

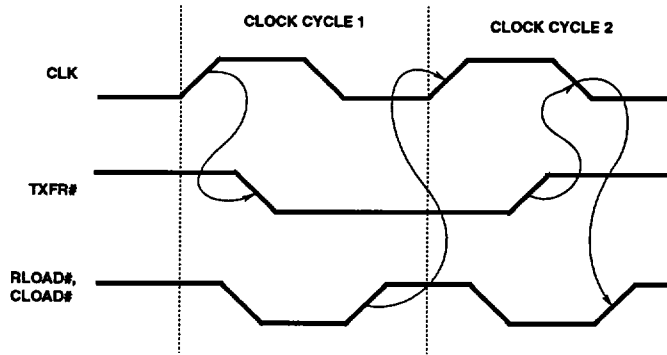FIGURE 5. LOADING AND TRANSFERRING DATA DURING THE SAME CLOCK CYCLE

Absolute Maximum Ratings

Supply Voltage	+8.0V
Input, Output or I/O Voltage	GND-0.5V to V_{CC}+0.5V
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C (PLCC), +175°C (PGA)
Lead Temperature (Soldering 10s)	+300°C
ESD Classification	Class 1

Thermal Resistance θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}
PLCC Package	34°C/W	11.3°C/W
PGA Package	36°C/W	10°C/W

Maximum Package Power Dissipation at +125°C

PLCC Package	2.2W
PGA Package	2.9W
Gate Count	13,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range	+4.75V to +5.25V
Operating Temperature Range	0°C to +70°C

DC Electrical Specifications

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Logical One Input Voltage	V_{IH}	2.0	-	V	$V_{CC} = 5.25V$
Logical Zero Input Voltage	V_{IL}	-	0.8	V	$V_{CC} = 4.75V$
High Level Clock Input	V_{IHC}	3.0	-	V	$V_{CC} = 5.25V$
Low Level Clock Input	V_{ILC}	-	0.8	V	$V_{CC} = 4.75V$
Output High Voltage	V_{OH}	2.6	-	V	$I_{OH} = 400\mu A$, $V_{CC} = 4.75V$
Output Low Voltage	V_{OL}	-	0.4	V	$I_{OL} = +2.0mA$, $V_{CC} = 4.75V$
Input Leakage Current	I_I	-10	10	μA	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.25V$
Output Leakage Current	I_O	-10	10	μA	$V_{OUT} = V_{CC}$ or GND, $V_{CC} = 5.25V$
Standby Power Supply Current	I_{CCSB}	-	500	μA	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.25V$, Note 3
Operating Power Supply Current	I_{CCOP}	-	179	mA	f = 25.6MHz, $V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.25V$, Note 1, Note 3

Capacitance ($T_A = 25°C$, Note 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_{IN}	-	10	pF	Frequency = 1MHz, V_{CC} = Open. All measurements are referenced to device ground.
Output Capacitance	C_O	-	10	pF	

NOTES:

1. Power supply current is proportional to operating frequency. Typical rating for ICCOP is 7mA/MHz.

2. Not tested, but characterized at initial design and at major process/design changes.

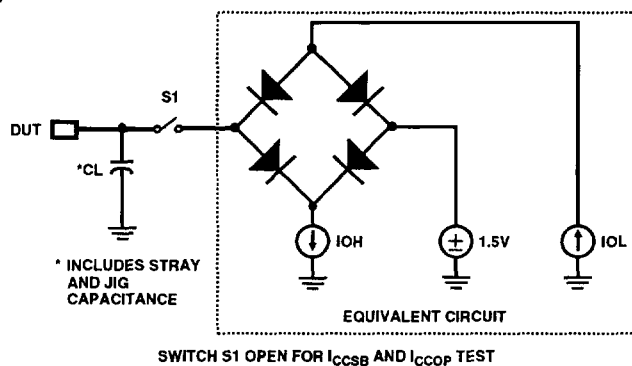3. Output load per test load circuit and $C_L = 40pF$.

7

SPECIAL FUNCTION

AC Electrical Specifications   (V$_{CC}$ = 5.0V ±5%, T$_A$ = 0°C to +70°C, Note 1)

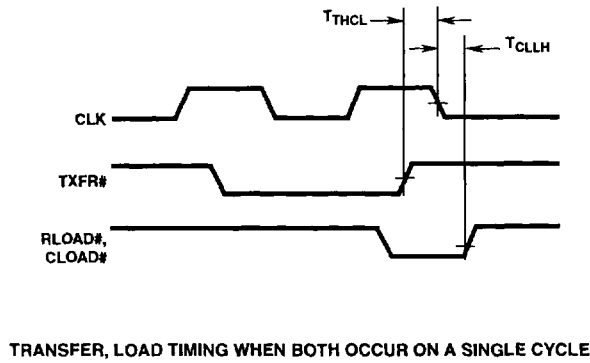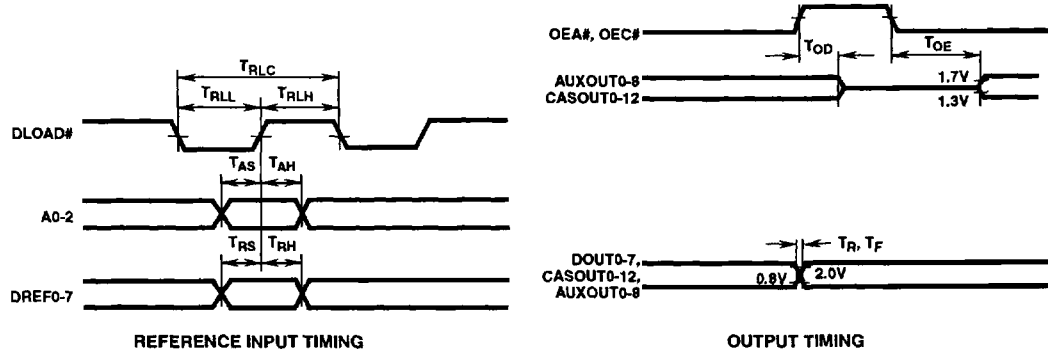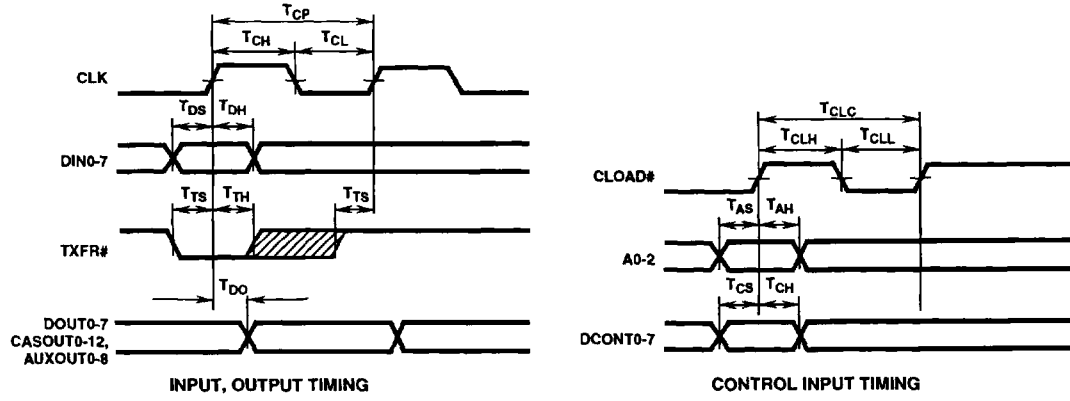| PARAMETER	SYMBOL	33MHz		25.6MHz		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
CLK Period	T$_{CP}$	30	-	39	-	ns	
CLK High	T$_{CH}$	12	-	15	-	ns	
CLK Low	T$_{CL}$	12	-	15	-	ns	
Set-Up Time DIN to CLK High	T$_{DS}$	12	-	13	-	ns	
Hold Time CLK High to DIN	T$_{DH}$	0	-	0	-	ns	
TXFR# Set-Up Time	T$_{TS}$	12	-	13	-	ns	
TXFR# Hold Time	T$_{TH}$	0	-	0	-	ns	
Output Delay DOUT, AUXOUT, CASOUT	T$_{DO}$	-	15	-	20	ns	
CLOAD# Cycle Time	T$_{CLC}$	30	-	39	-	ns	
CLOAD# High	T$_{CLH}$	12	-	15	-	ns	
CLOAD# Low	T$_{CLL}$	12	-	15	-	ns	
Set-Up Time, A to RLOAD#, CLOAD#	T$_{AS}$	12	-	13	-	ns	
Hold Time, RLOAD#, CLOAD# to A	T$_{AH}$	0	-	0	-	ns	
RLOAD# Cycle Time	T$_{RLC}$	30	-	39	-	ns	
RLOAD# High	T$_{RLH}$	12	-	15	-	ns	
RLOAD# Low	T$_{RLL}$	12	-	15	-	ns	
Set-Up Time, DCONT to CLOAD#	T$_{DCS}$	12	-	13	-	ns	
Hold Time, CLOAD# to DCONT	T$_{DCH}$	0	-	0	-	ns	
Set-Up Time, DREF to RLOAD#	T$_{RS}$	12	-	13	-	ns	
Hold Time, RLOAD# to DREF	T$_{RH}$	0	-	0	-	ns	
Output Enable Time	T$_{OE}$	-	15	-	15	ns	
Output Disable Time	T$_{OD}$	-	15	-	15	ns	Note 2
Output Rise, Fall Time	T$_{RF}$	-	6		6	ns	Note 2
TXFR# High to CLK Low	T$_{THCL}$	3	-	3	-	ns	Note 2
CLK Low to RLOAD#, CLOAD# High	T$_{CLLH}$	1	-	1	-	ns	Note 2

NOTES:

1. AC testing is performed as follows: Input levels (CLK Input) 4.0V and 0V; Input levels (all other inputs) 0V and 3.0V; Timing reference levels (CLK) 2.0V; All others 1.5V. Output load per test load circuit with C$_L$ = 40pF. Output transition is measured at V$_{OH}$ > 1.5V and V$_{OL}$ < 1.5V.

2. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.

Test Load Circuit

* INCLUDES STRAY AND JIG CAPACITANCE

EQUIVALENT CIRCUIT

SWITCH S1 OPEN FOR I$_{CCSB}$ AND I$_{CCOP}$ TEST

Timing Waveforms

INPUT, OUTPUT TIMING

CONTROL INPUT TIMING

REFERENCE INPUT TIMING

OUTPUT TIMING

TRANSFER, LOAD TIMING WHEN BOTH OCCUR ON A SINGLE CYCLE

7

SPECIAL FUNCTION