



PESD3V3F2UT

ESD protection diode

8 February 2021

Product data sheet

1. General description

ESD protection device in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package designed to protect two high-speed data lines from the damage caused by ElectroStatic discharge (ESD) and other transients. This product protects especially multimedia applications such as USB, HDMI and others.

2. Features and benefits

- Reverse stand-off voltage: $V_{RWM} = 3.3\text{ V}$
- Low clamping voltage: $V_{CL} = 3.3\text{ V}$ at $I_{TLP} = 8\text{ A}$
- ESD protection up to 8 kV (IEC 61000-4-2)
- Ultra low capacitance: $C_d = 0.56\text{ pF}$
- ESD protection up to 8 kV (ISO 10605; $C = 150\text{ pF}$; $R = 330\ \Omega$)
- High temperature capability: $T_j = 175\text{ °C}$

3. Applications

ESD protection for high-speed data lines

- USB2.0, HDMI, DisplayPort, eSATA and LVDS

4. Quick reference data

Table 1. Quick reference data

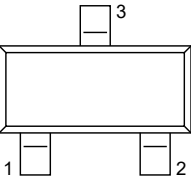
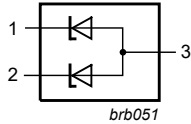
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-----------|--------------------------|--|---------|-----|------|-----|------|
| V_{RWM} | reverse standoff voltage | $T_{amb} = 25\text{ °C}$ | | - | - | 3.3 | V |
| I_{PPM} | rated peak pulse current | $t_p = 8/20\ \mu\text{s}$ | [1] [2] | - | - | 4 | A |
| C_d | diode capacitance | $f = 1\text{ MHz}$; $V_R = 0\text{ V}$; $T_{amb} = 25\text{ °C}$ | [2] | - | 0.56 | 0.7 | pF |

[1] According to IEC 61000-4-5.

[2] Measured from pin 1 or 2 to pin 3.

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------------|---|--|
| 1 | K1 | cathode (diode 1) |  <p style="text-align: center;">SOT23</p> |  <p style="text-align: center;"><i>brb051</i></p> |
| 2 | K2 | cathode (diode 2) | | |
| 3 | CA | common anode | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------|---------|--|---------|
| | Name | Description | Version |
| PESD3V3F2UT | SOT23 | plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body | SOT23 |

7. Marking

Table 4. Marking codes

| Type number | Marking code ^[1] |
|-------------|-----------------------------|
| PESD3V3F2UT | Q3% |

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|----------------------------|---------------------------------|--|---------|-----|-----|------|
| I_{PPM} | rated peak pulse current | $t_p = 8/20 \mu s$ | [1] [2] | - | 4 | A |
| T_j | junction temperature | | | - | 175 | °C |
| T_{amb} | ambient temperature | | | -55 | 175 | °C |
| T_{stg} | storage temperature | | | -65 | 175 | °C |
| ESD maximum ratings | | | | | | |
| V_{ESD} | electrostatic discharge voltage | IEC 61000-4-2; contact discharge | [2] [3] | - | 8 | kV |
| | | ISO 10605; contact discharge; C = 150 pF, R = 330 Ω | [2] [3] | - | 8 | kV |
| | | ISO 10605; contact discharge; C = 330 pF, R = 330 Ω | [2] [3] | - | 6 | kV |

- [1] According to IEC 61000-4-5.
- [2] Measured from pin 1 or 2 to pin 3.
- [3] Device stressed with ten non-repetitive ESD pulses.

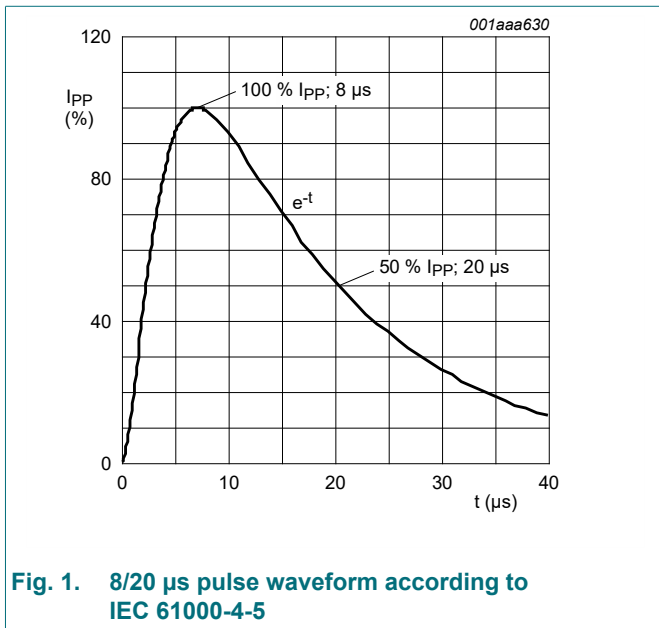


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5

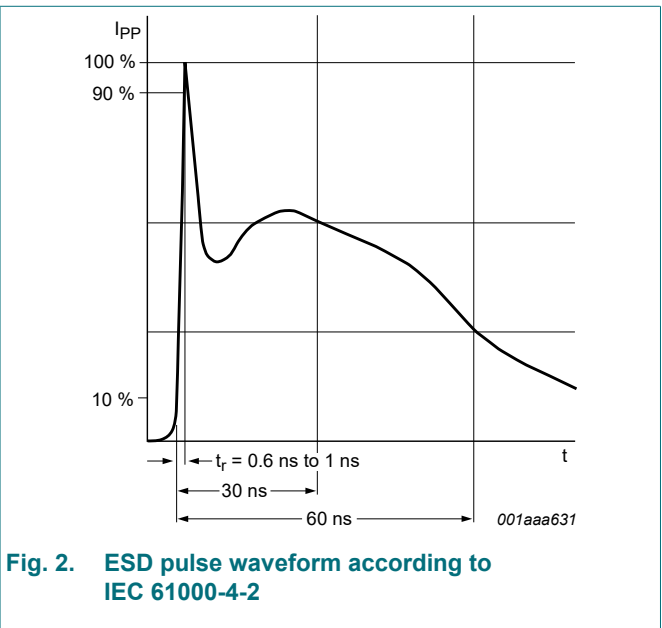


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|------------------|----------------------------|---|---------|-----|------|------|----------|
| V_{RWM} | reverse standoff voltage | $T_{amb} = 25\text{ }^{\circ}\text{C}$ | - | - | 3.3 | V | |
| V_{BR} | breakdown voltage | $I_R = 1\text{ mA}; T_{amb} = 25\text{ }^{\circ}\text{C}$ | [1] | 4.2 | 6.7 | 8 | V |
| I_{RM} | reverse leakage current | $V_{RWM} = 3.3\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ | [1] | - | 1 | 50 | nA |
| C_d | diode capacitance | $f = 1\text{ MHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$ | [1] | - | 0.56 | 0.7 | pF |
| $\Delta C_d/C_d$ | diode capacitance matching | | [2] | - | 1 | - | % |
| V_{CL} | clamping voltage | $I_{PP} = 8\text{ A}; t_p = \text{TLP}; T_{amb} = 25\text{ }^{\circ}\text{C}$ | [3] [1] | - | 3.3 | - | V |
| R_{dyn} | dynamic resistance | $I_R = 10\text{ A}; T_{amb} = 25\text{ }^{\circ}\text{C}$ | [3] [1] | - | 0.3 | - | Ω |

- [1] Measured from pin 1 or 2 to pin 3.
- [2] ΔC_d is the difference of the capacitance measured between pin 1 and pin 3 and the capacitance measured between pin 2 and pin 3.
- [3] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008

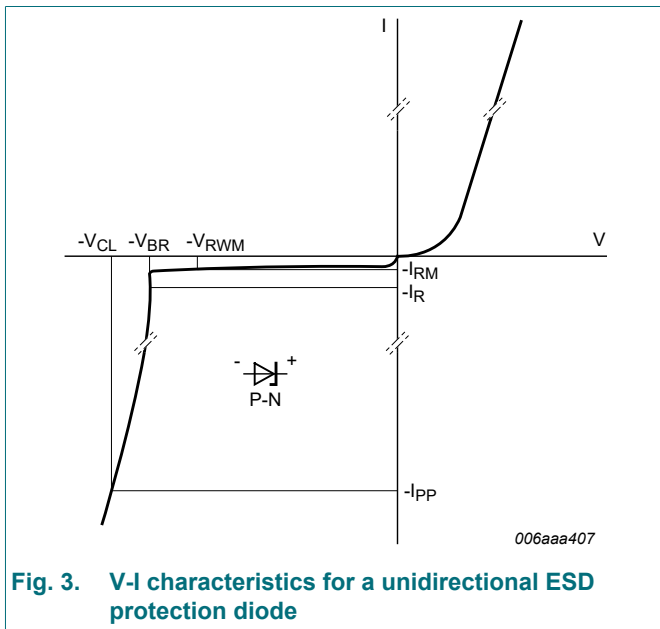


Fig. 3. V-I characteristics for a unidirectional ESD protection diode

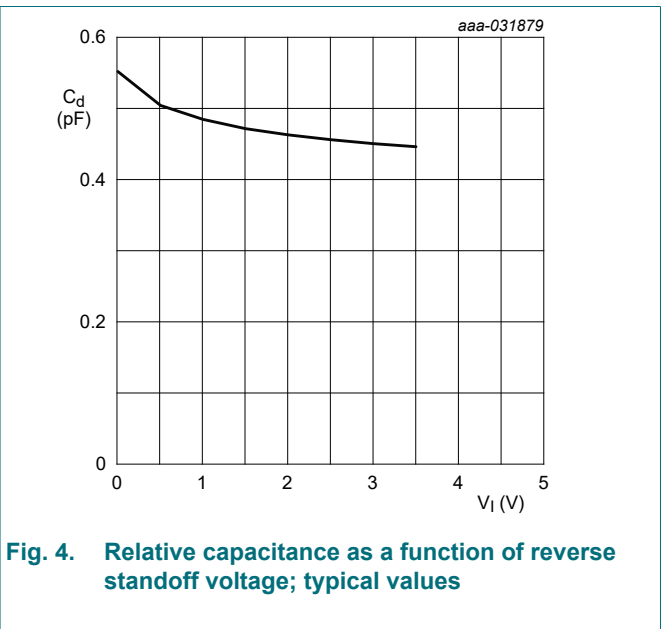
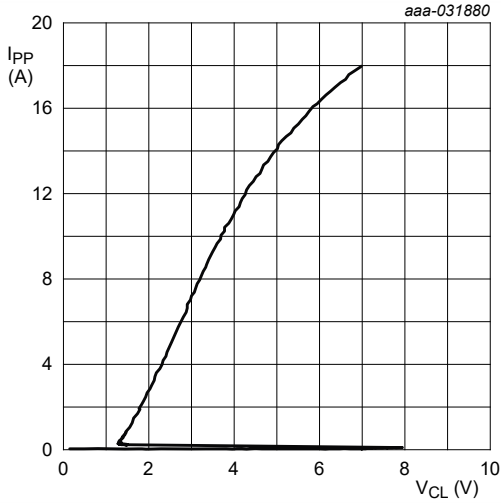
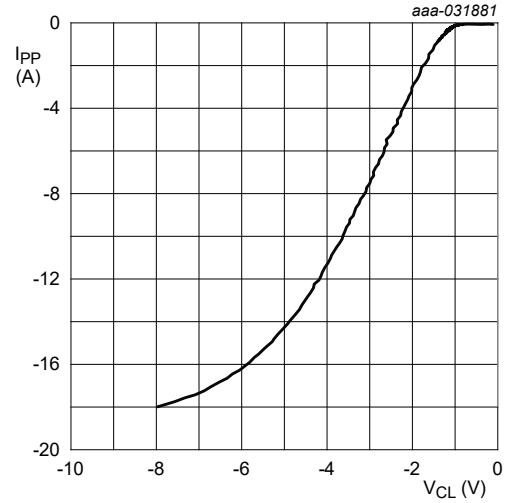


Fig. 4. Relative capacitance as a function of reverse standoff voltage; typical values



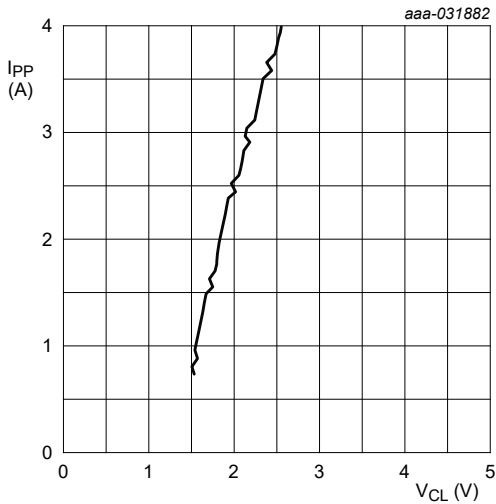
Transmission Line Pulse (TLP);
 $t_p = 100 \text{ ns}$; rise time = 1 ns

Fig. 5. Dynamic resistance with positive clamping; typical values



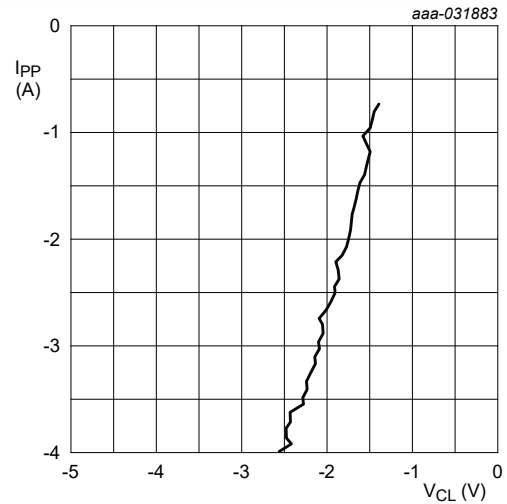
Transmission Line Pulse (TLP);
 $t_p = 100 \text{ ns}$; rise time = 1 ns

Fig. 6. Dynamic resistance with negative clamping; typical values



IEC 61000-4-5; $t_p = 8/20 \text{ }\mu\text{s}$; positive pulse

Fig. 7. Dynamic resistance with positive clamping; typical values



IEC 61000-4-5; $t_p = 8/20 \text{ }\mu\text{s}$; positive pulse

Fig. 8. Dynamic resistance with negative clamping; typical values

10. Application information

The device is designed to provide high-level ESD protection for high-speed serial data buses such as USB, HDMI, DisplayPort, eSATA and LVDS data lines.

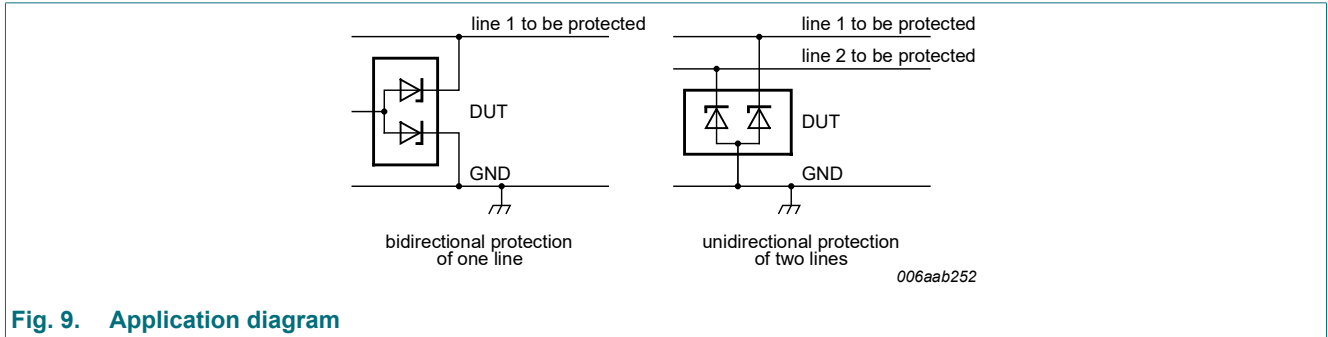


Fig. 9. Application diagram

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

Note: When designing the PCB, give careful consideration to impedance matching and signal coupling. Do not connect the signal lines to unlimited current sources like, for example, a battery.

11. Package outline

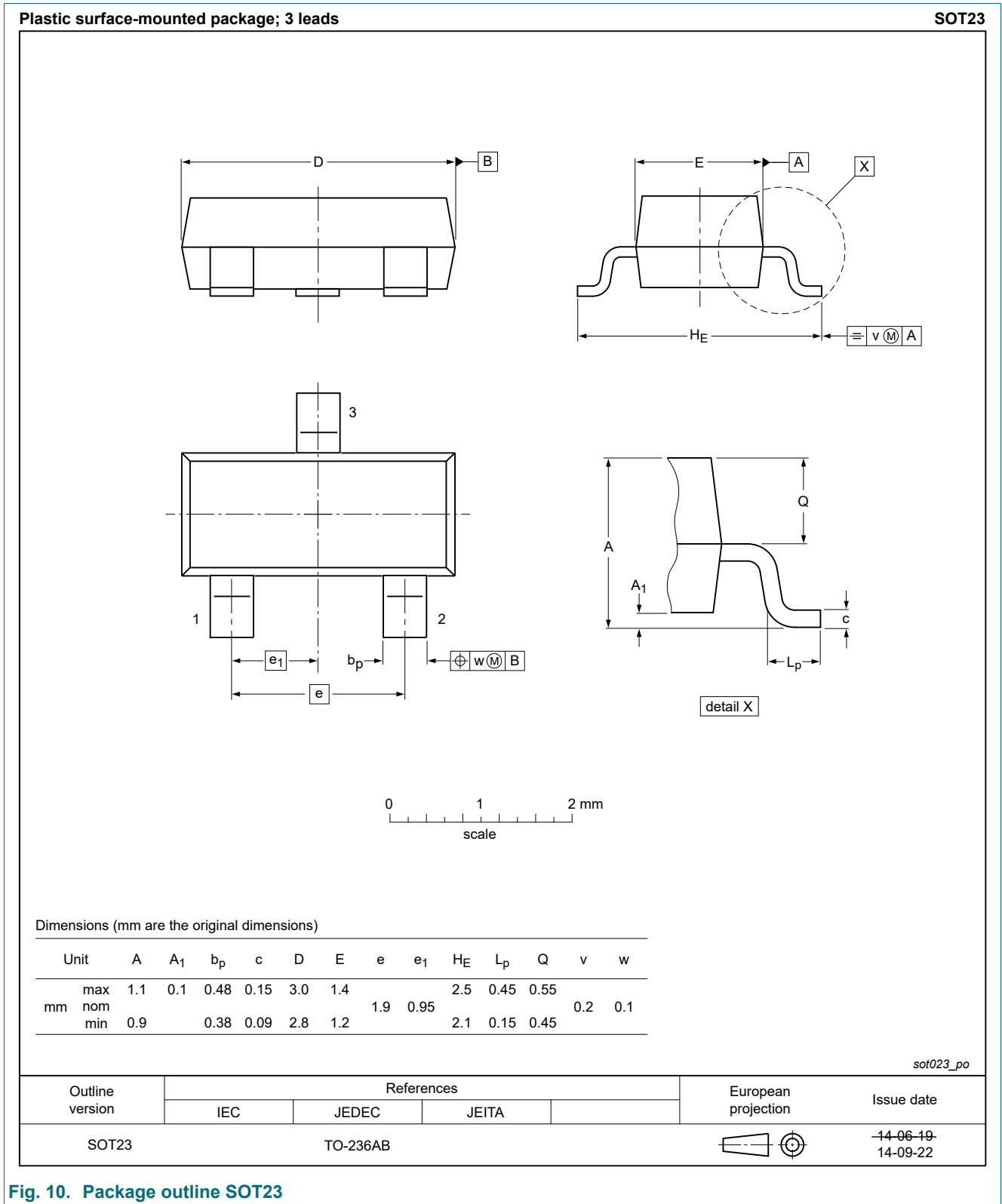


Fig. 10. Package outline SOT23

12. Soldering

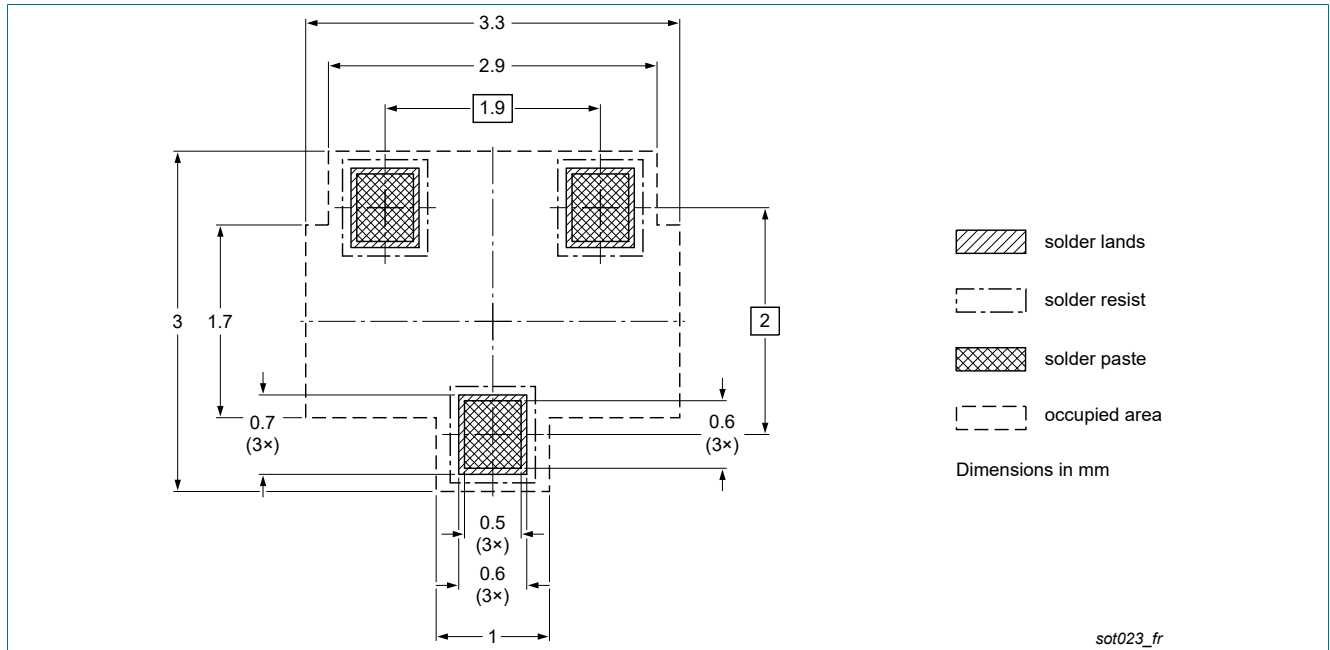


Fig. 11. Reflow soldering footprint for SOT23

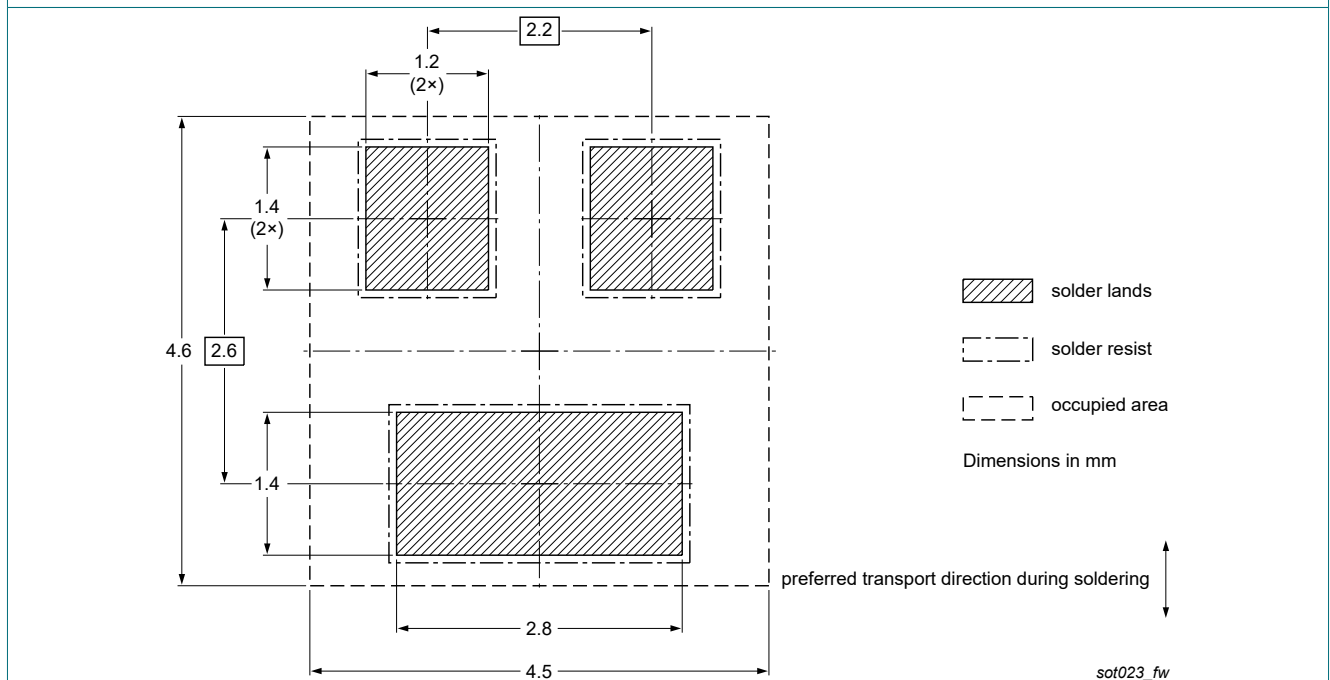


Fig. 12. Wave soldering footprint for SOT23

13. Revision history

Table 7. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------|--------------|--------------------|---------------|------------|
| PESD3V3F2UT v.1 | 20210208 | Product data sheet | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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