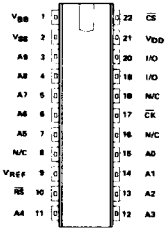
TMS 4062 JL, NL; TMS 4063 JL, NL
1024-WORD BY 1-BIT DYNAMIC RAM

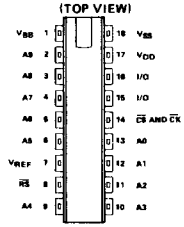
NOVEMBER 1977

- 1024 x 1 Organization
- Access Time . . . 130 ns Maximum
- Cycle Time . . . 200 ns Maximum
- Low Power Dissipation:
  Operating . . . 120 mW Typical
  Standby . . . 2 mW Typical
- Differential Output
- Wire-OR Capability
- Chip Select For Simplified Memory Expansion
- 22-Pin or 18-Pin Dual-In-Line Package

TMS 4062 JL, NL
22-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



TMS 4063 JL, NL
18-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description and operation

The TMS 4062 JL, NL and TMS 4063 JL, NL are fabricated on a single monolithic chip with P-channel enhancement type MOS processing. The devices are designed for use in low-cost, high performance memory applications. Data is read or written through 2 input/output terminals. Clock and chip-select clock pulses allow the transfer of information to or from input/output lines. Refresh must occur at least once every 2 milliseconds.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages:
- V_{DD} and V_{REF}, with respect to V_{SS} . . . . . −27 V to 0.5 V
- V_{DD} and V_{REF}, with respect to V_{BB} . . . . . −30 V to 0.5 V
- V_{BB}, with respect to V_{SS} . . . . . −0.5 V to 10 V

All input voltages, with respect to V_{SS} . . . . . −30 V to 0.5 V
Operating free-air temperature range . . . . . −0°C to 70°C
Storage temperature range . . . . . −55°C to 125°C

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, $V_{BB}-V_{SS}$ (see Notes 1 and 2)	2.3	2.5	2.7	V
Supply voltage, V_{DD}		0		V
Supply voltage, V_{SS}	19	20	21	V
Supply voltage, V_{REF}	6.6	7	7.4	V
High-level input voltage, all inputs, V_{IH}	$V_{SS}-2$		V_{SS}	V
Low-level address input voltage, $V_{IL(ad)}$ (see Note 3)	−2	0	1	V
Low-level input voltage at reset and both clocks, $V_{IL(rs,\,\phi)}$ (see Note 3)	−5	0	0.4	V
Low-level input voltage at I/O, $V_{IL(I/O)}$	$V_{REF}-1$	V_{REF}	$V_{REF}+1$	V
Refresh time, $t_{refresh}$			2	ms
Operating free-air temperature, T_A	0		70	°C

NOTES: 1. Throughout this data sheet supply voltage values are with respect to V_{DD}, unless otherwise noted.
2. V_{BB} must be applied prior to V_{SS}.
3. The algebraic convention where the most positive limit is designated as maximum is used in this data sheet for logic voltage levels only.

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

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