General Description

The 932S890C is a main clock synthesizer chip for SR5690/SR5670 AMD Servers. An SMBus interface allows full control of the device.

Recommended Application

SR5690/SR5670 AMD-based Servers

Output Features

- Low power differential outputs with integrated series resistors for Zo=50ohm systems
- 4 -Differential 200MHz CPU pairs
- 2 - Differential 100MHz HT3 pairs
- 14 - Differential PCIe Gen2 SRC pairs
- 1 - Differential non-spread SATA clock
- 2 - 48MHz USB clocks (180 degrees out of phase for EMI reduction)
- 2 - SIO clocks (selectable 48MHz or 24MHz). 180 degrees out of phase for EMI reduction
- 2 - 14.318MHz REF clock outputs

Features/Benefits

- Spread Spectrum; EMI reduction
- Outputs may be disabled via SMBus; saves power
- External crystal load capacitors; maximum frequency accuracy

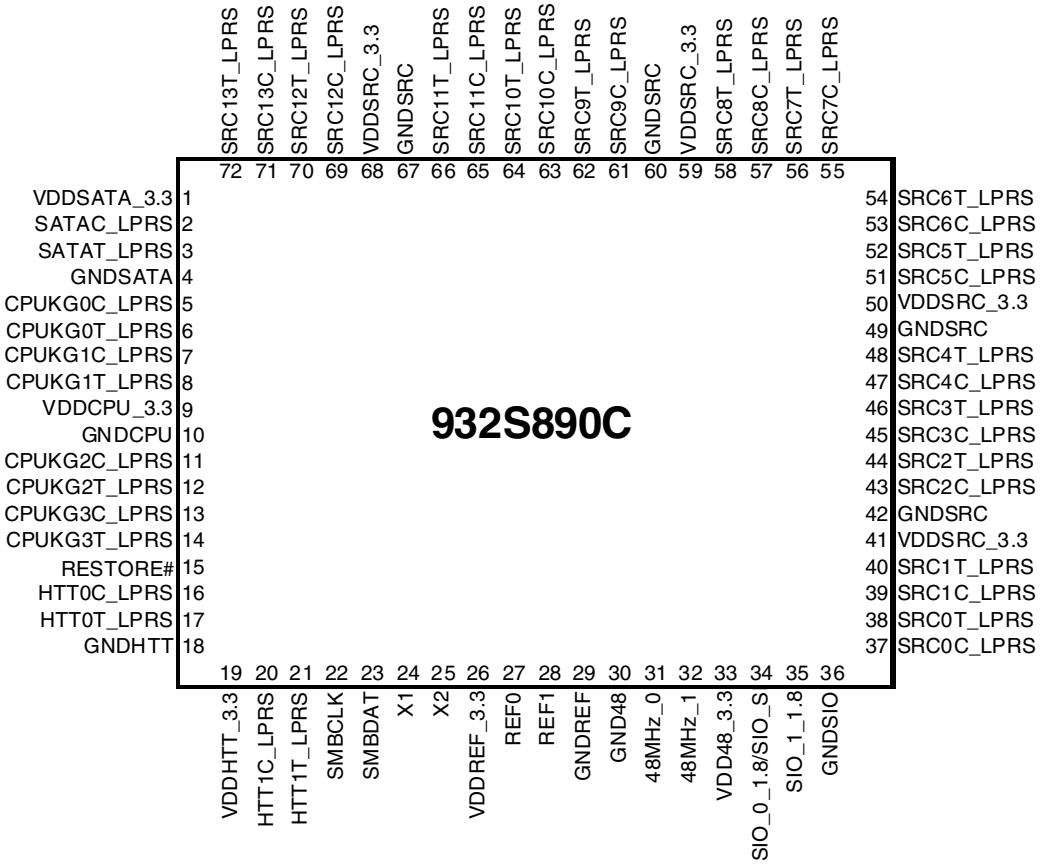
Key Specifications

- CPU output cycle-to-cycle jitter <100ps
- SRC output cycle-to-cycle jitter <125ps
- 48MHz output cycle-to-cycle jitter <130ps
- SIO output cycle-to-cycle jitter <150ps
- SRC output phase jitter <3.1ps rms (PCIe Gen2)
- +/- 50ppm frequency accuracy on all clocks, assuming REF is trimmed to 0 ppm)

Table 1: 932S890 Functionality

CPU MHz	HTT MHz	SRC MHz	SATA	REF MHz	SIO	USB MHz	DOT MHz
200.00	100.00	100.00	100.00	14.318	24/48	48.00	96.00

Pin Configuration



*** Indicates that pin has 120Kohm internal pullup resistor.**

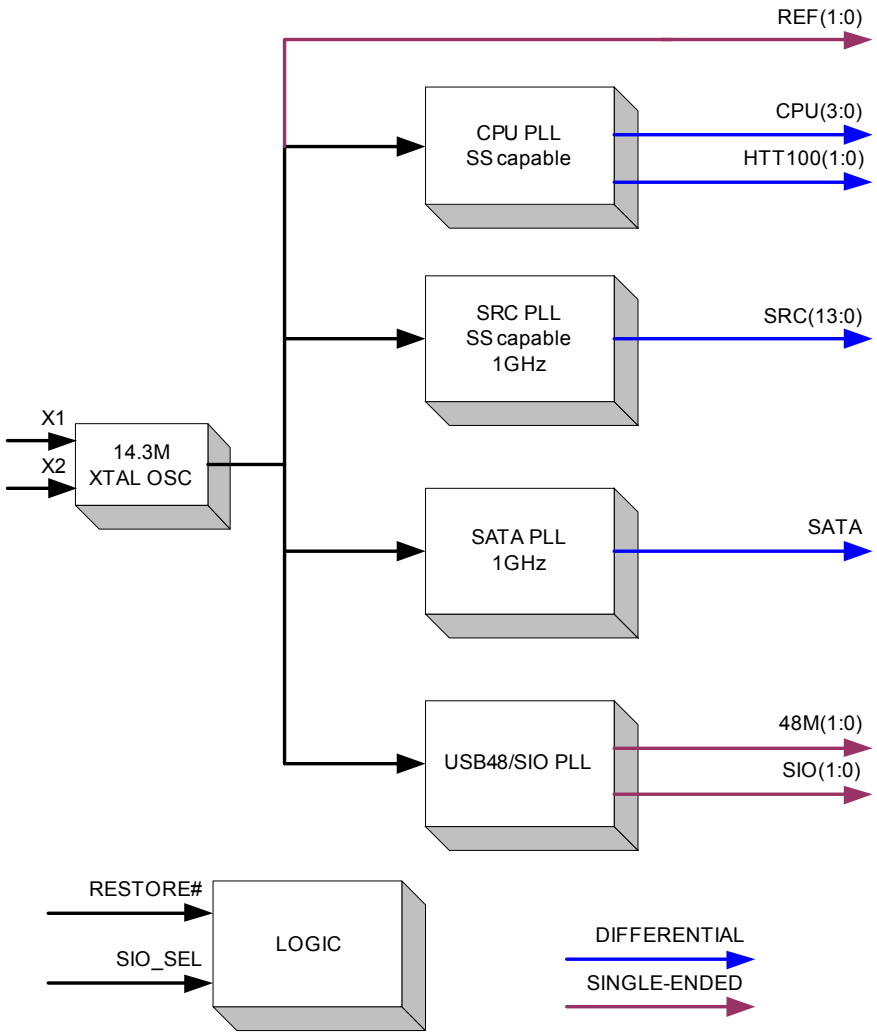
Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDDSATA_3.3	PWR	Power supply for SATA core logic, nominal 3.3V
2	SATAC_LPRS	OUT	Complement clock of low power differential SATA clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
3	SATAT_LPRS	OUT	True clock of low power differential SATA clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
4	GNDSATA	GND	Ground pin for the SATA output
5	CPUKG0C_LPRS	OUT	Complementary signal of low-power differential push-pull AMD "Greyhound" clock with integrated series resistor. (no 33 ohm series resistor needed and no 50 ohm pull down resistor needed)
6	CPUKG0T_LPRS	OUT	True signal of low-power differential push-pull AMD "Greyhound" CPU clock with integrated series resistor(no 33 ohm series resistor needed and no 50 ohm pull down resistor needed)
7	CPUKG1C_LPRS	OUT	Complementary signal of low-power differential push-pull AMD "Greyhound" CPU clock with integrated series resistor. (no 33 ohm series resistor needed and no 50 ohm pull down resistor needed)
8	CPUKG1T_LPRS	OUT	True signal of low-power differential push-pull AMD "Greyhound" CPU clock with integrated series resistor(no 33 ohm series resistor needed and no 50 ohm pull down resistor needed)
9	VDDCPU_3.3	PWR	Supply for CPU core and outputs, 3.3V nominal
10	GNDCPU	GND	Ground pin for the CPU outputs
11	CPUKG2C_LPRS	OUT	Complementary signal of low-power differential push-pull AMD "Greyhound" CPU clock with integrated series resistor. (no 33 ohm series resistor needed and no 50 ohm pull down resistor needed)
12	CPUKG2T_LPRS	OUT	True signal of low-power differential push-pull AMD "Greyhound" CPU clock with integrated series resistor(no 33 ohm series resistor needed and no 50 ohm pull down resistor needed)
13	CPUKG3C_LPRS	OUT	Complementary signal of low-power differential push-pull AMD "Greyhound" CPU clock with integrated series resistor. (no 33 ohm series resistor needed and no 50 ohm pull down resistor needed)
14	CPUKG3T_LPRS	OUT	True signal of low-power differential push-pull AMD "Greyhound" CPU clock with integrated series resistor(no 33 ohm series resistor needed and no 50 ohm pull down resistor needed)
15	RESTORE#	I/O	Open Drain I/O. As an input it restores the PLL's to power up default state. As an output, this signal is driven low when the internal watchdog hardware timer expires. It is cleared when the internal watchdog hardware timer is reset or disabled. The input is falling edge triggered. 0 = Restore Settings, 1 = normal operation.
16	HTT0C_LPRS	OUT	Complementary signal of low-power differential push-pull Hypertransport 3 clock with integrated series resistor. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
17	HTT0T_LPRS	OUT	True signal of low-power differential push-pull Hypertransport 3 clock with integrated series resistor. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
18	GNDHTT	PWR	Ground pin for the HTT outputs
19	VDDHTT_3.3	PWR	Supply for HTT clocks, nominal 3.3V.
20	HTT1C_LPRS	OUT	Complementary signal of low-power differential push-pull Hypertransport 3 clock with integrated series resistor. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
21	HTT1T_LPRS	OUT	True signal of low-power differential push-pull Hypertransport 3 clock with integrated series resistor. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
22	SMBCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
23	SMBDAT	I/O	Data pin for SMBus circuitry, 5V tolerant.
24	X1	IN	Crystal input, nominally 14.318MHz
25	X2	OUT	Crystal output, nominally 14.318MHz
26	VDDREF_3.3	PWR	Ref, XTAL power supply, nominal 3.3V
27	REF0	OUT	14.318 MHz reference clock, 3.3V
28	REF1	OUT	14.318 MHz reference clock, 3.3V
29	GNDREF	GND	Ground pin for the REF outputs.
30	GND48	GND	Ground pin for the 48MHz outputs
31	48MHz_0	OUT	48MHz clock output.
32	48MHz_1	OUT	48MHz clock output. (180 degrees out of phase with 48MHz_0)
33	VDD48_3.3	PWR	Power pin for the 48MHz and SIO outputs and core. 3.3V
34	SIO_0_1.8/SIO_SEL	I/O	Selectable 48MHz or 24MHz output/SIO Select Latched Input 0 = 24MHz, 1 = 48MHz.
35	SIO_1_1.8	OUT	Selectable 48MHz or 24MHz output. (180 out of phase with SIO 0. Selected by SIO latched input. 0 = 24MHz, 1 = 48MHz.
36	GNDSIO	GND	Ground pin for the SIO outputs

Pin Descriptions (cont.)

PIN #		PIN TYPE	DESCRIPTION
37	SRC0C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
38	SRC0T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
39	SRC1C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
40	SRC1T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
41	VDDSRC_3.3	PWR	Supply for SRC core and outputs, 3.3V nominal
42	GNDSRC	GND	Ground pin for the SRC outputs
43	SRC2C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
44	SRC2T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
45	SRC3C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
46	SRC3T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
47	SRC4C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
48	SRC4T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
49	GNDSRC	GND	Ground pin for the SRC outputs
50	VDDSRC_3.3	PWR	Supply for SRC core and outputs, 3.3V nominal
51	SRC5C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
52	SRC5T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
53	SRC6C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
54	SRC6T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
55	SRC7C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
56	SRC7T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
57	SRC8C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
58	SRC8T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
59	VDDSRC_3.3	PWR	Supply for SRC core and outputs, 3.3V nominal
60	GNDSRC	GND	Ground pin for the SRC outputs
61	SRC9C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
62	SRC9T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
63	SRC10C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
64	SRC10T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
65	SRC11C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
66	SRC11T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
67	GNDSRC	GND	Ground pin for the SRC outputs
68	VDDSRC_3.3	PWR	Supply for SRC core and outputs, 3.3V nominal
69	SRC12C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
70	SRC12T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
71	SRC13C_LPRS	OUT	Complement clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)
72	SRC13T_LPRS	OUT	True clock of low power differential SRC clock pair. (no 50 ohm shunt resistor to GND and no 33 ohm series resistor needed)

Block Diagram



932S890 Power Hookup

Pin Number		Description
VDD	GND	
1	4	SATA PLL and output
9	10	CPU PLL and outputs
19	18	HTT outputs
26	29	XTAL Osc and REF outputs
33	30	48MHz PLL and Outputs
33	36	SIO Outputs
41, 50, 59, 68	42, 49, 60, 67	SRC PLL and Outputs

Table 2: IO_Vout select table

B5b2	B5b1	B5b0	IO_Vout
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V
1	1	0	0.9V
1	1	1	1.0V

CPU Frequency Selection Table

Line	CPU FS4 Byte 3, bit 4 (Spread Enable)	CPU FS3 Byte 3, bit 3 (DN/CTR Spread)	CPU FS2 Byte3, bit2	CPU FS1 Byte3, bit1	CPU FS0 Byte3, bit0	CPU Speed (MHz)	HTT Speed (MHz)	Spread %
0	0	0	0	0	0	184.47	92.24	SS OFF 0%
1	0	0	0	0	1	188.24	94.12	
2	0	0	0	1	0	192.08	96.04	
3	0	0	0	1	1	196.00	98.00	
4	**0**	**0**	**1**	**0**	**0**	200.00	100.00	
5	0	0	1	0	1	204.00	102.00	
6	0	0	1	1	0	208.08	104.04	
7	0	0	1	1	1	212.24	106.12	
8	0	1	0	0	0	184.47	92.24	SS OFF 0%
9	0	1	0	0	1	188.24	94.12	
10	0	1	0	1	0	192.08	96.04	
11	0	1	0	1	1	196.00	98.00	
12	0	1	1	0	0	200.00	100.00	
13	0	1	1	0	1	204.00	102.00	
14	0	1	1	1	0	208.08	104.04	
15	0	1	1	1	1	212.24	106.12	
16	1	0	0	0	0	184.47	92.24	DOWN SPREAD'-0.5%
17	1	0	0	0	1	188.24	94.12	
18	1	0	0	1	0	192.08	96.04	
19	1	0	0	1	1	196.00	98.00	
20	1	0	1	0	0	200.00	100.00	
21	1	0	1	0	1	204.00	102.00	
22	1	0	1	1	0	208.08	104.04	
23	1	0	1	1	1	212.24	106.12	
24	1	1	0	0	0	184.47	92.24	CENTER SPREAD '+/-0.25%
25	1	1	0	0	1	188.24	94.12	
26	1	1	0	1	0	192.08	96.04	
27	1	1	0	1	1	196.00	98.00	
28	1	1	1	0	0	200.00	100.00	
29	1	1	1	0	1	204.00	102.00	
30	1	1	1	1	0	208.08	104.04	
31	1	1	1	1	1	212.24	106.12	

SRC Frequency Selection Table

Line	SRC FS4 Byte 4, bit 4 (Spread Enable)	SRC FS3 Byte 4, bit 3 (DWN/CTR Spread)	SRC FS2 Byte 4, bit2	SRC FS1 Byte 4, bit1	SRC FS0 Byte 4, bit0	SRC (MHz)	Sprd %
0	0	0	0	0	0	92.24	SS OFF 0%
1	0	0	0	0	1	94.12	
2	0	0	0	1	0	96.04	
3	0	0	0	1	1	98.00	
4	**0**	**0**	**1**	**0**	**0**	100.00	
5	0	0	1	0	1	102.00	
6	0	0	1	1	0	104.04	
7	0	0	1	1	1	106.12	
8	0	1	0	0	0	92.24	SS OFF 0%
9	0	1	0	0	1	94.12	
10	0	1	0	1	0	96.04	
11	0	1	0	1	1	98.00	
12	0	1	1	0	0	100.00	
13	0	1	1	0	1	102.00	
14	0	1	1	1	0	104.04	
15	0	1	1	1	1	106.12	
16	1	0	0	0	0	92.24	DOWN SPREAD'- 0.5%
17	1	0	0	0	1	94.12	
18	1	0	0	1	0	96.04	
19	1	0	0	1	1	98.00	
20	1	0	1	0	0	100.00	
21	1	0	1	0	1	102.00	
22	1	0	1	1	0	104.04	
23	1	0	1	1	1	106.12	
24	1	1	0	0	0	92.24	CENTER SPREAD '+/-0.25%
25	1	1	0	0	1	94.12	
26	1	1	0	1	0	96.04	
27	1	1	0	1	1	98.00	
28	1	1	1	0	0	100.00	
29	1	1	1	0	1	102.00	
30	1	1	1	1	0	104.04	
31	1	1	1	1	1	106.12	

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 932S890C. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDDxxx	-		3.3	GND + 3.9V	V	1
Storage Temperature	Ts	-	-65		150	°C	1
Ambient Operating Temp	Tambient	-	0		70	°C	1
Case Temperature	Tcase	-			115	°C	1
Input ESD protection HBM	ESD prot	-	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics–Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
3.3V Core Supply Voltage	VDDxxx	-	3.135	3.3	3.465	V	1
Input High Voltage	V_{IH}	VDD = 3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	VDD = 3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Operating Current	$I_{DD3.3OP}$	all outputs driven			250	mA	1
Input Frequency	F_i	VDD = 3.3 V +/-5%		14.31818		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From VDD Power-Up to 1st clock			1.8	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
SMBus Voltage	V_{DDSMB}		2.7		5.5	V	1
Low-level Output Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	$I_{PULLUPSMB}$		4	6		mA	1
SMBCLK/SMBDAT Clock/Data Rise Time	T_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SMBCLK/SMBDAT Clock/Data Fall Time	T_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Input frequency should be measured at the REF pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.

AC Electrical Characteristics–Low-Power DIF Outputs: CPUKG and HTT

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Crossing Point Variation	ΔV_{CROSS}	Single-ended Measurement			140	mV	1,2,5
CPU Frequency (HTT = 1/2 of CPU Frequency)	f_{CPU}	Spread Specturm On	198.8		200	MHz	1,3
Long Term Accuracy	ppm	Spread Specturm Off	-50		+50	ppm	1,11
Rising Edge Slew Rate	S_{RISE}	Differential Measurement	0.5		10	V/ns	1,4
Falling Edge Slew Rate	S_{FALL}	Differential Measurement	0.5		10	V/ns	1,4
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement			20	%	1
CPU, DIF HTT Jitter - Cycle to Cycle	$CPUJ_{C2C}$	Differential Measurement			150	ps	1,6
Accumulated Jitter	t_{JACC}	See Notes			1	ns	1,7
Peak to Peak Differential Voltage	$V_{D(PK-PK)}$	Differential Measurement	400		2400	mV	1,8
Differential Voltage	V_D	Differential Measurement	200		1200	mV	1,9
Duty Cycle	D_{CYC}	Differential Measurement	45		55	%	1
Amplitude Variation	ΔV_D	Change in V_D DC cycle to cycle	-75		75	mV	1,10
CPU[3:0] Skew	CPU_{SKEW30}	Differential Measurement			200	ps	1
HTT[1:0] Skew	HTT_{SKEW10}	Differential Measurement			100	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Single-ended measurement at crossing point. Value is maximum – minimum over all time. DC value of common mode is not important due to the blocking cap.

[3] Minimum Frequency is a result of 0.5% down spread spectrum

[4] Differential measurement through the range of ±100 mV, differential signal must remain monotonic and within slew rate spec when crossing through this region.

[5] Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.

[6] Max difference of t_{CYCLE} between any two adjacent cycles.

[7] Accumulated tjc over a 10 µs time period, measured with JIT2 TIE at 50ps interval.

[8] VD(PK-PK) is the overall magnitude of the differential signal.

[9] VD(min) is the amplitude of the ring-back differential measurement, guaranteed by design, that ring-back will not cross 0V VD. VD(max) is the largest amplitude allowed.

[10] The difference in magnitude of two adjacent VD_DC measurements. VD_DC is the stable post overshoot and ring-back part of the signal.

[11] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

AC Electrical Characteristics–Low-Power DIF Outputs: SRC, SATA

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SRC/SATA Frequency	f_{SRC_SATA}	Spread Specturm Off		100		MHz	1,6
Long Term Accuracy	ppm	Spread Specturm Off	-50		+50	ppm	1,6
Rising Edge Slew Rate	t_{SLR}	Differential Measurement	2.5		8	V/ns	1,2
Falling Edge Slew Rate	t_{FLR}	Differential Measurement	2.5		8	V/ns	1,2
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement			20	%	1
Maximum Output Voltage	V_{HIGH}	Includes overshoot			1150	mV	1
Minimum Output Voltage	V_{LOW}	Includes undershoot	-300			mV	1
Differential Voltage Swing	V_{SWING}	Differential Measurement	300			mV	1
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300		550	mV	1,3,4
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement			140	mV	1,3,5
Duty Cycle	D_{CYC}	Differential Measurement	45		55	%	1
Jitter - Cycle to Cycle	$SRCJ_{C2C}$	Differential Measurement			125	ps	1
SRC[13:0] Skew Even Outputs	SRC_{SKEW_E}	Differential Measurement			200	ps	1,8
SRC[13:0] Skew Odd Outputs	SRC_{SKEW_O}	Differential Measurement			200	ps	1,8
SRC[13:0] Even to Odd Skew	SRC_{SKEW}	Differential Measurement	1275	1375	1475	ps	1,8
Jitter, Phase	$t_{jphaseSRC}$	PCIe Gen 1 specs (1.5 - 22 MHz)		40	86	ps	1, 7
		PCIe Gen 2 (8-16 MHz, 5-16 MHz) Lo-band content (10kHz to 1.5MHz)		1.6	3	ps rms	1, 7
		PCIe Gen 2 (8-16 MHz, 5-16 MHz) Hi-band content (1.5MHz to Nyquist)		2.6	3.1	ps rms	1, 7

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through Vswing centered around differential zero

[3] Vxabs is defined as the voltage where CLK = CLK#

[4] Only applies to the differential rising edge (CLK rising and CLK# falling)

[5] Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.

[6] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[7] Applicable to all SRC outputs. See http://www.pcisig.com for complete specs. Guaranteed by design and characterization, not tested in production.

[8] SRC outputs are divided into two banks, odd and even. The odd bank skew window is 200 ps. The even bank skew window is 200ps. The skew between the even and odd banks is intentionally set at 1375ps.

Electrical Characteristics–USB - 48MHz, SIO 48/24MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-50		+50	ppm	1,2
Clock period	T_{PERIOD}	USB output nominal	20.702	20.833	20.964	ns	3,5
Clock Low Time	T_{LOW}	Measure from < 0.6V	9.375		11.458	ns	3
Clock High Time	T_{HIGH}	Measure from > 2.0V	9.375		11.458	ns	3
Rise Time	t_{r_USB}	V_{OL} = 20% of Voh, V_{OH} = 80%of Voh	0.5		3	ns	1
Fall Time	t_{f_USB}	V_{OL} = 20% of Voh, V_{OH} = 80%of Voh	0.5		3	ns	1
Output High Voltage	V_{OHUSB}	I_{OH} = -1 mA	2.4			V	1,3
Output Low Voltage	V_{OLUSB}	I_{OL} = 1 mA			0.4	V	1,3
Output High Voltage	V_{OHSIO}	I_{OH} = -0.2 mA	1.8	2	2.2	V	1,4
Output Low Voltage	V_{OLSIO}	I_{OL} = 0.2 mA			0.4	V	1,4
Duty Cycle	d_{CYCUSB}	V_T = 1.5 V	45		55	%	1,3
Skew	t_{SKEW}	V_T = 1.5 V			250	ps	1
Jitter, Cycle to cycle	$t_{jCYC-CYC}$	V_T = 1.5 V			130	ps	1,3

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]IDT recommended and/or chipset vendor layout guidelines must be followed to meet this specification

[3]Applies to USB outputs only

[4]Applies to SIO outputs only

[5]SIO 24MHz outputs are 1/2 of USB48MHz frequency (twice the period). Includes cycle to cycle jitter.

Electrical Characteristics–REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-50		+50	ppm	1,2
Long Term Jitter	t_{jLT}	@ 1us			500	ps	1,2
Clock period	T_{PERIOD}	14.318MHz output nominal	69.6378	69.8413	70.0448	ns	2,3
Clock Low Time	T_{LOW}	Measure from V_T = 50%	2			ns	2
Clock High Time	T_{HIGH}	Measure from V_T = 50%	2			ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4	2.8	3.3	V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA	0		0.4	V	1
Rise Time	t_R	V_{OL} = 20% of V_{OH}, V_{OH} = 80%of V_{OH}			1.5	ns	1
Fall Time	t_F	V_{OL} = 20% of V_{OH}, V_{OH} = 80%of V_{OH}			1.5	ns	1
Skew	t_{SKEW}	Measure from V_T = 50%			250	ps	1
Duty Cycle	d_{t1}	$V_T = V_{OH}/2$	45		55	%	1
Jitter, Cycle to Cycle	$t_{jCYC-CYC}$	Measure from V_T = 50%			200	ps	1
Jitter, Peak to Peak	t_{jPK-PK}	Measure from V_T = 50% (0.9V) $t_{jpk-pk} = [\|t_{jcyc-cyc}max\| + \|t_{jcyc-cyc}min\|]/2$			200	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

[3] Includes cycle to cycle jitter.

Clock Periods–Differential Outputs with Spread Spectrum Enabled

Measurement Window		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Symbol		Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+		
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
		Minimum Absolute Period	Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum	Units	Notes
Signal Name	HTT/SRC 100	9.87456	9.99956	10.02456	10.02506	10.02556	10.05056	10.17556	ns	1,2
	CPU 200	4.84978	4.99978	5.01228	5.01253	5.01278	5.02528	5.17528	ns	1,2

Clock Periods–Differential Outputs with Spread Spectrum Disabled

Measurement Window		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Symbol		Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+		
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
		Minimum Absolute Period	Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum	Units	Notes
Signal Name	SRC 100	9.87450		9.99950	10.00000	10.00050		10.12550	ns	1,2
	SATA 100	9.87450		9.99950	10.00000	10.00050		10.12550	ns	1,2
	CPU 200	4.84975		4.99975	5.00000	5.00025		5.15025	ns	1,2

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Read Address	Write Address
$D3_{(H)}$	$D2_{(H)}$

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Output Enable Control Register

Byte	0	Name	Description	Type	0	1	Default
	Bit 7	HTT1_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 6	HTT0_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 5	REF0_OE	Output Enable	RW	Low	Enabled	1
	Bit 4	REF1_OE	Output Enable	RW	Low	Enabled	1
	Bit 3	SIO_0_OE	Output Enable	RW	**Hi-Z**	Enabled	1
	Bit 2	SIO_1_OE	Output Enable	RW	Low	Enabled	1
	Bit 1	48MHz_1_OE	Output Enable	RW	Low	Enabled	1
	Bit 0	48MHz_0_OE	Output Enable	RW	Low	Enabled	1

SMBus Table:Output Enable Control Register

Byte	1	Name	Control Function	Type	0	1	Default
	Bit 7	SRC13_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 6	SRC12_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 5	SRC11_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 4	SRC10_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 3	SRC9_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 2	SRC8_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 1	SRC7_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 0	SRC6_OE	Output Enable	RW	Low/Low	Enabled	1

SMBus Table: Output Enable Control Register

Byte	2	Name	Control Function	Type	0	1	Default
	Bit 7	SRC5_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 6	SRC4_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 5	SRC3_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 4	SRC2_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 3	SRC1_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 2	SRC0_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 1	SATA_OE	Output Enable	RW	Low/Low	Enabled	1
	Bit 0	CPU0_OE	Output Enable	RW	Low/Low	Enabled	1

SMBus Table: CPU/HTT Frequency and Output Enable Control Register

Byte	3	Name	Control Function	Type	0	1	Default
	Bit 7	CPU3_OE	Output enable	RW	Low/Low	Enabled	1
	Bit 6	CPU2_OE	Output enable	RW	Low/Low	Enabled	1
	Bit 5	CPU1_OE	Output enable	RW	Low/Low	Enabled	1
	Bit 4	CPU SS Enable	Spread Enable	RW	SS Off	SS On	0
	Bit 3	CPU Spread Type	Down or Center Spread	RW	0.5% Down Spread	0.5% Center Spread (+/-0.25%)	0
	Bit 2	CPU_FS2	CPU Frequency Select	RW	See CPU Frequency Select Table Default value corresponds to 200MHz. Note that HTT frequency tracks the CPU frequency and is equal to 1/2 for CPU.		1
	Bit 1	CPU_FS1	CPU Frequency Select	RW			0
	Bit 0	CPU_FS0	CPU Frequency Select LSB	RW			0

SMBus Table: SRC Frequency Control Register

Byte	4	Name	Control Function	Type	0	1	Default
	Bit 7	Reserved					0
	Bit 6	Reserved					0
	Bit 5	Reserved					0
	Bit 4	SRC SS Enable	Spread Enable	RW	SS Off	SS On	0
	Bit 3	SRC Spread Type	Down or Center Spread	RW	0.5% Down Spread	0.5% Center Spread	0
	Bit 2	SRC_FS2	SRC Frequency Select	RW	See SRC Frequency Select Table Default Corresponds to 100MHz		1
	Bit 1	SRC_FS1	SRC Frequency Select	RW			0
	Bit 0	SRC_FS0	SRC Frequency Select LSB	RW			0

SMBus Table: N-Step Select and SIO Readback Register

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	SIO_SEL	Selects 24MHz or 48MHz	R	24MHz	48MHz	Latch
Bit 6	CPU M/N En	CPU PLL M/N Prog. Enable	RW	M/N Prog. Disabled	M/N Prog. Enabled	0
Bit 5	SRC M/N En	SRC M/N Prog.Enable	RW	M/N Prog. Disabled	M/N Prog. Enabled	0
Bit 4	Test_Sel	Selects Test Mode	RW	Normal mode	All ouputs are REF/N	0
Bit 3	Reserved					0
Bit 2	IO_VOUT2	IO Output Voltage Select (Most Significant Bit)	RW	See Table 2: V_IO Selection (Default is 0.8V)		1
Bit 1	IO_VOUT1	IO Output Voltage Select	RW			0
Bit 0	IO_VOUT0	IO Output Voltage Select (Least Significant Bit)	RW			1

SMBus Table: Byte Count Register

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	BC5	Byte Count bit 5 (MSB)	RW	Determines the number of bytes that are read back from the device. Default is 08 hex.		0
Bit 4	BC4	Byte Count bit 4	RW			0
Bit 3	BC3	Byte Count bit 3	RW			1
Bit 2	BC2	Byte Count bit 2	RW			0
Bit 1	BC1	Byte Count bit 1	RW			0
Bit 0	BC0	Byte Count bit 0 (LSB)	RW			0

SMBus Table: Device ID register

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	Device ID7	Device ID	R	89 hex for 932S820		x
Bit 6	Device ID6		R			x
Bit 5	Device ID5		R			x
Bit 4	Device ID4		R			x
Bit 3	Device ID3		R			x
Bit 2	Device ID2		R			x
Bit 1	Device ID1		R			x
Bit 0	Device ID0		R			x

SMBus Table: Vendor & Revision ID Register

Byte 8	Name	Control Function	Type	0	1	Default
Bit 7	RID3	REVISION ID	R	Rev A = 0000 Rev B = 0001 Rev C = 0010		x
Bit 6	RID2		R			x
Bit 5	RID1		R			x
Bit 4	RID0		R			x
Bit 3	VID3	VENDOR ID	R	-	-	0
Bit 2	VID2		R	-	-	0
Bit 1	VID1		R	-	-	0
Bit 0	VID0		R	-	-	1

SMBus Table: WatchDog Timer Control Register

Byte 9	Name	Control Function	Type	0	1	Default
Bit 7	HWD_EN	Watchdog Hard Alarm Enable	RW	Disable and Reload Hartd Alarm Timer, Clear WD Hard status bit.	Enable Timer	0
Bit 6	SWD_EN	Watchdog Soft Alarm Enable	RW	Disable	Enable	0
Bit 5	WD Hard Status	WD Hard Alarm Status	R	Normal	Alarm	X
Bit 4	WD Soft Status	WD Soft Alarm Status	R	Normal	Alarm	X
Bit 3	WDTCtrl	Watch Dog Alarm Time base Control	RW	290ms Base	1160ms Base	0
Bit 2	HWD2	WD Hard Alarm Timer Bit 2	RW	These bits represent the number of Watch Dog Time Base Units that pass before the Watch Alarm expires. Default is 7 X 290ms = 2s.		1
Bit 1	HWD1	WD Hard Alarm Timer Bit 1	RW			1
Bit 0	HWD0	WD Hard Alarm Timer Bit 0	RW			1

SMBus Table: WD Timer Safe Frequency Control Register

Byte	10	Name	Control Function	Type	0	1	Default
	Bit 7	SWD2	WD Soft Alarm Timer Bit 2	RW	These bits represent the number of Watch Dog Time Base Units that pass before the Watch Alarm expires. Default is 7 X 290ms = 2s.		1
	Bit 6	SWD1	WD Soft Alarm Timer Bit 1	RW			1
	Bit 5	SWD0	WD Soft Alarm Timer Bit 0	RW			1
	Bit 4	WD SF4	Watch Dog Hard Alarm Safe Freq Programming bits	RW	These bits configure the safe frequency that the device returns to if the Watchdog Hardware Timer expires. The value show here corresponds to the power up default of the device. See the various Frequency Select Tables for the exact frequencies.		0
	Bit 3	WD SF3		RW			0
	Bit 2	WD SF2		RW			1
	Bit 1	WD SF1		RW			0
	Bit 0	WD SF0		RW			0

SMBus Table: CPU PLL Frequency Control Register

Byte	11	Name	Control Function	Type	0	1	Default
	Bit 7	N Div2	N Divider Prog bit 2	RW	The decimal representation of M and N Divider in Byte 16 and 17 will configure the VCO frequency. Default at power up = Byte 3 Rom table. See M/N Caculation Tables for VCO frequency formulas.		X
	Bit 6	N Div1	N Divider Prog bit 1	RW			X
	Bit 5	M Div5	M Divider Programming bits	RW			X
	Bit 4	M Div4		RW			X
	Bit 3	M Div3		RW			X
	Bit 2	M Div2		RW			X
	Bit 1	M Div1		RW			X
	Bit 0	M Div0		RW			X

SMBus Table: CPU PLL Frequency Control Register

Byte	12	Name	Control Function	Type	0	1	Default
	Bit 7	N Div10	N Divider Programming b(10:3)	RW	The decimal representation of M and N Divider in Byte 16 and 17 will configure the VCO frequency. Default at power up = Byte 3 Rom table. See M/N Caculation Tables for VCO frequency formulas.		X
	Bit 6	N Div9		RW			X
	Bit 5	N Div8		RW			X
	Bit 4	N Div7		RW			X
	Bit 3	N Div6		RW			X
	Bit 2	N Div5		RW			X
	Bit 1	N Div4		RW			X
	Bit 0	N Div3		RW			X

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte	13	Name	Control Function	Type	0	1	Default
	Bit 7	SSP7	Spread Spectrum Programming b(7:0)	RW	These bits set the CPU spread pecentage.Please contact IDT for the appropriate values.		X
	Bit 6	SSP6		RW			X
	Bit 5	SSP5		RW			X
	Bit 4	SSP4		RW			X
	Bit 3	SSP3		RW			X
	Bit 2	SSP2		RW			X
	Bit 1	SSP1		RW			X
	Bit 0	SSP0		RW			X

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte	14	Name	Control Function	Type	0	1	Default
	Bit 7	SSP15	Spread Spectrum Programming b(15:8)	RW	These bits set the CPU spread pecentage.Please contact IDT for the appropriate values.		X
	Bit 6	SSP14		RW			X
	Bit 5	SSP13		RW			X
	Bit 4	SSP12		RW			X
	Bit 3	SSP11		RW			X
	Bit 2	SSP10		RW			X
	Bit 1	SSP9		RW			X
	Bit 0	SSP8		RW			X

Note: If CLKREQA and CLKREQB are both selected to control an output, the control condition is an OR function. CLKREQA# = 0 OR CLKREQB = 0 results in the controlled output running.

SMBUS Table: SRC Frequency Control Register

Byte	15	Name	Control Function	Type	0	1	Default
	Bit 7	N Div2	N Divider Prog bit 2	RW	The decimal representation of M and N Divider in Byte 15 and 16 configure the SRC VCO frequency. See M/N Caculation Tables for VCO frequency formulas.		X
	Bit 6	N Div1	N Divider Prog bit 1	RW			X
	Bit 5	M Div5	M Divider Programming bit (5:0)	RW			X
	Bit 4	M Div4		RW			X
	Bit 3	M Div3		RW			X
	Bit 2	M Div2		RW			X
	Bit 1	M Div1		RW			X
	Bit 0	M Div0		RW			X

SMBUS Table: SRC Frequency Control Register

Byte	16	Name	Control Function	Type	0	1	Default
	Bit 7	N Div10	N Divider Programming Byte16 bit(7:0) and Byte15 bit(7:6)	RW	The decimal representation of M and N Divider in Byte 15 and 16 configure the SRC VCO frequency. See M/N Caculation Tables for VCO frequency formulas.		X
	Bit 6	N Div9		RW			X
	Bit 5	N Div8		RW			X
	Bit 4	N Div7		RW			X
	Bit 3	N Div6		RW			X
	Bit 2	N Div5		RW			X
	Bit 1	N Div4		RW			X
	Bit 0	N Div3		RW			X

SMBUS Table: SRC Spread Spectrum Control Register

Byte	17	Name	Control Function	Type	0	1	Default
	Bit 7	SSP7	Spread Spectrum Programming bit(7:0)	RW	These bits set the SRC spread pecentages.Please contact IDT for the appropriate values.		X
	Bit 6	SSP6		RW			X
	Bit 5	SSP5		RW			X
	Bit 4	SSP4		RW			X
	Bit 3	SSP3		RW			X
	Bit 2	SSP2		RW			X
	Bit 1	SSP1		RW			X
	Bit 0	SSP0		RW			X

SMBUS Table: SRC Spread Spectrum Control Register

Byte	18	Name	Control Function	Type	0	1	Default
	Bit 7	SSP15	Spread Spectrum Programming bit(15:8)	RW	These bits set the SRC spread pecentages.Please contact IDT for the appropriate values.		X
	Bit 6	SSP14		RW			X
	Bit 5	SSP13		RW			X
	Bit 4	SSP12		RW			X
	Bit 3	SSP11		RW			X
	Bit 2	SSP10		RW			X
	Bit 1	SSP9		RW			X
	Bit 0	SSP8		RW			X

SMBus Table: SRC N Divider Control Register

Byte	19	Name	Control Function	Type	0	1	Default
	Bit 7	SRC NDiv0	LSB N Divider Programming	RW	N Divider LSB (bit 0) for SRC M/N programming.		X
	Bit 6	Reserved					0
	Bit 5	Reserved					0
	Bit 4	Reserved					0
	Bit 3	Reserved					0
	Bit 2	Reserved					0
	Bit 1	Reserved					0
	Bit 0	Reserved					0

SMBUS Table: CPU Output Divider Register

Byte	20	Name	Control Function	Type	0	1	Default
	Bit 7	CPU NDiv0	LSB N Divider Programming	RW	Byte 20 has the N Divider LSB (bit 0) for CPU M/N		X
	Bit 6	Reserved					0
	Bit 5	Reserved					0
	Bit 4	Reserved					0
	Bit 3	CPUDiv3	CPU Divider Ratio Programming Bits	RW	0000:/2 ; 0100:/4	1000:/8 ; 1100:/16	X
	Bit 2	CPUDiv2		RW	0001:/3 ; 0101:/6	1001:/12 ; 1101:/24	X
	Bit 1	CPUDiv1		RW	0010:/5 ; 0110:/10	1010:/20 ; 1110:/40	X
	Bit 0	CPUDiv0		RW	0011:/9 ; 0111:/18	1011:/36 ; 1111:/72	X

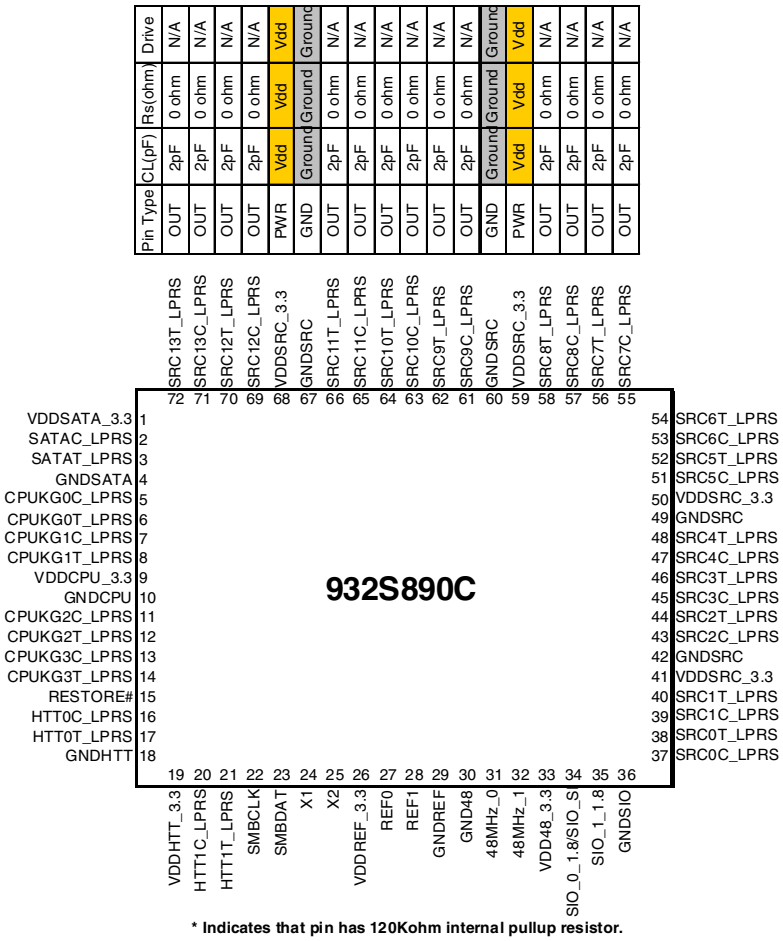
Bytes 21 to 63 Are Reserved

CPU, SRC and PCI Divider Ratios

Div(3:0)	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
Divider	2	3	5	15	4	6	10	30	8	12	20	60	16	24	40	120

Drive Strength and Terminations

Drive	Rs(ohm)	CL(pF)	Pin Type
Vdd	Vdd	Vdd	PWR
N/A	0 ohm	2pF	OUT
N/A	0 ohm	2pF	OUT
Ground	Ground	Ground	GND
N/A	0 ohm	2pF	OUT
N/A	0 ohm	2pF	OUT
N/A	0 ohm	2pF	OUT
N/A	0 ohm	2pF	OUT
Vdd	Vdd	Vdd	PWR
Ground	Ground	Ground	GND
N/A	0 ohm	2pF	OUT
N/A	0 ohm	2pF	OUT
N/A	0 ohm	2pF	OUT
N/A	0 ohm	2pF	OUT
I/O	I/O	I/O	I/O
N/A	0 ohm	2pF	OUT
N/A	0 ohm	2pF	OUT
Ground	Ground	Ground	PWR

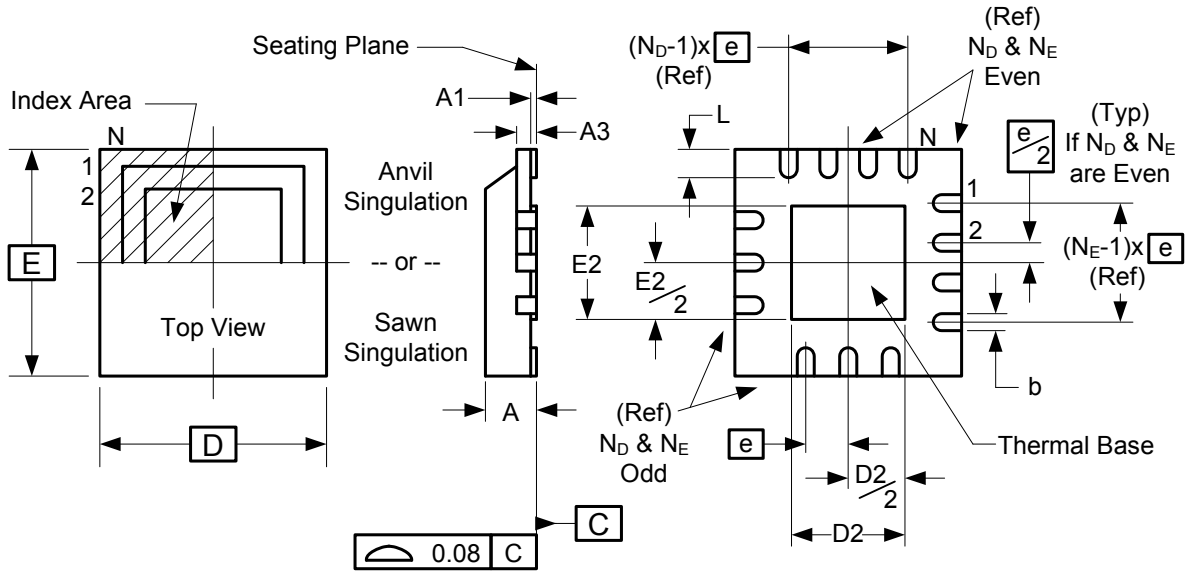


*** Indicates that pin has 120Kohm internal pullup resistor.**

Pin Type	CL(pF)	Rs(ohm)
OUT	2pF	0 ohm
OUT	2pF	0 ohm
OUT	2pF	0 ohm
OUT	2pF	0 ohm
PWR	Vdd	Vdd
GND	Ground	Ground
OUT	2pF	0 ohm
OUT	2pF	0 ohm
OUT	2pF	0 ohm
OUT	2pF	0 ohm
OUT	2pF	0 ohm
OUT	2pF	0 ohm
GND	Ground	Ground
PWR	Vdd	Vdd
OUT	2pF	0 ohm
OUT	2pF	0 ohm
OUT	2pF	0 ohm
OUT	2pF	0 ohm

Resistor values are for default drive strength driving a single transmission line with
Zo = 50 ohms!

Package Outline and Package Dimensions (72-pin MLF)



	Millimeters	
Symbol	**Min**	**Max**
A	0.8	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.3
e	0.50 BASIC	
D x E BASIC	10.00 x 10.00	
D2 MIN./MAX.	5.75	6.15
E2 MIN./MAX.	5.75	6.15
L MIN./MAX.	0.3	0.5
N_D	18	
N_E	18	

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
932S890CKLF	see page 13	Trays	72-pin MLF	0 to +70° C
932S890CKLFT		Tape and Reel	72-pin MLF	0 to +70° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“C” is the device revision designator (will not correlate with the datasheet revision).

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Revision History

Rev.	Issue Date	Who	Description	Page #
A	1/15/2009	RDW	Updates to pin descriptions, electrical tables, power tables, release to final	Various
B	2/26/2009	RDW	Updates to pin 71 & 72 descriptions.	3
C	2/10/2011	RDW	1. Updated PPM tolerances to +/-50ppm from +/-100ppm 2. Updated clock periods to reflect this. 3. Added footnote 3 to 14.318M Electrical Table 4. Updated ppm reference on page 1 to reflect this. 5. Added clock periods table after page 10.	1,8,9,10,19
D	5/20/2011	RDW	Updated to new datasheet template.	Various

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