CUI INC®

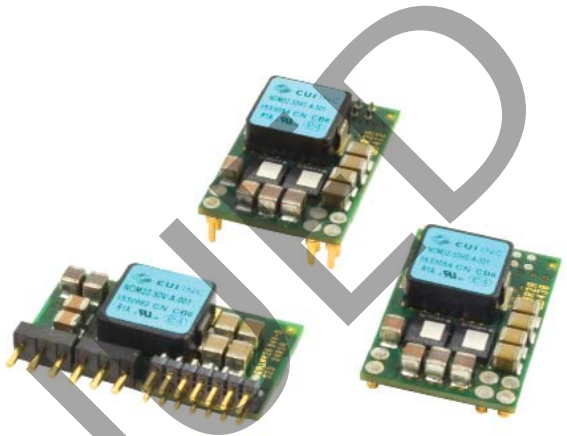
SERIES: NDM2Z-50 | **DESCRIPTION**: AUTO COMPENSATED, DIGITAL DC-DC POL CONVERTER

GENERAL CHARACTERISTICS

- 4.5~14 V input range
- 0.6~3.3 V programmable output
- voltage tracking
- voltage margining
- active current sharing
- *Snapshot*™ parametric capture
- voltage/current/temperature monitoring
- synchronization and phase spreading
- remote differential voltage sense
- programmable soft start and soft stop
- fault management

FEATURES

- pin and function compatible with Architects of Modern Power™ product standards
- compact package, horizontal: 30.85 x 20.0 x 8.2 mm
- compact package, vertical: 33.0 x 7.60 x 18.1 mm
- 50 A output
- high efficiency
- auto compensation
- SMBus interface
- PMBus™ Compatible



AMP™ Architects of Modern Power PMBus RoHS

DISCONTINUED

MODEL

MODEL	input voltage (Vdc)	output voltage (Vdc)	output current max (A)	output wattage max (W)
NDM2Z-50	4.5~14	0.6~3.3	50	165

PART NUMBER KEY

NDM2Z-50 X - X - XXX

- Base Number
- Module Orientation and Pin Style:
  HS = horizontal, surface mount
  HT = horizontal, through hole mount
  V = vertical
- Pin Configuration:
  A = 3.56 mm pin length (HT)
  4.0 mm pin length (V)
  B = 5.5 mm pin length (V)
- Firmware Configuration:
  000~ZZZ

Example part number: **NDM2Z-50V-A-002**

vertical module
4.00 mm pin length
firmware configuration 002

* HS and HT modules are delivered on tape and reel
* V modules are delivered in trays

ABSOLUTE MAXIMUM RATINGS

parameter	conditions/description	min	typ	max	units
operating temperature (see thermal consideration section) (T_{P1}, T_{P2})		-40		125	°C
storage temperature (T_S)		-40		125	°C
input voltage (see operating information section for input and output voltage relations)(V_I)		-0.3		16	V
logic I/O voltage	CTRL, SA0, SA1, SALERT, SCL, SDA, VSET, SYNC, DDC, PG	-0.3		6.5	V
ground voltage differential	-S, PREF, GND	-0.3		0.3	V
analog pin voltage	V_O, +S, VTRK	-0.3		6.5	V

Notes: Stress in excess of Absolute Maximum Ratings may cause permanent damage. Absolute Maximum Ratings, sometimes referred to as no destruction limits, are normally tested with one parameter at a time exceeding the limits in the Electrical Specification. If exposed to stress above these limits, function and performance may degrade in an unspecified manner.

Configuration File

This product is designed with a digital control circuit. The control circuit uses a configuration file which determines the functionality and performance of the product. The Electrical Specification table shows parameter values of functionality and performance with the default configuration file, unless otherwise specified. The default configuration file is designed to fit most application needs with focus on high efficiency. If different characteristics are required it is possible to change the configuration file to optimize certain performance characteristics. Note that current sharing operation requires changed configuration file.

PRODUCT ELECTRICAL SPECIFICATION, HORIZONTAL

T_{P1} = -30 to +95 °C, V_I = 4.5 to 14 V, V_I> V_O + 1.0 V
Typical values given at: T_{P1} = +25 °C, V_I = 12.0 V, max I_O, unless otherwise specified under conditions.
External C_{IN} = 470 µF/10 mΩ, C_{OUT} = 470 µF/10 mΩ. See Operating Information section for selection of capacitor types.
Sense pins are connected to the output pins.

parameter	conditions/description	min	typ	max	units
input voltage rise time (V_I)	monotonic			2.4	V/ms
output voltage without pin-strap (V_O)			1.2		V
output voltage adjustment range (V_O)		0.60		3.3	V
output voltage adjustment including margining (V_O)	see note 17	0.54		3.63	V
output voltage set-point resolution (V_O)			±0.025		%FS
output voltage accuracy (V_O)	including line, load, temp see note 14	-1		1	%
	current sharing operation see note 15	-2		2	%
internal resistance +S/-S to VOUT/GND (V_O)			47		Ω
line regulation (V_O)	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V		2 2 2 3		mV mV mV mV
load regulation (V_O) I_O = 0~100%	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V		2 2 2 2		mV mV mV mV
output ripple & noise (V_{oac}) C_O= 470 µF (minimum external capacitance) see note 11	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V		20 25 30 35		mVp-p mVp-p mVp-p mVp-p

DISCONTINUED

PRODUCT ELECTRICAL SPECIFICATION, HORIZONTAL (CONTINUED)

parameter	conditions/description		min	typ	max	units
output current (I_O)	see note 18		0.001		50	A
static input current at max I_O (I_S)	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V			3.10 4.80 8.19 14.53		A A A A
current limit threshold (I_{lim})			52		65	A
short circuit current(I_{SC})	RMS, hiccup mode, see note 3	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V		11 9 7 6		A A A A
efficiency (η)	50% of max I_O	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V		85.6 90.4 93.7 95.7		% % % %
	max I_O	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V		80.5 86.9 91.6 94.6		% % % %
power dissipation at max I_O (P_d)	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V			7.25 7.54 8.28 9.36		W W W W
input idling power (no load)(P_{li})	default configuration: continues conduction mode, CCM	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V		0.90 0.90 1.10 1.67		W W W W
input standby power (P_{CTRL})	turned off with CTRL-pin	default configuration: monitoring enabled, precise timing enabled		170		mW
internal input capacitance (C_i)				140		µF
internal output capacitance (C_o)				400		µF
total external output capacitance (C_{OUT})	see note 9		470		30,000	µF
ESR range of capacitors (per single capacitor) (C_{OUT})	see note 9		5		30	mΩ
load transient peak voltage deviation (L to H/H to L) load step 25-75-25% of max I_O(V_{tr1})	default configuration di/dt = 2 A/µs C_O = 470 µF (minimum external capacitance) see note 12	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V		79/256 127/298 144/324 210/327		mV mV mV mV
load transient recovery time note 5 (L to H/H to L) load step 25-75-25% of max I_O(t_{tr1})	default configuration di/dt = 2 A/µs C_O = 470 µF (minimum external capacitance) see note 12	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V		60/100 100/100 100/100 100/100		µs µs µs µs
switching frequency (f_s)				320		kHz
switching frequency range (f_s)	PMBus configurable			200-640		kHz
switching frequency set-point accuracy (f_s)			-5		5	%
control circuit PWM duty cycle			5		95	%
minimum sync pulse width			150			ns
input clock frequency drift tolerance	external clock source		-13		13	%

DISCONTINUED

PRODUCT ELECTRICAL SPECIFICATION, HORIZONTAL (CONTINUED)

parameter	conditions/description		min	typ	max	units
input under voltage lockout, UVLO	UVLO threshold			3.85		V
	UVLO threshold range	PMBus configurable		3.85-14		V
	set point accuracy		-150		150	mV
	UVLO hysteresis			0.35		V
	UVLO hysteresis range	PMBus configurable		0-10.15		V
	delay			2.5		µs
	fault response	see note 3		automatic restart, 70 ms		
input over voltage protection, IOVP	IOVP threshold			16		V
	IOVP threshold range	PMBus configurable		4.2-16		V
	set point accuracy		-150		150	mV
	IOVP hysteresis			1		V
	IOVP hysteresis range	PMBus configurable		0-11.8		V
	delay			2.5		µs
	fault response	see note 3		automatic restart, 70 ms		
power good, PG, see note 2	PG threshold			90		$\%V_o$
	PG hysteresis			5		$\%V_o$
	PG delay	see note 19		direct after DLC		ms
	PG delay range	PMBus configurable		0-500		s
output voltage over/under voltage protection, OVP/UVP	UVP threshold			85		$\%V_o$
	UVP threshold range	PMBus configurable		0-100		$\%V_o$
	UVP hysteresis			5		$\%V_o$
	OVP threshold			115		$\%V_o$
	OVP threshold range	PMBus configurable		100-115		$\%V_o$
	UVP/OVP response time			25		µs
	UVP/OVP response time range	PMBus configurable		5-60		µs
	fault response	see note 3		automatic restart, 70 ms		
over current protection, OCP	OCP threshold			62		A
	OCP threshold range	PMBus configurable		0-62		A
	protection delay	see note 4		32		T_{sw}
	protection delay range	PMBus configurable		1-32		T_{sw}
	fault response	see note 3		automatic restart, 70 ms		
over temperature protection, OTP at P2 see note 8	OTP threshold			120		°C
	OTP threshold range	PMBus configurable	-40		125	°C
	OTP hysteresis			25		°C
	OTP hysteresis range	PMBus configurable		0-165		°C
	fault response	see note 3		automatic restart, 240 ms		

DISCONTINUED

PRODUCT ELECTRICAL SPECIFICATION, HORIZONTAL (CONTINUED)

parameter	conditions/description		min	typ	max	units
logic input low threshold(V_{IL})	SYNC, SA0, SA1, SCL, SDA, DDC, CTRL, VSET				0.8	V
logic input high threshold (V_{IH})			2			V
logic input low sink current(I_{IL})	CTRL				0.6	mA
logic output low signal level (V_{OL})	SYNC, SCL, SDA, SALERT, DDC, PG				0.4	V
logic output high signal level (V_{OH})			2.25			V
logic output low sink current (I_{OL})					4	mA
logic output high source current (I_{OH})					2	mA
setup time, SMBus(t_{SET})	see note 1		300			ns
hold time, SMBus(t_{hold})	see note 1		250			ns
bus free time, SMBus(t_{free})	see note 1		2			ms
internal capacitance on logic pins (C_P)				10		pF
initialization time		see note 10		40		ms
output voltage delay time see note 6	delay duration	see note 16		10		ms
	delay duration range	PMBus configurable		5-500,000		ms
	delay accuracy turn-on			-0.25/+4		ms
	delay accuracy turn-off			-0.25/+4		ms
output voltage ramp time see note 13	ramp duration			10		ms
	ramp duration range	PMBus configurable		0-200		ms
	ramp time accuracy			100		µs
		current sharing operation		20		%
VTRK input bias current	V_{VTRK} = 5.5 V			110	200	µA
VTRK tracking ramp accuracy (V_O - V_{VTRK})	100% tracking, see note 7		-100		100	mV
	current sharing operation 2 phases, 100% tracking V_O = 1.0 V, 10 ms ramp			±100		mV
VTRK regulation accuracy (V_O - V_{VTRK})	100% Tracking		-1		1	%
	current sharing operation 100% Tracking		-2		2	%
current difference between products in a current sharing group	steady state operation			Max 2 x READ_IOUT monitoring accuracy		
	ramp-up			4		A
number of products in a current sharing group					7	
monitoring accuracy	READ_VIN vs V_I			3		%
	READ_VOUT vs V_O			1		%
	READ_IOUT vs I_O	I_O = 0-50 A, T_{P1} = 0 to +95 °C V_I = 4.5-14 V, V_O = 1.0 V		±3		A
	READ_IOUT vs I_O	I_O = 0-50 A, T_{P1} = 0 to +95 °C V_I = 4.5-14 V, V_O = 0.6-3.3 V		±5		A

DISCONTINUED

PRODUCT ELECTRICAL SPECIFICATION, HORIZONTAL (CONTINUED)

Notes:
1: See section I²C/SMBus Setup and Hold Times – Definitions.
2: Monitorable over PMBus Interface.
3: Automatic restart ~70 or 240 ms after fault if the fault is no longer present. Continuous restart attempts if the fault reappear after restart.
4: T_{sw} is the switching period.
5: Within +/-3% of VO
6: See section Soft-start Power Up.
7: Tracking functionality is designed to follow a VTRK signal with slew rate < 2.4 V/ms. For faster VTRK signals accuracy will depend on the regulator bandwidth.
8: See section Over Temperature Protection (OTP).
9: See section External Capacitors.
10: See section Initialization Procedure.
11: See graph Output Ripple vs External Capacitance and Operating information section Output Ripple and Noise.
12: See graph Load Transient vs. External Capacitance and Operating information section External Capacitors.
13: Time for reaching 100% of nominal Vout.
14: For Vout < 1.0 V accuracy is +/-10 mV. For further deviations see section Output Voltage Adjust using PMBus.
15: Accuracy here means deviation from ideal output voltage level given by configured droop and actual load. Includes line, load and temperature variations.
16: For current sharing the Output Voltage Delay Time must be reconfigured to minimum 15 ms.
17: For steady state operation above 1.05 x 3.3 V, please contact your local CUI sales representative.
18: A minimum load current is not required if Low Power mode is used (monitoring disabled).
19: See sections Dynamic Loop Compensation and Power Good.

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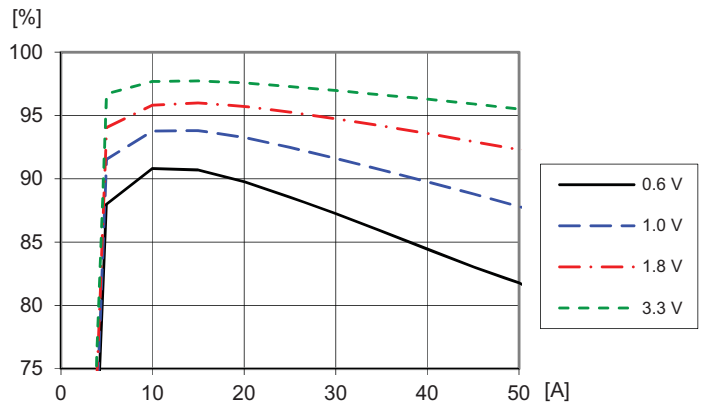
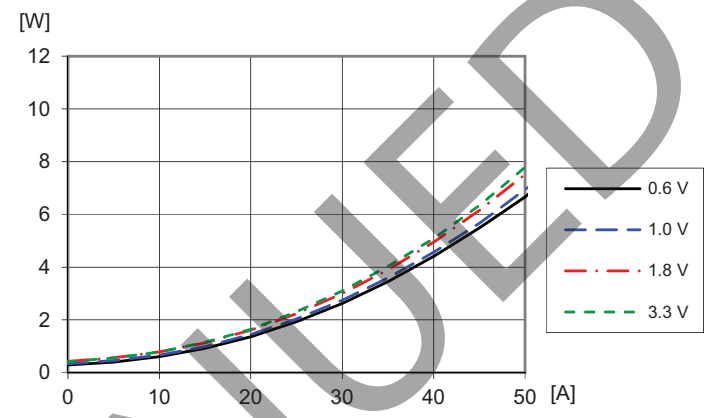
TYPICAL CHARACTERISTICS, HORIZONTAL

Efficiency vs. Output Current, V_I = 5 V



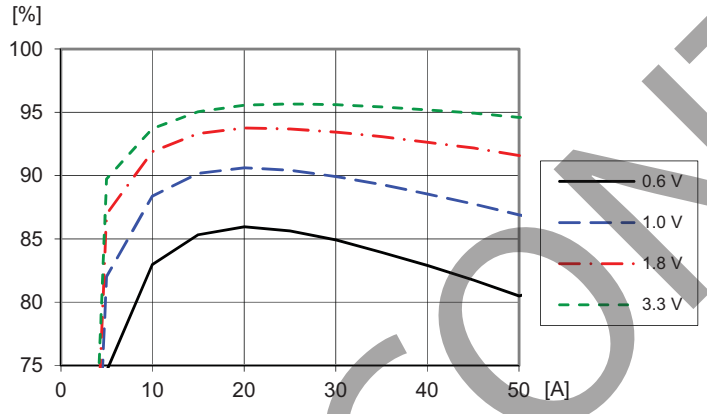
Efficiency vs. load current and output voltage:
T_{P1} = +25 °C, V_I = 5 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Power Dissipation vs. Output Current, V_I = 5 V



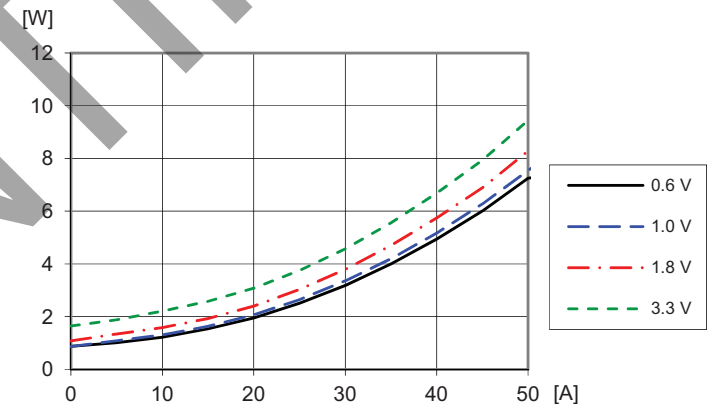
Dissipated power vs. load current and output voltage:
T_{P1} = +25 °C, V_I = 5 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Efficiency vs. Output Current, V_I = 12 V



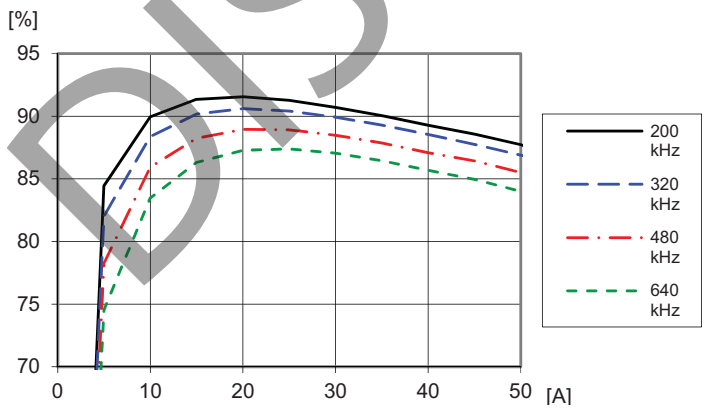
Efficiency vs. load current and output voltage at
T_{P1} = +25 °C, V_I = 12 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Power Dissipation vs. Output Current, V_I = 12 V



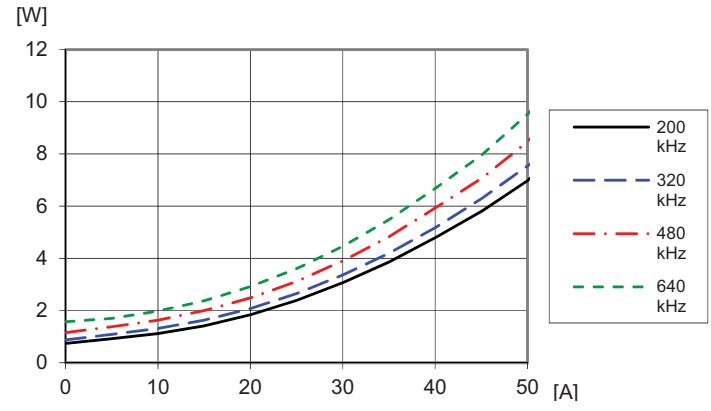
Dissipated power vs. load current and output voltage:
T_{P1} = +25 °C, V_I = 12 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Efficiency vs. Output Current and Switching Frequency



Efficiency vs. load current and switch frequency at
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ.
Default configuration except changed frequency

Power Dissipation vs. Output Current and Switching frequency

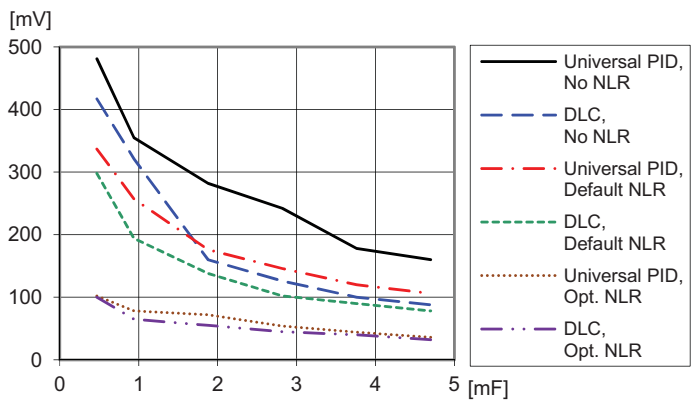


Dissipated power vs. load current and switch frequency at
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ.
Default configuration except changed frequency

DISCONTINUED

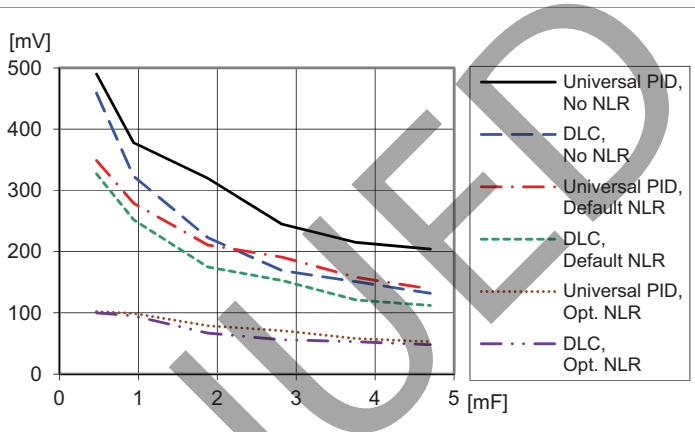
TYPICAL CHARACTERISTICS, HORIZONTAL (CONTINUED)

Load Transient vs. External Capacitance, V_O = 1.0 V



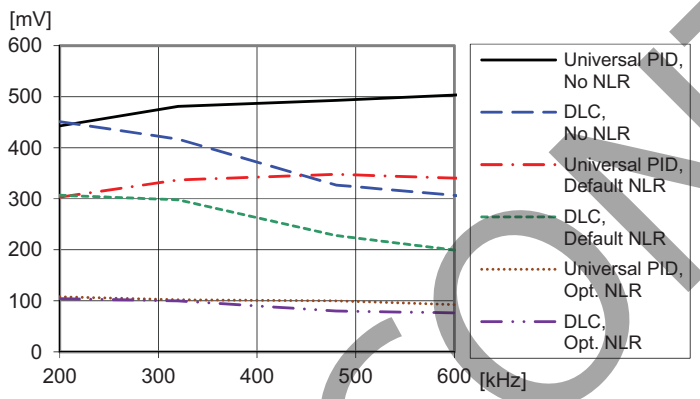
Load transient peak voltage deviation vs. external capacitance.
Step (12.5-37.5-12.5 A). Parallel coupling of capacitors with 470 µF/10 mΩ,
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, f_{sw} = 320 kHz, di/dt = 2 A/µs

Load Transient vs. External Capacitance, V_O = 3.3 V



Load transient peak voltage deviation vs. external capacitance.
Step (12.5-37.5-12.5 A). Parallel coupling of capacitors with 470 µF/10 mΩ,
T_{P1} = +25 °C, V_I = 12 V, V_O = 3.3 V, f_{sw} = 320 kHz, di/dt = 2 A/µs

Load transient vs. Switch Frequency



Load transient peak voltage deviation vs. frequency.
Step-change (12.5-37.5-12.5 A).
T_{P1} = +25 °C. V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ

Note 1: For Universal PID, see section Dynamic Loop Compensation (DLC).
Note 2: In the load transient graphs, the worst-case scenario (load step 37.5-12.5 A) has been considered.

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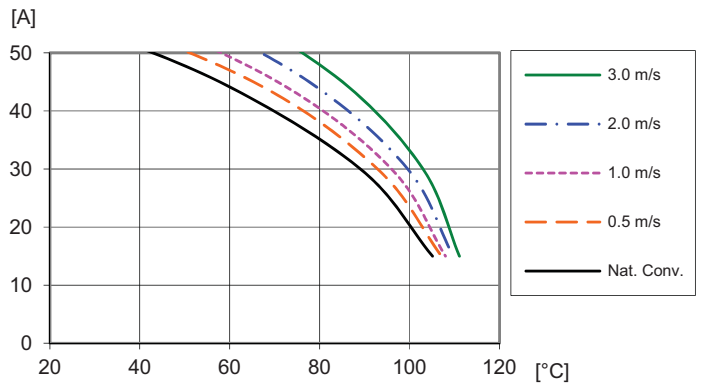
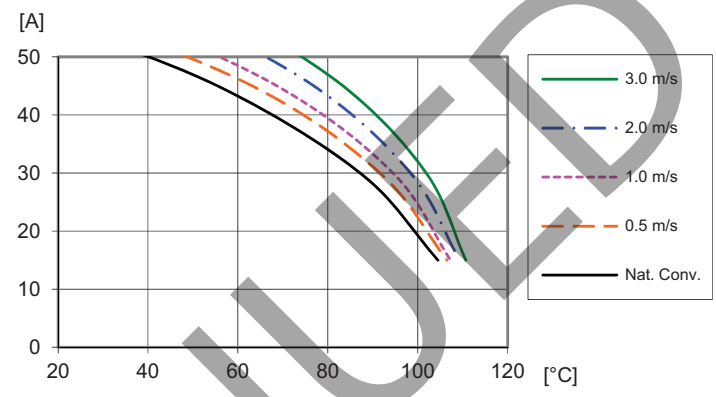
TYPICAL CHARACTERISTICS, HORIZONTAL (CONTINUED)

Output Current Derating, V_O = 0.6 V



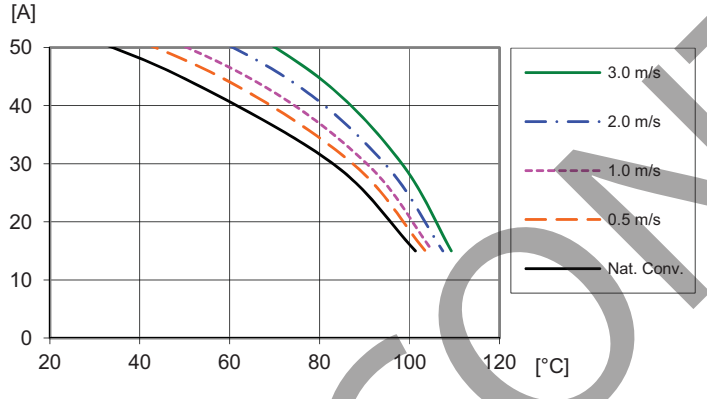
Available load current vs. ambient air temperature and airflow at V_O = 0.6 V, V_I = 12 V. See Thermal Consideration section.

Output Current Derating, V_O = 1.0 V



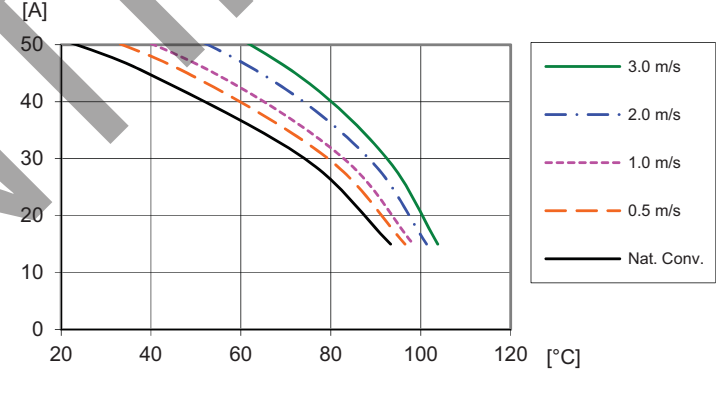
Available load current vs. ambient air temperature and airflow at V_O = 1.0 V, V_I = 12 V. See Thermal Consideration section.

Output Current Derating, V_O = 1.8 V



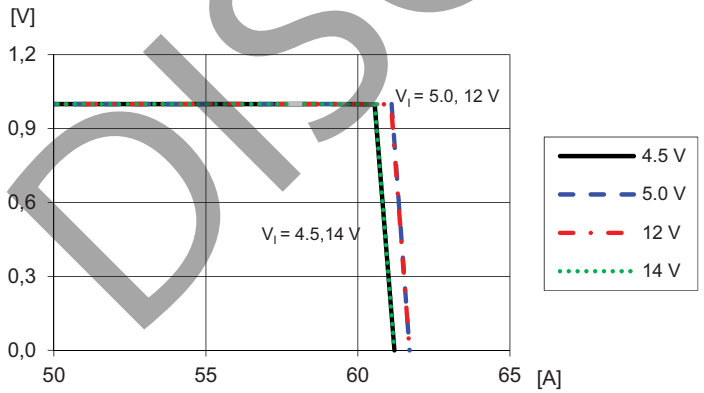
Available load current vs. ambient air temperature and airflow at V_O = 1.8 V, V_I = 12 V. See Thermal Consideration section.

Output Current Derating, V_O = 3.3 V



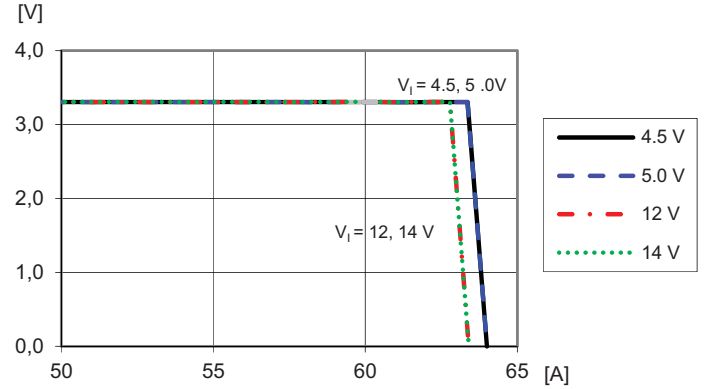
Available load current vs. ambient air temperature and airflow at V_O = 3.3 V, V_I = 12 V. See Thermal Consideration section.

Current Limit Characteristics, V_O = 1.0 V



Output voltage vs. load current at T_{P1} = +25 °C, V_O = 1.0 V.
Note: Output enters hiccup mode at current limit.

Current Limit Characteristics, V_O = 3.3 V

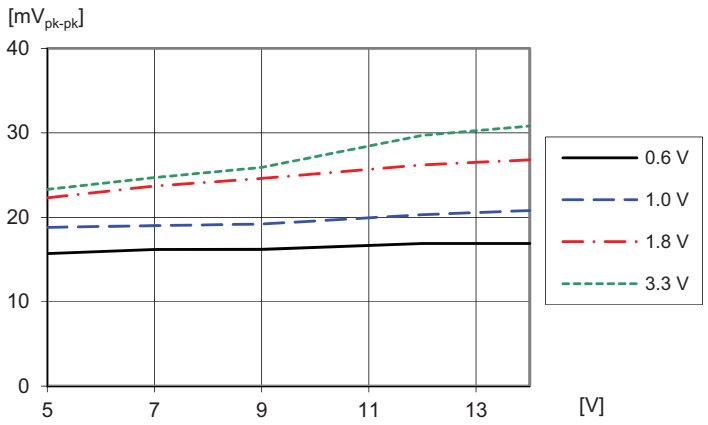


Output voltage vs. load current at T_{P1} = +25 °C, V_O = 3.3 V.
Note: Output enters hiccup mode at current limit.

DISCONTINUED

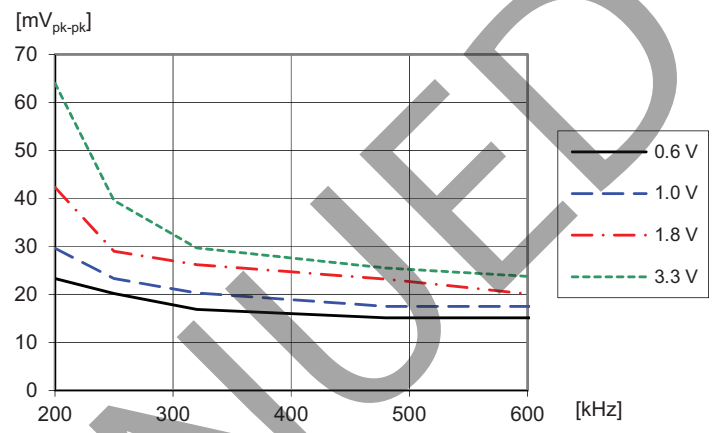
TYPICAL CHARACTERISTICS, HORIZONTAL (CONTINUED)

Output Ripple vs. Input Voltage



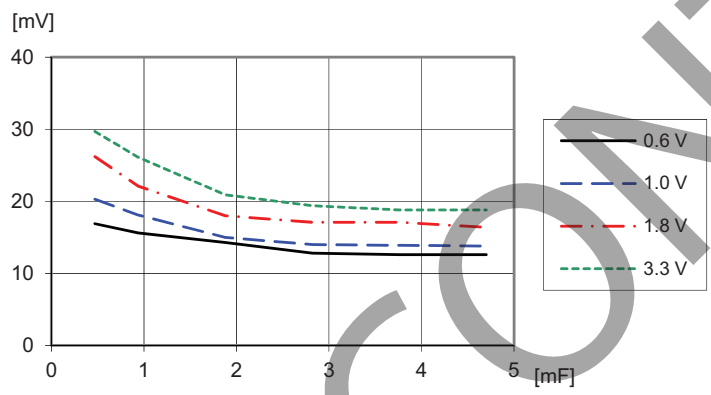
Output voltage ripple V_{pk-pk} at: T_{P1} = +25 °C, C_O = 470 µF/10 mΩ, I_O = 50 A

Output Ripple vs. Frequency



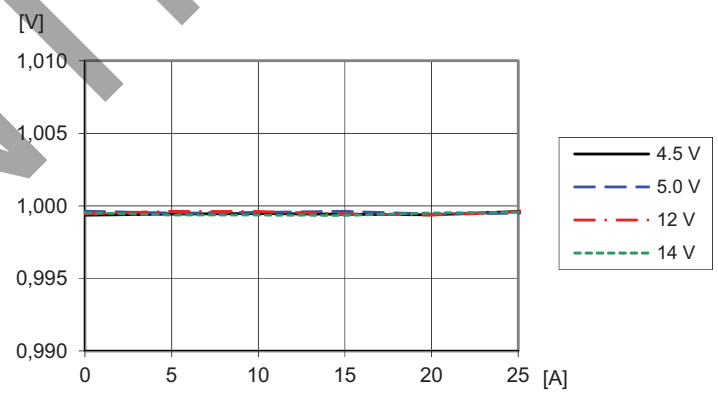
Output voltage ripple V_{pk-pk} at: T_{P1} = +25 °C, V_I = 12 V, C_O = 470 µF/10 mΩ, I_O = 50 A. Default configuration except changed frequency.

Output Ripple vs. External Capacitance



Output voltage ripple V_{pk-pk} at: T_{P1} = +25 °C, V_I = 12 V. I_O = 50 A.
Parallel coupling of capacitors with 470 µF/10 mΩ

Load regulation, V_O = 1.0 V

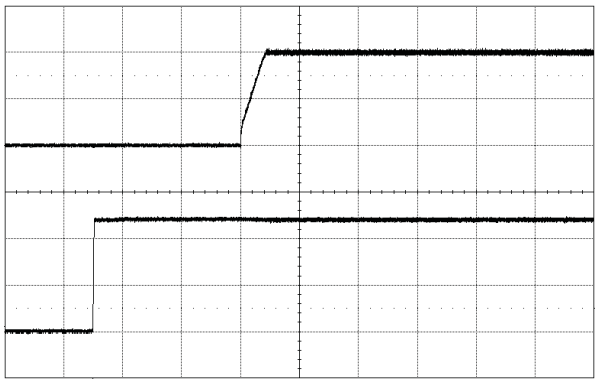


Load regulation at V_O = 1.0 V, T_{P1} = +25 °C, C_O = 470 µF/10 mΩ

DISCONTINUED

TYPICAL CHARACTERISTICS, HORIZONTAL (CONTINUED)

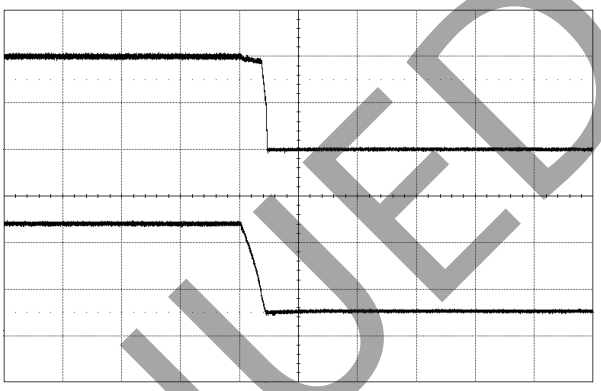
Start-up by input source



Start-up enabled by connecting V_I at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 50 A

Top trace: output voltage (0.5 V/div.).
Bottom trace: input voltage (5 V/div.).
Time scale: (20 ms/div.).

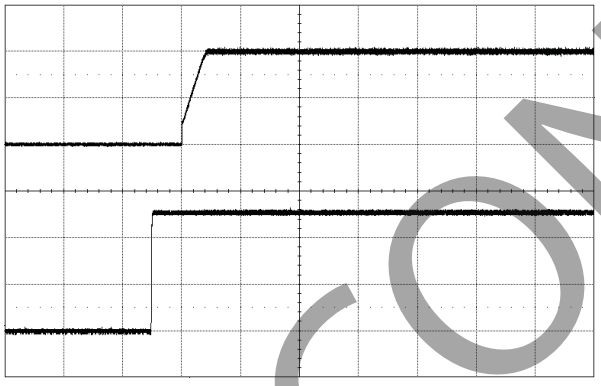
Shut-down by input source



Shut-down enabled by disconnecting V_I at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 50 A

Top trace: output voltage (0.5 V/div.).
Bottom trace: input voltage (5 V/div.).
Time scale: (2 ms/div.).

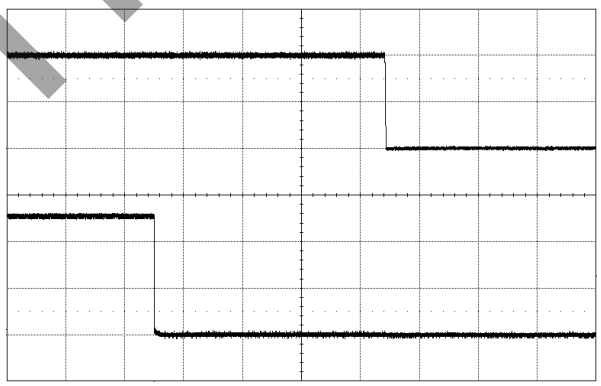
Start-up by CTRL signal



Start-up by enabling CTRL signal at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 50 A

Top trace: output voltage (0.5 V/div.).
Bottom trace: CTRL signal (2 V/div.).
Time scale: (20 ms/div.).

Shut-down by CTRL signal



Shut-down enabled by disconnecting V_I at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 50 A

Top trace: output voltage (0.5 V/div).
Bottom trace: CTRL signal (2 V/div.).
Time scale: (2 ms/div.).

DISCONTINUED

PRODUCT ELECTRICAL SPECIFICATION, VERTICAL

T_{P1} = -30 to +95 °C, V_I = 4.5 to 14 V, V_I> V_O + 1.0 V
Typical values given at: T_{P1} = +25 °C, V_I = 12.0 V, max I_O, unless otherwise specified under conditions.
External C_{IN} = 470 µF/10 mΩ, C_{OUT} = 470 µF/10 mΩ. See Operating Information section for selection of capacitor types.
Sense pins are connected to the output pins.

parameter	conditions/description		min	typ	max	units
input voltage rise time (V_I)	monotonic				2.4	V/ms
output voltage without pin-strap (V_O)				1.2		V
output voltage adjustment range (V_O)			0.60		3.3	V
output voltage adjustment including margining (V_O)	see note 17		0.54		3.63	V
output voltage set-point resolution (V_O)				±0.025		%FS
output voltage accuracy (V_O)	including line, load, temp see note 14		-1		1	%
	current sharing operation see note 15		-2		2	%
internal resistance +S/-S to VOUT/GND (V_O)				47		Ω
line regulation (V_O)	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V			2 3 3 3		mV mV mV mV
load regulation (V_O) I_O = 0~100%	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V			2 2 2 2		mV mV mV mV
output ripple & noise (V_{oac}) C_O= 470 µF (minimum external capacitance) see note 11	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V			20 25 30 40		mVp-p mVp-p mVp-p mVp-p
output current (I_O)	see note 18		0.001		50	A
static input current at max I_O (I_S)	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V			3.12 4.81 8.22 14.59		A A A A
current limit threshold (I_{lim})			52		65	A
short circuit current(I_{SC})	RMS, hiccup mode, see note 3	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V		10 8 6 5		A A A A
efficiency (η)	50% of max I_O	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V		85.2 90.2 93.3 95.3		% % % %
	max I_O	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V		80.2 86.6 91.2 94.2		% % % %
power dissipation at max I_O (P_d)	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V			7.4 7.73 8.68 10.15		W W W W
input idling power (no load)(P_{li})	default configuration: continues conduction mode, CCM	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V		0.95 0.95 1.22 1.88		W W W W

DISCONTINUED

PRODUCT ELECTRICAL SPECIFICATION, VERTICAL (CONTINUED)

input standby power (P_{CTRL})	turned off with CTRL-pin	default configuration: monitoring enabled, precise timing enabled		170		mW
internal input capacitance (C_i)				140		µF
internal output capacitance (C_o)				400		µF
total external output capacitance (C_{OUT})	see note 9		470		30,000	µF
ESR range of capacitors (per single capacitor) (C_{OUT})	see note 9		5		30	mΩ
load transient peak voltage deviation (L to H/H to L) load step 25-75-25% of max I_O(V_{tr1})	default configuration di/dt = 2 A/µs C_O = 470 µF (minimum external capacitance) see note 12	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V		90/300 120/300 160/305 230/315		mV mV mV mV
load transient recovery time note 5 (L to H/H to L) load step 25-75-25% of max I_O(t_{tr1})	default configuration di/dt = 2 A/µs C_O = 470 µF (minimum external capacitance) see note 12	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 3.3 V		70/100 100/100 100/100 100/100		µs µs µs µs
switching frequency (f_s)				320		kHz
switching frequency range (f_s)	PMBus configurable			200-640		kHz
switching frequency set-point accuracy (f_s)			-5		5	%
control circuit PWM duty cycle			5		95	%
minimum sync pulse width			150			ns
input clock frequency drift tolerance	external clock source		-13		13	%
input under voltage lockout, UVLO	UVLO threshold			3.85		V
	UVLO threshold range	PMBus configurable		3.85-14		V
	set point accuracy		-150		150	mV
	UVLO hysteresis			0.35		V
	UVLO hysteresis range	PMBus configurable		0-10.15		V
	delay			2.5		µs
	fault response	see note 3		automatic restart, 70 ms		
input over voltage protection, IOVP	IOVP threshold			16		V
	IOVP threshold range	PMBus configurable		4.2-16		V
	set point accuracy		-150		150	mV
	IOVP hysteresis			1		V
	IOVP hysteresis range	PMBus configurable		0-11.8		V
	delay			2.5		µs
	fault response	see note 3		automatic restart, 70 ms		
power good, PG, see note 2	PG threshold			90		%V_o
	PG hysteresis			5		%V_o
	PG delay	see note 19		direct after DLC		ms
	PG delay range	PMBus configurable		0-500		s

DISCONTINUED

PRODUCT ELECTRICAL SPECIFICATION, VERTICAL (CONTINUED)

parameter	conditions/description		min	typ	max	units
output voltage over/under voltage protection, OVP/UVP	UVP threshold			85		$\%V_o$
	UVP threshold range	PMBus configurable		0-100		$\%V_o$
	UVP hysteresis			5		$\%V_o$
	OVP threshold			115		$\%V_o$
	OVP threshold range	PMBus configurable		100-115		$\%V_o$
	UVP/OVP response time			25		µs
	UVP/OVP response time range	PMBus configurable		5-60		µs
	fault response	see note 3		automatic restart, 70 ms		
over current protection, OCP	OCP threshold			60		A
	OCP threshold range	PMBus configurable		0-60		A
	protection delay	see note 4		32		T_{SW}
	protection delay range	PMBus configurable		1-32		T_{SW}
	fault response	see note 3		automatic restart, 70 ms		
over temperature protection, OTP at P2 see note 8	OTP threshold			120		°C
	OTP threshold range	PMBus configurable	-40		125	°C
	OTP hysteresis			25		°C
	OTP hysteresis range	PMBus configurable		0-165		°C
	fault response	see note 3		automatic restart, 240 ms		
logic input low threshold(V_{IL})	SYNC, SA0, SA1, SCL, SDA, DDC, CTRL, VSET				0.8	V
logic input high threshold (V_{IH})			2			V
logic input low sink current(I_{IL})	CTRL				0.6	mA
logic output low signal level (V_{OL})	SYNC, SCL, SDA, SALERT, DDC, PG				0.4	V
logic output high signal level (V_{OH})			2.25			V
logic output low sink current (I_{OL})					4	mA
logic output high source current (I_{OH})					2	mA
setup time, SMBus(t_{SET})	see note 1		300			ns
hold time, SMBus(t_{hold})	see note 1		250			ns
bus free time, SMBus(t_{free})	see note 1		2			ms
internal capacitance on logic pins (C_P)				10		pF
initialization time		see note 10		40		ms
output voltage delay time see note 6	delay duration	see note 16		10		ms
	delay duration range	PMBus configurable		5-500,000		ms
	delay accuracy turn-on			-0.25/+4		ms
	delay accuracy turn-off			-0.25/+4		ms
output voltage ramp time see note 13	ramp duration			10		ms
	ramp duration range	PMBus configurable		0-200		ms
	ramp time accuracy			100		µs
		current sharing operation		20		%
VTRK input bias current	V_{VTRK} = 5.5 V			110	200	µA

DISCONTINUED

PRODUCT ELECTRICAL SPECIFICATION, VERTICAL (CONTINUED)

parameter	conditions/description	min	typ	max	units
VTRK tracking ramp accuracy (V_O - V_{VTRK})	100% tracking, see note 7	-100		100	mV
	current sharing operation 2 phases, 100% tracking V_O = 1.0 V, 10 ms ramp		±100		mV
VTRK regulation accuracy (V_O - V_{VTRK})	100% Tracking	-1		1	%
	current sharing operation 100% Tracking	-2		2	%
current difference between products in a current sharing group	steady state operation		Max 2 x READ_IOUT monitoring accuracy		
	ramp-up		4		A
number of products in a current sharing group				7	
monitoring accuracy	READ_VIN vs V_I		3		%
	READ_VOUT vs V_O		1		%
	READ_IOUT vs I_O I_O = 0-50 A, T_{P1} = 0 to +95 °C V_I = 4.5-14 V, V_O = 1.0 V		±3		A
	READ_IOUT vs I_O I_O = 0-50 A, T_{P1} = 0 to +95 °C V_I = 4.5-14 V, V_O = 0.6-3.3 V		±5		A

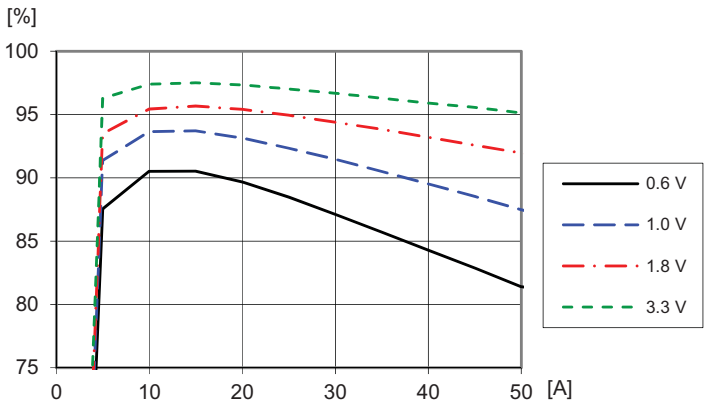
Notes:
1: See section I^2C/SMBus Setup and Hold Times – Definitions.
2: Monitorable over PMBus Interface.
3: Automatic restart ~70 or 240 ms after fault if the fault is no longer present. Continuous restart attempts if the fault reappear after restart.
4: T_{sw} is the switching period.
5: Within +/-3% of VO
6: See section Soft-start Power Up.
7: Tracking functionality is designed to follow a VTRK signal with slew rate < 2.4 V/ms. For faster VTRK signals accuracy will depend on the regulator bandwidth.
8: See section Over Temperature Protection (OTP).
9: See section External Capacitors.
10: See section Initialization Procedure.
11: See graph Output Ripple vs External Capacitance and Operating information section Output Ripple and Noise.
12: See graph Load Transient vs. External Capacitance and Operating information section External Capacitors.
13: Time for reaching 100% of nominal Vout.
14: For Vout < 1.0 V accuracy is +/-10 mV. For further deviations see section Output Voltage Adjust using PMBus.
15: Accuracy here means deviation from ideal output voltage level given by configured droop and actual load. Includes line, load and temperature variations.
16: For current sharing the Output Voltage Delay Time must be reconfigured to minimum 15 ms.
17: For steady state operation above 1.05 x 3.3 V, please contact your local CUI sales representative.
18: A minimum load current is not required if Low Power mode is used (monitoring disabled).
19: See sections Dynamic Loop Compensation and Power Good.

DISCONTINUED

TYPICAL CHARACTERISTICS, VERTICAL

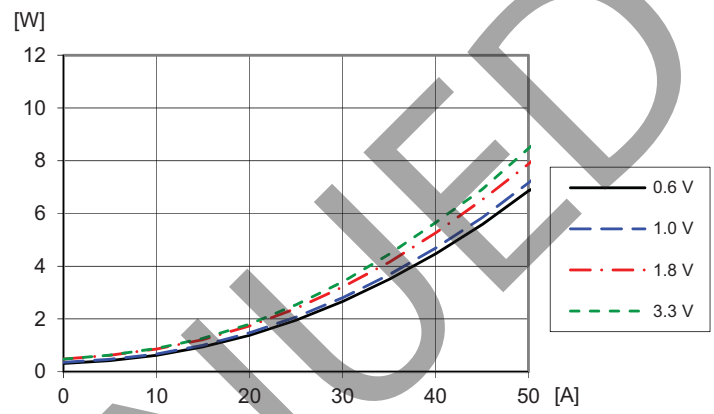
DISCONTINUED

Efficiency vs. Output Current, V_I = 5 V



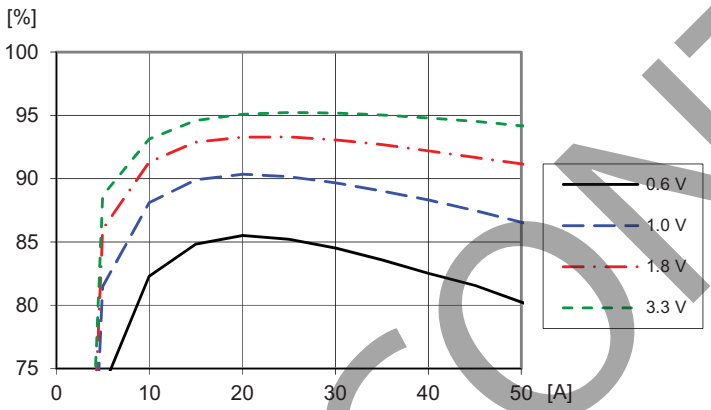
Efficiency vs. load current and output voltage:
T_{P1} = +25 °C, V_I = 5 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Power Dissipation vs. Output Current, V_I = 5 V



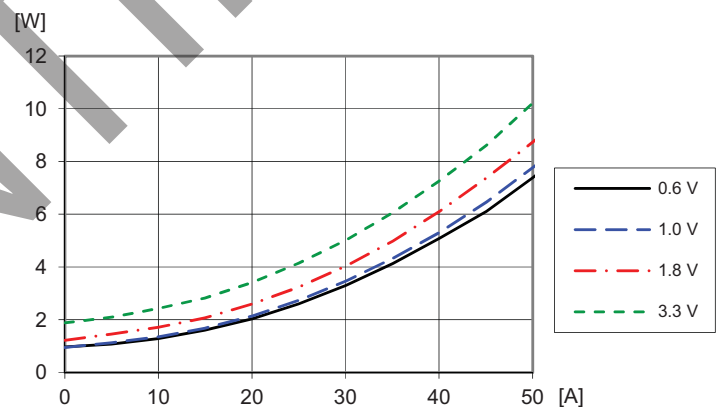
Dissipated power vs. load current and output voltage:
T_{P1} = +25 °C, V_I = 5 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Efficiency vs. Output Current, V_I = 12 V



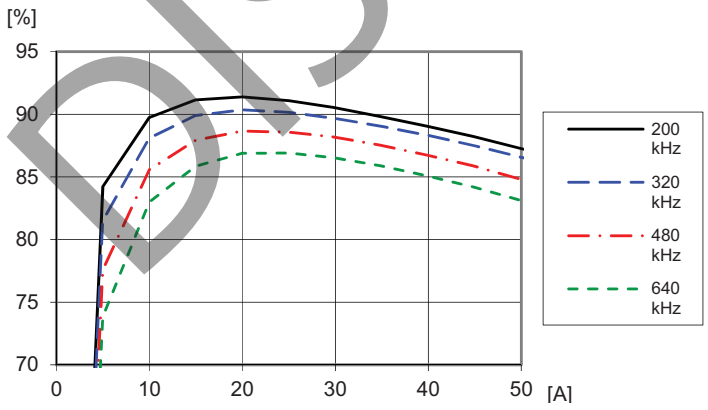
Efficiency vs. load current and output voltage at
T_{P1} = +25 °C, V_I=12 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Power Dissipation vs. Output Current, V_I = 12 V



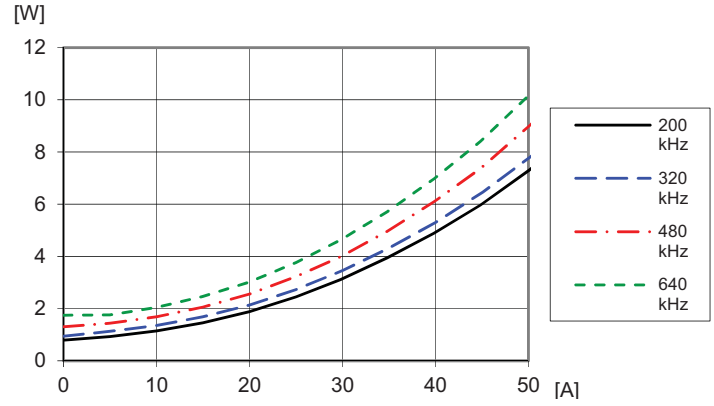
Dissipated power vs. load current and output voltage:
T_{P1} = +25 °C, V_I=12 V, f_{sw} = 320 kHz, C_O = 470 µF/10 mΩ.

Efficiency vs. Output Current and Switching Frequency



Efficiency vs. load current and switch frequency at
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ.
Default configuration except changed frequency

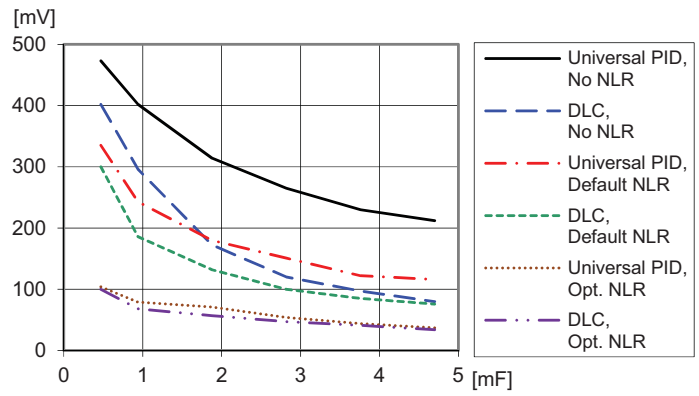
Power Dissipation vs. Output Current and Switching frequency



Dissipated power vs. load current and switch frequency at
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ.
Default configuration except changed frequency

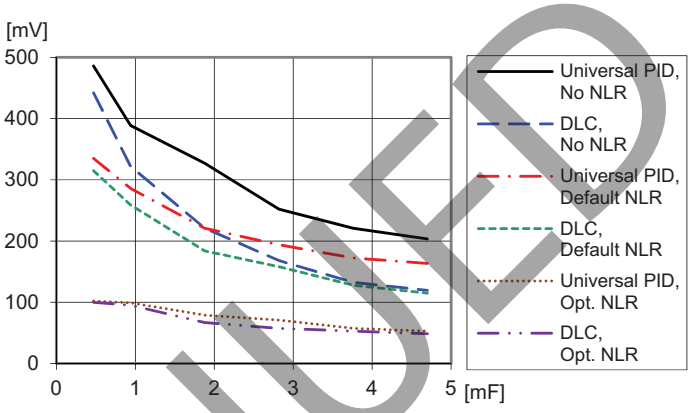
TYPICAL CHARACTERISTICS, VERTICAL (CONTINUED)

Load Transient vs. External Capacitance, V_O = 1.0 V



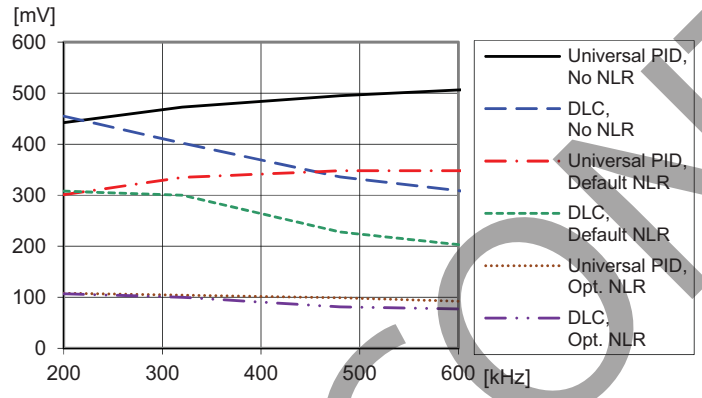
Load transient peak voltage deviation vs. external capacitance.
Step (12.5-37.5-12.5 A). Parallel coupling of capacitors with 470 µF/10 mΩ,
T_{P1} = +25 °C. V_I = 12 V, V_O = 1.0 V, f_{sw} = 320 kHz, di/dt = 2 A/µs

Load Transient vs. External Capacitance, V_O = 3.3 V



Load transient peak voltage deviation vs. external capacitance.
Step (12.5-37.5-12.5 A). Parallel coupling of capacitors with 470 µF/10 mΩ,
T_{P1} = +25 °C. V_I = 12 V, V_O = 3.3 V, f_{sw} = 320 kHz, di/dt = 2 A/µs

Load transient vs. Switch Frequency



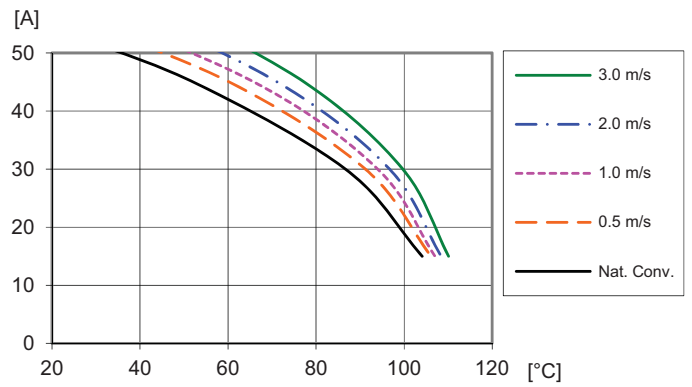
Load transient peak voltage deviation vs. frequency.
Step-change (12.5-37.5-12.5 A).
T_{P1} = +25 °C. V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ

Note 1: For Universal PID, see section Dynamic Loop Compensation (DLC).
Note 2: In these graphs, the worst-case scenario (load step 37.5-12.5 A) has been considered.

DISCONTINUED

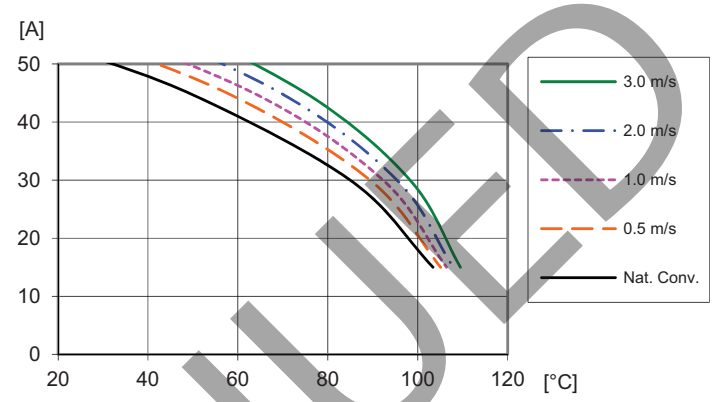
TYPICAL CHARACTERISTICS, VERTICAL (CONTINUED)

Output Current Derating, V_O = 0.6 V



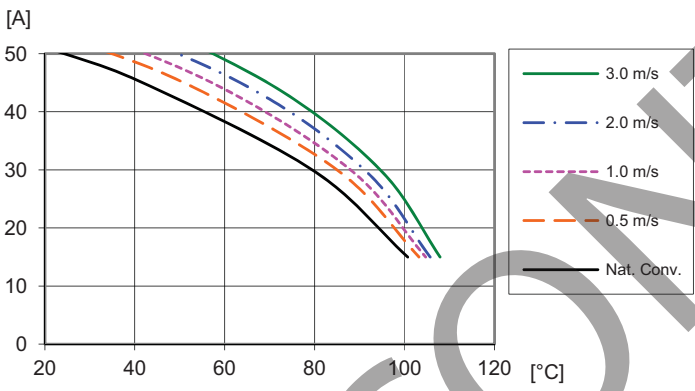
Available load current vs. ambient air temperature and airflow at V_O = 0.6 V, V_I = 12 V. See Thermal Consideration section.

Output Current Derating, V_O = 1.0 V



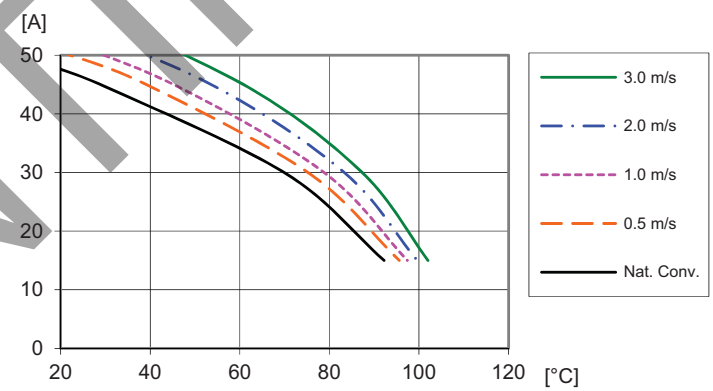
Available load current vs. ambient air temperature and airflow at V_O = 1.0 V, V_I = 12 V. See Thermal Consideration section.

Output Current Derating, V_O = 1.8 V



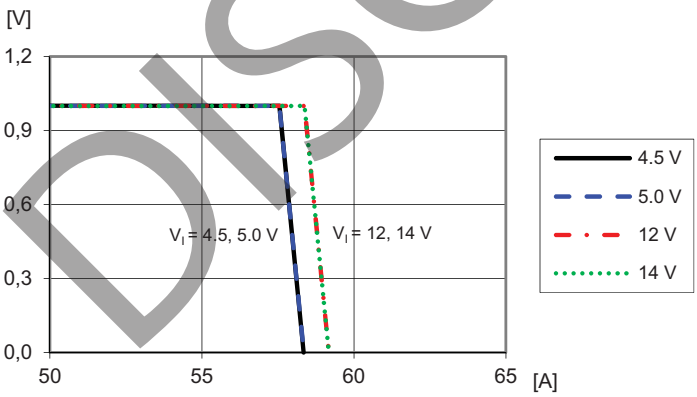
Available load current vs. ambient air temperature and airflow at V_O = 1.8 V, V_I = 12 V. See Thermal Consideration section.

Output Current Derating, V_O = 3.3 V



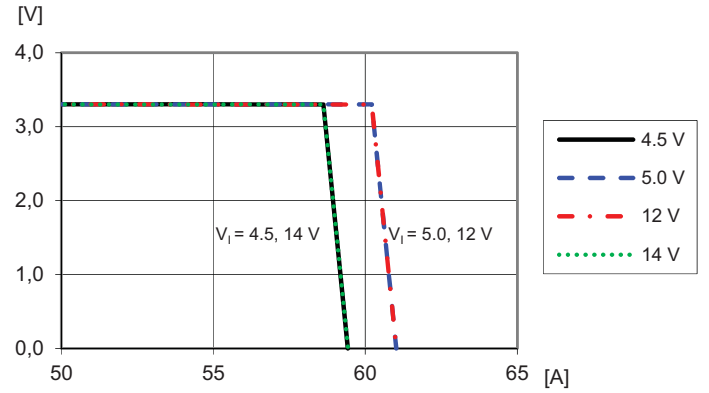
Available load current vs. ambient air temperature and airflow at V_O = 3.3 V, V_I = 12 V. See Thermal Consideration section.

Current Limit Characteristics, V_O = 1.0 V



Output voltage vs. load current at T_{P1} = +25 °C, V_O = 1.0 V.
Note: Output enters hiccup mode at current limit.

Current Limit Characteristics, V_O = 3.3 V

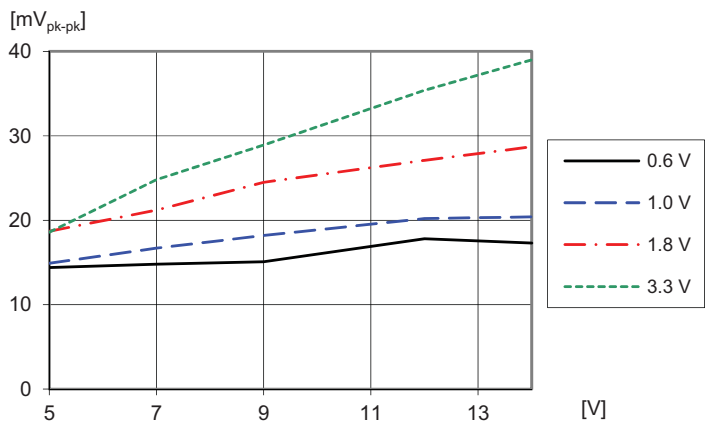


Output voltage vs. load current at T_{P1} = +25 °C, V_O = 3.3 V.
Note: Output enters hiccup mode at current limit.

DISCONTINUED

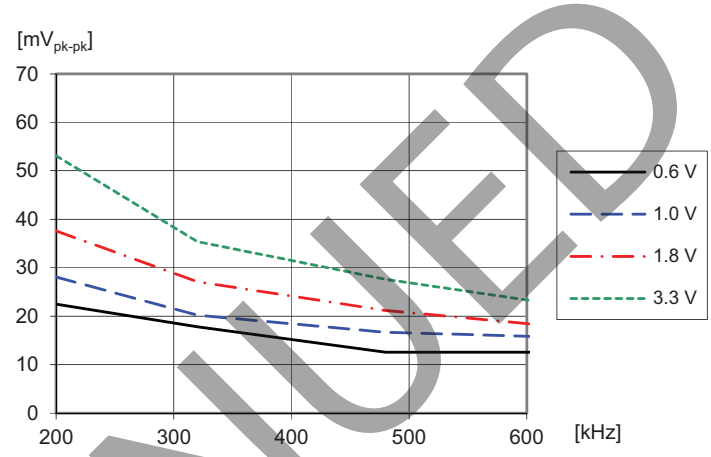
TYPICAL CHARACTERISTICS, VERTICAL (CONTINUED)

Output Ripple vs. Input Voltage



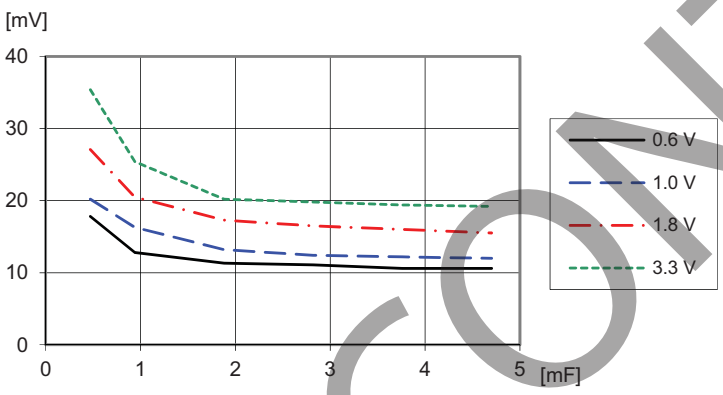
Output voltage ripple V_{pk-pk} at: T_{P1} = +25 °C, C_O = 470 µF/10 mΩ, I_O = 50 A.

Output Ripple vs. Frequency



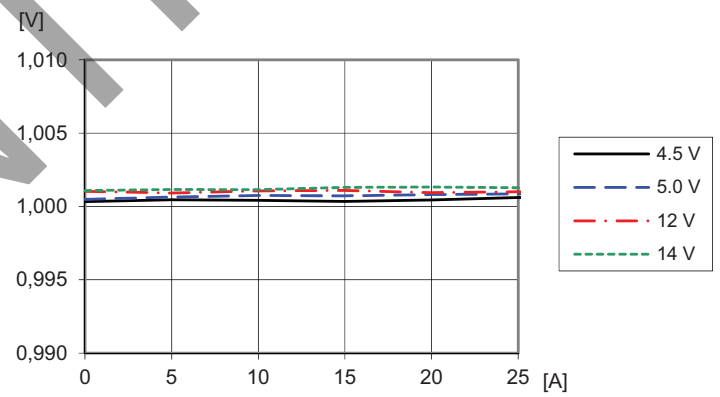
Output voltage ripple V_{pk-pk} at: T_{P1} = +25 °C, V_I = 12 V, C_O = 470 µF/10 mΩ, I_O = 50 A. Default configuration except changed frequency.

Output Ripple vs. External Capacitance



Output voltage ripple V_{pk-pk} at: T_{P1} = +25 °C, V_I = 12 V, I_O = 50 A.
Parallel coupling of capacitors with 470 µF/10 mΩ

Load regulation, V_O = 1.0 V

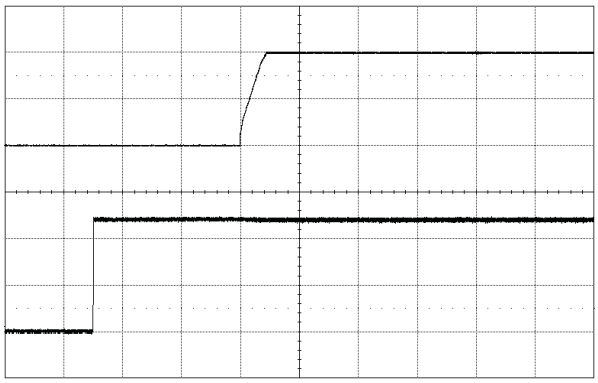


Load regulation at V_O = 1.0 V, T_{P1} = +25 °C, C_O = 470 µF/10 mΩ

DISCONTINUED

TYPICAL CHARACTERISTICS, VERTICAL (CONTINUED)

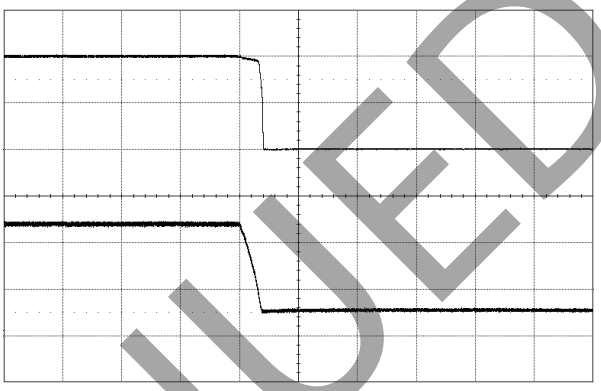
Start-up by input source



Start-up enabled by connecting V_I at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 50 A

Top trace: output voltage (0.5 V/div.).
Bottom trace: input voltage (5 V/div.).
Time scale: (20 ms/div.).

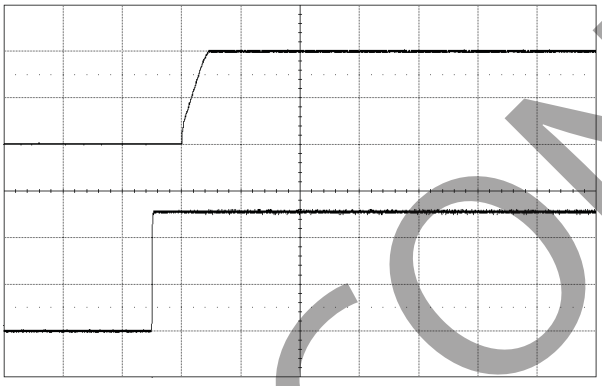
Shut-down by input source



Shut-down enabled by disconnecting V_I at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 50 A

Top trace: output voltage (0.5 V/div).
Bottom trace: input voltage (5 V/div.).
Time scale: (2 ms/div.).

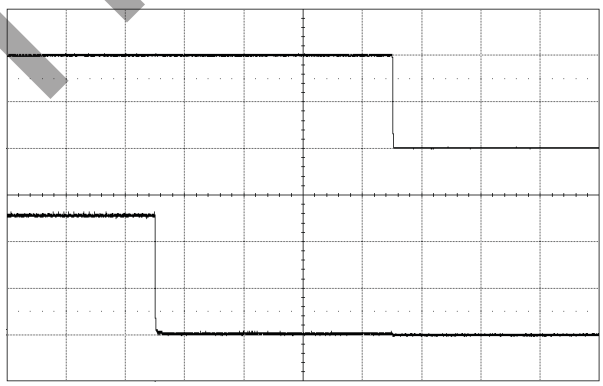
Start-up by CTRL signal



Start-up by enabling CTRL signal at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 50 A

Top trace: output voltage (0.5 V/div.).
Bottom trace: CTRL signal (2 V/div.).
Time scale: (20 ms/div.).

Shut-down by CTRL signal



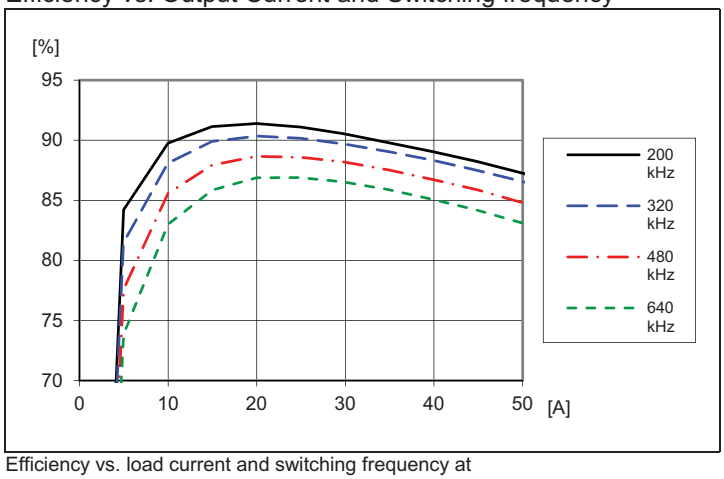
Shut-down enabled by disconnecting V_I at:
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V
C_O = 470 µF/10 mΩ, I_O = 50 A

Top trace: output voltage (0.5 V/div).
Bottom trace: CTRL signal (2 V/div.).
Time scale: (2 ms/div.).

DISCONTINUED

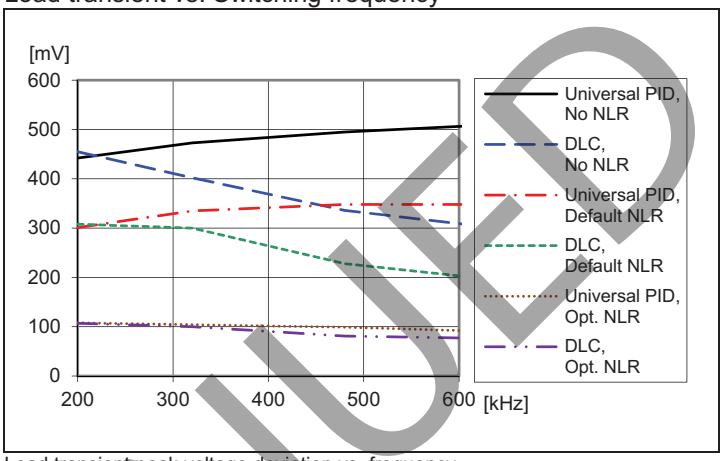
TYPICAL CHARACTERISTICS

Efficiency vs. Output Current and Switching frequency



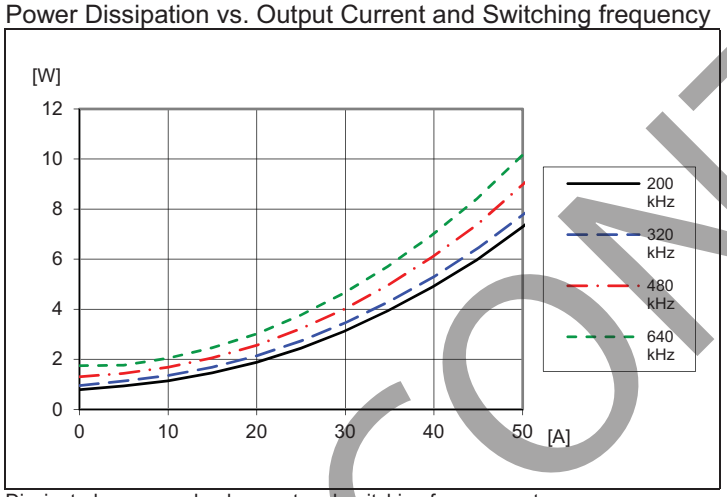
Efficiency vs. load current and switching frequency at
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ
Default configuration except changed frequency

Load transient vs. Switching frequency



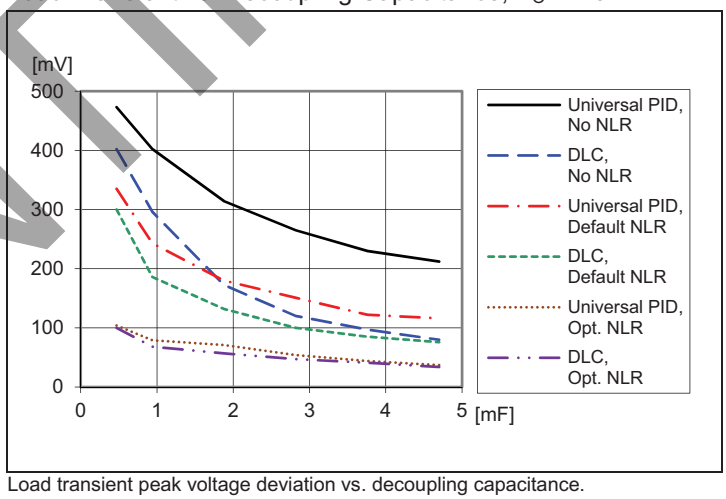
Load transient peak voltage deviation vs. frequency.
Step-change (12.5-37.5-12.5 A).
T_{P1} = +25 °C, V_I = 12 V, V_O =1.0 V, C_O = 470 µF/10 mΩ

Power Dissipation vs. Output Current and Switching frequency



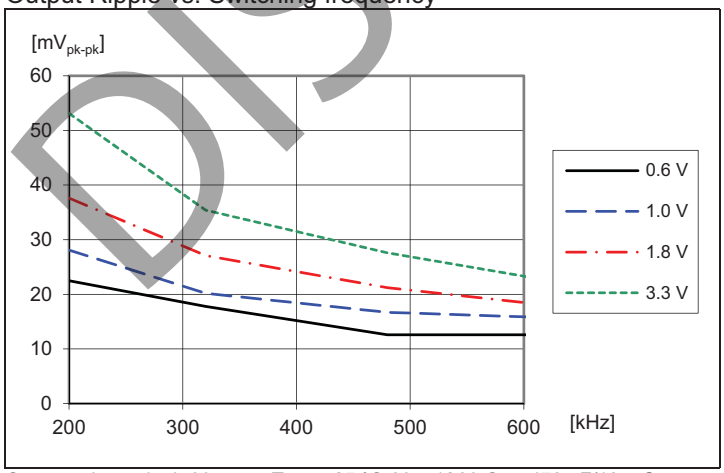
Dissipated power vs. load current and switching frequency at
T_{P1} = +25 °C, V_I = 12 V, V_O = 1.0 V, C_O = 470 µF/10 mΩ
Default configuration except changed frequency

Load Transient vs. Decoupling Capacitance, V_O = 1.0 V



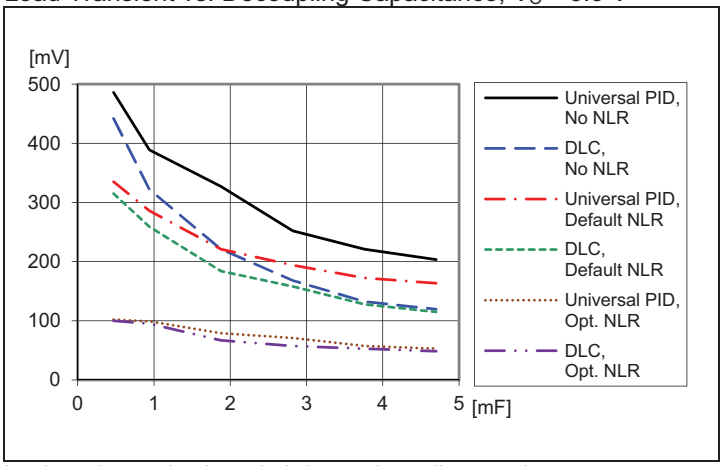
Load transient peak voltage deviation vs. decoupling capacitance.
Step (12.5-37.5-12.5 A). Parallel coupling of capacitors with 470 µF/10 mΩ,
T_{P1} = +25 °C. V_I = 12 V, V_O = 1.0 V, f_{sw} = 320 kHz, di/dt = 2 A/µs

Output Ripple vs. Switching frequency



Output voltage ripple V_{pk-pk} at: T_{P1} = +25 °C, V_I = 12 V, C_O = 470 µF/10 mΩ,
I_O = 50 A resistive load. Default configuration except changed frequency.

Load Transient vs. Decoupling Capacitance, V_O = 3.3 V



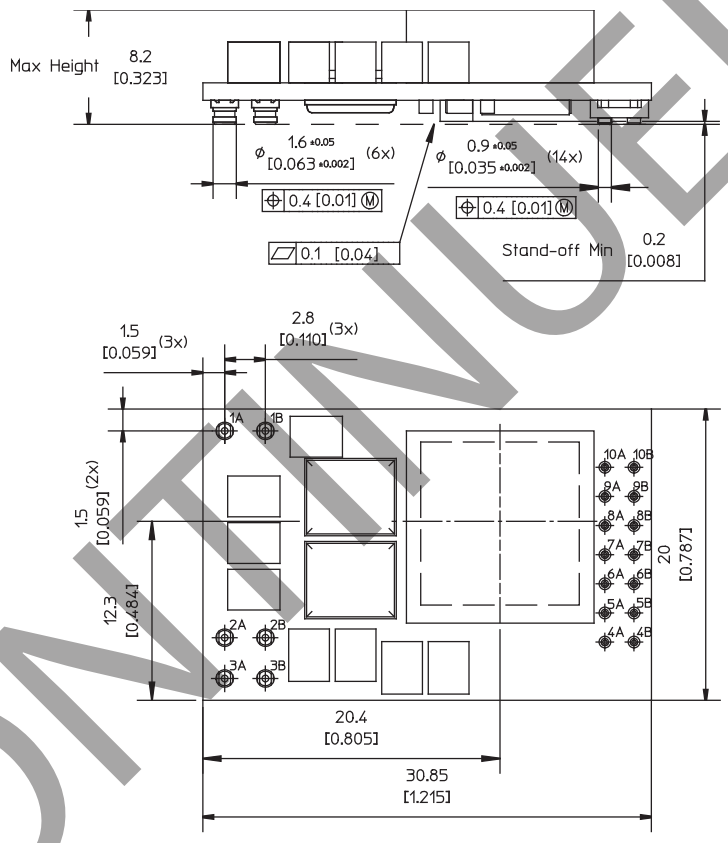
Load transient peak voltage deviation vs. decoupling capacitance.
Step (12.5-37.5-12.5 A). Parallel coupling of capacitors with 470 µF/10 mΩ,
T_{P1} = +25 °C. V_I = 12 V, V_O = 3.3 V, f_{sw} = 320 kHz, di/dt = 2 A/µs

DISCONTINUED

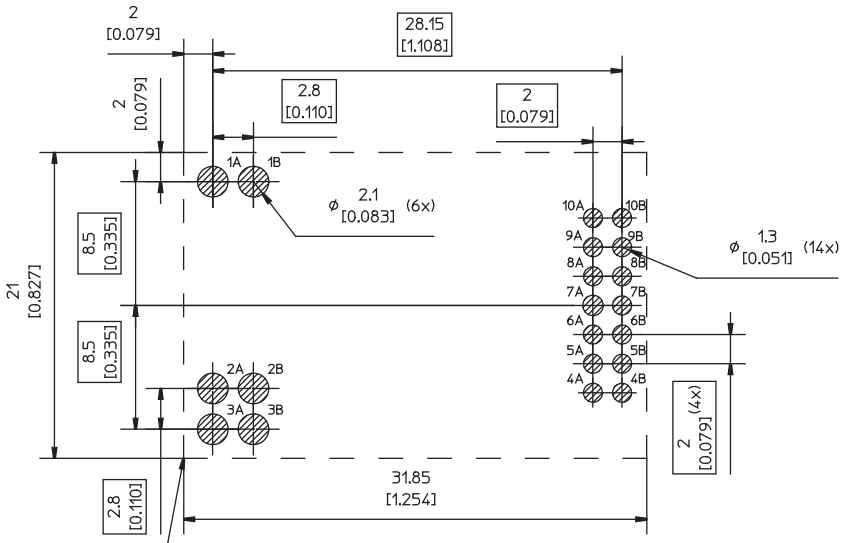
MECHANICAL DRAWING (HORIZONTAL, SURFACE MOUNT)

units: mm [inches]
tolerance unless specified:
X.X ±0.50 [0.02]
X.XX ±0.25 [0.01]
(not applied on footprint or typical values)

PIN NUMBER	PIN NAME	MATERIAL	PLATING
1A, 1B	VIN	Copper Alloy	Min 0.1 µm Au over 1~3 µm Ni
2A, 2B	GND		
3A, 3B	VOUT		
4A	VTRK	Brass	Min 0.1 µm Au over 2 µm Ni
4B	PREF		
5A	+S		
5B	-S		
6A	SA0		
6B	DDC		
7A	SCL		
7B	SDA		
8A	VSET		
8B	SYNC		
9A	SLRT		
9B	CTRL		
10A	PG		
10B	SA1		



TOP VIEW
Pin positions according
to recommended footprint



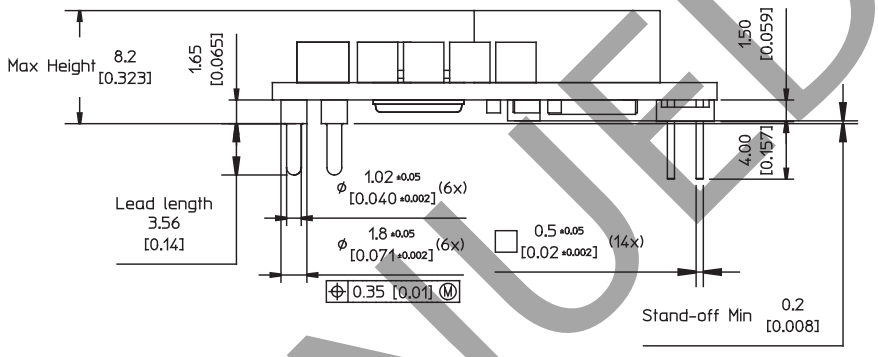
Recommended keep out area for user components
RECOMMENDED FOOTPRINT - TOP VIEW

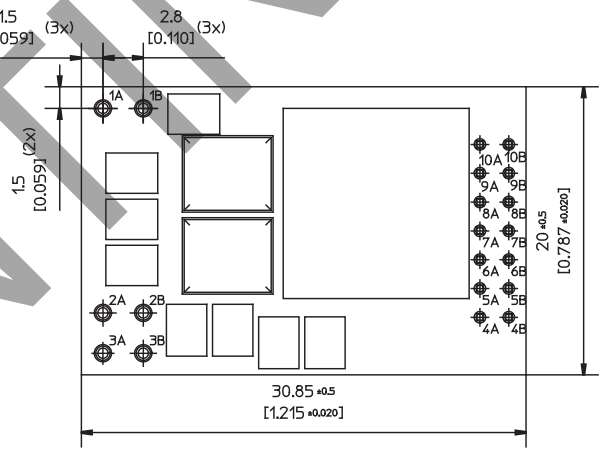
DISCONTINUED

MECHANICAL DRAWING (HORIZONTAL, THROUGH HOLE MOUNT)

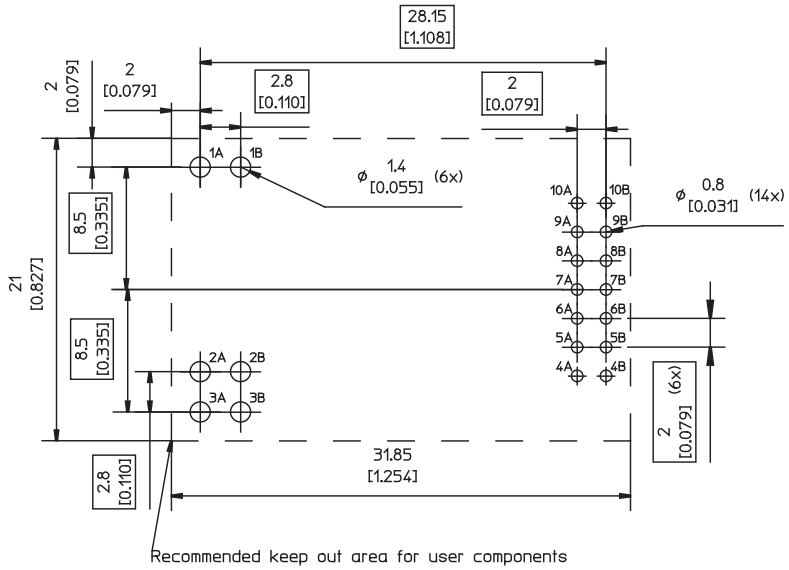
units: mm [inches]
tolerance unless specified:
X.X ±0.50 [0.02]
X.XX ±0.25 [0.01]
(not applied on footprint or typical values)

PIN NUMBER	PIN NAME	MATERIAL	PLATING
1A, 1B	VIN	Copper Alloy	Min 8~13 µm matte tin over 2.5~5 µm Ni
2A, 2B	GND		
3A, 3B	VOUT		
4A	VTRK	Brass	Min 0.2 µm Au over 1.27 µm Ni
4B	PREF		
5A	+S		
5B	-S		
6A	SA0		
6B	DDC		
7A	SCL		
7B	SDA		
8A	VSET		
8B	SYNC		
9A	SLRT		
9B	CTRL		
10A	PG		
10B	SA1		





TOP VIEW
Pin positions according to recommended footprint



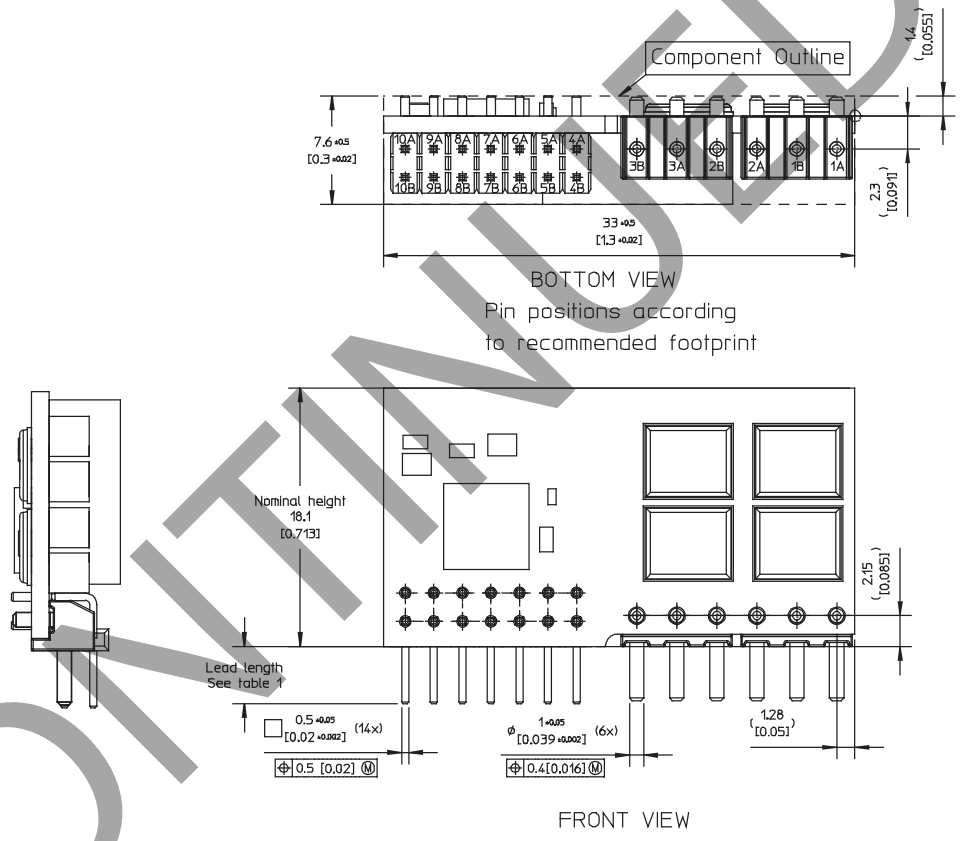
RECOMMENDED FOOTPRINT – TOP VIEW

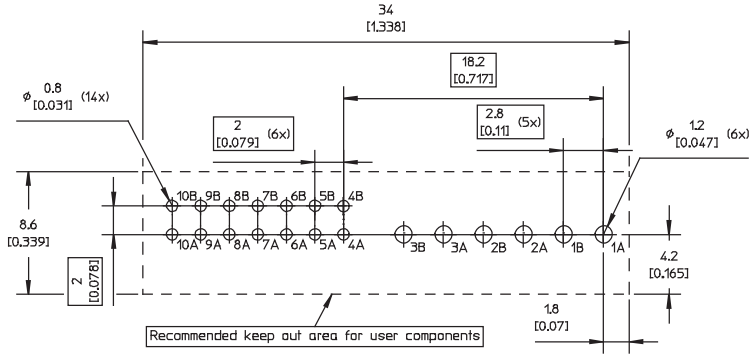
DISCONTINUED

MECHANICAL DRAWING (VERTICAL, THROUGH HOLE MOUNT)

units: mm [inches]
tolerance unless specified:
X.X ±0.50 [0.02]
X.XX ±0.25 [0.01]
(not applied on footprint or typical values)

PIN NUMBER	PIN NAME	MATERIAL	PLATING
1A	VIN	Copper Alloy	Min 0.1 µm Au over 1~3 µm Ni
1B	VIN		
2A	GND		
2B	GND		
3A	VOUT		
3B	VOUT		
4A	+S		Min 0.1 µm Au over 1 µm Ni
4B	-S		
5A	VSET		
5B	VTRK		
6A	SALRT		
6B	SDA		
7A	SCL		
7B	SA1		
8A	SA0		
8B	SYNC		
9A	PG		
9B	CTRL		
10A	DDC		
10B	PREF		





DISCONTINUED

OPERATING INFORMATION

The Novum Z Products PMBus Commands application note defines the available PMBus™ commands.

REQUIRED CONFIGURATIONS

NDM2Z-50 Module Pins

Each NDM2Z-50 module should have a resistor placed between VSET and PREF to set the output voltage of the module. The maximum output voltage which can be configured by PMBus commands can never exceed 110% of the voltage set by the VSET pin. The SMBus address of each module is set by either pin-strap configuration or resistor value associated with the SA0 and SA1 pins. More information regarding setting the SMBus address for a module can be found in the section titled "SMBus".

PCB Layout

Good performance of any point of load voltage regulator module can only be achieved with careful PCB layout considerations. Ground planes or very wide traces should be used for power and ground routing. Input capacitors should be placed close to the input voltage pins of the module and output capacitors should be placed close to the load. The module should also be placed as close as possible to the load.

INPUT AND OUTPUT CAPACITORS

Input Capacitors

Input capacitors are recommended to be used with the NDM2Z-50 module in order to minimize input voltage ripple. A 330 µF POSCAP or electrolytic and 3x 22 µF ceramic capacitors should be placed as close as possible to the input pins of the module. Additional input capacitors may be used if less input voltage ripple is desired.

Output Capacitors

Output capacitors are recommended to be used with the NDM2Z-50 module in order to improve transient response and minimize output voltage ripple. A 330 µF POSCAP or electrolytic and 3x 22 µF ceramic capacitors should be placed as close as possible to the load. Additional output capacitors may be used to further improve the output voltage characteristics.

POWER CONVERSION AND MANAGEMENT

Power Conversion Overview

The NDM2Z-50 module has several features to enable high power conversion efficiency. Non-linear loop response (NLR) improves the response time and reduces the output deviation as a result of load transients. The incorporation of DFM enhances the performance of CUI modules over that available from conventional analog POL offerings.

Power Management Overview

The NDM2Z-50 module incorporates a wide range of power management features. All power management functions can be configured via the SMBus interface. The NDM2Z-50 can monitor and report many characteristics of the module including input voltage, output voltage, output current and internal temperature. Additionally, the NDM2Z-50 includes circuit protection features that protect the module and load from damage due to system faults. Monitoring parameters can also be configured to provide alerts for specific conditions. The ability of CUI modules to digitally control, configure and monitor OS features provides significant benefits over traditional analog POL products.

CONFIGURING THE MODULE

Pin Settings

Pins SA0 and SA1 are used to set the SMBus address of the NDM2Z-50 module. Details of this feature are discussed in the section titled "SMBus". Pin SYNC is used to synchronize the switching clock of the module to an external clock source. More information regarding synchronization can be found in the section titled "SWITCHING FREQUENCY AND SYNCHRONIZATION".

Pin VSET is used to configure the output voltage of the module. The voltage established by the VSET pin limits the maximum output voltage that can be configured by SMBus commands.

The SA0, SA1, SYNC and VSET pin configurations are read by the module when power is applied or whenever a SMBus RESTORE command is issued.

The CTRL pin is active high and can be used to enable the module. Internal connections on the module will drive the CTRL pin high if it is left floating.

Pins +S and -S are used for remote voltage sensing of the output voltage.

DISCONTINUED

Unused Pins

Table 1 describes the required or allowed connections for unused pins on the NDM2Z-50 module.

Table 1: Unused Pins

VSET	Tie to PREF with 133 kΩ resistor, see VOUT_COMMAND PMBus command
VTRK, SA0, SA1, SYNC, CTRL, +S, -S	Float
DDC, SCL, SDA, SALRT	Pulled high with resistor, see "RECOMMENDED OPERATIN CONDITIONS"

Configuration of Parameters Using the SMBus

The NDM2Z-50 module is supplied with default settings. All module settings (except for module SMBus address, configured by pins SA0 and SA1) can be re-configured via the SMBus interface. The output voltage can not be set to greater than 110% of the voltage set by the VSET pin.

START-UP PROCEDURE

Start-up Sequence

The NDM2Z-50 module follows an internal start-up procedure after power is applied to pin VIN. Table 2 describes the start-up sequence. If the module is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting CTRL (or applying input voltage to the module if CTRL is not used). Once this process is completed, the module is ready to accept assertion of CTRL and commands via the SMBus interface.

Table 2: NDM2Z-50 Start-up sequence

STEP	STEP NAME	DESCRIPTION	TIME DURATION
1	Power applied or RESTORE_FACTORY	Input voltage is applied to NDM2Z-50 module pin VIN or RESTORE_FACTORY PMBus command issued	Depends on input supply ramp time
2	Factory configuration settings	Module loads factory configuration settings. This step is also performed after using PMBus commands to restore the factory configuration file.	Approximately 10 ms (module will ignore a CTRL signal and PMBus commands during this period)
3	SA0, SA1, SYNC and VSET pin settings	Module loads values configured by the SA0, SA1, SYNC and VSET pins.	
4	Default configuration settings	Module loads default configuration settings. This data over-rides pin setting data, except for maximum limit for VOUT_COMMAND. This step also performed after using PMBus commands to restore the default configuration file.	
5	User configuration settings	Module loads user configuration settings. This data over-rides pin setting and default configuration data, except for maximum limit for VOUT_COMMAND. This step also performed after using PMBus commands to restore the user configuration file.	
6	Module ready	The module is ready to accept a CTRL signal.	---
7	Pre-ramp delay	The module requires approximately 5 ms following a CTRL signal and prior to ramping its output. Additional pre-ramp delay may be configured using PMBus commands.	Approximately 5 ms

Soft-start Delay Ramp Times

Once CTRL is asserted the NDM2Z-50 module requires a pre-ramp delay time before the output voltage may be allowed to start the ramp-up process. After the delay period has expired, the output will begin to ramp towards the target voltage according to the pre-configured soft-start ramp time that has been set. It is recommended to set the soft-start ramp time to a value greater than 500 µs in order to prevent fault conditions due to excessive inrush current. Soft start delay and ramp times may be set using PMBus commands.

Output Pre-Bias

An output pre-bias condition exists when a non-zero voltage is present on the NDM2Z-50 module output before the module output voltage is enabled. If a pre-bias voltage exists, the output voltage of the module is set to match the existing pre-bias voltage. The output voltage is then ramped to the final regulation value in the specified ramp time. The pre-bias voltage can be higher or lower than the final output voltage. Higher pre-bias output voltages will cause energy to be pumped into the input voltage rail powering the module. This condition could cause the module to report an error condition if the input voltage exceeds the input over voltage lock out threshold. The module will report an error condition if the pre-bias output voltage exceeds the output over voltage protection threshold.

DISCONTINUED

Power Good

The PG pin on the NDM2Z-50 module will assert if the output of the module is within tolerance of the target voltage and no fault conditions exist. A PG delay period is defined as the time from when all conditions within the module for asserting PG are met to when PG is actually asserted. By default, PG delay is set equal to the soft-start ramp time setting. The tolerance, polarity and delay of PG may be configured via PMBus commands.

Soft-stop Delay and Ramp Times

After CTRL is de-asserted the NDM2Z-50 module utilizes a pre-ramp delay time before the output starts the ramp-down process. After the delay period has expired, the output will begin to ramp towards ground according to the pre-configured soft-stop ramp time that has been set. It is recommended to set the soft-start ramp down to a value greater than 500 µs in order to prevent voltage spikes in the module input supply rail due the energy stored in the output capacitors. There will be a delay after the output voltage has reached ground potential and then the output of the module will be set to high impedance. Once the output of the module is high impedance the output voltage may float to a non-zero value if another source or leakage path is connected to the output. The soft-stop delay and ramp times may be configured via PMBus commands. PMBus commands can be used to set the output of the NDM2Z-50 module to high impedance as soon as the output voltage drops below a selectable threshold.

OUTPUT VOLTAGE SETTING

Pin-Strap and Resistor Setting Methods

Using the pin-strap method, the voltage on the VOUT pin of the NDM2Z-50 module can be set to one of three default voltages as shown in Table 3. Table 4 lists the available output voltage settings with a resistor connected between VSET and PREF.

Table 3: Pin-strap VOUT voltage settings

VSET	VOUT (V)
LOW (< 0.8 V)	0.6
OPEN (N/C)	1.2
HIGH (> 2.0 V)	2.5

Table 4: Resistor VOUT voltage settings

RESISTOR (kΩ)	VOUT (V)	RESISTOR (kΩ)	VOUT (V)
10.0	0.60	38.3	1.30
11.0	0.65	42.2	1.40
12.1	0.70	46.4	1.50
13.3	0.75	51.1	1.60
14.7	0.80	56.2	1.70
16.2	0.85	61.9	1.80
17.8	0.90	68.1	1.90
19.6	0.95	75.0	2.00
21.5	1.00	82.5	2.10
23.7	1.05	90.9	2.20
26.1	1.10	100.0	2.30
28.7	1.15	110.0	2.50
31.6	1.20	121.0	3.00
34.8	1.25	133.0	3.30

SMBus Setting Method

The voltage present at the VOUT pin of the NDM2Z-50 module can be reconfigured using PMBus commands. A voltage level reconfigured by a PMBus command overrides the voltage set by the VSET pin, but cannot be set to greater than 110% of the voltage set by the VSET pin.

Voltage Tracking

The NDM2Z-50 module includes a feature that allows the output ramp voltage to track the ramp of a reference voltage which is applied to the VTRK pin. The voltage ramp tracking capability can be configured so that member modules track at either 50% or 100% of the reference voltage ramp rate. In addition, a member module can be configured so that the termination voltage either tracks or ignores perturbations on the reference voltage once it has stabilized. Tracking at 50% and tracking final voltage perturbations is intended for DDR memory applications. All other applications which required voltage tracking should use 100% tracking and ignore final voltage perturbations. The reference voltage for tracking must have a target voltage which is equal to or greater than the target voltage of the member modules. The turn-on delay of the reference voltage must be at least 10 ms greater than that set for the member modules. In voltage tracking mode, the turn-off delay of the member modules establishes the time duration which the member modules will track the reference voltage after CTRL is de-asserted. The turn-off delay of the member modules must be at least 5 ms greater than the sum of the turn-off delay and fall time of the reference voltage.

DISCONTINUED

Current sharing modules which are also configured to track a voltage must have all of the VTRK pins tied together. All of the CTRL pins of the member modules must also be connected together and driven by a common source. The rise and fall times of the member modules should be set between 5 ms and 10 ms to ensure current sharing while ramping. PMBus commands can be used to configure the voltage tracking features.

Voltage Margining

The NDM2Z-50 module offers a means to vary the output voltage higher or lower relative to the nominal voltage setting. The rate of change of the output voltage during voltage margining is also configurable. The margin feature can be reconfigured through PMBus commands.

SWITCHING FREQUENCY AND SYNCHRONIZATION

Switching Frequency

The switching frequency of the NDM2Z-50 module can be reconfigured by PMBus commands or controlled by an external clock source connected to the SYNC pin. If the module is operated at a switching frequency of other than the factory default setting, the compensation may need to be adjusted and the ripple, noise, transient response and efficiency may be affected.

SYNC Auto Detect

The NDM2Z-50 module will automatically check for a clock signal on the SYNC pin after CTRL is asserted (or applying input voltage to the module if CTRL is not used). If a clock signal is present, the module will synchronize to the rising edge of the external clock. The external clock signal must be stable and conform to the "RECOMMENDED OPERATING CONDITIONS" parameters when CTRL is asserted (or applying input voltage to the module if CTRL is not used). In the event of a loss of the external clock signal, the output voltage of the module may show transient overshoot or undershoot and the module will automatically configure to switch at a frequency close to the previous incoming frequency. If no incoming clock signal is present when CTRL is asserted (or applying input voltage to the module if CTRL is not used), the module will switch at the frequency set by the configuration file.

CONTROL LOOP

Adaptive Loop Compensation

The NDM2Z-50 module employs automatic adaptive loop compensation to increase the performance and stability of the module over a wide range of conditions. The default setting configures the module to re-compensate the control loop every time the output voltage ramps to the regulated level. PMBus commands can be used to configure when the module re-compensates the loop.
The user also has the option to manually configure the loop compensation.

Non-Linear Response (NLR) Settings

The NDM2Z-50 module incorporates a non-linear response (NLR) loop that decreases the response time and the output voltage deviation in the event of a sudden output load current step. This implementation results in a higher equivalent loop bandwidth than what would be possible using a traditional linear loop. PMBus commands can be used to configure the NLR response of the module.

Adaptive Diode Emulation

Please contact CUI technical support regarding the implementation of adaptive diode emulation.

Adaptive Frequency Control

The NDM2Z-50 module includes adaptive frequency control to improve conversion efficiency. Adaptive frequency control is not available for current sharing groups and is not allowed when the module is placed in auto-detect mode and a clock source is present on the SYNC pin.
Adaptive frequency control is only available while the module is operating within adaptive diode emulation mode. Adaptive frequency control can be enabled and disabled with PMBus commands.

MULTI-MODULE CONFIGURATION

Output Sequencing

Multiple device sequencing of NDM2Z-50 modules may be achieved by issuing PMBus commands to assign the preceding device in the sequencing chain as well as the device that will follow in the sequencing chain. The CTRL pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn-on of the group. CTRL must be driven low to initiate a sequenced turnoff of the group.

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Fault Spreading

NDM2Z-50 modules can be configured to broadcast a fault event over the DDC (Digital-DC Communication bus) to the other modules in the group. When a nondestructive fault occurs and the module is configured to shut down on a fault, the module will shut down and broadcast the fault event over the DDC. The other modules on the DDC will shut down together if configured to do so, and will attempt to re-start in their prescribed order if configured to do so. PMBus commands can be used to configure the transmission and reception of faults.

Active Current Sharing

Paralleling multiple NDM2Z-50 modules can be used to increase the output current capability of a single power rail. By connecting the DDC of each module together and configuring the modules as a current sharing rail, the units will share the load current.

Upon system start-up, the module with the lowest SMBus address is defined as the reference module; the remaining modules are members. The reference module broadcasts the current over the DDC. The output voltages of the member modules are controlled by the reference current information to balance the current loading of each module in the system.

A current sharing rail can be part of a system sequencing group. For fault configuration, the current share rail is configured in a quasi-redundant mode. In this mode, when a member module fails the remaining members will continue to operate and attempt to maintain regulation. If fault spreading is enabled, the current share rail failure is broadcast only after the entire current share rail fails. Members of the current sharing rail can be disabled to improve system power conversion efficiency. If the reference module fails or is disabled then the remaining module with the lowest SMBus address will become the new reference module. A change to the number of members of a current sharing rail will cause automatic phase re-distribution of the members of that current sharing rail. If the members of a current sharing rail are forced to shut down due to an observed fault, all members of the rail will attempt to re-start simultaneously after the fault has cleared. PMBus commands can be used to configure current sharing. A maximum of seven modules can be configured in a single current share group.

Phase Spreading

When multiple NDM2Z-50 modules share a common DC input supply, it may be desirable to adjust the clock phase offset of each module. In order to enable phase spreading, all modules must be synchronized to the same switching clock. For modules driven by a common synchronizing clock the phase offset of each module is controlled by the module addresses; phase offset = device address x 45°.

For example:

- A module address of 0x00 or 0x20 would configure 0° of phase offset
- A module address of 0x01 or 0x21 would configure 45° of phase offset
- A module address of 0x02 or 0x22 would configure 90° of phase offset

The phase offset of each module may also be set via the PMBus INTERLEAVE command.

POWER FAULT MANAGEMENT

Input Under and Over Voltage Lockout

Input under voltage lockout (UVLO) and input over voltage lockout (OVLO) indicate faults for the NDM2Z-50 module when the input voltage falls outside of preset thresholds. The default response due to an input voltage fault is an immediate shutdown of the module. The module will continuously check for the presence of the fault condition. Once the fault condition is no longer present, the module will be re-enabled. PMBus commands can be used to configure the thresholds and response of the module to the fault condition.

Output Under and Over Voltage Protection

The NDM2Z-50 module employs an output voltage protection circuit that can be used to protect load circuitry from being subjected to voltages outside of prescribed limits. A hardware comparator is used to compare the voltage seen at the +S pin to voltage thresholds. If the +S pin voltage is outside of these thresholds the PG pin will de-assert and the module will indicate a fault condition. The default response to an output voltage fault is to immediately shut down. The module will continuously check for the presence of the fault condition, when the fault condition no longer exists the module will be re-enabled. PMBus commands can be used to set the voltage thresholds and configure the response of the module to the fault condition. When operating from an external clock the only allowed response to an output voltage fault is an immediate shutdown.

DISCONTINUED

Output Over Current Protection

Output over current protection will protect the NDM2Z-50 module and load from damage if an overload condition is imposed on the output. The module will indicate a fault condition when the output current limit threshold is exceeded. The default response from an output current fault is an immediate shutdown of the module. The module will continuously check for the presence of the fault condition, and if the fault condition no longer exists the module will be re-enabled. PMBus commands can be used to configure the current limit threshold and the response of the module to the fault condition.

Thermal Overload Protection

The NDM2Z-50 module includes a thermal sensor that measures the temperature of the module and indicates a fault when the temperature exceeds a preset limit. The default response from a temperature fault is an immediate shutdown of the module. The module will continuously check for the fault condition and once the fault has cleared the module will be re-enabled. PMBus commands can be used to configure the thermal protection threshold and the response of the module to the fault condition. Permanent damage to the module may result if the thermal limit is set too high.

SMBUS

SMBus Communications

The NDM2Z-50 module provides a SMBus interface that enables the user to configure the module operation as well as monitor input and output parameters. The module can be used with any standard 2-wire I^2C host device, accepts most standard PMBus commands, is compatible with SMBus version 2.0 and includes an SALRT line to help mitigate bandwidth limitations related to continuous fault monitoring. It is recommended that CTRL be pulled low while configuring the module with PMBus commands. Pull-up resistors are required on the SMBus lines as described in "RECOMMENDED OPERATING CONDITIONS".

SMBus Addresses

When communicating with multiple SMBus devices using the SMBus interface, each device must have a unique address so the host can distinguish between the devices. The NDM2Z-50 module address can be set according to the pin-strap options listed in Table 5; address values are right-justified.

If additional module addresses are required, a resistor can be connected to pin SA0 as shown in Table 6 to provide up to 25 unique module addresses.

Table 5: Pin-strap SMBus Addressing

SA0	ADDRESS
HIGH	0x22
OPEN	0x21
LOW	0x20

Table 6: Single Resistor SMBus Addressing

R_{SA0} (kΩ)	ADDRESS	R_{SA0} (kΩ)	ADDRESS
10.0	0x00	34.8	0x0D
11.0	0x01	38.3	0x0E
12.1	0x02	42.2	0x0F
13.3	0x03	46.4	0x10
14.7	0x04	51.1	0x11
16.2	0x05	56.2	0x12
17.8	0x06	61.9	0x13
19.6	0x07	68.1	0x14
21.5	0x08	75.0	0x15
23.7	0x09	82.5	0x16
26.1	0x0A	90.9	0x17
28.7	0x0B	100.0	0x18
31.6	0x0C		

When using only pin SA0 to set the SMBus address, pin SA1 should be tied to PREF.

If more than 25 unique module addresses are required or if other SMBus address values are desired, pins SA0 and SA1 can be configured with a resistor to PREF as listed in Table 7.

Using this method, the user can theoretically configure up to 625 unique SMBus addresses. However, the SMBus is inherently limited to 128 modules so attempting to configure an address higher than 128 (0x80) will cause the module address to repeat (i.e, attempting to configure a module address of 129 (0x81) would result in a module address of 1).

Therefore, the user should use index values 0-4 on pin SA1 and the full range of index values on pin SA0, which will provide 125 module address combinations. Note that the SMBus address 0x4B is reserved for module test and cannot be used in the system.

DISCONTINUED

Table 7: Dual Resistor SMBus Addressing

	10.0	11.0	12.1	13.3	14.7	R_{SA1} (kΩ)
10.0	0x00	0x19	0x32	0x4B	0x64	
11.0	0x01	0x1A	0x33	0x4C	0x65	
12.1	0x02	0x1B	0x34	0x4D	0x66	
13.3	0x03	0x1C	0x35	0x4E	0x67	
14.7	0x04	0x1D	0x36	0x4F	0x68	
16.2	0x05	0x1E	0x37	0x50	0x69	
17.8	0x06	0x1F	0x38	0x51	0x6A	
19.6	0x07	0x20	0x39	0x52	0x6B	
21.5	0x08	0x21	0x3A	0x53	0x6C	
23.7	0x09	0x22	0x3B	0x54	0x6D	
26.1	0x0A	0x23	0x3C	0x55	0x6E	
28.7	0x0B	0x24	0x3D	0x56	0x6F	
31.6	0x0C	0x25	0x3E	0x57	0x70	
34.8	0x0D	0x26	0x3F	0x58	0x71	
38.3	0x0E	0x27	0x40	0x59	0x72	
42.2	0x0F	0x28	0x41	0x5A	0x73	
46.4	0x10	0x29	0x42	0x5B	0x74	
51.1	0x11	0x2A	0x43	0x5C	0x75	
56.2	0x12	0x2B	0x44	0x5D	0x76	
61.9	0x13	0x2C	0x45	0x5E	0x77	
68.1	0x14	0x2D	0x46	0x5F	0x78	
75.0	0x15	0x2E	0x47	0x60	0x79	
82.5	0x16	0x2F	0x48	0x61	0x7A	
90.9	0x17	0x30	0x49	0x62	0x7B	
100.0	0x18	0x31	0x4A	0x63	0x7C	
R_{SA0} (kΩ)						

Monitoring Via SMBus

A system controller can be used to monitor the NDM2Z-50 module system parameters through the SMBus. Fault conditions can be detected by monitoring the SALRT pin, which will be asserted when pre-configured fault conditions occur. Modules can also be monitored for power conversion parameters including but not limited to the following:

- Input voltage
- Output voltage
- Output current
- Module temperature
- Switching frequency
- Duty cycle

SINGLE WIRE COMMUNICATIONS

Digital-DC Bus

The DDC (Digital-DC Communication Bus) is used to communicate between NDM2Z modules. This dedicated bus provides the communication channel between modules for features such as sequencing, fault spreading, and current sharing. A pull-up resistor is required on the DDC as defined in "RECOMMENDED OPERATING CONDITIONS".

Snapshot™ Parameter Capture

The NDM2Z-50 module offers features that enable the user to capture parametric data during normal operation or following a fault. The Snapshot feature enables the user to read status and parameter values via a block read transfer through the SMBus. This can be done during normal operation, although it should be noted that reading the 22 bytes will occupy the SMBus for up to 1400 µs.
The SNAPSHOT_CONTROL command enables the user to store the snapshot parameters to flash memory in response to a pending fault as well as to read the stored data from flash memory after a fault has occurred. Automatic writes to flash memory following a fault are triggered when any fault threshold level is exceeded, provided that the specific response to that fault is to shut down (writing to flash memory is not allowed if the module is configured to re-try following the specific fault condition). It should also be noted that the input voltage to the module must be maintained during the time when the module is writing the data to flash memory; a process that requires between 700 µs to 1400 µs depending on whether the data is set up for a block write. Undesirable results may be observed if the input voltage to the module drops too low during this process. In the event that the module experiences a fault and power is lost, the user can extract the last SNAPSHOT parameters stored during the fault by using the SMBus to transfer data from flash memory to RAM and then using the SMBus to read data from RAM.

THERMAL CONSIDERATIONS

Mounting

Heat from the NDM2Z-50 module will be conducted through the pins to the host board. Provisions must be made for the host board to accommodate this additional heating.

Airflow

Airflow past the NDM2Z-50 module will assist in cooling the module. Factors affecting the efficiency of the cooling include the rate, direction and temperature of the airflow.

DISCONTINUED

REVISION HISTORY

rev.	date
1.0	09/28/2015
1.1	12/16/2015

The revision history provided is for informational purposes only and is believed to be accurate.

DISCONTINUED

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