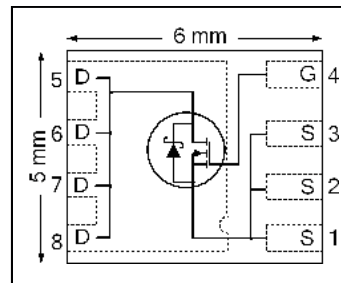


HEXFET® Power MOSFET

$V_{DSS}$	25	V
$R_{DS(on) max}$ (@ $V_{GS} = 10V$ )	1.10	mΩ
(@ $V_{GS} = 4.5V$ )	1.35	
$Qg$ (typical)	36	nC
$I_D$ (@ $T_C (Bottom) = 25°C$ )	100Ⓣ	A



### Applications

- Synchronous Rectifier MOSFET for Synchronous Buck Converters

### Features

Low $R_{DS(ON)}$ (<1.10 mΩ)
Schottky Intrinsic Diode with Low Forward Voltage
Low Thermal Resistance to PCB (<1.0°C/W)
Low Profile (<0.9 mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant, Halogen-Free
MSL1, Industrial Qualification

results in  
⇒

### Benefits

Lower Conduction Losses
Lower Switching Losses
Enable better thermal dissipation
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFH4209DPbF	PQFN 5mm x 6 mm	Tape and Reel	4000	IRFH4209DTRPbF

### Absolute Maximum Ratings

	Parameter	Max.	Units
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$I_D @ T_A = 25°C$	Continuous Drain Current, $V_{GS} @ 10V$	44	A
$I_D @ T_{C(Bottom)} = 25°C$	Continuous Drain Current, $V_{GS} @ 10V$	260ⓉⓈ	
$I_D @ T_{C(Bottom)} = 100°C$	Continuous Drain Current, $V_{GS} @ 10V$	165ⓉⓈ	
$I_D @ T_{C(Bottom)} = 25°C$	Continuous Drain Current, $V_{GS} @ 10V$ (Source Bonding Technology Limited)	100Ⓣ	
$I_{DM}$	Pulsed Drain Current ①	400	
$P_D @ T_A = 25°C$	Power Dissipation ⑤	3.5	W
$P_D @ T_{C(Bottom)} = 25°C$	Power Dissipation	125	
	Linear Derating Factor	0.028	W/°C
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑦ are on page 9

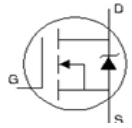
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions	
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	25	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA	
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	18	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 10mA	
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	0.85	1.10	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 50A ③	
		—	1.10	1.35		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 50A ③	
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.1	1.6	2.1	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100μA	
ΔV <sub>GS(th)</sub>	Gate Threshold Voltage Coefficient	—	-9.0	—	mV/°C		
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	250	μA	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V	
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V	
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V	
g <sub>fs</sub>	Forward Transconductance	300	—	—	S	V <sub>DS</sub> = 13V, I <sub>D</sub> = 50A	
Q <sub>g</sub>	Total Gate Charge	—	74	—	nC	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 13V, I <sub>D</sub> = 50A	
Q <sub>g</sub>	Total Gate Charge	—	36	54	nC	V <sub>DS</sub> = 13V V <sub>GS</sub> = 4.5V I <sub>D</sub> = 50A	
	Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—	7.5			—
	Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	—	4.4			—
	Q <sub>gd</sub>	Gate-to-Drain Charge	—	12.0			—
	Q <sub>godr</sub>	Gate Charge Overdrive	—	12.1			—
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—	16.4	—			
Q <sub>oss</sub>	Output Charge	—	37	—	nC	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V	
R <sub>G</sub>	Gate Resistance	—	0.8	—	Ω		
t <sub>d(on)</sub>	Turn-On Delay Time	—	15	—	ns	V <sub>DD</sub> = 13V, V <sub>GS</sub> = 4.5V I <sub>D</sub> = 50A R <sub>G</sub> = 1.8Ω	
t <sub>r</sub>	Rise Time	—	49	—			
t <sub>d(off)</sub>	Turn-Off Delay Time	—	21	—			
t <sub>f</sub>	Fall Time	—	17	—			
C <sub>iss</sub>	Input Capacitance	—	4620	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 13V f = 1.0MHz	
C <sub>oss</sub>	Output Capacitance	—	1450	—			
C <sub>rss</sub>	Reverse Transfer Capacitance	—	340	—			

**Avalanche Characteristics**

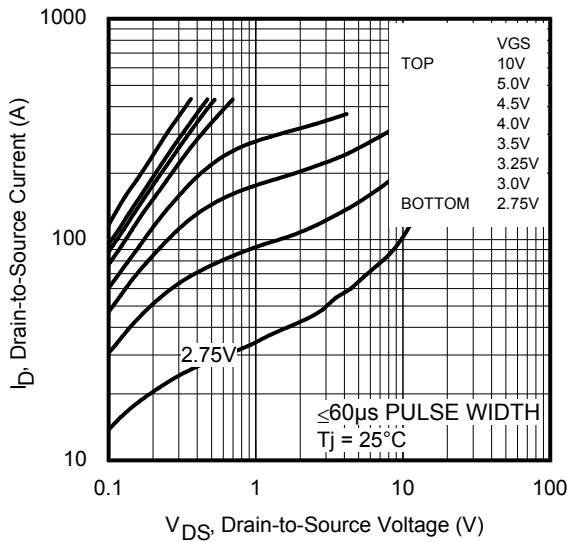
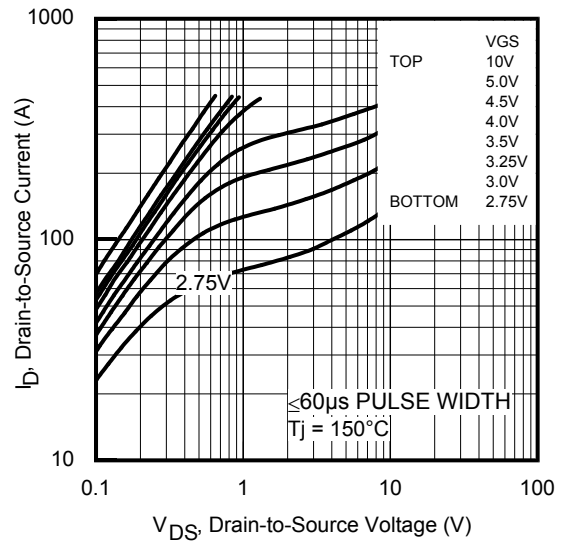
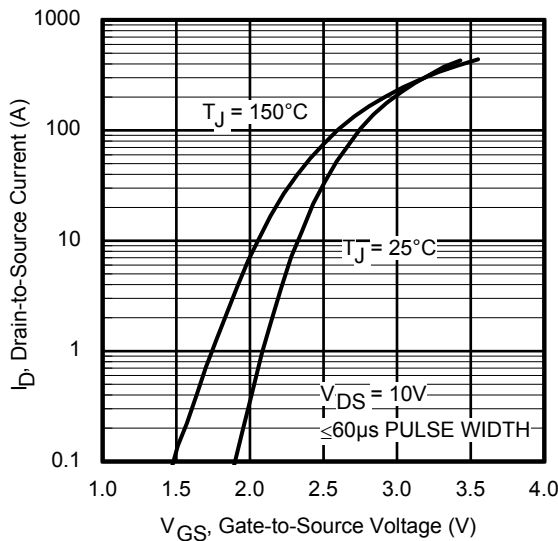
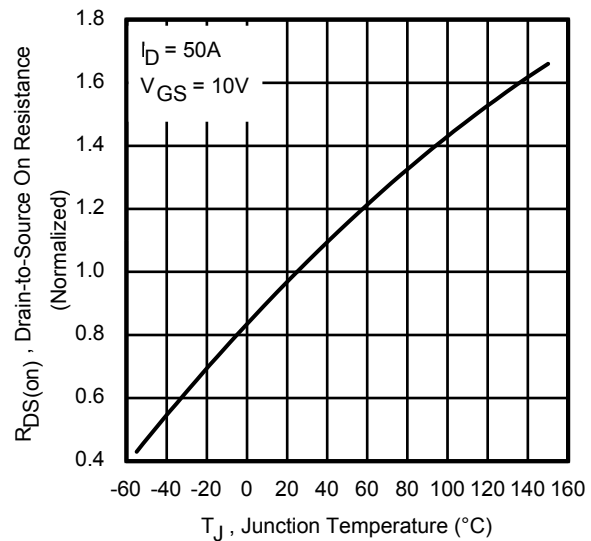
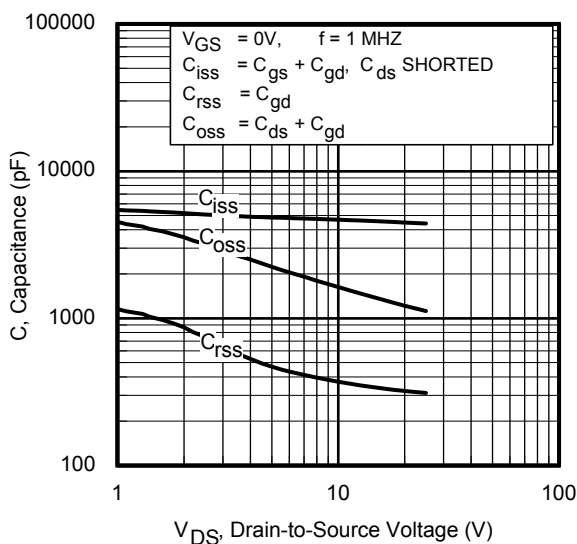
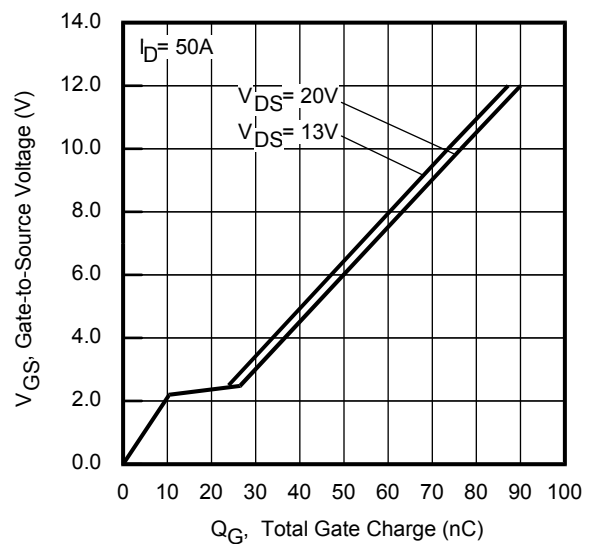
	Parameter	Typ.	Max.
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	247
I <sub>AR</sub>	Avalanche Current ①	—	50

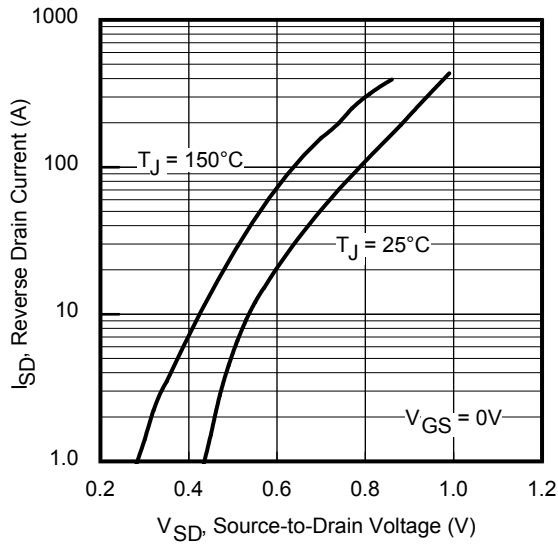
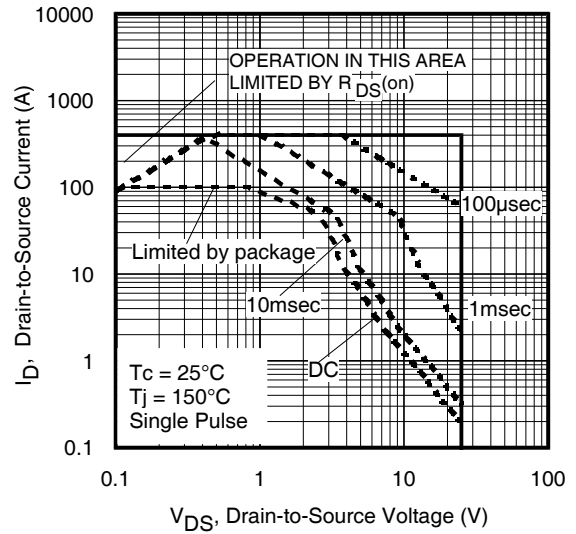
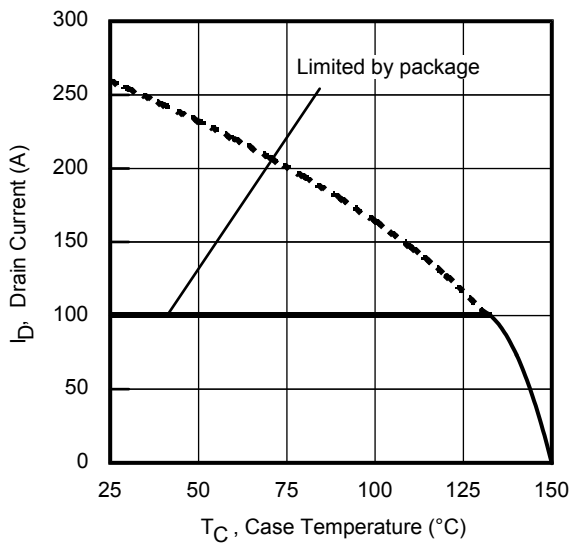
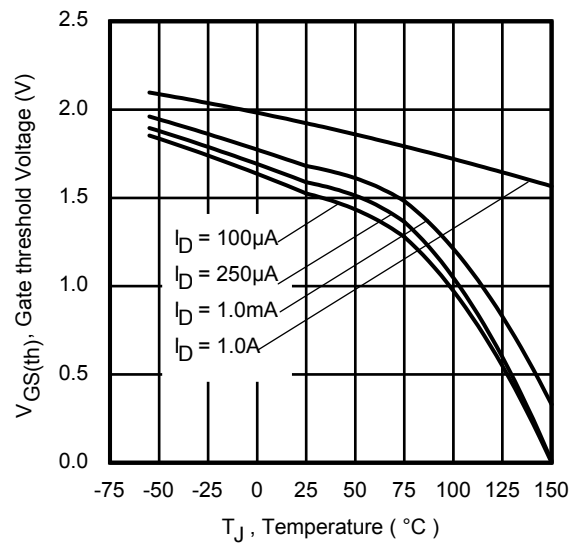
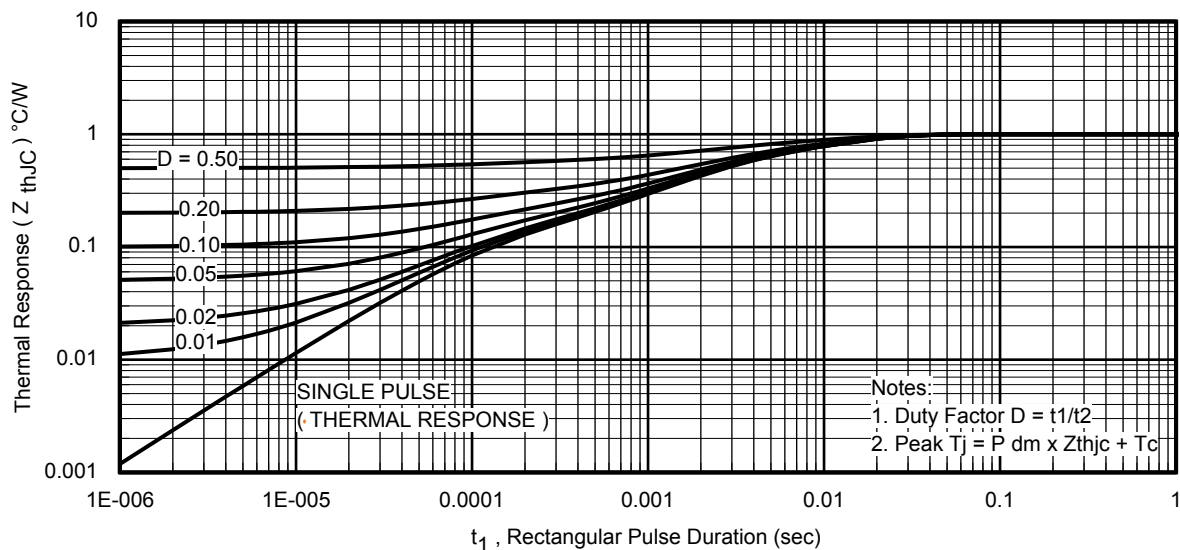
**Diode Characteristics**

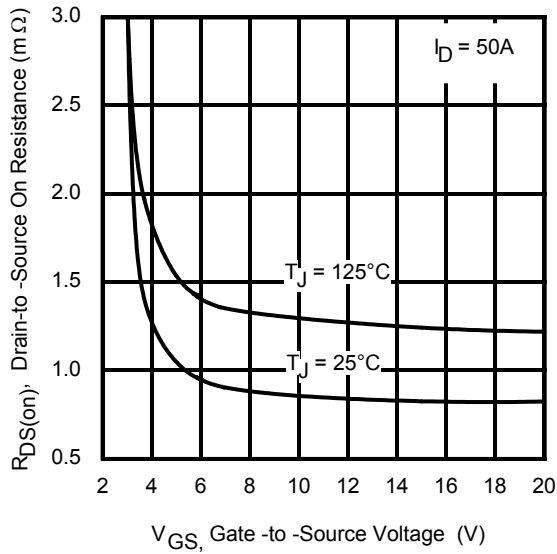
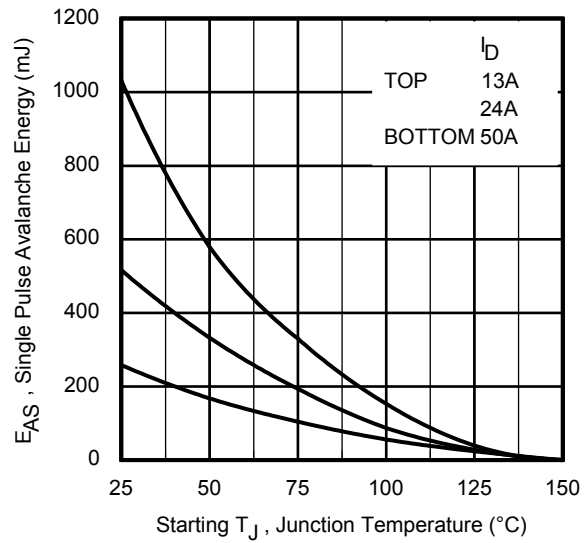
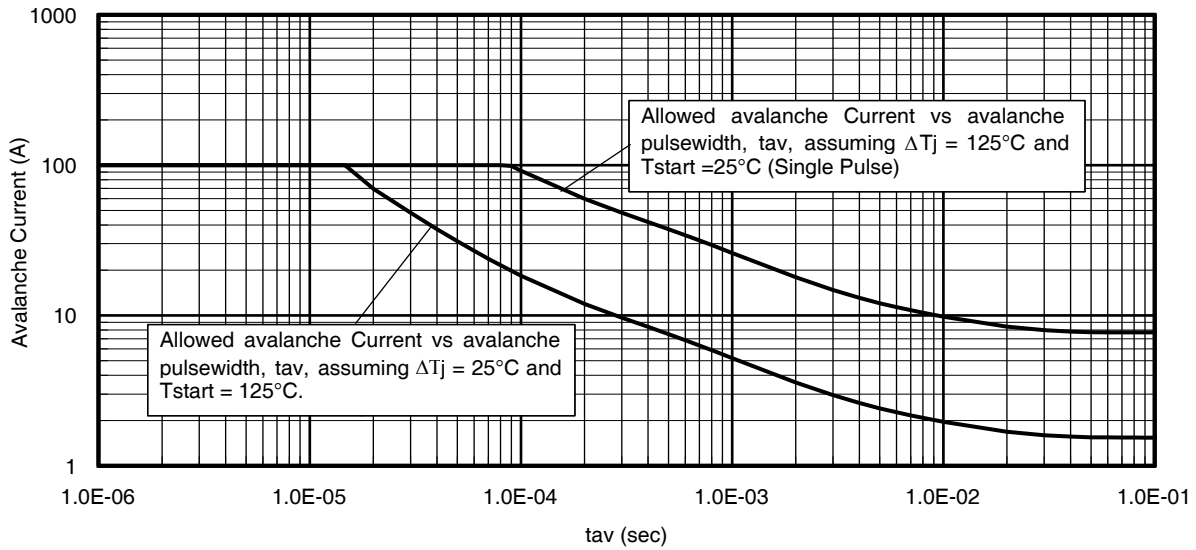
	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	100 <sup>⑦</sup>	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	400		
V <sub>SD</sub>	Diode Forward Voltage	—	—	0.75	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 50A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	33	50	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 50A, V <sub>DD</sub> = 13V
Q <sub>rr</sub>	Reverse Recovery Charge	—	83	125	nC	di/dt = 300A/μs ③

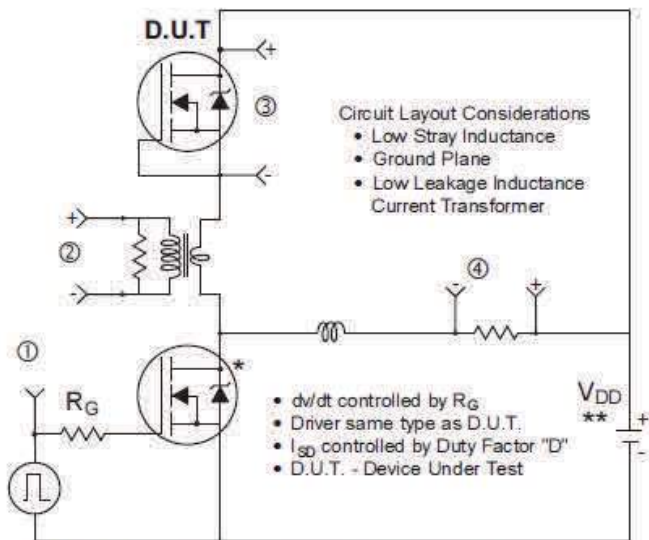
**Thermal Resistance**

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub> (Bottom)	Junction-to-Case ④	—	1.0	°C/W
R <sub>θJC</sub> (Top)	Junction-to-Case ④	—	22	
R <sub>θJA</sub>	Junction-to-Ambient ⑤	—	36	
R <sub>θJA</sub> (<10s)	Junction-to-Ambient ⑤	—	21	

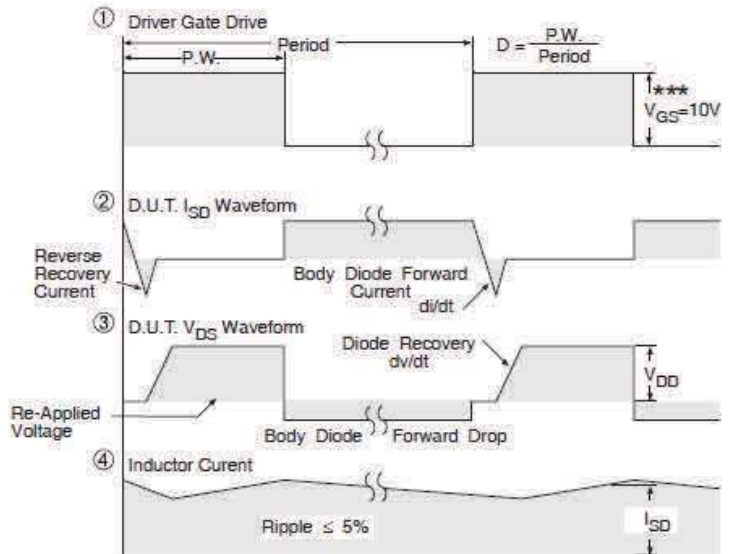

**Fig 1. Typical Output Characteristics**

**Fig 2. Typical Output Characteristics**

**Fig 3. Typical Transfer Characteristics**

**Fig 4. Normalized On-Resistance vs. Temperature**

**Fig 5. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 7.** Typical Source-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area

**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10.** Drain-to-Source Breakdown Voltage

**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case


**Fig 12.** On-Resistance vs. Gate Voltage

**Fig 13.** Maximum Avalanche Energy vs. Drain Current

**Fig 14.** Typical Avalanche Current vs. Pulse Width

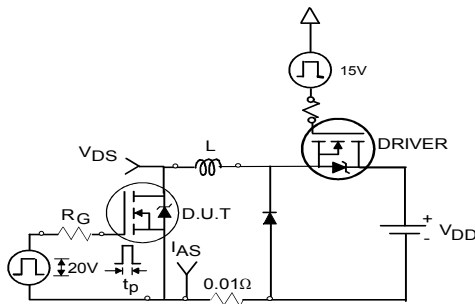


\* Use P-Channel Driver for P-Channel Measurements  
 \*\* Reverse Polarity for P-Channel

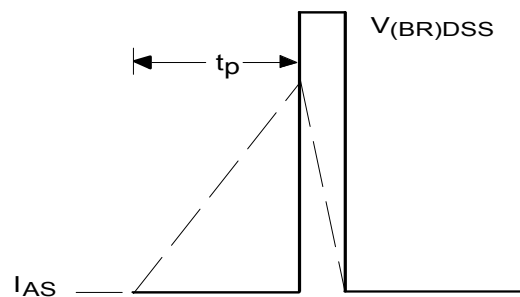


\*\*\*  $V_{GS} = 5V$  for Logic Level Devices

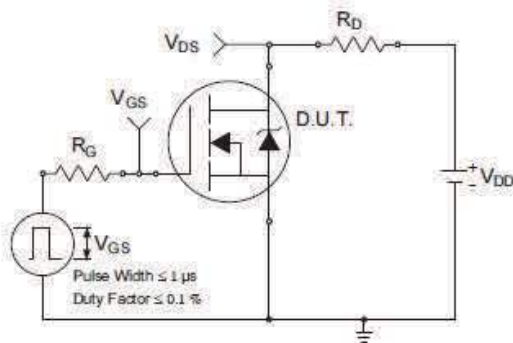
**Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**



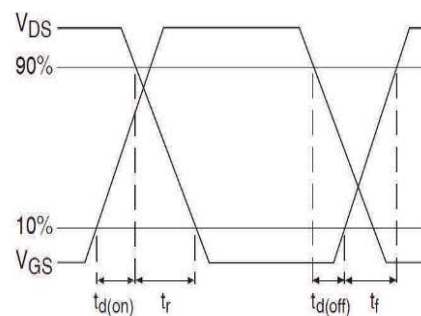
**Fig 16a. Unclamped Inductive Test Circuit**



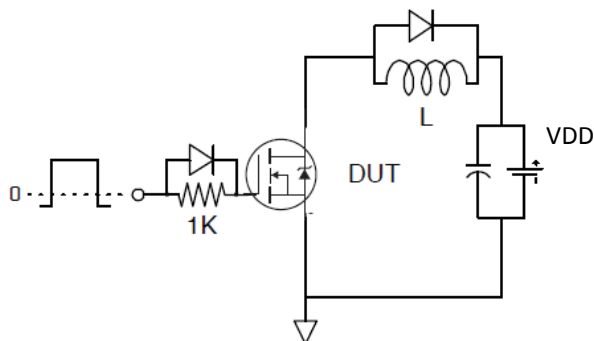
**Fig 16b. Unclamped Inductive Waveforms**



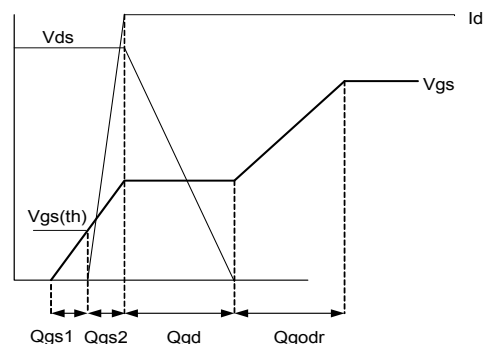
**Fig 17a. Switching Time Test Circuit**



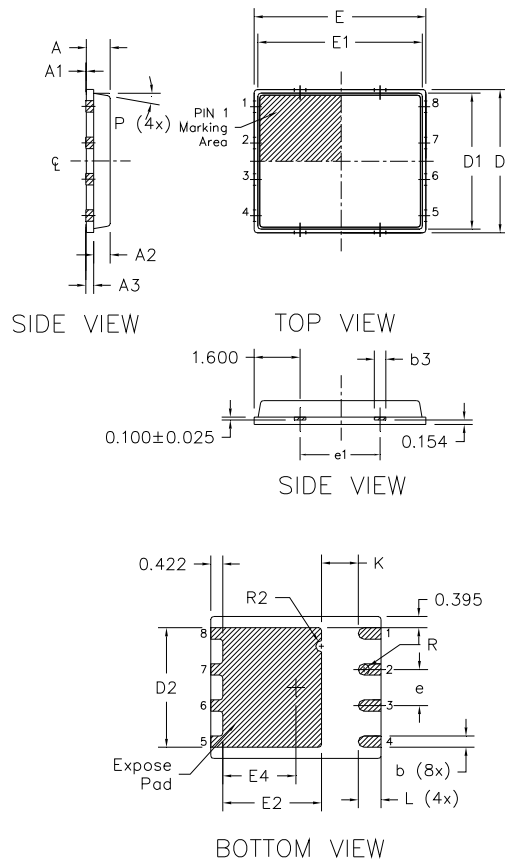
**Fig 17b. Switching Time Waveforms**



**Fig 18. Gate Charge Test Circuit**



**Fig 19. Gate Charge Waveform**

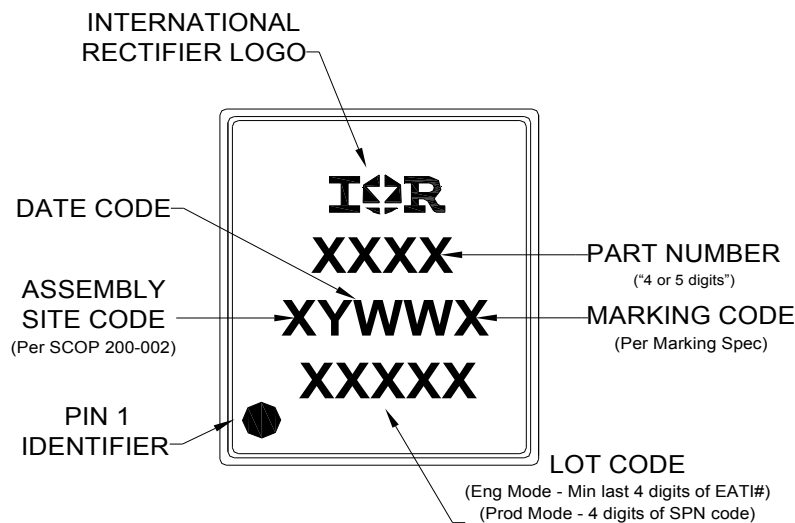
**PQFN 5x6 Outline "B" Package Details**


DIM SYMBOL	MILLIMETERS		INCH	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.0315	0.0543
A1	0.000	0.050	0.0000	0.0020
A3	0.200	REF	0.0079	REF
b	0.350	0.470	0.0138	0.0185
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.150	0.450	0.0059	0.0177
D	5.000	BSC	0.1969	BSC
D1	4.750	BSC	0.1870	BSC
D2	4.100	4.300	0.1614	0.1693
E	6.000	BSC	0.2362	BSC
E1	5.750	BSC	0.2264	BSC
E2	3.380	3.780	0.1331	0.1488
e	1.270	REF	0.0500	REF
e1	2.800	REF	0.1102	REF
K	1.200	1.420	0.0472	0.0559
L	0.710	0.900	0.0280	0.0354
P	0°	12°	0°	12°
R	0.200	REF	0.0079	REF
R2	0.150	0.200	0.0059	0.0079

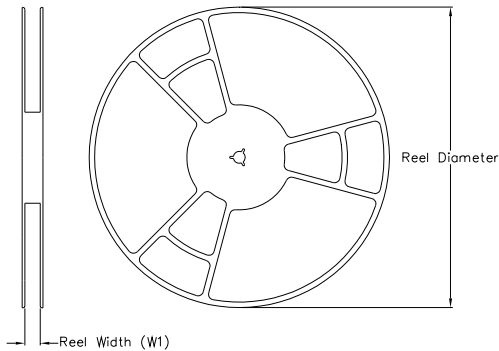
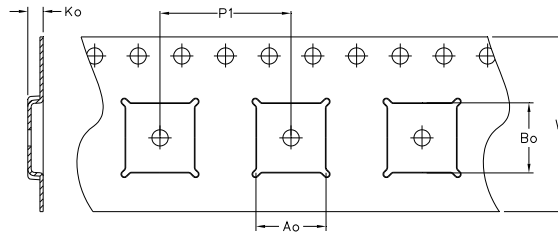
**Note:**

1. Dimensions and tolerancing confirm to ASME Y14.5M-1994
2. Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
3. Coplanarity applies to the expose Heat Slug as well as the terminal
4. Radius on terminal is Optional

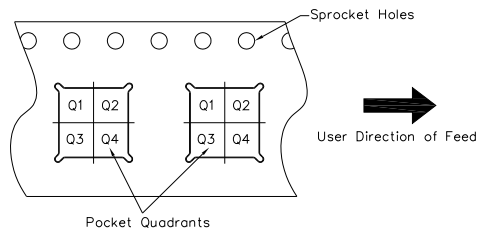
For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>  
 For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

**PQFN 5x6 Part Marking**


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**PQFN 5x6 Tape and Reel**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


CODE	DESCRIPTION
Ao	Dimension design to accommodate the component width
Bo	Dimension design to accommodate the component length
Ko	Dimension design to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>



**Qualification Information†**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F†† guidelines)	
<b>Moisture Sensitivity Level</b>	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D††)
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability>

†† Applicable version of JEDEC standard at the time of product release.

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.21\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 50\text{A}$ .
- ③ Pulse width  $\leq 400 \mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ⑤ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:  
<http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
- ⑦ Current is limited to 100A by source bonding technology.

**Revision History**

3/16/2015	• Updated package outline and tape and reel on pages 7 and 8.
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