DRV883x Low-Voltage H-Bridge Driver

1 Features

- H-Bridge Motor Driver
  - Drives a DC Motor or Other Loads
  - Low MOSFET On-Resistance: HS + LS 280 mΩ
- 1.8-A Maximum Drive Current
- Separate Motor and Logic Supply Pins:
  - Motor VM: 0 to 11 V
  - Logic VCC: 1.8 to 7 V
- PWM or PH-EN Interface
  - DRV8837: PWM, IN1 and IN2
  - DRV8838: PH and EN
- Low-Power Sleep Mode With 120-nA Maximum Sleep Current
  - nSLEEP pin
- Small Package and Footprint
  - 8-Pin WSON With Thermal Pad
  - 2.0 × 2.0 mm
- Protection Features
  - VCC Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)

2 Applications

- Cameras
- DSLR Lenses
- Consumer Products
- Toys
- Robotics
- Medical Devices

3 Description

The DRV883x family of devices provides an integrated motor driver solution for cameras, consumer products, toys, and other low-voltage or battery-powered motion control applications. The device can drive one dc motor or other devices like solenoids. The output driver block consists of N-channel power MOSFETs configured as an H-bridge to drive the motor winding. An internal charge pump generates needed gate drive voltages.

The DRV883x family of devices can supply up to 1.8 A of output current. It operates on a motor power supply voltage from 0 to 11 V, and a device power supply voltage of 1.8 V to 7 V.

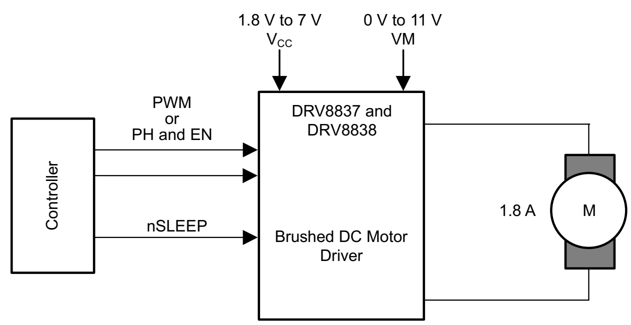
The DRV8837 device has a PWM (IN1-IN2) input interface; the DRV8838 device has a PH-EN input interface. Both interfaces are compatible with industry-standard devices.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, undervoltage lockout, and overtemperature.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8837	WSON (8)	2.00 mm × 2.00 mm
DRV8838		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



DRV883x Simplified Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (June 2016) to Revision F (April 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document.......1
- Added in the *Independent Half-Bridge Control* section.......13

Changes from Revision D (December 2015) to Revision E (June 2016) **Page**

- Changed the threshold type to the input logic voltage parameters in the *Electrical Characteristics* table.......8
- Changed the units for the input logic hysteresis parameter from mV to V in the *Electrical Characteristics* table 8
- Added the *Receiving Notification of Documentation Updates* section 21

Changes from Revision C (February 2014) to Revision D (December 2015) **Page**

- Clarified the input interface for each device in the *Description* section 1
- Added CDM and HBM ESD ratings to the *ESD Ratings* table 6

Changes from Revision B (December 2013) to Revision C (February 2014) **Page**

- Added the DRV8838 device information, specifications, and timing diagrams.......1
- Added Device Information table.......1
- Added a PWM interface diagram 1
- Added more information to the Detailed Description and moved information from the Functional Description ... 11
- Added functional block diagram for DRV8838 11
- Added the *Application and Implementation* section 17
- Added *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections.......19

Changes from Revision A (August 2012) to Revision B (December 2013) **Page**

5 Pin Configuration and Functions

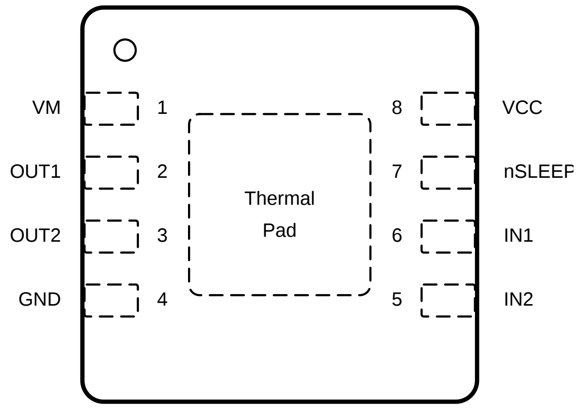


Figure 5-1. DSG Package 8-Pin WSON With Thermal Pad DRV8837 Top View

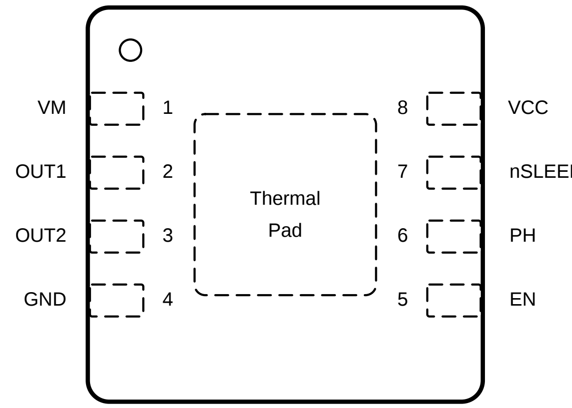


Figure 5-2. DSG Package 8-Pin WSON With Thermal Pad DRV8838 Top View

Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	DRV8837	DRV8838		
POWER AND GROUND				
GND	4	4	—	Device ground This pin must be connected to ground.
VCC	8	8	I	Logic power supply Bypass this pin to the GND pin with a 0.1-µF ceramic capacitor rated for VCC.
VM	1	1	I	Motor power supply Bypass this pin to the GND pin with a 0.1-µF ceramic capacitor rated for VM.
CONTROL				
EN	—	5	I	ENABLE input
IN1	6	—	I	IN1 input See the *Section 7* section for more information.
IN2	5	—	I	IN2 input See the *Section 7* section for more information.
PH	—	6	I	PHASE input See the *Section 7* section for more information.
nSLEEP	7	7	I	Sleep mode input When this pin is in logic low, the device enters low-power sleep mode. The device operates normally when this pin is logic high. Internal pulldown
OUTPUT				
OUT1	2	2	O	Motor output Connect these pins to the motor winding.
OUT2	3	3	O	

5.1 Dapper Pin Functions

PIN			I/O	DESCRIPTION
NAME	DRV8837 NO.	DRV8838 NO.		
GND	4	4	—	Device ground This pin must be connected to ground.
VCC	8	8	I	Logic power supply Bypass this pin to the GND pin with a 0.1-µF ceramic capacitor rated for VCC.

PIN			I/O	DESCRIPTION
NAME	DRV8837 NO.	DRV8838 NO.		
VM	1	1	I	Motor power supply Bypass this pin to the GND pin with a 0.1-µF ceramic capacitor rated for VM.
EN	—	5	I	ENABLE input
IN1	6	—	I	IN1 input See the *Section 7* section for more information.
IN2	5	—	I	IN2 input See the *Section 7* section for more information.
PH	—	6	I	PHASE input See the *Section 7* section for more information.
nSLEEP	7	7	I	Sleep mode input When this pin is in logic low, the device enters low-power sleep mode. The device operates normally when this pin is logic high. Internal pulldown
OUT1	2	2	O	Motor output Connect these pins to the motor winding.
OUT2	3	3	O	

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[(1)] [(2)]

		MIN	MAX	UNIT
Motor power-supply voltage	VM	–0.3	12	V
Logic power-supply voltage	VCC	–0.3	7	V
Control pin voltage	IN1, IN2, PH, EN, nSLEEP	–0.5	7	V
Peak drive current	OUT1, OUT2	Internally limited		A
Operating virtual junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

6.2 ESD Ratings

over operating ambient temperature range (unless otherwise noted)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
VM	Motor power supply voltage	0	11	V
VCC	Logic power supply voltage	1.8	7	V
I_{OUT}	Motor peak current	0	1.8	A
f_{PWM}	Externally applied PWM frequency	0	250	kHz
V_{LOGIC}	Logic level input voltage	0	5.5	V
T_A	Operating ambient temperature	–40	85	°C

(1) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC[(1)]		DRV883x DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.8	°C/W

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC[1]		DRV883x DSG (WSON) 8 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.8	°C/W

(1) For more information about traditional and new thermal limits, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, VCC)						
VM	VM operating voltage		0		11	V
I_{VM}	VM operating supply current	VM = 5 V; VCC = 3 V; No PWM		40	100	µA
		VM = 5 V; VCC = 3 V; 50 kHz PWM		0.8	1.5	mA
I_{VMQ}	VM sleep mode supply current	VM = 5 V; VCC = 3 V; nSLEEP = 0		30	95	nA
VCC	VCC operating voltage		1.8		7	V
I_{VCC}	VCC operating supply current	VM = 5 V; VCC = 3 V; No PWM		300	500	µA
		VM = 5 V; VCC = 3 V; 50 kHz PWM		0.7	1.5	mA
I_{VCCQ}	VCC sleep mode supply current	VM = 5 V; VCC = 3 V; nSLEEP = 0		5	25	nA
CONTROL INPUTS (IN1 or PH, IN2 or EN, nSLEEP)						
V_{IL}	Input logic-low voltage falling threshold		0.25 × VCC	0.38 × VCC		V
V_{IH}	Input logic-high voltage rising threshold			0.46 × VCC	0.5 × VCC	V
V_{HYS}	Input logic hysteresis			0.08 × VCC		V
I_{IL}	Input logic low current	V_{IN} = 0 V	–5		5	µA
I_{IH}	Input logic high current	V_{IN} = 3.3 V			50	µA
		V_{IN} = 3.3 V, DRV8838 nSLEEP pin		60		µA
R_{PD}	Pulldown resistance			100		kΩ
		DRV8838 nSLEEP pin		55		kΩ
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
$r_{DS(on)}$	HS + LS FET on-resistance	VM = 5 V; VCC = 3 V; I_O = 800 mA; T_J = 25°C		280	330	mΩ
I_{OFF}	Off-state leakage current	V_{OUT} = 0 V	–200		200	nA
PROTECTION CIRCUITS						
V_{UVLO}	VCC undervoltage lockout	VCC falling			1.7	V
		VCC rising			1.8	
I_{OCP}	Overcurrent protection trip level		1.9		3.5	A
t_{DEG}	Overcurrent deglitch time			1		µs
t_{RETRY}	Overcurrent retry time			1		ms
T_{TSD}	Thermal shutdown temperature	Die temperature T_J	150	160	180	°C

6.6 Timing Requirements

T_A = 25°C, VM = 5 V, VCC = 3 V, RL = 20 Ω

NO.				MIN	MAX	UNIT
1	t_1	Delay time, PHASE high to OUT1 low	See Figure 6-1.		160	ns
2	t_2	Delay time, PHASE high to OUT2 high			200	ns
3	t_3	Delay time, PHASE low to OUT1 high			200	ns
4	t_4	Delay time, PHASE low to OUT2 low			160	ns
5	t_5	Delay time, ENBL high to OUTx high			200	ns
6	t_6	Delay time, ENBL low to OUTx low			160	ns
7	t_7	Output enable time	See Figure 6-2.		300	ns
8	t_8	Output disable time			300	ns
9	t_9	Delay time, INx high to OUTx high			160	ns
10	t_{10}	Delay time, INx low to OUTx low			160	ns
11	t_{11}	Output rise time		30	188	ns
12	t_{12}	Output fall time		30	188	ns
	t_{wake}	Wake time, nSLEEP rising edge to part active			30	μs

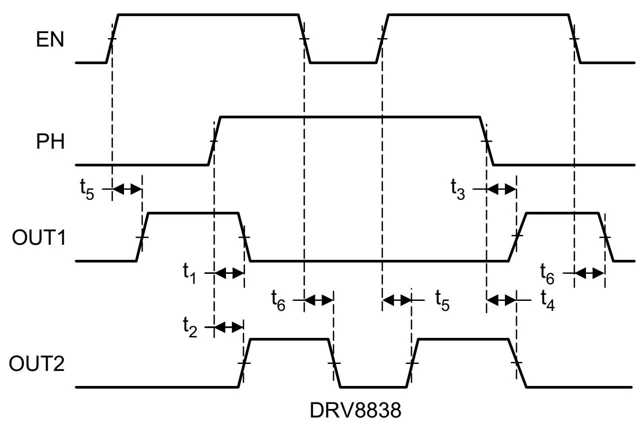


Figure 6-1. Input and Output Timing for DRV8838

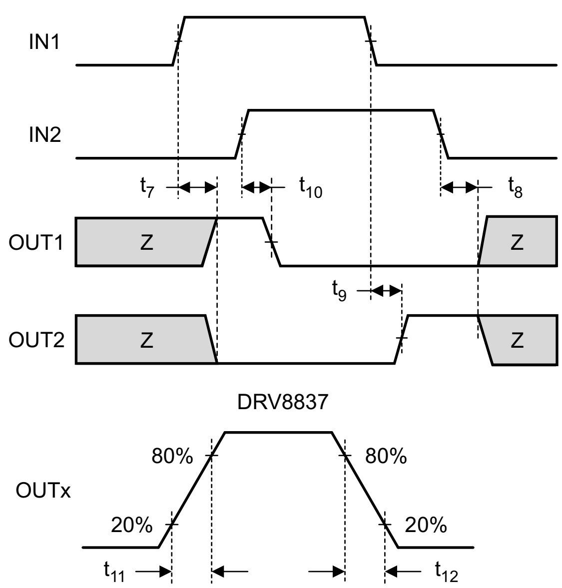


Figure 6-2. Input and Output Timing for DRV8837

6.7 Typical Characteristics

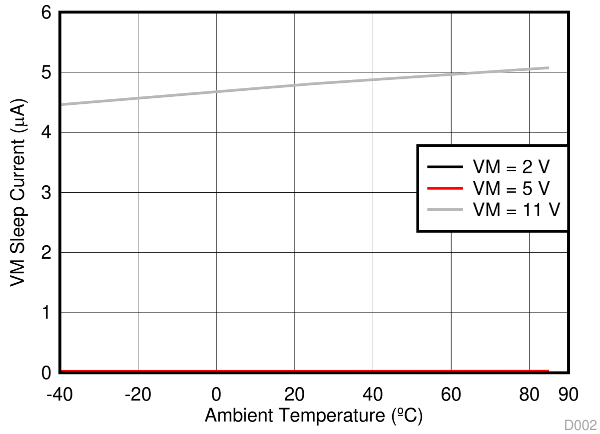


Figure 6-3. I_{VMQ} vs T_A

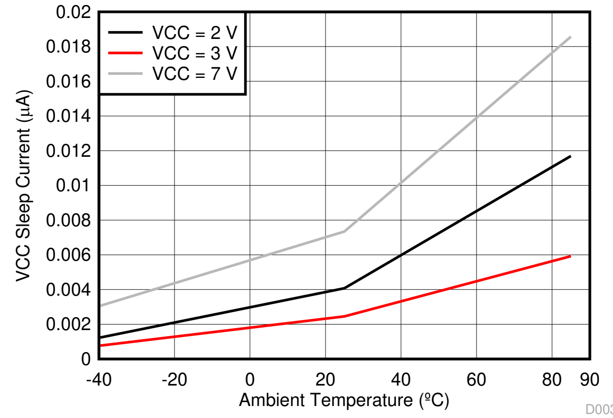


Figure 6-4. I_{VCCQ} vs T_A

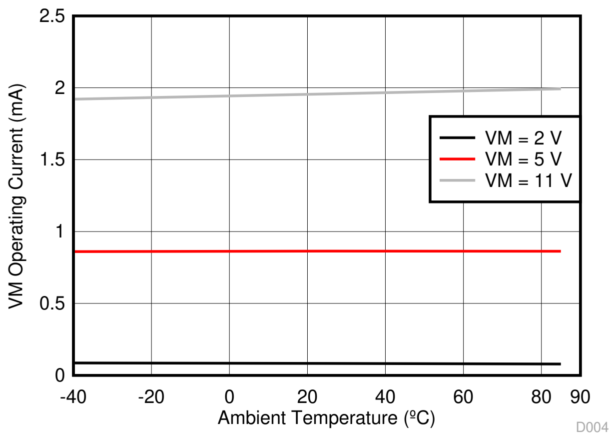


Figure 6-5. I_{VM} vs T_A (50-kHz PWM)

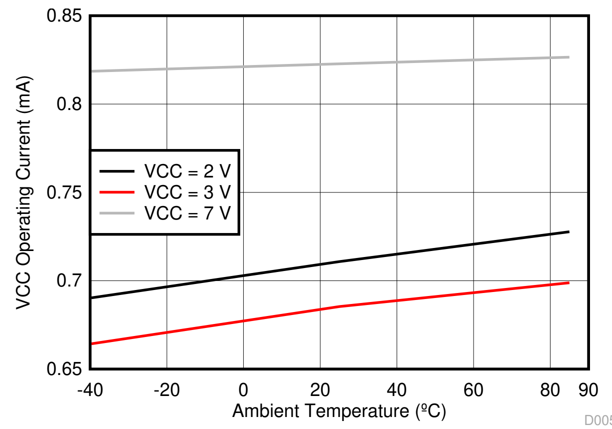


Figure 6-6. I_{VCC} vs T_A (50-kHz PWM)

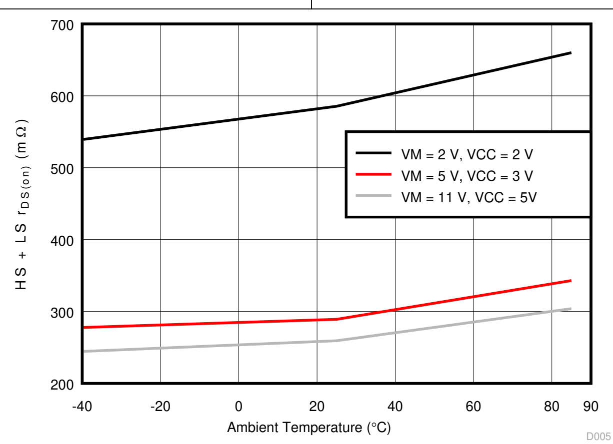


Figure 6-7. HS + LS $r_{DS(on)}$ vs T_A

7 Detailed Description

7.1 Overview

The DRV883x family of devices is an H-bridge driver that can drive one dc motor or other devices like solenoids. The outputs are controlled using either a PWM interface (IN1 and IN2) on the DRV8837 device or a PH-EN interface on the DRV8838 device.

A low-power sleep mode is included, which can be enabled using the nSLEEP pin.

These devices greatly reduce the component count of motor driver systems by integrating the necessary driver FETs and FET control circuitry into a single device. In addition, the DRV883x family of devices adds protection features beyond traditional discrete implementations: undervoltage lockout, overcurrent protection, and thermal shutdown.

7.2 Functional Block Diagram

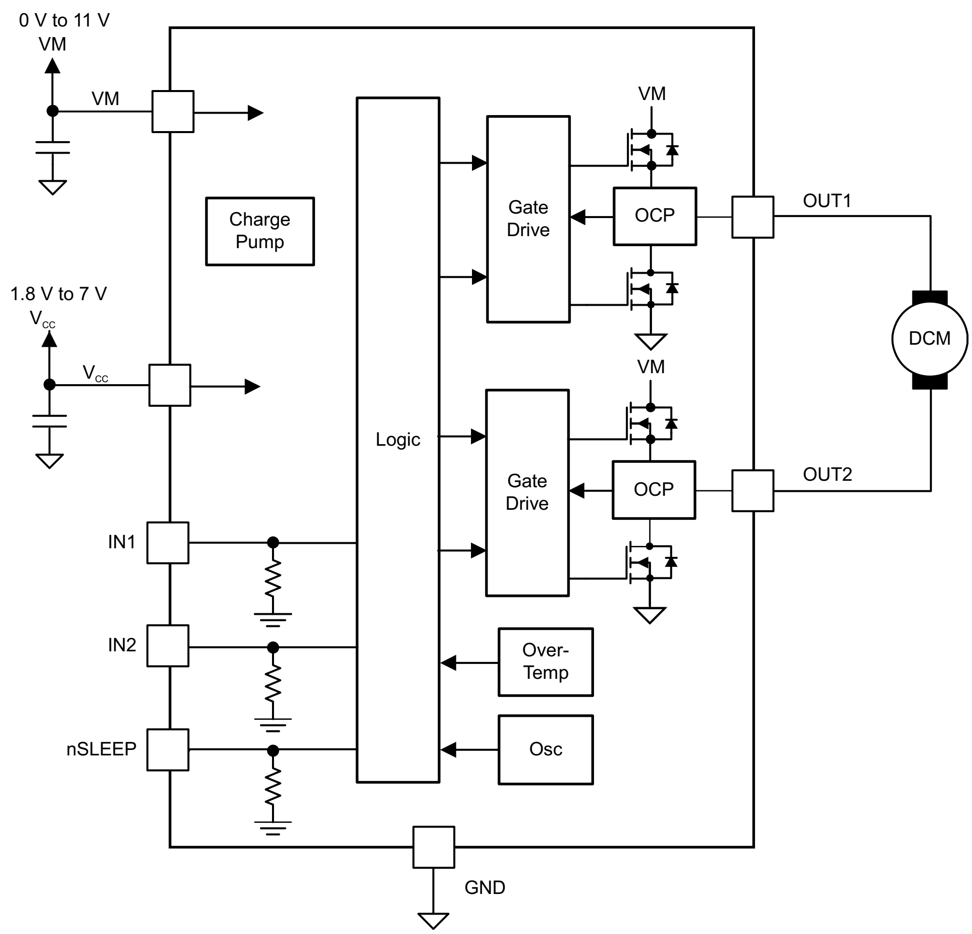


Figure 7-1. DRV8837 Functional Block Diagram

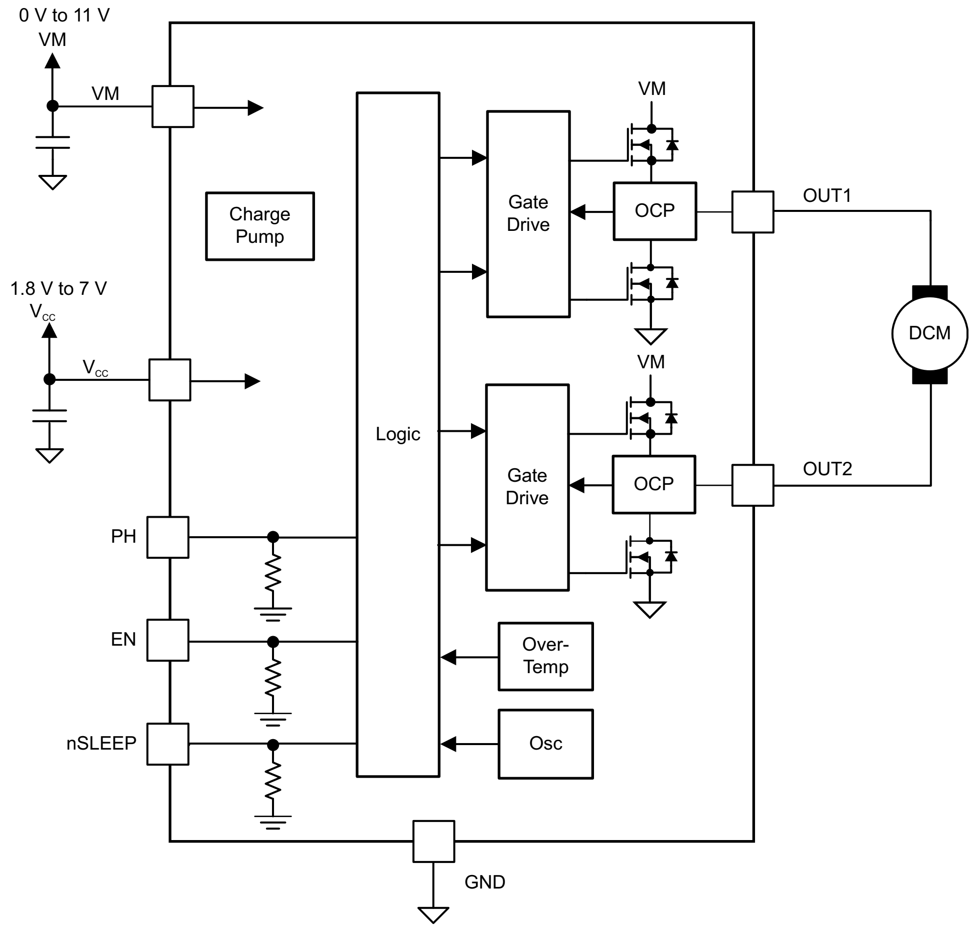


Figure 7-2. DRV8838 Functional Block Diagram

7.3 Feature Description

7.3.1 Bridge Control

The DRV8837 device is controlled using a PWM input interface, also called an IN-IN interface. Each output is controlled by a corresponding input pin.

Table 7-1 shows the logic for the DRV8837 device.

Table 7-1. DRV8837 Device Logic

nSLEEP	IN1	IN2	OUT1	OUT2	FUNCTION (DC MOTOR)
0	X	X	Z	Z	Coast
1	0	0	Z	Z	Coast
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake

The DRV8838 device is controlled using a PHASE/ENABLE interface. This interface uses one pin to control the H-bridge current direction, and one pin to enable or disable the H-bridge.

Table 7-2 shows the logic for the DRV8838.

Table 7-2. DRV8838 Device Logic

nSLEEP	PH	EN	OUT1	OUT2	FUNCTION (DC MOTOR)
0	X	X	Z	Z	Coast
1	X	0	L	L	Brake
1	1	1	L	H	Reverse
1	0	1	H	L	Forward

7.3.2 Independent Half-Bridge Control

Independent half-bridge control is possible with the DRV8837 without adopting more discrete components, as shown in Section 7.3.2. Two inductive loads (M1 and M2), which could be motors or solenoids, are tied between VM and OUTx, while the corresponding inputs (C1 and C2) are swapped before being fed to INx.

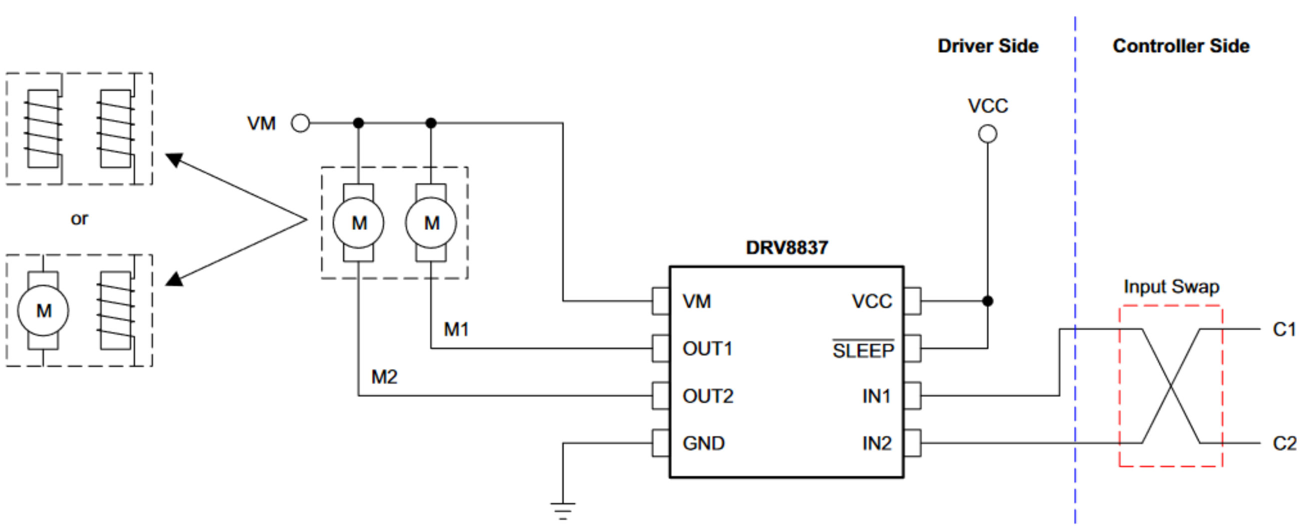


Figure 7-3. Independent Half-Bridge Control Circuit

The control logic for independent half-bridge drive is shown in Table 7-3. Columns INx and OUTx show the original logic of the DRV8837. Note that although a swap is included in this implementation, it is still valid that

Cx = 1 spins a motor or energizes a solenoid connected at corresponding Mx, while Cx = 0, stops the motor or discharges the solenoid.

Table 7-3. Independent Half-Bridge Drive Logic

C1	C2	IN1	IN2	OUT1	OUT2	M1	M2
0	0	0	0	Z	Z	Off: Braking mode 1	Off: Braking mode 1
1	0	0	1	L	H	On: Driving mode	Off: Braking mode 2
0	1	1	0	H	L	Off: Braking mode 2	On: Driving mode
1	1	1	1	L	L	On: Driving mode	On: Driving mode

Figure 7-4 shows the driving mode and the two current decay paths during current regulation when PWM input control is used. The driving mode occurs when the corresponding half-bridge Cx signal is ***HIGH***. When the Cx signal is ***LOW***, the corresponging half bridge can go into either braking mode 1 or braking mode 2. In braking mode 1, both the high- and low-side MOSFETs of the half-bridge are tri-stated, and the recirculation current flows through the body diode of the high-side MOSFET as well as the motor itself. This braking mode happens when both C1 and C2 are ***LOW***. If one of the Cx input is ***LOW*** and the other HIGH, the half-bridge corresponding to the ***LOW*** Cx input will go into braking mode 2. In braking mode 2, the low-side FET is ***OFF*** while its high-side counterpart is ***ON***. The recirculation current flows through the high-side MOSFET and the motor.

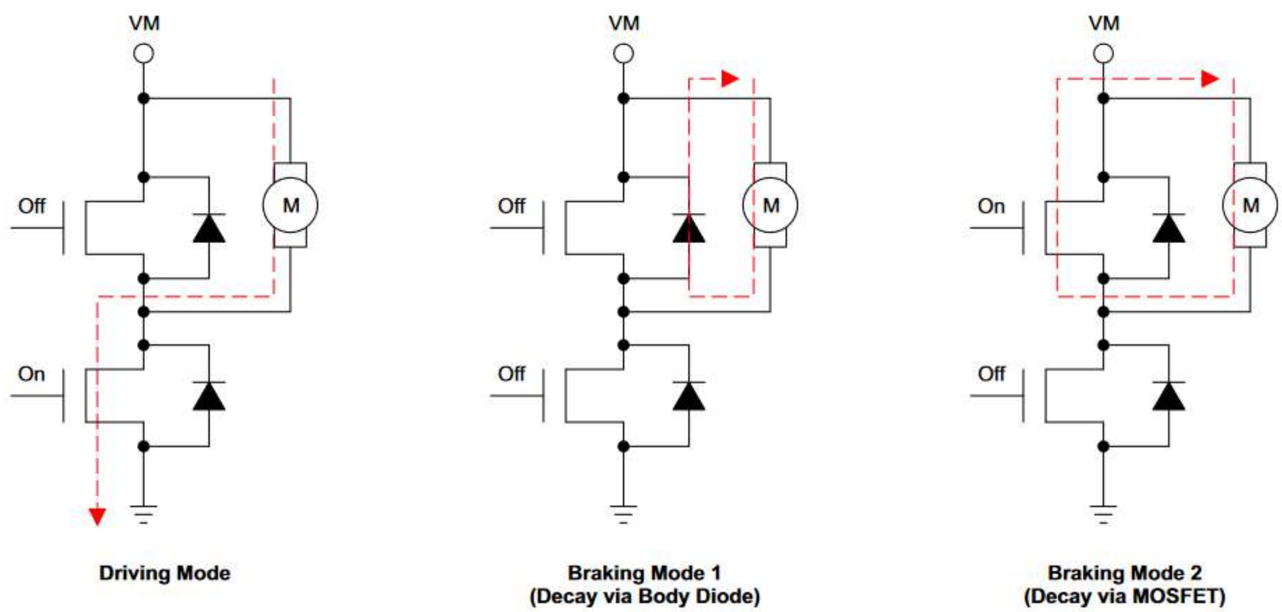


Figure 7-4. Normal Driving and Current Decay Modes

When each of the Cx inputs are independently controlled with different PWM frequencies and duty cycle, each half-bridge will go into a combination of braking mode 1 and braking mode 2. Figure 7-5 show a driving and decay example with independent PWM inputs. If the half-bridge spends more time in braking mode 1, the motor average speed will be lower since more power is dissipated through the MOSFET body diode. To reduce the power dissipated during braking mode 1, it is recommended to placed Schottky diodes with forward voltage less than 0.6V across the motors as shown in Figure 7-6. Note that if On/Off control mode (constant HIGH or LOW at inputs) is used, the two braking modes do not interact with each other and hence have no effect on the average speed of the two motors.

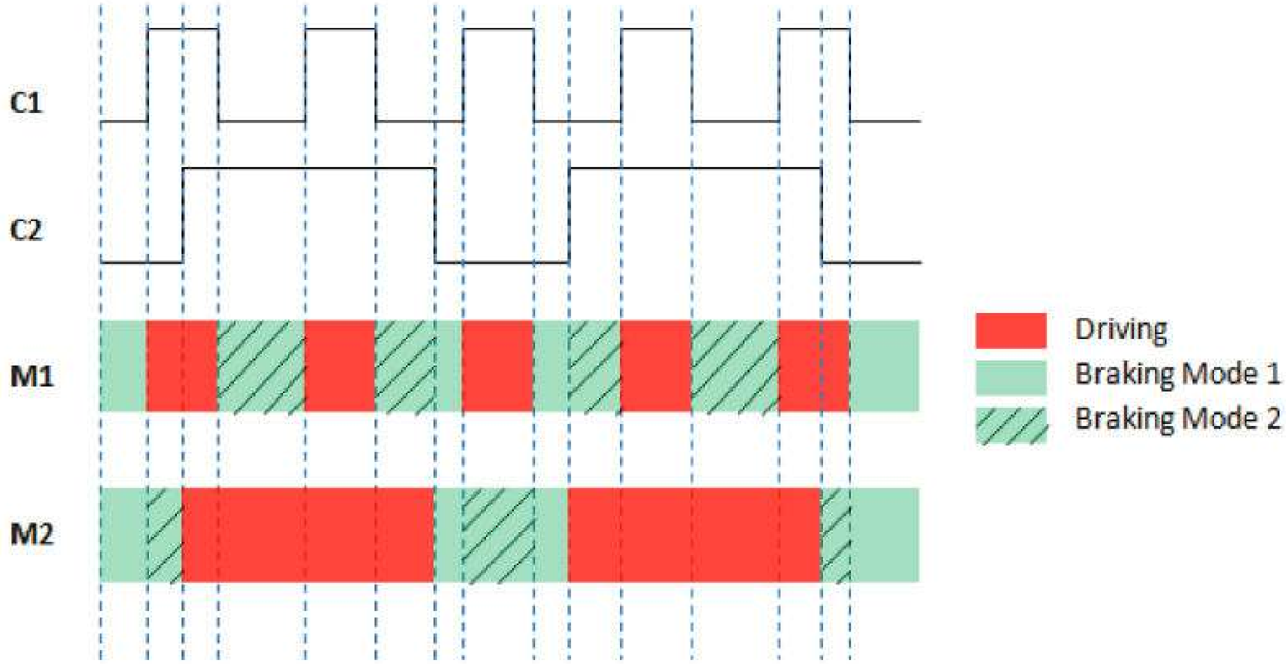


Figure 7-5. Driving and Decay Examples with Independent PWM Inputs

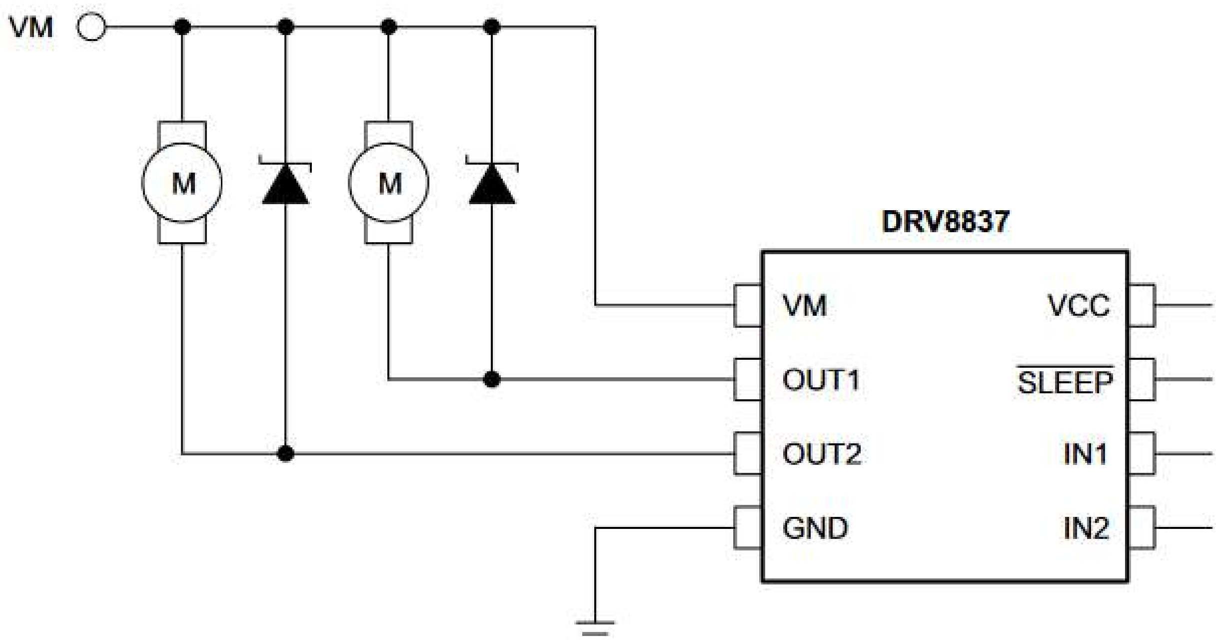


Figure 7-6. Improved Application Circuit for Better Motor Performance

7.3.3 Sleep Mode

If the nSLEEP pin is brought to a logic-low state, the DRV883x family of devices enters a low-power sleep mode. In this state, all unnecessary internal circuitry is powered down.

7.3.4 Power Supplies and Input Pins

The input pins can be driven within the recommended operating conditions with or without the VCC, VM, or both power supplies present. No leakage current path will exist to the supply. Each input pin has a weak pulldown resistor (approximately 100 kΩ) to ground.

The VCC and VM supplies can be applied and removed in any order. When the VCC supply is removed, the device enters a low-power state and draws very little current from the VM supply. The VCC and VM pins can be connected together if the supply voltage is between 1.8 and 7 V.

The VM voltage supply does not have any undervoltage-lockout protection (UVLO) so as long as VCC > 1.8 V; the internal device logic remains active, which means that the VM pin voltage can drop to 0 V. However, the load cannot be sufficiently driven at low VM voltages.

7.3.5 Protection Circuits

The DRV883x family of devices is fully protected against VCC undervoltage, overcurrent, and overtemperature events.

7.3.5.1 VCC Undervoltage Lockout

If at any time the voltage on the VCC pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge are disabled. Operation resumes when the VCC pin voltage rises above the UVLO threshold.

7.3.5.2 Overcurrent Protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than t_{DEG}, all FETs in the H-bridge are disabled. Operation resumes automatically after t_{RETRY} has elapsed. Overcurrent conditions are detected on both the high-side and low-side FETs. A short to the VM pin, GND, or from the OUT1 pin to the OUT2 pin results in an overcurrent condition.

7.3.5.3 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature falls to a safe level, operation automatically resumes.

7.3.5.4

Table 7-4. Fault Behavior

FAULT	CONDITION	H-BRIDGE	RECOVERY
VCC undervoltage (UVLO)	VCC < 1.7 V	Disabled	VCC > 1.8 V
Overcurrent (OCP)	I_{OUT} > 1.9 A (MIN)	Disabled	t_{RETRY} elapses
Thermal Shutdown (TSD)	T_J > 150°C (MIN)	Disabled	T_J < 150°C

7.4 Device Functional Modes

The DRV883x family of devices is active unless the nSLEEP pin is brought logic low. In sleep mode, the H-bridge FETs are disabled Hi-Z. The DRV883x is brought out of sleep mode automatically if nSLEEP is brought logic high.

The H-bridge outputs are disabled during undervoltage lockout, overcurrent, and overtemperature fault conditions.

Table 7-5. Operation Modes

MODE	CONDITION	H-BRIDGE
Operating	nSLEEP pin = 1	Operating
Sleep mode	nSLEEP pin = 0	Disabled
Fault encountered	Any fault condition met	Disabled

Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV883x family of devices is device is used to drive one dc motor or other devices like solenoids. The following design procedure can be used to configure the DRV883x family of devices.

8.2 Typical Application

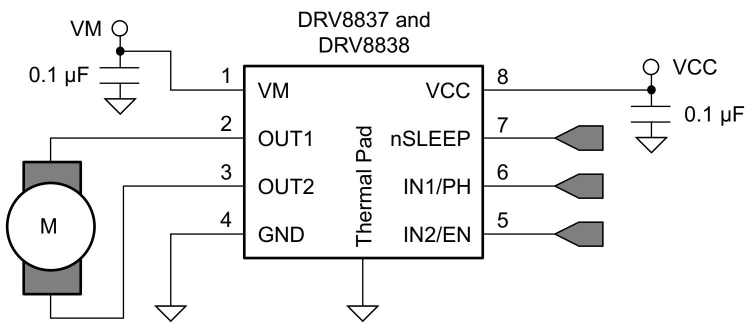


Figure 8-1. Schematic of DRV883x Application

8.2.1 Design Requirements

Table 8-1 lists the required parameters for a typical usage case.

Table 8-1. System Design Requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	VM	9 V
Logic supply voltage	VCC	3.3 V
Target rms current	I_{OUT}	0.8 A

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The appropriate motor voltage depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed dc motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.2.2 Low-Power Operation

When entering sleep mode, TI recommends setting all inputs as a logic low to minimize system power.

8.2.3 Application Curves

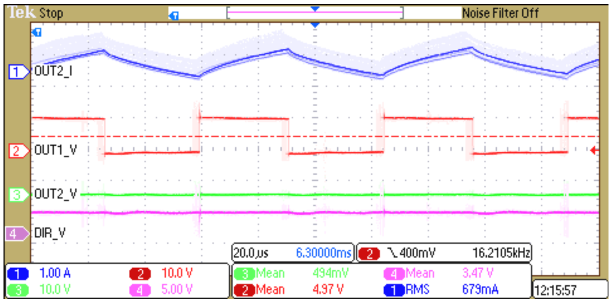


Figure 8-2. 50% Duty Cycle, Forward Direction

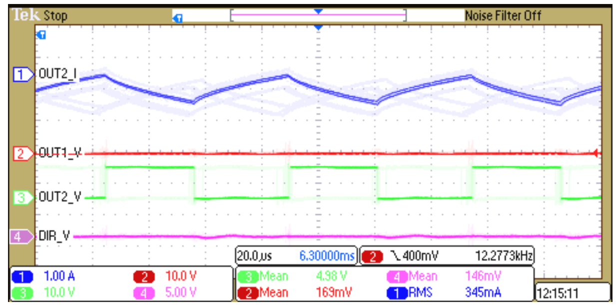


Figure 8-3. 50% Duty Cycle, Reverse Direction

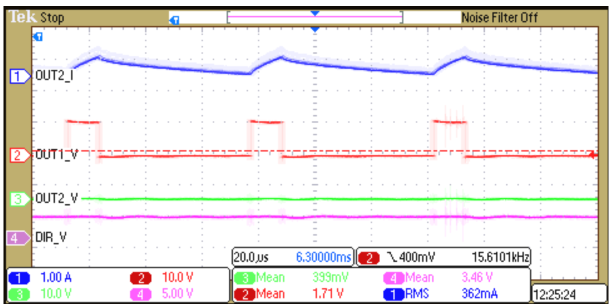


Figure 8-4. 20% Duty Cycle, Forward Direction

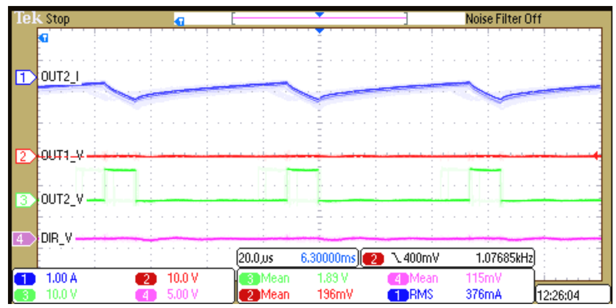


Figure 8-5. 20% Duty Cycle, Reverse Direction

Note

DIR_V is an indication of the motor direction. It is not a pin of the DRV883x device.

8 Power Supply Recommendations

8.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor-drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power-supply capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless dc, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate size of bulk capacitor.

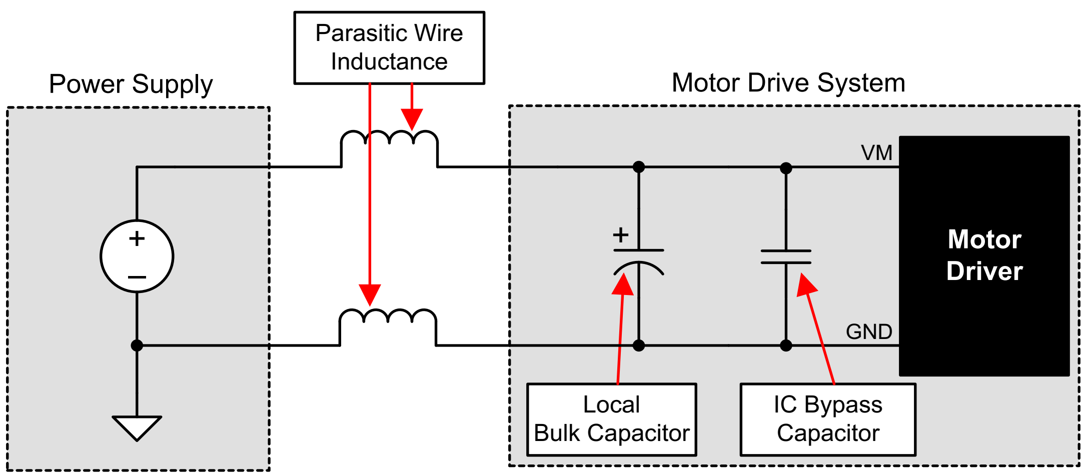


Figure 8-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply

9 Layout

9.1 Layout Guidelines

The VM and VCC pins should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1 µF rated for VM and VCC . These capacitors should be placed as close to the VM and VCC pins as possible with a thick trace or ground plane connection to the device GND pin.

9.2 Layout Example

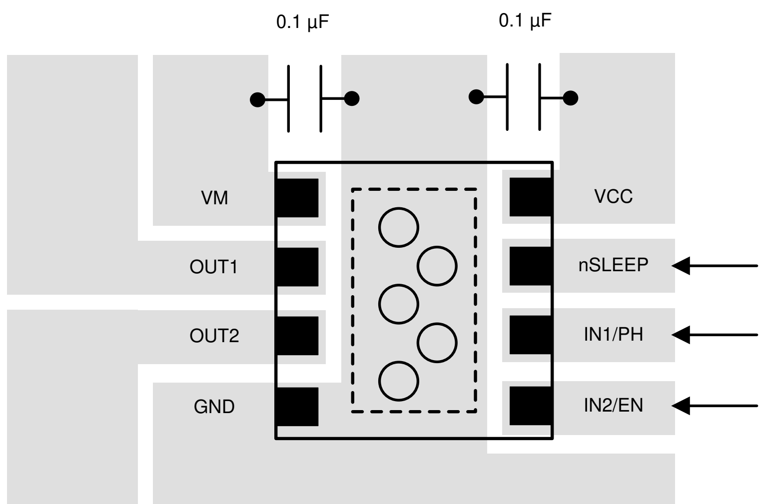


Figure 9-1. Simplified Layout Example

9.3 Power Dissipation

Power dissipation in the DRV883x family of devices is dominated by the power dissipated in the output FET resistance, or $r_{DS(on)}$. Use Equation 1 to estimate the average power dissipation when running a stepper motor.

$$P_{TOT} = r_{DS(on)} \times (I_{OUT(RMS)})^2 \quad (1)$$

where

- P_{TOT} is the total power dissipation
- $r_{DS(on)}$ is the resistance of the HS plus LS FETs
- $I_{OUT(RMS)}$ is the rms or dc output current being supplied to the load

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note

The value of $r_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases.

The DRV883x family of devices has thermal shutdown protection. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- *Calculating Motor Driver Power Dissipation*
- *DRV8837EVM User's Guide*
- *DRV8838EVM User's Guide*
- *Independent Half-Bridge Drive with DRV8837*
- *Understanding Motor Driver Current Ratings*

10.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DRV8837	Click here	Click here	Click here	Click here	Click here
DRV8838	Click here	Click here	Click here	Click here	Click here

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Community Resources

10.5 Trademarks

All trademarks are the property of their respective owners.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8837DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	837	Samples
DRV8837DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	837	Samples
DRV8838DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	838	Samples
DRV8838DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	838	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

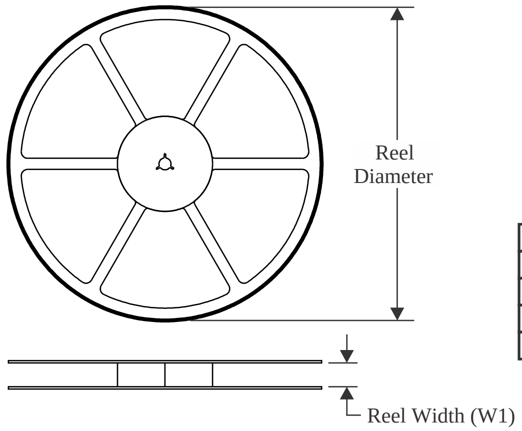
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

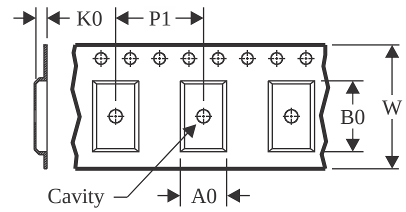
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

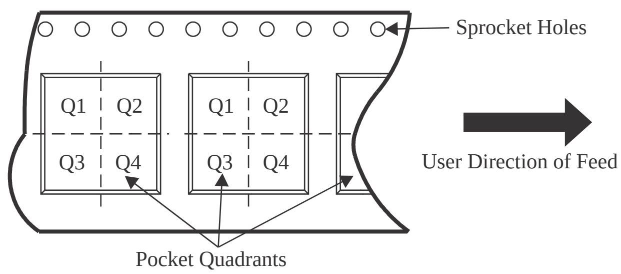


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

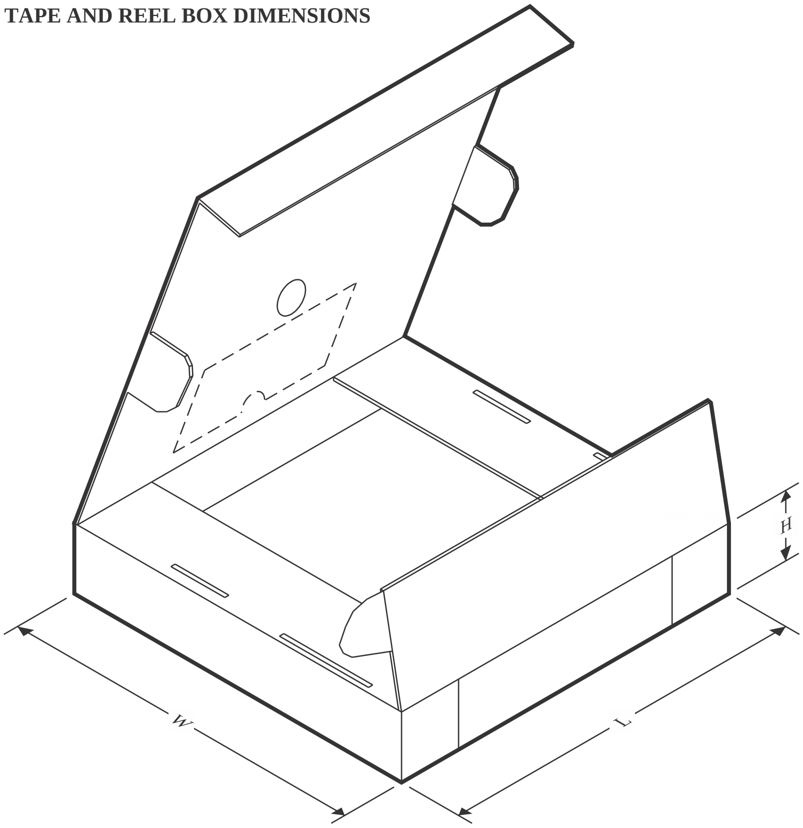
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8837DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8837DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8838DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
DRV8838DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

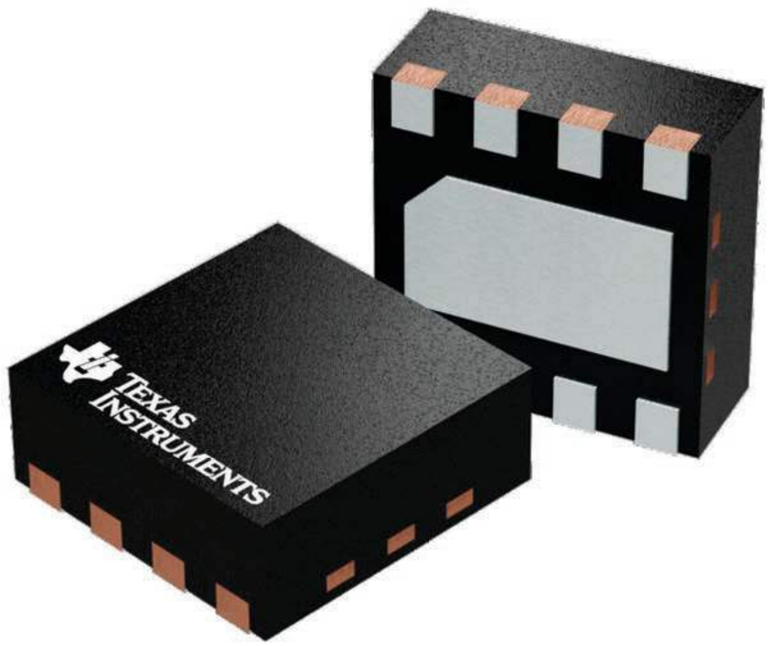
TAPE AND REEL BOX DIMENSIONS

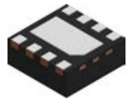


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8837DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
DRV8837DSGT	WSON	DSG	8	250	182.0	182.0	20.0
DRV8838DSGR	WSON	DSG	8	3000	182.0	182.0	20.0
DRV8838DSGT	WSON	DSG	8	250	182.0	182.0	20.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

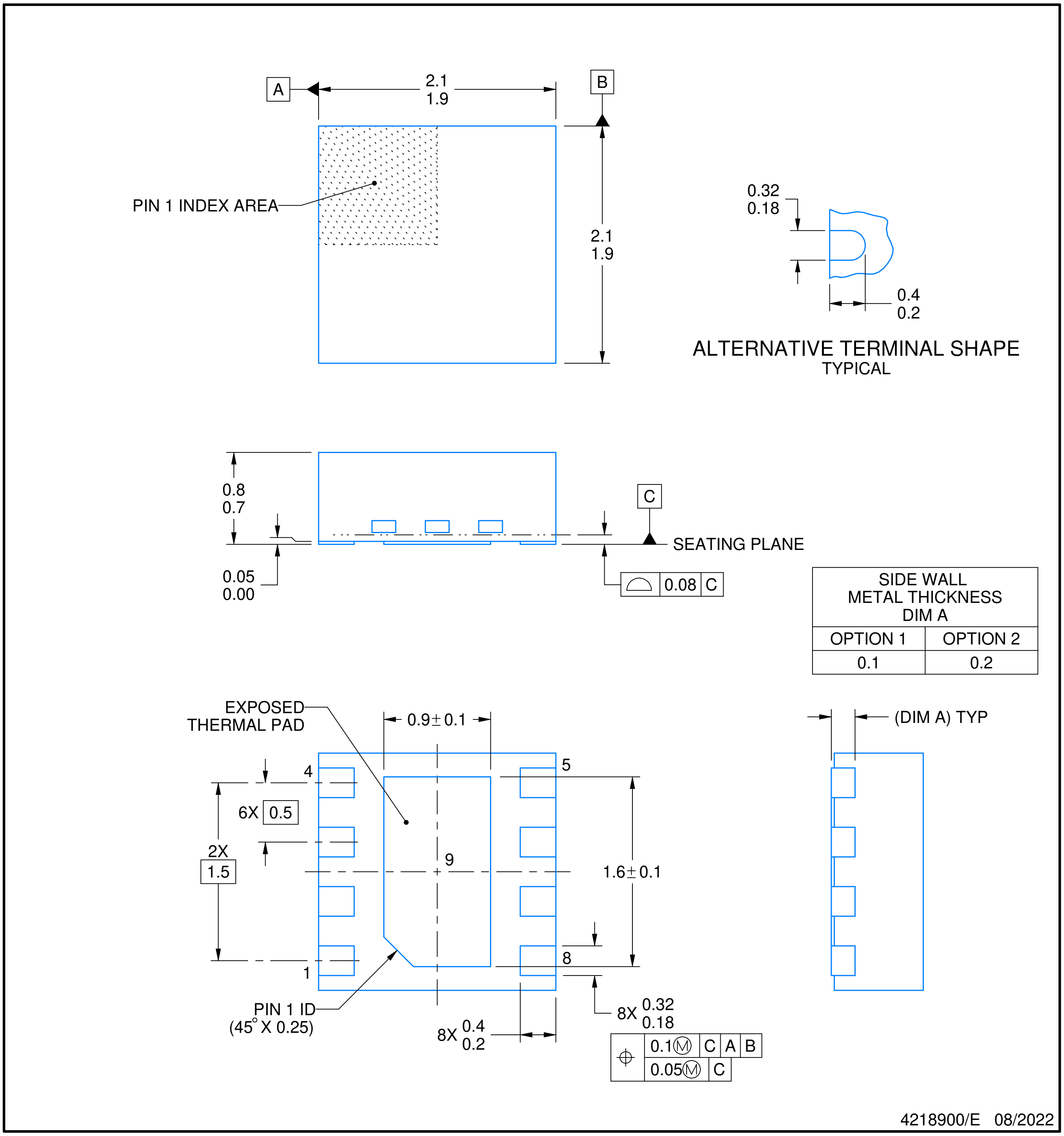




PACKAGE OUTLINE

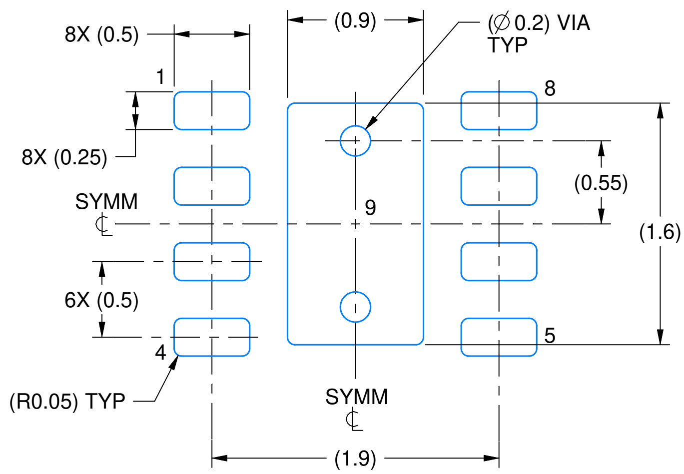
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

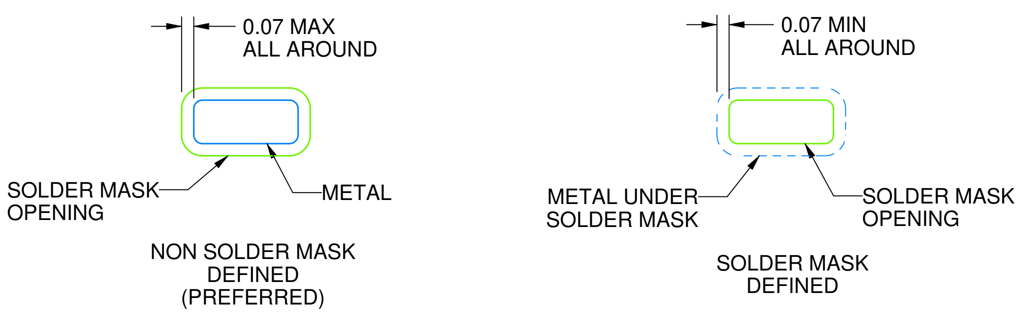


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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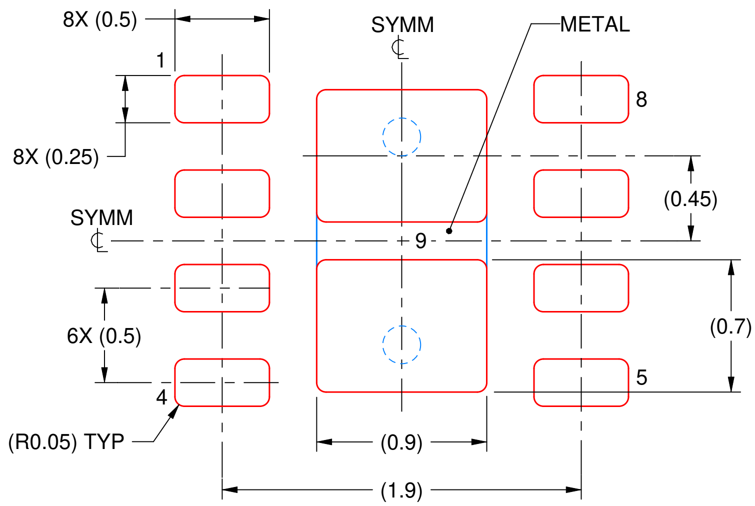
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.