MP2303

3A, 28V, 340KHz Synchronous Rectified Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2303 is a monolithic synchronous buck regulator. The device integrates power MOSFETS that provide 3A continuous load current over a wide operating input voltage of 4.75V to 28V. Current mode control provides fast transient response and cycle-by-cycle current limit.

An adjustable soft-start prevents inrush current at turn-on. In shutdown mode, the supply current drops to 1μA.

This device, available in 8-pin SOIC and 3x3 10-pin QFN packages, provides a very compact system solution with minimal reliance on external components.

EVALUATION BOARD REFERENCE

Board Number	Dimensions
EV2303DN-00A	2.0"X x 1.5"Y x 0.5"Z

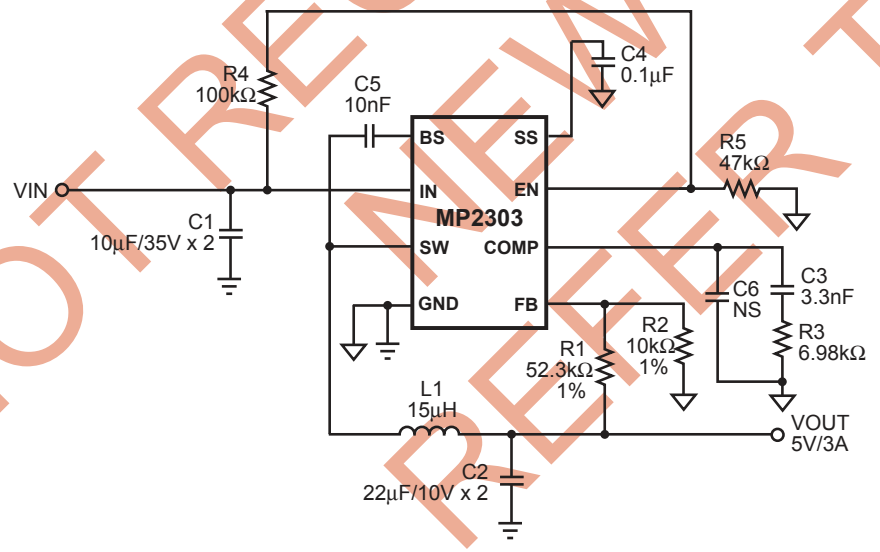
FEATURES

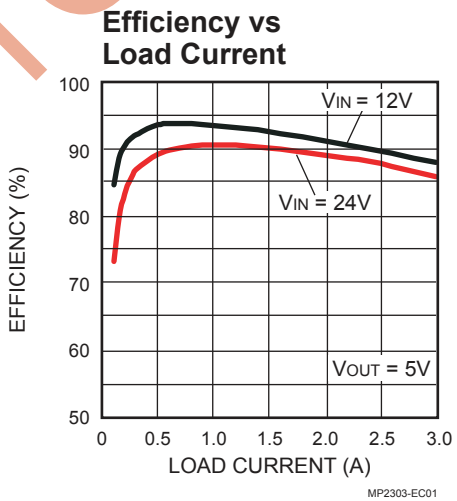
- 3A Output Current
- Wide 4.75V to 28V Operating Input Range
- Integrated Power MOSFET Switches
- Output Adjustable from 0.8V to 25V
- Up to 95% Efficiency
- Programmable Soft-Start
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 340KHz Frequency
- Cycle-by-Cycle Over Current Protection
- Input Under Voltage Lockout
- Thermally Enhanced 8-Pin SOIC and 3x3 QFN10 Packages

APPLICATIONS

- Distributed Power Systems
- Pre-Regulator for Linear Regulators
- Notebook Computers

TYPICAL APPLICATION



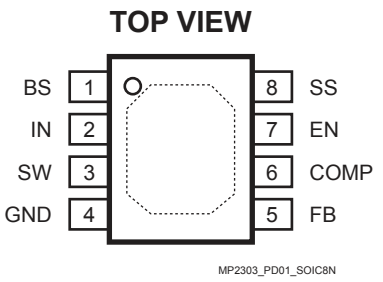


ORDERING INFORMATION

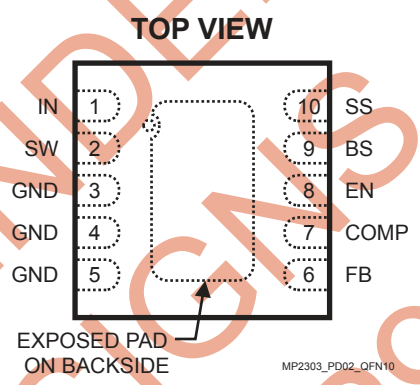
Part Number	Package	Top Marking	Temperature
MP2303DN*	SOIC8E (Exposed Pad)	MP2303DN	–40°C to +85°C
MP2303DQ**	QFN10 (3mm x 3mm)	K2	MP2303DQ

* For Tape & Reel, add suffix –Z (e.g. MP2303DN–Z);
For RoHS compliant packaging, add suffix –LF (e.g. MP2303DN–LF–Z)
** For Tape & Reel, add suffix –Z (e.g. MP2303DQ–Z);
For RoHS compliant packaging, add suffix –LF (e.g. MP2303DQ–LF–Z)

PACKAGE REFERENCE



SOIC8E (Exposed Pad)



QFN10 (3mm x 3mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} ..... –0.3V to +30V
Switch Voltage V_{SW} 31V
Boost Voltage V_{BS} ..... V_{SW} – 0.3V to V_{SW} + 6V
All Other Pins ..... –0.3V to +6V
Junction Temperature ..... 150°C
Continuous Power Dissipation (T_A = +25°C)(2)
SOIC8E 2.5W
QFN10 (3mmx3mm) 2.5W
Lead Temperature ..... 260°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions (3)

Input Voltage V_{IN} ..... 4.75V to 28V
Output Voltage V_{OUT} ..... 0.8V to 25V
Ambient Operating Temperature ... –40°C to +85°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
SOIC8E	50	10 °C/W
3x3 QFN10	50	12 °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS (5)

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ (5)	Max	Units
Shutdown Supply Current		V_{EN} = 0V		0.3	3.0	μA
Supply Current		V_{EN} = 2.7V, V_{FB} = 1.0V		1.3	1.5	mA
Feedback Voltage	V_{FB}	4.75V ≤ V_{IN} ≤ 28V, T_A = +25°C	0.780	0.800	0.820	V
		–40°C ≤ T_A ≤ +85°C	0.772		0.828	V
OVP Threshold Voltage			0.90	0.95	1.00	V
Error Amplifier Voltage Gain	A_{EA}			400		V/V
Error Amplifier Transconductance	G_{EA}	ΔI_C = ±10μA	550	820	1100	μA/V
High-Side Switch-On Resistance	$R_{DS(ON)1}$			125		mΩ
Low-Side Switch-On Resistance	$R_{DS(ON)2}$			125		mΩ
High-Side Switch Leakage Current		V_{EN} = 0V, V_{SW} = 0V		0	10	μA
Upper-Switch Current Limit			4.3	6.3	8.3(5)	A
Lower-Switch Current Limit		From Drain to Source		1.25		A
COMP to Current Sense Transconductance	G_{CS}			9		A/V
Oscillation Frequency	F_{osc1}	T_A = +25°C	300	340	380	KHz
		–40°C ≤ T_A ≤ +85°C	270		400	KHz
Short Circuit Oscillation Frequency	F_{osc2}	V_{FB} = 0V		110		KHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.7V		90		%
Minimum On-Time				220		ns
EN Shutdown Threshold Voltage		V_{EN} Rising	1.1	1.5	2.0	V
EN Shutdown Threshold Voltage Hysteresis				220		mV
EN Lockout Threshold Voltage			2.2	2.5	2.7	V
		–40°C ≤ T_A ≤ +85°C	2.1		2.8	V
EN Lockout Hysteresis				210		mV
Input Under Voltage Lockout Threshold	UVLO	V_{IN} rising, T_A = +25°C	3.8	4.05	4.30	V
		–40°C ≤ T_A ≤ +85°C	3.5		4.70	V
Input Under Voltage Lockout Threshold Hysterisis				210		mV
Soft-Start Current		V_{SS} = 0V		6		μA
Thermal Shutdown				160		°C

Note:

5) 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

6) Guaranteed by design

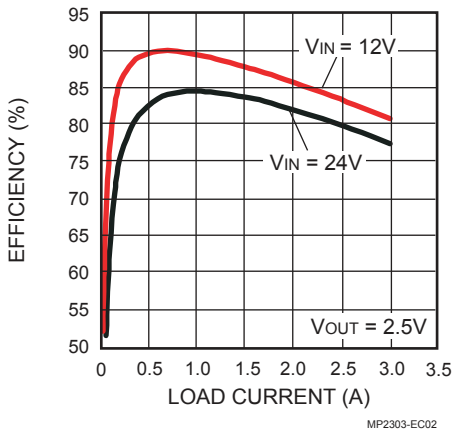
PIN FUNCTIONS

SOIC8N Pin #	3x3 QFN10 Pin #	Name	Description
1	9	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 0.01μF or greater capacitor from SW to BS to power the high side switch.
2	1	IN	Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.75V to 28V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See *Input Capacitor.*
3	2	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.
4	3, 4, 5	GND	Ground. SOIC8: Connect the exposed pad to pin 4. 3x3 QFN10: Connect to pins 3, 4 and 5 and ensure that said pins are tied together.
5	6	FB	Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback reference voltage is 0.8V. See *Setting the Output Voltage.*
6	7	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required. See *Compensation Components.*
7	8	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN higher than 2.7V to turn on the regulator, drive it lower than 1.1V to turn it off. Pull up by a resistive voltage divider to the IN pin for automatic startup, a 47kΩ resistor from EN to Ground and a 100kΩ resistor from EN to V_{IN}.
8	10	SS	Soft-start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. See *Soft-Start Capacitor.*

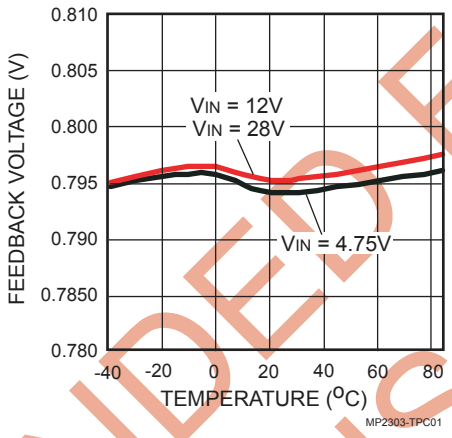
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_O = 3.3V, L = 10µH, C1 = 10µF, C2 = 22µF x 2, T_A = +25°C, unless otherwise noted.

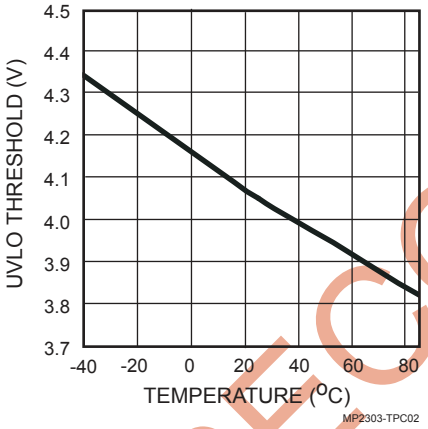
Efficiency vs Load Current



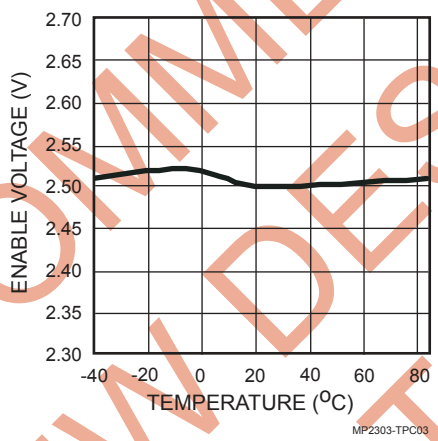
Feeback Voltage vs. Temperature



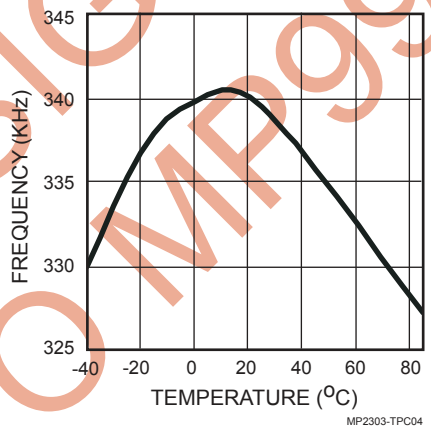
UVLO Rising vs. Temperature



Enable Lockout Threshold vs. Temperature



Oscillator Frequency

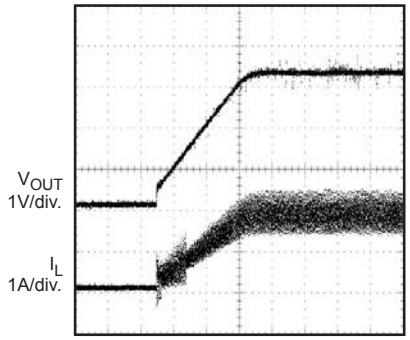


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_O = 3.3V, L = 10µH, C1 = 10µF, C2 = 22µF x 2, T_A = +25°C, unless otherwise noted.

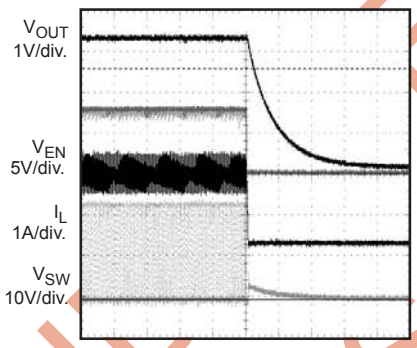
Power Up

V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 2A, C_{SS} = 0.1µF



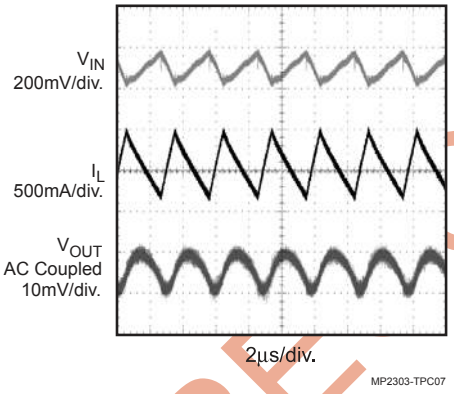
Power Off through Enable

V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 2A



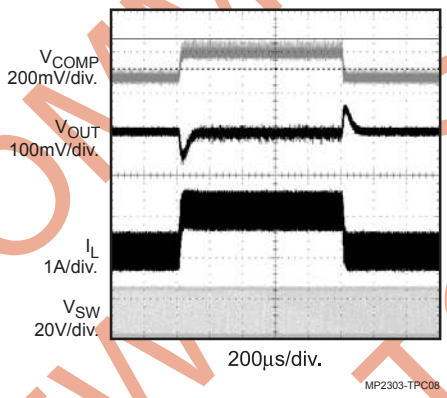
Steady State Test

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1A



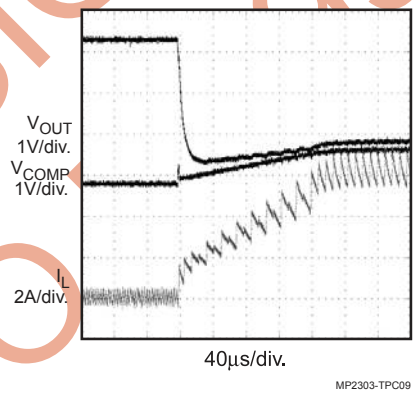
Load Transient Test

V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 0A-1A step with C_{FF} = 470pF



Short Circuit Protection

V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 0A



OPERATION

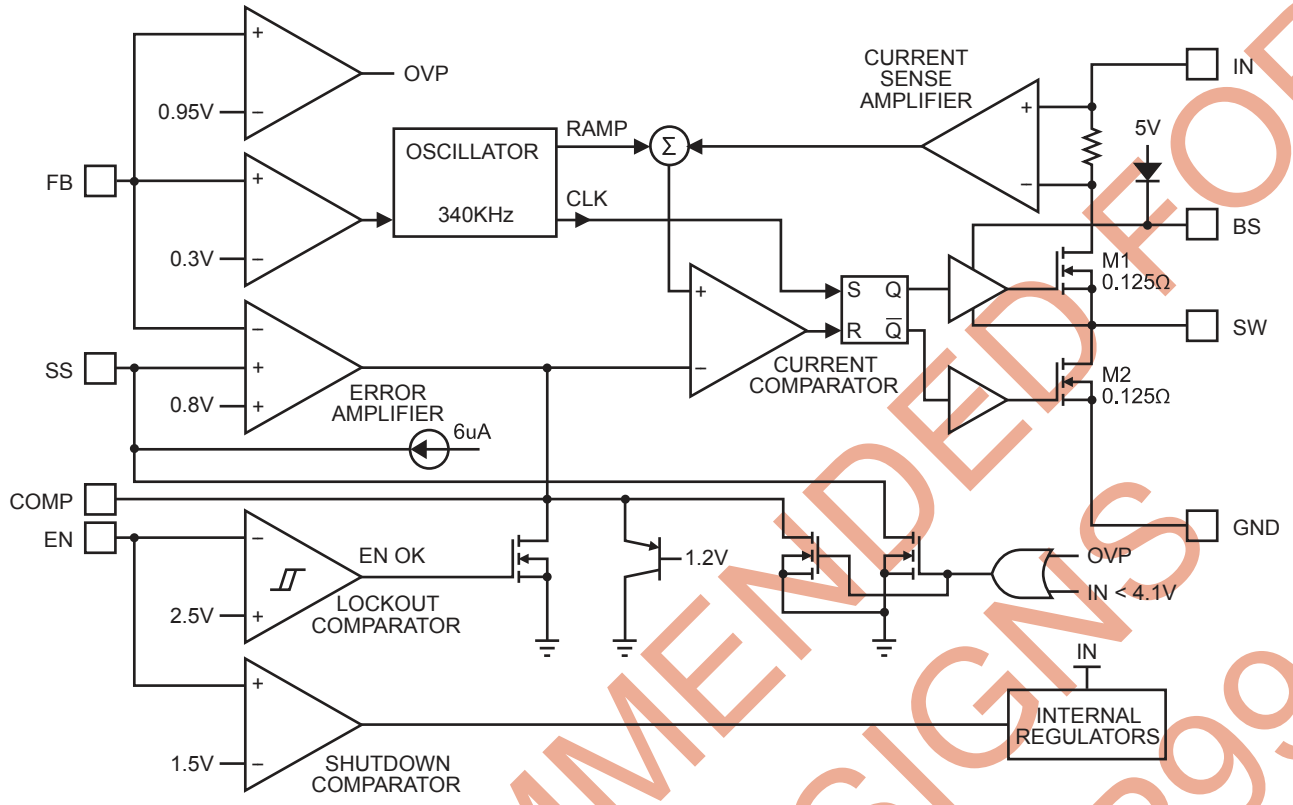


Figure 1—Functional Block Diagram

The MP2303 is a synchronous rectified, current-mode, step-down regulator. It regulates input voltages from 4.75V to 28V down to an output voltage as low as 0.8V, and supplies up to 3A of load current.

The MP2303 uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal transconductance error amplifier. The voltage at COMP pin is compared to the switch current measured internally to control the output voltage.

The converter uses internal N-Channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high-side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS is needed to drive the high-side gate. The boost capacitor is charged from the internal 5V rail when SW is low.

When the MP2303 FB pin exceeds 20% of the nominal regulation voltage of 0.8V, the over voltage comparator is tripped; the COMP pin and the SS pin are discharged to GND, forcing the high-side switch off.

APPLICATIONS INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R2}{R1+R2}$$

Thus the output voltage is:

$$V_{OUT} = 0.8 \times \frac{R1+R2}{R2}$$

Where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

A typical value for R2 can be as high as 100kΩ, but a typical value is 10kΩ. Using that value, R1 is determined by:

$$R1 = 12.5 \times (V_{OUT} - 0.8)(k\Omega)$$

For example, for a 3.3V output voltage, R2 is 10kΩ, and R1 is 31.3kΩ.

Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \times \Delta I} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where V_{IN} is the input voltage, f_S is the 340KHz switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where I_{LOAD} is the load current.

Optional Schottky Diode

During the transition between high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode may be paralleled between the SW pin and GND pin to improve overall efficiency. Table 2 lists example Schottky diodes and their Manufacturers.

Table 2—Diode Selection Guide

Part Number	Voltage/Current Rating	Vendor
B130	30V, 1A	Diodes, Inc.
SK13	30V, 1A	Diodes, Inc.
MBRS130	30V, 1A	International Rectifier

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where C2 is the output capacitance value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP2303 can be optimized for a wide range of capacitance and ESR values.

Compensation Components

MP2303 employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP pin is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system.

The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{VEA} \times \frac{V_{FB}}{V_{OUT}}$$

Where A_{VEA} is the error amplifier voltage gain, 400V/V; G_{CS} is the current sense transconductance, 9.0A/V; R_{LOAD} is the load resistor value.

The system has 2 poles of importance. One is due to the compensation capacitor (C3) and the output resistor of error amplifier, and the other is due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}}$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}}$$

Where, G_{EA} is the error amplifier transconductance, 820μA/V, and R_{LOAD} is the load resistor value.

The system has one zero of importance, due to the compensation capacitor (C3) and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}}$$

In this case, a third pole set by the optional compensation capacitor (C6) and the compensation resistor (R3) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = \frac{1}{2\pi \times C6 \times R3}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important.

Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system instability. A good rule of thumb is to set the crossover frequency to approximately one-tenth of the switching frequency. Switching frequency for the MP2303 is 340KHz, so the desired crossover frequency is 34KHz.

Table 3 lists the typical values of compensation components for some standard output voltages with various output capacitors and inductors. The values of the compensation components have been optimized for fast transient responses and good stability at given conditions.

Table 3—Compensation Values for Typical Output Voltage/Capacitor Combinations

V_{OUT}	L	C2	R3	C3	C6
1.8V	4.7µH	100µF Ceramic	6.6kΩ	3.3nF	None
2.5V	4.7µH - 6.8µH	47µF Ceramic	4.7kΩ	5.6nF	None
3.3V	6.8µH - 10µH	22µFx2 Ceramic	5.6kΩ	4.7nF	None
5V	10µH - 15µH	22µFx2 Ceramic	8.2kΩ	4.7nF	None
12V	15µH - 22µH	22µFx2 Ceramic	20kΩ	2.2nF	None
2.5V	4.7µH - 6.8µH	560µF Al. 30mΩ ESR	56kΩ	2.2nF	300pF
3.3V	6.8µH - 10µH	560µF Al. 30mΩ ESR	68kΩ	2.2nF	200pF
5V	10µH - 15µH	470µF Al. 30mΩ ESR	91kΩ	2.2nF	50pF
12V	15µH - 22µH	220µF Al. 30mΩ ESR	100kΩ	2.2nF	None

To optimize the compensation components for conditions not listed in Table 2, the following procedure can be used.

1. Choose the compensation resistor (R3) to set the desired crossover frequency. Determine the R3 value by the following equation:

$$R3 = \frac{2\pi \times C2 \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

Where f_C is the desired crossover frequency, 34KHz.

2. Choose the compensation capacitor (C3) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero, f_{Z1}, below one forth of the crossover frequency provides sufficient phase margin. Determine the C3 value by the following equation:

$$C3 > \frac{4}{2\pi \times R3 \times f_C}$$

3. Determine if the second compensation capacitor (C6) is required. It is required if the ESR zero of the output capacitor is located at less than half of the 340KHz switching frequency, or the following relationship is valid:

$$\frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_S}{2}$$

If this is the case, then add the optional compensation capacitor (C6) to set the pole f_{P3} at the location of the ESR zero. Determine the C6 value by the equation:

$$C6 = \frac{C2 \times R_{ESR}}{R3}$$

Soft-Start Capacitor

To reduce input inrush current during startup, a programmable soft-start is provided by connecting a capacitor (C4) from pin SS to GND. The soft-start time is given by:

$$t_{SS} = C4 \times \frac{0.8V}{6\mu A}$$

To reduce the susceptibility to noise, do not leave SS pin open. Use a capacitor with small value if you do not need soft-start function.

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, and it will be a must if the applicable condition is:

- V_{OUT} is 5V or 3.3V, and duty cycle is high:

  $D = \frac{V_{OUT}}{V_{IN}} > 65\%$

In these cases, an external BST diode is recommended from the output of the voltage regulator to BST pin, as shown in Figure.2

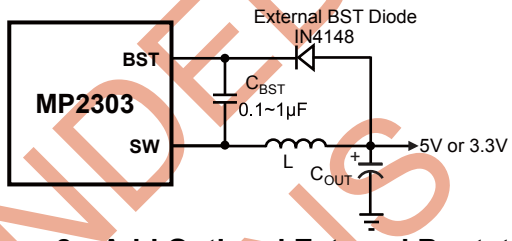


Figure 2—Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST cap is 0.1~1μF.

TYPICAL APPLICATION CIRCUITS

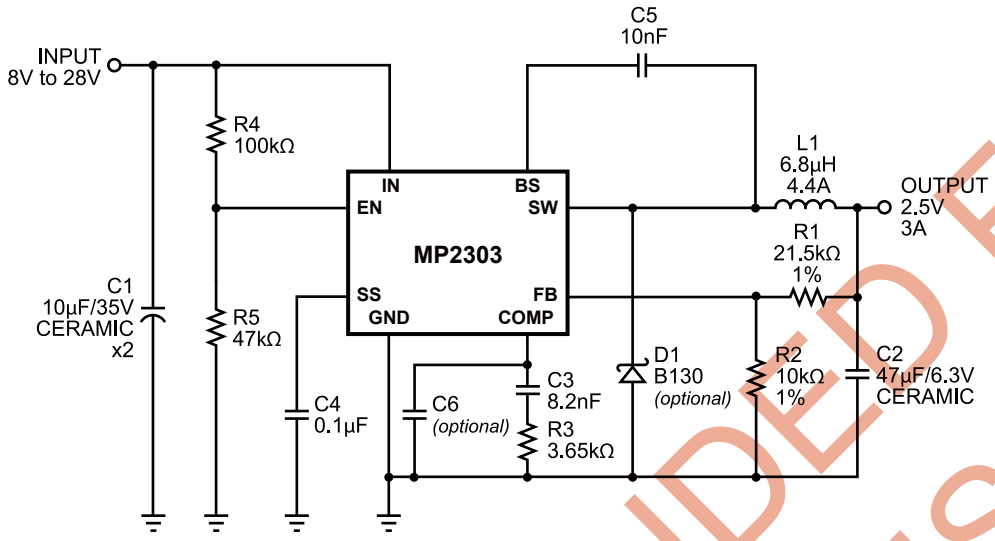


Figure 3—MP2303 with 2.5V Output, 47µF/6.3V Ceramic Output Capacitor

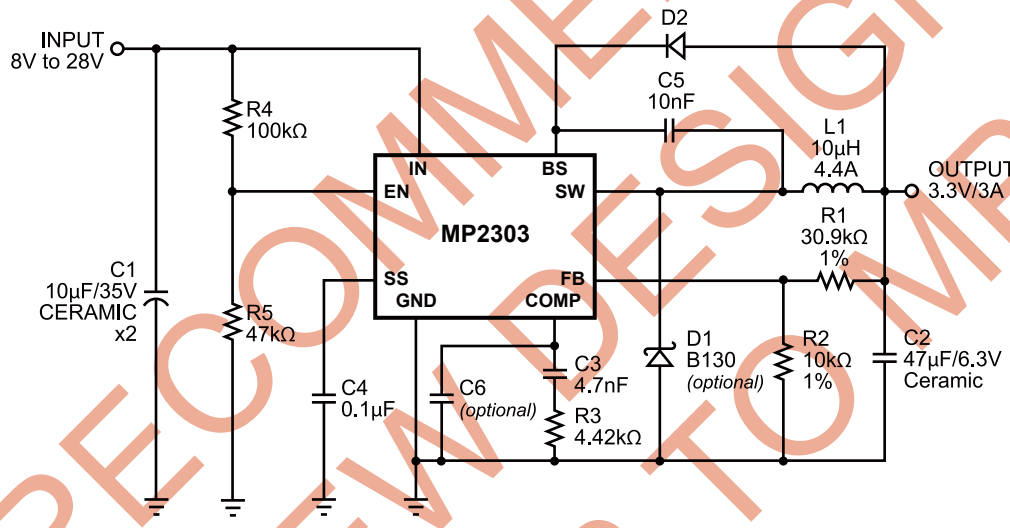


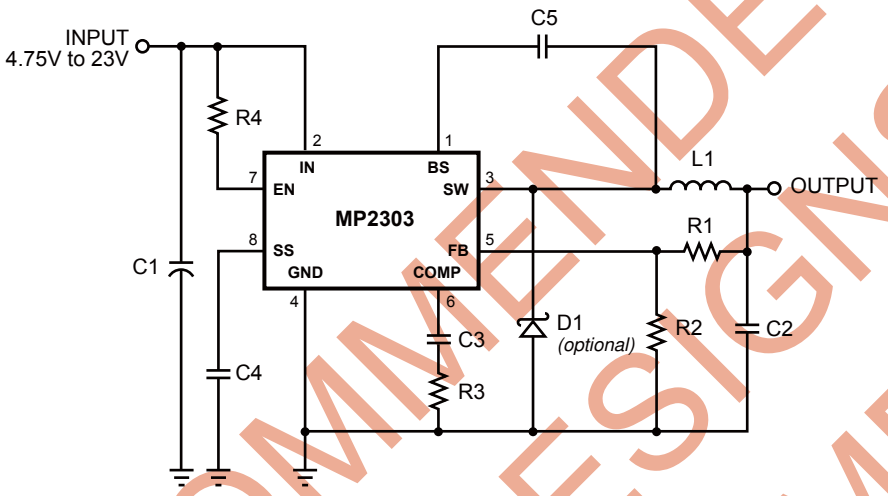
Figure 4—MP2303 with 3.3V Output, 47µF/6.3V Ceramic Output Capacitor

PCB LAYOUT GUIDE

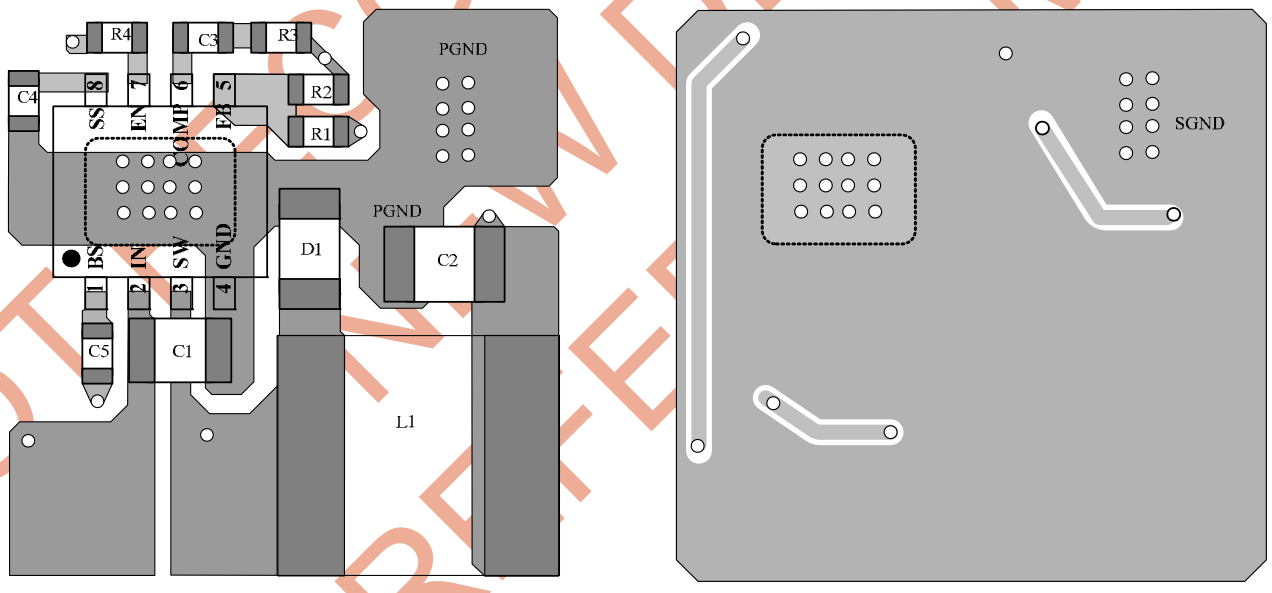
PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance.

If change is necessary, please follow these guidelines and take Figure 5 for reference.

1) Keep the path of switching current short and minimize the loop area formed by Input cap, high-side MOSFET and low-side MOSFET.
2) Bypass ceramic capacitors are suggested to be put close to the V_{IN} Pin.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Route SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



MP2303 Typical Application Circuit

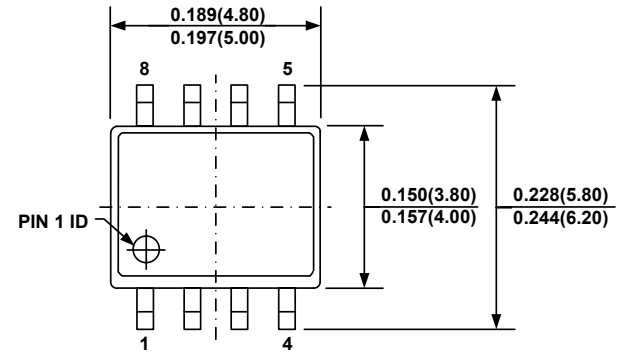


TOP Layer **Bottom Layer**

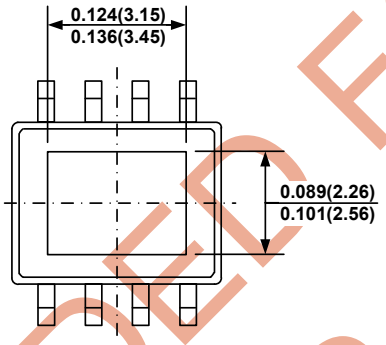
Figure 5—MP2303 Typical Application Circuit and PCB Layout Guide

PACKAGE INFORMATION

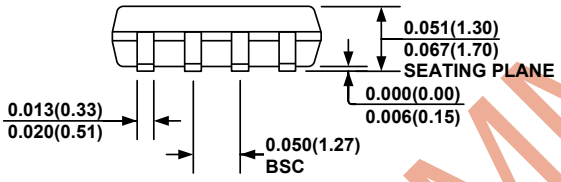
SOIC8E (EXPOSED PAD)



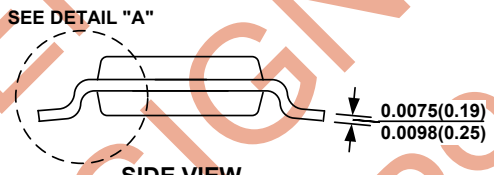
TOP VIEW



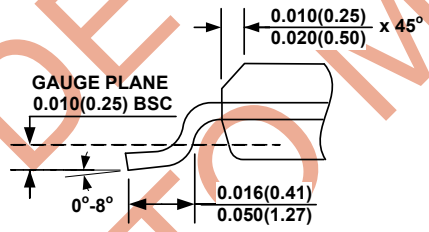
BOTTOM VIEW



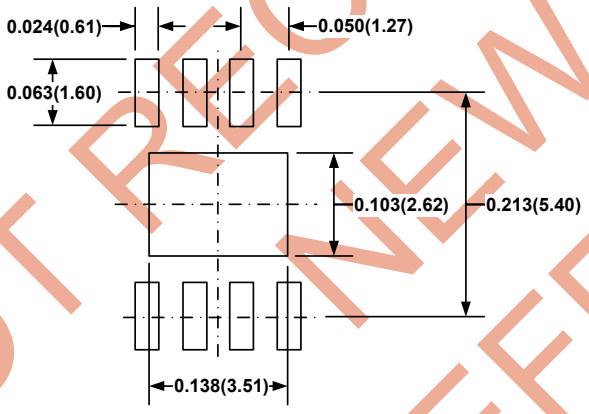
FRONT VIEW



SIDE VIEW



DETAIL "A"

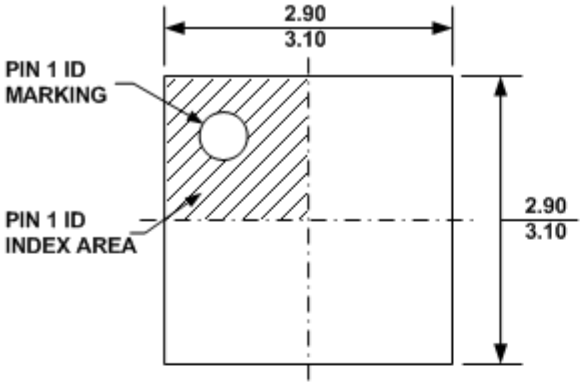


RECOMMENDED LAND PATTERN

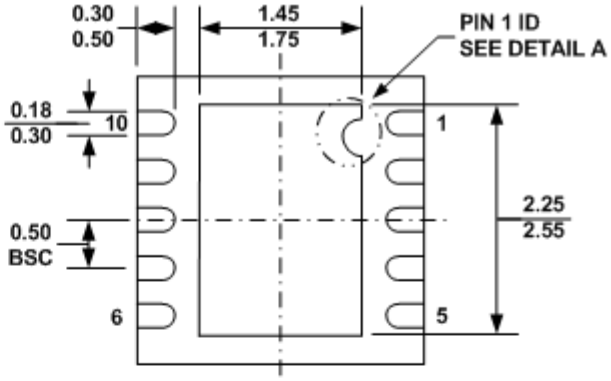
NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

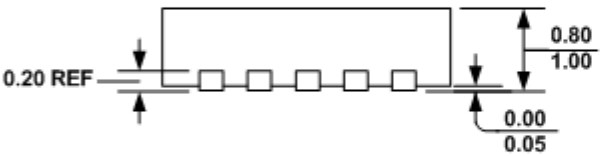
QFN10 (3mm x 3mm)



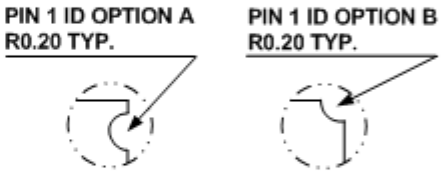
TOP VIEW



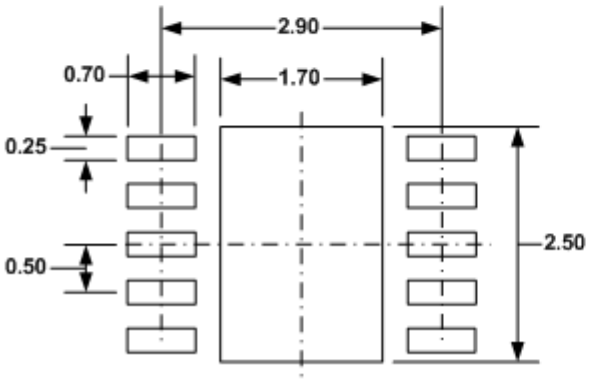
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.