TCA5013 Feature Rich Smartcard Interface IC with 1 User Card and 3 SAM Card Support

1 Features

- Operating supply voltage range of 2.7 V to 5.5 V
- Supports EMV 4.3, ISO7816-3 and ISO7816-10 standards
- Supports 1 user card and 3 secure access module cards
- IEC61000-4-2 8-kV Contact discharge esd protection on all smartcard interface pins
- Low power mode for power saving when inactive (shutdown mode)
- Automatic card deactivation in the event of short circuit, card pull out, over temperature or power supply fault
- Integrated DC-DC boost to generate V_{CC} for 5 V and 3 V on all card interfaces
- Automatic card clock generation for synchronous card activation
- 4-byte FIFO for storing ATR from ISO7816-10 Type 1 cards
- Programmable rise/fall time control for IO and clock lines of all smartcards
- Input clock frequency up to 26 MHz
- Tamper proof package design

2 Applications

- High-end point of sale (POS) terminals
- Multi secure accesscard capable EPOS systems

3 Description

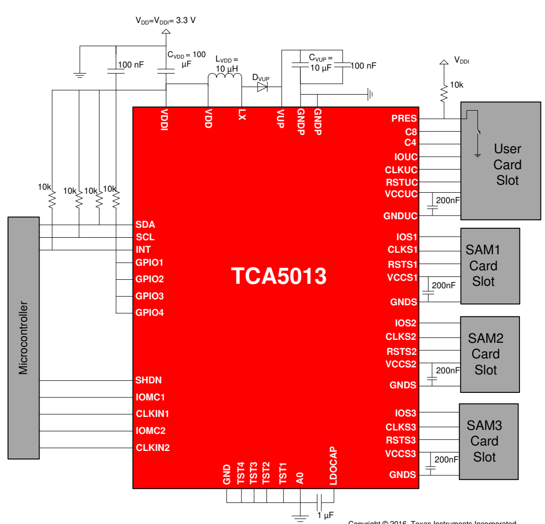
TCA5013 is a smartcard interface IC that is targeted for use in Point of Sale (POS) terminals. The device enables POS terminals to interface with EMV4.3, ISO7816-3 and ISO7816-10 compliant cards. It supports up to 3 Secure Access Module (SAM) cards in addition to 1 user card. It operates from a single supply and generates all the card voltages. The device is controlled by a standard I^2C interface and is capable of card activation and deactivation per EMV4.3 and ISO7816-3 standards. In addition it also supports ISO7816-10 synchronous cards. It has a 4-byte FIFO that stores the ATR (Answer to Reset) sequence in ISO7816-10 type 1 cards. Synchronous cards (ISO7816-10 type 1 and type 2) can be set up for automatic activation or manual activation. The device has multiple power saving modes and also supports power saving in the smartcard itself by "clock stop" or lowering clock frequency to lowest allowable levels per the ISO7816 - 3 standard. TCA5013 has IEC 61000-4-2 8kV contact discharge on all pins that interface with smartcards. This enables the system to be resistant to ESD in the field without the need for external ESD devices. It is available in an 5 mm x 5 mm BGA package. The pin out of the device is such that all the IO pins are securely surrounded by other pins. This prevents the secure pins from being probed during device operation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCA5013	NFBGA (48)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

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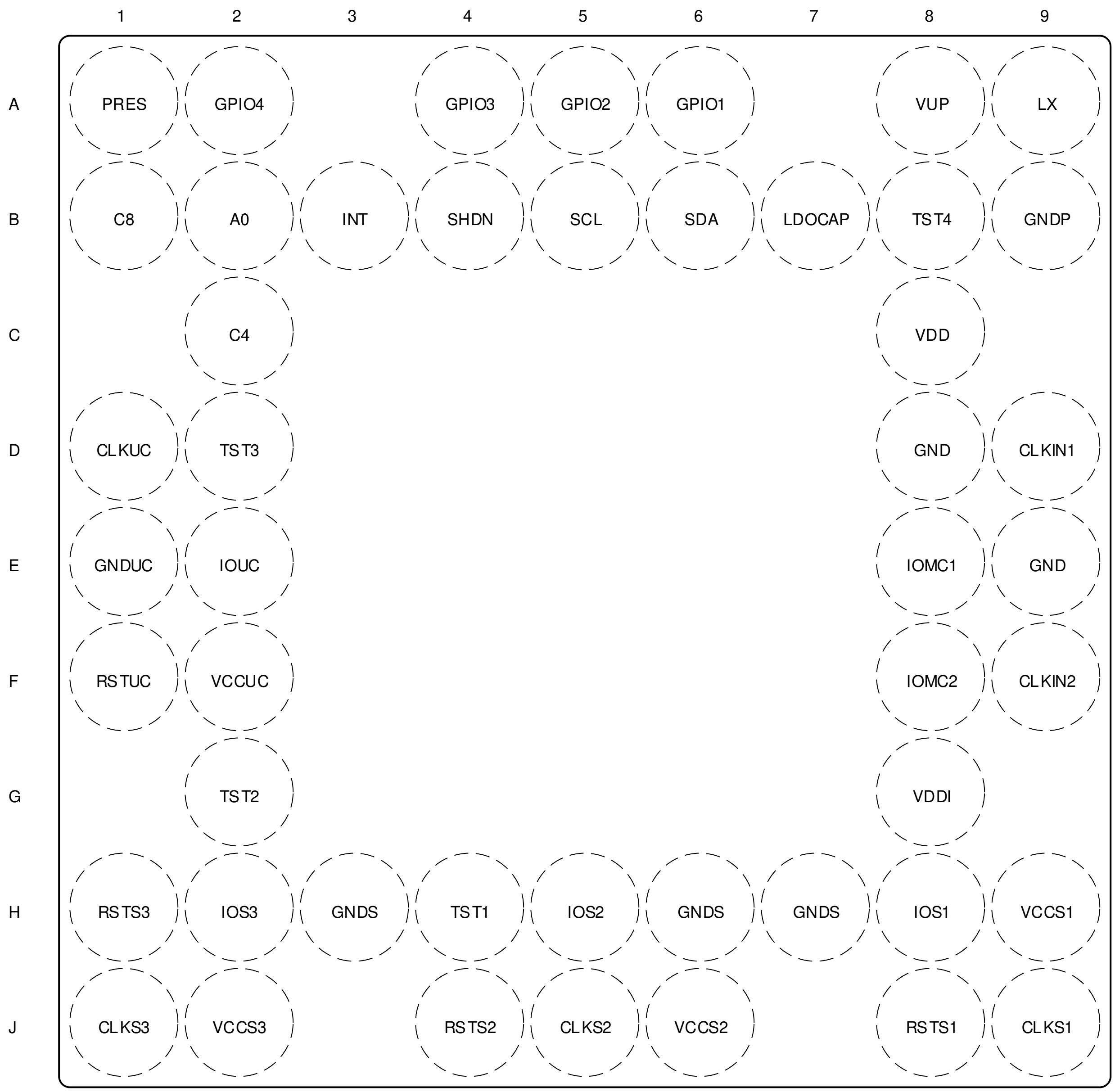
• Changed the Pin Configuration view	3
• Added: (Cold reset sequence) to Figure 6	22

Changes from Revision A (July 2014) to Revision B	Page
• Changed the datasheet title to "TCA5013 Feature Rich Smartcard Interface IC with 1 User Card and 3 SAM Card Support"	1
• Added the Features: Tamper proof package design	1
• Changed the Applications	1
• Full Version release of document	1

Changes from Original (July 2014) to Revision A	Page
• Full version release of document.	1

5 Pin Configuration and Functions

ZAH Package
NFBGA 48-Pins
Bottom View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	PRES	INPUT	User card presence detection
A2	GPIO4	I/O	General purpose IO (5-V tolerant)
A4	GPIO3	I/O	General purpose IO (5-V tolerant)
A5	GPIO2	I/O	General purpose IO (5-V tolerant)
A6	GPIO1	I/O	General purpose IO (5-V tolerant)
A8	VUP	PWR	Boost output terminal
A9	LX	PWR	Boost inductor input terminal
B1	C8	I/O	User card auxiliary IO (Open Drain)
B2	A0	INPUT	I^2C address selection pin. Connect to VDDI, GND.
B3	INT	OUTPUT	Interrupt output (open drain)
B4	SHDN	INPUT	Shutdown and reset pin
B5	SCL	INPUT	I^2C clock input
B6	SDA	I/O	I^2C data
B7	LDOCAP	PWR	Internal LDO output. Connect to 1 µf decoupling capacitor.
B8	TST4	NA	Test pin. Grounded in application.
B9	GNDP	PWR	Power ground
C2	C4	I/O	User card auxiliary IO (Open drain)
C8	VDD	PWR	Device main power supply
D1	CLKUC	OUTPUT	User card clock
D2	TST3	NA	Test pin. Grounded in application.
D8	GND	PWR	Device ground
D9	CLKIN1	INPUT	User card external clock input pin
E1	GNDUC	PWR	User card ground pin
E2	IOUC	I/O	User card IO pin
E8	IOMC1	I/O	User card microcontroller data IO
E9	GND	PWR	Device ground
F1	RSTUC	OUTPUT	User card reset output pin
F2	VCCUC	PWR	User card VCC pin
F8	IOMC2	I/O	SAM microcontroller data IO
F9	CLKIN2	INPUT	User card external clock input pin
G2	TST2	NA	Test pin. Grounded in application.
G8	VDDI	PWR	Microcontroller interface supply voltage.
H1	RSTS3	OUTPUT	Reset output for SAM3
H2	IOS3	I/O	IO pin for SAM3
H3	GNDS	PWR	Ground for all SAMs
H4	TST1	NA	Test pin. Grounded in application
H5	IOS2	I/O	IO pin for SAM2
H6	GNDS	PWR	Ground for all SAMs
H7	GNDS	PWR	Ground for all SAMs
H8	IOS1	I/O	IO pin for SAM1
H9	VCCS1	PWR	VCC for SAM1
J1	CLKS3	OUTPUT	Clock output for SAM3
J2	VCCS3	PWR	VCC for SAM3
J4	RSTS2	OUTPUT	Reset output for SAM2
J5	CLKS2	OUTPUT	Clock output for SAM2
J6	VCCS2	PWR	VCC for SAM2
J8	RSTS1	OUTPUT	Reset output for SAM1
J9	CLKS1	OUTPUT	Clock output for SAM1

6 Specifications

6.1 Absolute Maximum Ratings[(1)(2)]

over operating free-air temperature range (unless otherwise noted)[(3)]

		MIN	MAX	UNIT
V_{DD}	Supply voltage range	–0.3	6	V
V_{DDI}	Interface voltage range	–0.3	4	V
V_I	Input voltage range on digital I/O pins referenced to V_{DDI}	-0.3	V_{DDI} + 0.3	V
	Input voltage range on digital I/O pins referenced to V_{CC}	-0.3	V_{CC} + 0.3	V
I_{OL}	Load current on GPIO pins	-15		mA
	Load current on INT and SDA pins	-6		mA

(1) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.
(3) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	–4	4	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	-1.5	1.5	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage range – DC-DC enabled	2.7	5.5	V
	Supply voltage Range – DC-DC disabled	5.25	5.5	V
V_{DDI}	Interface voltage range	1.65	3.6	V
$I_{CC(TOT)}$	Sum of the currents that can be drawn on all Card VCC pins		180	mA
T_A	Operating temperature range	–40	85	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		TCA5013 ZAH 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	96.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	
ψ_{JT}	Junction-to-top characterization parameter	1.9	
ψ_{JB}	Junction-to-board characterization parameter	58.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics—Power Supply and ESD

$V_{DD} = V_{DDI} = 3.3$ V; $L_{VDD} = 10$ µH; $C_{VDD} = 10$ µF; $C_{VUP} = 10$ µF; $T_A = –40°C$ to 85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DDTH}	VDD supervisor fault threshold	V_{DD} voltage below which SUPL fault is asserted	2.45		2.7	V
V_{DDSH}	VDD shutdown threshold	V_{DD} voltage below which device will shutdown			2.0	V
V_{DDITH}	VDDI shutdown threshold	V_{DDI} voltage below which device will shutdown	1.4		1.6	V
I_{DDSH}	VDD Shutdown current	Shutdown Mode at $T_{ambient}$ = 25 C		22	28	µA
I_{DDST}	VDD Standby current	Shutdown Mode at $T_{ambient}$ = 25°C		300	650	µA
I_{DDA}	Supply current	IOMC1 = IOMC2 = V_{DDI}; CLKIN1 = CLKIN2 = GND; $T_{ambient}$= 25°C Current consumption per card interface activated			2	mA
I_{DDA1} (1)	Supply current	$V_{CCUC} = V_{CCS1} = V_{CCS2} = V_{CCS3} = 5$ V; $f_{CLKIN1} = f_{CLKIN2} = f_{CLKUC} = f_{CLKS1} = 5$ MHz; $I_{CCUC} = I_{CCS1} = 55$ mA; $I_{CCS2} = I_{CCS3} = 2$ mA; $T_{ambient}$ = 25°C		235	280	mA
I_{DDISH}	VDD Interface shutdown current	Shutdown Mode at 25°C		3.5	5	µA
I_{DDIA}	VDD Interface supply current	All Card V_{CC} = 5 V; CLKIN1 = CLKIN2 = 5 MHz; @ 25°C; IOMC1 = IOMC2 = V_{DDI}		290	300	µA
t_{WAKE}	Device wakeup time	Time from SHDN > V_{IH} to INT < V_{OL}	0.1		10	ms
f_{OSC}	Internal Oscillator Frequency	Measured on CLKUC, CLKS1,CLKS2,CLKS3	1	1.2	1.4	MHz
f_{DC-DC}	DC-DC switching frequency			2.4		MHz
V_{DC-DC}	DC-DC output voltage	If any card V_{CC} is 5 V		5.5		V
		If all card V_{CC} is 3 V or 1.8 V		3.5		
$V_{ESD-IEC}$	IEC61000-4-2 level 4 ESD protection on pins defined in Table 1		-8		8	kV

(1) Values highly dependent on external components like boost inductor and external rectifier. The specification is based on 75% boost efficiency for max value and 85% efficiency for typical value

6.6 Electrical Characteristics—Card V_{CC}

$V_{DD} = V_{DDI} = 3.3$ V; $L_{VDD} = 10$ µH; $C_{VDD} = 10$ µF; $C_{VUP} = 10$ µF; $T_A = –40°C$ to 85°C unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Card supply voltage		V_{CC} = 5 V; $I_{CC} \le 65$ mA	4.75	5	5.25	V
			V_{CC} = 3 V; $I_{CC} \le 65$ mA	2.85	3	3.15	
			V_{CC} = 1.8 V; $I_{CC} \le 45$ mA	1.71	1.8	1.89	
$\Delta V_{CC}/\Delta I_{CC}$	Load transient response	Current pulses I < 100 mA, t < 400 ns	V_{CC} = 5 V ; 40 nA.s current spike	4.65		5.35	V
			V_{CC} = 3 V ; 17.5 nA.s current spike	2.76		3.24	V
			V_{CC} = 1.8 V ; 11.1 nA.s current spike	1.62		1.98	V
V_{RIPPLE}	Peak to peak ripple voltage		Measured on V_{CC} = 5 V, 3 V, 1.8 V			90	mV
I_{CC}	Card supply Current		V_{CC} = 5 V			65	mA
			V_{CC} = 3 V			65	
			V_{CC} = 1.8 V			45	
V_{DO}	Card LDO dropout voltage		I_{CC} = 65 mA			250	mV

6.7 Electrical Characteristics—Card RST

$V_{DD} = V_{DDI} = 3.3$ V; $L_{VDD} = 10$ µH; $C_{VDD} = 10$ µF; $C_{VUP} = 10$ µF; $T_A = –40°C$ to 85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL-RST}	Output Low voltage	I_{OL} = -200 µA			0.1 V_{CC}	V
V_{OH-RST}	Output high voltage	I_{OH} = 150 µA	0.9 V_{CC}			V
t_{R-RST}	Rise time	C_L = 30 pF ; 10% to 90%			0.1	µs
t_{F-RST}	Fall time	C_L = 30 pF ; 90% to 10%			0.1	µs

6.8 Electrical Characteristics—Card CLK

$V_{DD} = V_{DDI} = 3.3$ V; $L_{VDD} = 10$ µH; $C_{VDD} = 10$ µF; $C_{VUP} = 10$ µF; $T_A = –40°C$ to 85°C unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OL\text{ - }CLK}$	Output Low voltage	I_{OL} = -100 µA				0.1 V_{CC}	V
$V_{OH\text{ - }CLK}$	Output high voltage	I_{OH} = 100 µA		0.9 V_{CC}			V
$t_{R\text{ - }CLK}$/ $t_{F\text{ - }CLK}$	Rise/Fall time	C_L = 30 pF ; 10% to 90%;	CLK slew rate settings register = 0000b		7		ns
			CLK slew rate settings register = 0001b		9		
			CLK slew rate settings register = 0010b		11		
			CLK slew rate settings register = 0011b		13		
			CLK slew rate settings register = 0100b		13.5		
			CLK slew rate settings register = 0101b		14		
			CLK slew rate settings register = 0110b		15		
			CLK slew rate settings register = 0111b		16		
			CLK slew rate settings register = 1000b		17		
			CLK slew rate settings register = 1001b		18		
			CLK slew rate settings register = 1010b		19		
			CLK slew rate settings register = 1011b		20		
			CLK slew rate settings register = 1100b		21		
			CLK slew rate settings register = 1101b		22		
			CLK slew rate settings register = 1110b		23		
			CLK slew rate settings register = 1111b		25		
$CLK_{PU\text{-}PD\text{-}SKEW}$	Clock pull-up / pull-down skew	$t_{R\text{-}CLK} – t_{F\text{-}CLK}$ / $t_{F\text{-}CLK}$; C_L = 30 pF				10	%
f_{CLK}	Frequency on CLK pin	C_L = 30 pF				20	MHz
D	Clock duty cycle	Internal clock = 1.2 MHz; C_L = 30 pF		45		55	%

6.9 Electrical Characteristics—Card Interface IO, C4 and C8

$V_{DD} = V_{DDI} = 3.3$ V; $L_{VDD} = 10$ µH; $C_{VDD} = 10$ µF; $C_{VUP} = 10$ µF; $T_A = –40°C$ to 85°C unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OL\text{ - }C4,\ C8}$	Output Low Voltage	V_{CC} = 5 V	I_{OL} = -1 mA			0.5	V
$V_{OH\text{ - }C4,\ C8}$	Output Low Voltage	V_{CC} = 5 V, 3 V, 1.8 V	I_{OH} = 20 µA	0.9 V_{CC}			V
$V_{IL\text{ - }IO,\ C4,\ C8}$	Output Low Voltage					0.4 V_{CC}	V
$V_{IH\text{ - }IO,\ C4,\ C8}$	Output High Voltage			0.6 V_{CC}			V
$V_{OL\text{ - }IO,\ 5\ V}$	Output Low Voltage	V_{CC} = 5 V; IO fall time register setting = 00b	I_{OL} = -1 mA			0.5	V
		V_{CC}= 5 V; IO fall time register setting = 01b				0.5	
		V_{CC}= 5 V; IO fall time register setting = 10b				0.5	
		V_{CC}= 5 V; IO fall time register setting = 11b				0.5	

Electrical Characteristics—Card Interface IO, C4 and C8 (continued)

$V_{DD} = V_{DDI} = 3.3$ V; $L_{VDD} = 10$ µH; $C_{VDD} = 10$ µF; $C_{VUP} = 10$ µF; $T_A = –40°C$ to 85°C unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OL - IO, 3 V}$	Output Low Voltage	V_{CC}= 3 V; IO fall time register setting = 01b	I_{OL}= -1 mA			0.3	V
		V_{CC}= 3 V; IO fall time register setting = 10b				0.3	
		V_{CC}= 3 V; IO fall time register setting = 11b				0.3	
$V_{OL - IO, 3 V, 500uA}$	Output Low Voltage	V_{CC}= 3 V; IO fall time register setting = 00b	I_{OL}= -500 µA			0.3	V
		V_{CC}= 3 V; IO fall time register setting = 01b				0.3	
		V_{CC}= 3 V; IO fall time register setting = 10b				0.3	
		V_{CC}= 3 V; IO fall time register setting = 11b				0.3	
$V_{OL - IO, 1.8 V}$	Output Low Voltage	V_{CC}= 1.8 V; IO fall time register setting = 11b	I_{OL}= -1 mA			0.18	V
$V_{OL - IO, 1.8 V, 500uA}$	Output Low Voltage	V_{CC}= 1.8 V; IO fall time register setting = 01b	I_{OL}= -500 µA			0.18	V
		V_{CC}= 1.8 V; IO fall time register setting = 10b				0.18	
		V_{CC}= 1.8 V; IO fall time register setting = 11b				0.18	
$t_{PD - R - IOMC - IO}$	Rising edge propagation delay	From IOMC pin to card IO; C_L on card IO = 30 pF; C_L on IOMC = 30 pF; Prop delay measured from 70% V_{DDI} to 70% of V_{CC} for rising edge				400	ns
$t_{PD - F - IOMC - IO}$	Falling edge propagation delay	From IOMC pin to card IO; C_L on card IO = 30 pF; C_L on IOMC = 30 pF; Prop delay measured from 30% V_{DDI} to 30% of V_{CC} for falling edge;				250	ns
$t_{FO - IO}$	IO Line output fall time	C_L = 30 pF ; 10% to 90%; IO fall time register setting = 00b			68		ns
$t_{RO - IO}$	IO Line output rise time	C_L = 30 pF ; 10% to 90%; IO rise time register setting = 100b			100		ns
$t_{RO - C4, C8}$	C4, C8 Line output rise time	C_L = 30 pF ; 10% to 90%				1.2	µs
$t_{FO - C4, C8}$	C4, C8 Line output fall time	C_L = 30 pF ; 90% to 10%				1.2	µs
$t_{RI - IO, C4, C8}$	IO, C4, C8 Input rise time	10% to 90%				1.2	µs
$t_{FI - IO, C4, C8}$	IO, C4, C8 Input fall time	90% to 10%				1.2	µs
$C_{I - IO, C4, C8}$	Input capacitance	F = 1 MHz				10	pF
$R_{PU - IO, C4, C8}$	Pull-up resistance	IO, C4, C8 pull-up to V_{CC}		4.25		8.1	kΩ

6.10 Electrical Characteristics—PRES

$V_{DD} = V_{DDI} = 3.3$ V; $L_{VDD} = 10$ µH; $C_{VDD} = 10$ µF; $C_{VUP} = 10$ µF; $T_A = –40°C$ to 85°C unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{IL - PRES}$	Input Low voltage				0.3 V_{DDI}	V
$V_{IH - PRES}$	Input high voltage		0.7 V_{DDI}			V
$I_{LEAK - PRES}$	Input leakage current	Voltage on pin = V_{DDI}			1	µA
$t_{DEB(P)}$	Debounce time	Time from transition on PRES pin to PRESL bit being set		20		ms
$t_{DEB(D)}$		Time from transition on PRES pin to start of deactivation sequence (RST going low)		100		µs

6.11 Electrical Characteristics—IOMC1 and IOMC2

$V_{DD} = V_{DDI} = 3.3$ V; $L_{VDD} = 10$ µH; $C_{VDD} = 10$ µF; $C_{VUP} = 10$ µF; $T_A = –40°C$ to 85°C unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{OL- IOMC}$	Output low voltage	I_{OL} = -100 µA			0.2 V_{DDI}	V
$V_{OH - IOMC}$	Output high voltage	I_{OH} = 20 µA	0.8 V_{DDI}			V
$V_{IL - IOMC}$	Input low signal				0.3 V_{DDI}	V
$V_{IH - IOMC}$	Input high signal		0.7 V_{DDI}			V
$t_{PD - F - IO - IOMC}$	Falling edge propagation delay	From Card IO pin to IOMC; C_L on card IO = 30 pF; Prop delay measured from 30% V_{CC} to 30% of V_{DDI} for falling edge;			250	ns
$t_{PD - F - IO - IOMC}$	Rising edge propagation delay	From Card IO pin to IOMC; C_L on card IO = 30 pF; Prop delay measured from 70% V_{CC} to 70% of V_{DDI} for rising edge;			400	ns
$t_{RO - IOMC}$	Output rise time	C_L = 30 pF ; 10% to 90%			1.2	µs
$t_{FO - IOMC}$	Output fall time	C_L = 30 pF ; 90% to 10%			1.2	µs
$t_{RI - IOMC}$	Input rise time	10% to 90%			1.2	µs
$t_{FI - IOMC}$	Input fall time	90% to 10%			1.2	µs
$C_{I - IOMC}$	Input capacitance				10	pF
$R_{PU - IOMC}$	Pull-up resistance	Pull-up to V_{DDI}		11		kΩ

6.12 Electrical Characteristics—CLKIN1 and CLKIN2

$V_{DD} = V_{DDI} = 3.3$ V; $L_{VDD} = 10$ µH; $C_{VDD} = 10$ µF; $C_{VUP} = 10$ µF; $T_A = –40°C$ to 85°C unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{IL - CLKIN}$	Input Low voltage				0.2 V_{DDI}	V
$V_{IH - CLKIN}$	Input high voltage		0.8 V_{DDI}			V
$t_{R - CLKIN}$	Rise time	10% to 90%			0.1	µs
$t_{F - CLKIN}$	Fall time	90% to 10%			0.1	µs
f_{CLKIN}	Input clock frequency				26	MHz

6.13 Electrical Characteristics—A0 and SHDN

$V_{DD} = V_{DDI} = 3.3$ V; $L_{VDD} = 10$ µH; $C_{VDD} = 10$ µF; $C_{VUP} = 10$ µF; $T_A = –40°C$ to 85°C unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{IL - A0, SHDN}$	input Low voltage				0.2 V_{DDI}	V
$V_{IH - A0, SHDN}$	input high voltage		0.8 V_{DDI}			V
$I_{LEAK - A0, SHDN}$	Input leakage current	Voltage on pin = V_{DDI}			1	µA
$C_{I - A0, SHDN}$	Input Capacitance				10	pF
$R_{PU - SHDN}$	Pull-up resistance on SHDN	Pull-up to V_{DDI}		2.5		MΩ

6.14 Electrical Characteristics—INT

$V_{DD} = V_{DDI} = 3.3$ V; $L_{VDD} = 10$ µH; $C_{VDD} = 10$ µF; $C_{VUP} = 10$ µF; $T_A = –40°C$ to 85°C unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$I_{LEAK - INT}$	Input leakage current	Voltage on pin = V_{DDI}			1	µA
$V_{OL - INT}$	Output low voltage	I_{OL} = -3 mA			0.2 V_{DDI}	V

6.15 Electrical Characteristics—GPIO

$V_{DD} = V_{DDI} = 3.3$ V; $L_{VDD} = 10$ µH; $C_{VDD} = 10$ µF; $C_{VUP} = 10$ µF; $T_A = –40°C$ to 85°C unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{OL - GPIO}$	Output low voltage	I_{OL} = -10 mA			0.2 V_{DDI}	V
$I_{OL - GPIO}$	Output low current				10	mA
$I_{LEAK - GPIO}$	Input leakage current	Voltage on pin = V_{DDI}			1	µA
$T_{PD - GPIO}$	State transition on GPIO to INT assertion	R_{PU} on INT= 10 k; C_L on INT 20 pF; GPIO and INT transition referenced to 0.5 V_{DDI}			4	µs

6.16 Electrical Characteristics—SDA and SCL

V_{DD} = V_{DDI} = 3.3 V; L_{VDD} = 10 µH; C_{VDD} = 10 µF; C_{VUP} = 10 µF; T_A = –40°C to 85°C unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$I_{LEAK\text{ - }SDA,\ SCL}$	Input leakage current	Voltage on pin = V_{DDI}			1	µA
$V_{OL\text{ - }SDA,\ SCL}$	SDA output low voltage	I_{OL} = -3 mA			0.1 V_{DDI}	V
$I_{OL\text{ - }SDA,\ SCL}$	SDA max output low current	V_{OL} = 0.3 V			10	mA
$V_{IL\text{ - }SDA,\ SCL}$	Input low signal				0.2 V_{DDI}	V
$V_{IH\text{ - }SDA,\ SCL}$	Input high signal		0.8 V_{DDI}			V

6.17 Electrical Characteristics—Fault Condition Detection

V_{DD} = V_{DDI} = 3.3 V; L_{VDD} = 10 µH; C_{VDD} = 10 µF; C_{VUP} = 10 µF; T_A = –40°C to 85°C unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
T_{SD}	Shutdown temperature		125		145	°C
I_{SD}	Shutdown current	On card VCC pins	160	200	260	mA
I_{LIM}	Output current limit	On card IO pins	–15		15	mA
		On card CLK pins	–70		70	mA
		On card RST pins	–20		20	mA

6.18 I^2C Interface Timing Requirements(1)

PARAMETER		STANDARD MODE I^2C BUS		FAST MODE I^2C BUS		FAST MODE PLUS (FM+) I^2C BUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{scl}	I^2C clock frequency		100		400		1000	kHz
t_{sch}	I^2C clock high time	4		0.6		0.26		µs
t_{scl}	I^2C clock low time	4.7		1.3		0.5		µs
t_{sp}	I^2C spike time		50		50		50	ns
t_{sds}	I^2C serial data setup time	250		100		50		ns
t_{sdh}	I^2C serial data hold time	0		0		0		ns
t_{icr}	I^2C input rise time		1000		300		120	ns
t_{icf}	I^2C input fall time		300		300		120	ns
t_{ocf}	I^2C output fall time; 10 pF to 400 pF bus		300		300		120	µs
t_{buf}	I^2C bus free time between Stop and Start	4.7		1.3		0.5		µs
t_{sts}	I^2C Start or repeater start condition setup time	4.7		0.6		0.26		µs
t_{sth}	I^2C Start or repeater start condition hold time	4		0.6		0.26		µs
t_{sps}	I^2C Stop condition setup time	4		0.6		0.26		µs

(1) Refer to the *Parameter Measurement Information* section for more information.

6.19 I^2C Interface Timing Characteristics(1)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{vd(data)}$	Valid data time; SCL low to SDA output valid			450	ns
$t_{vd(ack)}$	Valid data time of ACK condition; ACK signal from SCL low to SDA (out) low			450	ns

(1) Refer to *Parameter Measurement Information* section for more information.

6.20 Synchronous Type 1 Card Activation Timing Characteristics

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{S1\text{-}RST\text{-}HI}$	C_L= 30 pF ; V_{CC}= 5 V; See Figure 4.	60	70	80	µs
$t_{S1\text{-}CLK\text{-}HI}$	C_L= 30 pF ; V_{CC}= 5 V; See Figure 4.	10	12.5	15	µs
$t_{S1\text{-}RST\text{-}CLK}$	C_L= 30 pF ; V_{CC}= 5 V; See Figure 4.	25	28	32	µs
$t_{S1\text{-}CLK\text{-}RST}$	C_L= 30 pF ; V_{CC}= 5 V; See Figure 4.	25	28	32	µs
$t_{S1\text{-}CLK\text{-}LO}$	C_L= 30 pF ; V_{CC}= 5 V; See Figure 4.	70	80	90	µs
$t_{S1\text{-}CLK\text{-}PER}$	C_L= 30 pF ; V_{CC}= 5 V; See Figure 4.	22.5	25	27.5	µs
$t_{S1\text{-}ATR\text{-}SETUP}$	C_L= 30 pF ; V_{CC}= 5 V; See Figure 4.	1			µs
Duty cycle	C_L= 30 pF ; V_{CC}= 5 V; See Figure 4.	45	50	55	%

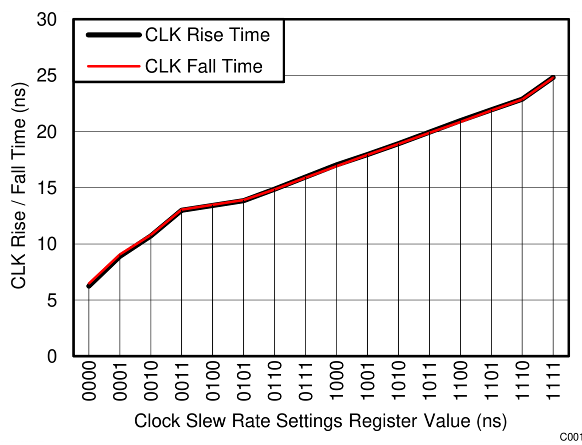
6.21 Synchronous Type 2 Card Activation Timing Characteristics

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{S2\text{-}VCC\text{-}CLK}$	C_L= 30 pF ; V_{CC}= 5 V; See Figure 5.	5	20		µs
$t_{S2\text{-}CLK\text{-}C4}$	C_L= 30 pF ; V_{CC}= 5 V; See Figure 5.	14	18	22	µs
$t_{S2\text{-}CLK\text{-}HI}$	C_L= 30 pF ; V_{CC}= 5 V; See Figure 5.	7	9	11	µs

6.22 Card Deactivation Timing Characteristics

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{DEAC\text{-}TOTS}$	C_L= 30 pF ; V_{CC}= 5 V; See Figure 7.		0.5	0.6	ms
$t_{DEAC\text{-}RST\text{-}CLK}$	C_L= 30 pF ; V_{CC}= 5 V; See Figure 7.	10	12	15	µs
$t_{DEAC\text{-}RST\text{-}IO}$	C_L= 30 pF ; V_{CC}= 5 V; See Figure 7.	22	24	26	µs
$t_{DEAC\text{-}RST\text{-}VCC}$	C_L= 30 pF ; V_{CC}= 5 V; See Figure 7.		45		µs

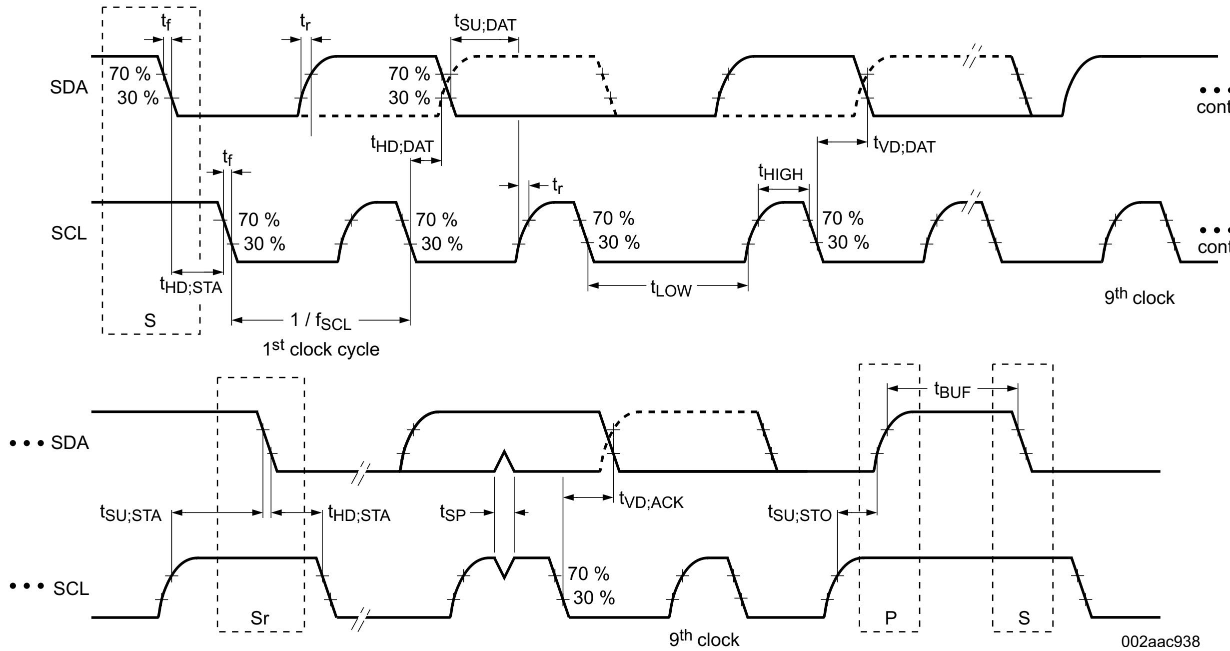
6.23 Typical Characteristics



C_L = 30 pF

Figure 1. CLK Rise/Fall Time vs Clock Slew Rate Settings Register Value

7 Parameter Measurement Information



$V_{IL} = 0.3\ V_{DDI}$

$V_{IH} = 0.7\ V_{DDI}$

Figure 2. Parameter Measurement Information for I²C Timing Characteristics and Requirements

8 Detailed Description

8.1 Overview

TCA5013 is a smartcard interface IC that enables POS terminals to interface with EMV4.3 and ISO7816-3 and ISO7816-10 compliant smartcards. The device has 4 smartcard interfaces (1 user card and 3 SAM cards). TCA5013 is capable of card activation and deactivation per EMV4.3, ISO7816-3 and ISO7816-10 standards.

TCA5013 has two power supply pins - VDD and VDDI. VDD is the main power supply for the device and VDDI is the reference supply for the interface operating voltage. V_{DD} and V_{DDI} need to ramped to within the recommended operating conditions for the device to operate properly. Upon power up an internal Power-On-Reset circuit initializes the digital core with all the registers in their default state as described in *Register Maps*.

TCA5013 can operate in various functional modes as defined in *Device Functional Modes*. When one of the device power supplies is not applied, that is, $V_{DD} < V_{DDSH}$ or $V_{DDI} < V_{DDITH}$ the device is in *Power Off Mode*. None of the device functions are available in this mode. *Shutdown Mode* is the lowest power operating mode in the device. Shutdown mode is entered by asserting the SHDN = 0 when $V_{DD} > V_{DDSH}$ and $V_{DDI} > V_{DDITH}$. The device can detect card insertion and removal even in Shutdown mode. The device is in Standby mode when $V_{DD} > V_{DDSH}$ or $V_{DDI} > V_{DDITH}$ and the SHDN pin = 1. When any of the 4 smartcard interfaces is activated, the device enters active mode (see *Active Mode*). The user card interface module can be activated in synchronous type 1, synchronous type 2, asynchronous or manual operation mode. For synchronous type 1 and synchronous type 2 operation modes, the device can automatically generate activation sequences per the ISO7816-10 standard (see *Synchronous Type 1 Operating Mode* and *Synchronous Type 2 Operating Mode*). For asynchronous cards the device performs the activation sequence and also verifies the response from the card meets the requirements per ISO7816-3 and EMV4.3 standards (see *Asynchronous Operating Mode*). The device also supports WARM reset (see *Warm Reset Sequence*) and card deactivation (see *Deactivation Sequence*) of smartcards per the ISO7816-3 and EMV4.3 standards. The SAM card interface modules can only be activated in aynchronous operation mode.

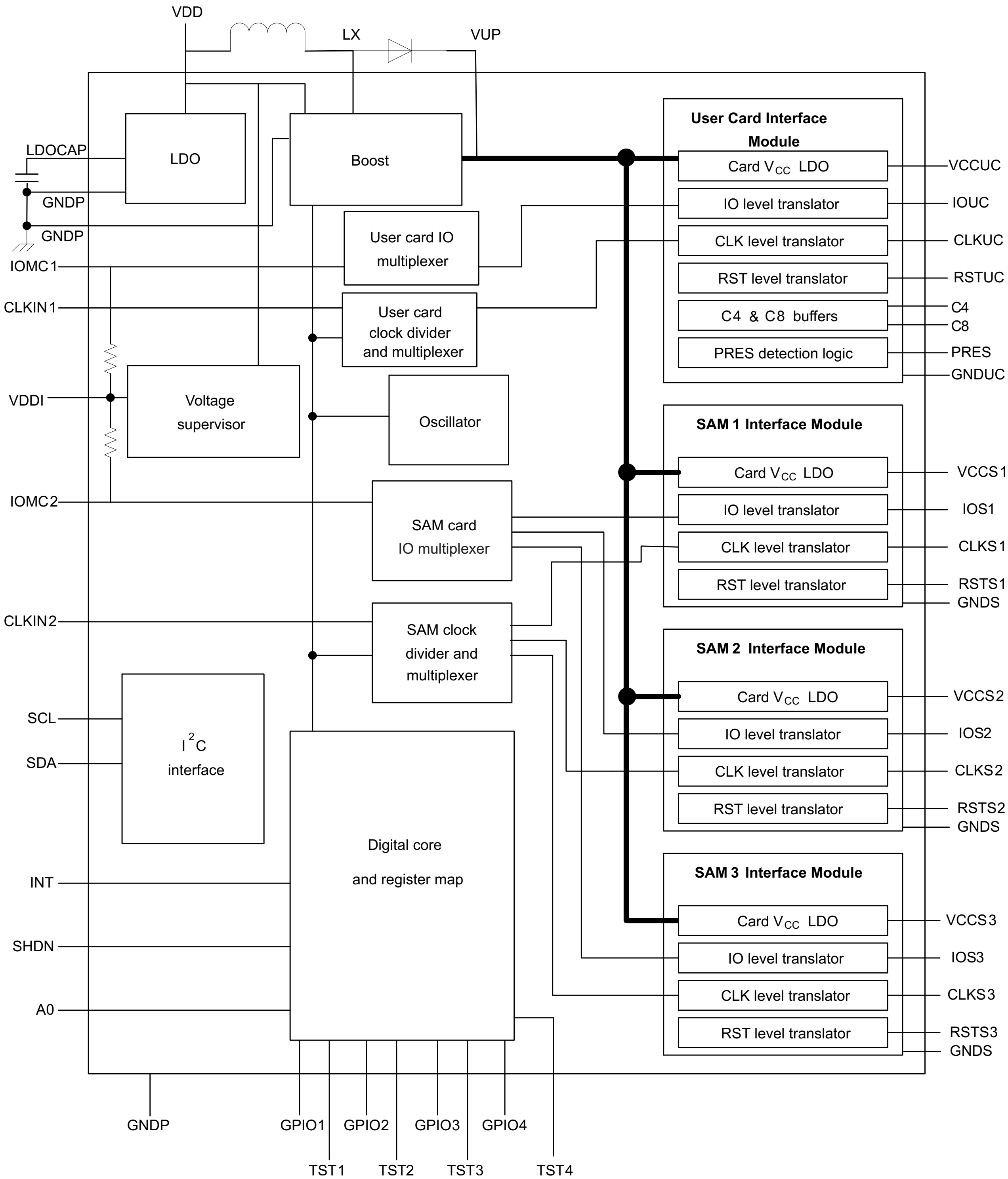
All smartcard interfaces have the standard CLK, IO and RST pins (as defined by EMV4.3 and ISO7816 standards). All these pins are designed to have internal current limiting to prevent device damage when shorted. CLK and IO pins also provide automatic level translation to the voltage at which the card has been activated. Rrise time and fall time of the CLK and IO pins can also be controlled using digital register settings (see *IO Rise Time and Fall Time control* and *CLK Rise Time and Fall Time Control*). In addition to the CLK, IO and RST pins the user card interface also has PRES pin to detect card insertion and removal (see *User Card Insertion / Removal Detection*). C4 and C8 pins, as defined by ISO7816-10, are also present on the user card interface (see *User Card Interface Module*).

The device has internal boost and LDOs to generate the card activation voltage depending on the operating voltage required by the specific card being interfaced with. It also has a voltage supervisor that monitors V_{DD} and V_{DDI} and responds as described in *Interrupt Operation* . The power management section is described in more detail in *Power Management*.

In addition to these functions the device provides 8kV IEC 61000-4-2 ESD protection on all pins that interface to smartcards. This removes the need for any external ESD protection on the board, thereby providing system robustness without compromising system security (removable components on secure lines).

TCA5013 is configured using a standard I^2C interface that is capable of up to 1 MHz operation. The I^2C interface is also used to read the status of various fault conditions that the device can detect. The I^2C operation is described in detail in *I^2C Interface Operation*.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Card Interface Modules

TCA5013 has 1 user card interface module and 3 SAM card interface modules. All card modules have level translators and an LDO to support interfacing with smartcards operating at different voltages.

8.3.2 SAM Card Interface Modules

All SAM card interface modules can operate per the EMV4.3 and ISO7816-3 standard and support asynchronous operating mode. All SAM card interface modules have the standard IO, CLK and RST pins. Detailed operation of these pins is described in section IO operation, CLK operation and RST operation.

8.3.3 User Card Interface Module

User card interface module can also operate per the EMV4.3 and ISO7816-3 standard and support asynchronous operating mode. In addition, the user card interface module also supports synchronous type 1 operating mode and synchronous type 2 operating mode, per ISO7816-10. Like the SAM card interface modules, the user card interface module also has IO, CLK, and RST pins. The user card interface module also has a PRES pin that is used for detection of user card insertion or removal.

C4 and C8 are two pins that are only present on the user card interface. These are open drain bi-directional IOs that are controlled by the bit [5] and bit [4] of user card synchronous mode settings register (Reg 0x09) when the card interface is activated. These bits act as both control and status bits for the C4 and C8 signals. If a ‘0’ is written to either of these bits the corresponding pin is driven low by the TCA5013. However, when a ‘1’ is written to the register bit, the corresponding pin is pulled up by an internal pull-up resistor. In this state an external device can drive the pin low. If the pin is driven low, then the corresponding bit in the register changes to reflect the status of the pin.

8.3.4 Clock Division and Multiplexing

TCA5013 card interface modules all have a CLK pin that provide a clock signal that is used for smartcard operation. This clock signal is generated based on an internal oscillator or from the CLKIN1/CLKIN2 input clock signals, by the clock divider and multiplexer circuitry. The user card has a dedicated clock divider and multiplexer. The user card CLK output can be a configured to be a function of the CLKIN1 frequency or the internal oscillator frequency. CLKIN2 is shared by all the SAM card interface modules. The CLK output of each SAM card can be independently configured based on the CLKIN2 frequency or the internal oscillator frequency. CLK operation section describes the clock division and multiplexing in detail.

8.3.5 IO Multiplexing

IOMC1 and IOMC2 are connected to the IO pins in the card interface modules through IO multiplexer blocks. The user card IO module has a dedicated IO multiplexer, that can be connect or disconnect IOUC from the IOMC1 pin. The IOMC2 is connected to the SAM card interface modules IO pins through the SAM IO multiplexer block. The IOMC2 can only be connected to one of the SAM interface modules at any given time. IO operation section describes IO multiplexing in detail.

8.3.6 GPIO Operation

The TCA5013 has four 5 V tolerant open drain GPIO pins that can be configured as inputs or outputs through device settings register (Reg 0x42). If configured as outputs, each is capable of sinking up to 10mA of current. If configured as inputs they will assert the INT line when a state change occurs on the pin. The minimum pulse width for transition detection is 10 µs, that is, when a state transition occurs on a GPIO configured as an input, it needs to hold its state for a minimum of 10 µs in order to guarantee detection by the TCA5013. This, however, does not imply any glitch rejection on the GPIO pins. The GPIOs are available in *Standby Mode* and *Active Mode*. GPIO state transitions are not tracked in shutdown mode.

8.3.7 Power Management Features

TCA5013 has a DC-DC boost and card LDOs that enable it to generate regulated smart card V_{CC} from its input power rails (V_{DD} and V_{DDI}). It also has an internal LDO that is used to power its internal circuits. The TCA5013 devices also have a voltage supervisor that monitors the V_{DD} and V_{DDI} rails to ensure they are stable and usable for smartcard operation.

Feature Description (continued)

8.3.8 ESD Protection

All the smart card interface pins in the TCA5013 devices are designed with in built IEC61000-4-2 level 4 8kV contact ESD protection. Table 1 shows a list of pins with the 8kV ESD protection. The pins not listed below all have 4kV HBM ESD protection.

Table 1. List of Pins with 8kV IEC ESD Protection

PIN	SYMBOL	TYPE	DESCRIPTION
A1	PRES	INPUT	User card presence detection
B1	C8	IO	User card auxiliary IO (Open Drain)
C2	C4	IO	User card auxiliary IO (Open Drain)
D1	CLKUC	OUTPUT	User card clock
E2	IOUC	IO	User card IO
F1	RSTUC	OUTPUT	User card RST
F2	VCCUC	PWR	User card VCC
H1	VCCUC	OUTPUT	SAM3 RST
H2	IOS3	IO	SAM3 IO
H5	IOS2	IO	SAM2 IO
H8	IOS1	IO	SAM1 IO
H9	VCCS1	PWR	SAM1 VCC
J1	CLKS3	OUTPUT	SAM3 CLK
J2	VCCS3	PWR	SAM3 VCC
J4	RSTS2	OUTPUT	SAM2 RST
J5	CLKS2	OUTPUT	SAM2 CLK
J6	VCCS2	PWR	SAM2 VCC
J8	RSTS1	OUTPUT	SAM1 RST
J9	CLKS1	OUTPUT	SAM1 CLK

8.3.9 I²C interface

The device has a standard I²C interface that is used to configure the device and to read the status of the device. For detailed I²C operation refer to *I²C Interface Operation*.

8.4 Device Functional Modes

At any given time the TCA5013 can be in one of several different functional modes. Figure 3 diagram shows the different functional modes and describes how the device transitions from one mode to another. The blue bubbles represent actual functional modes and the white bubbles represent transitional states that are used to move from one functional mode to another.

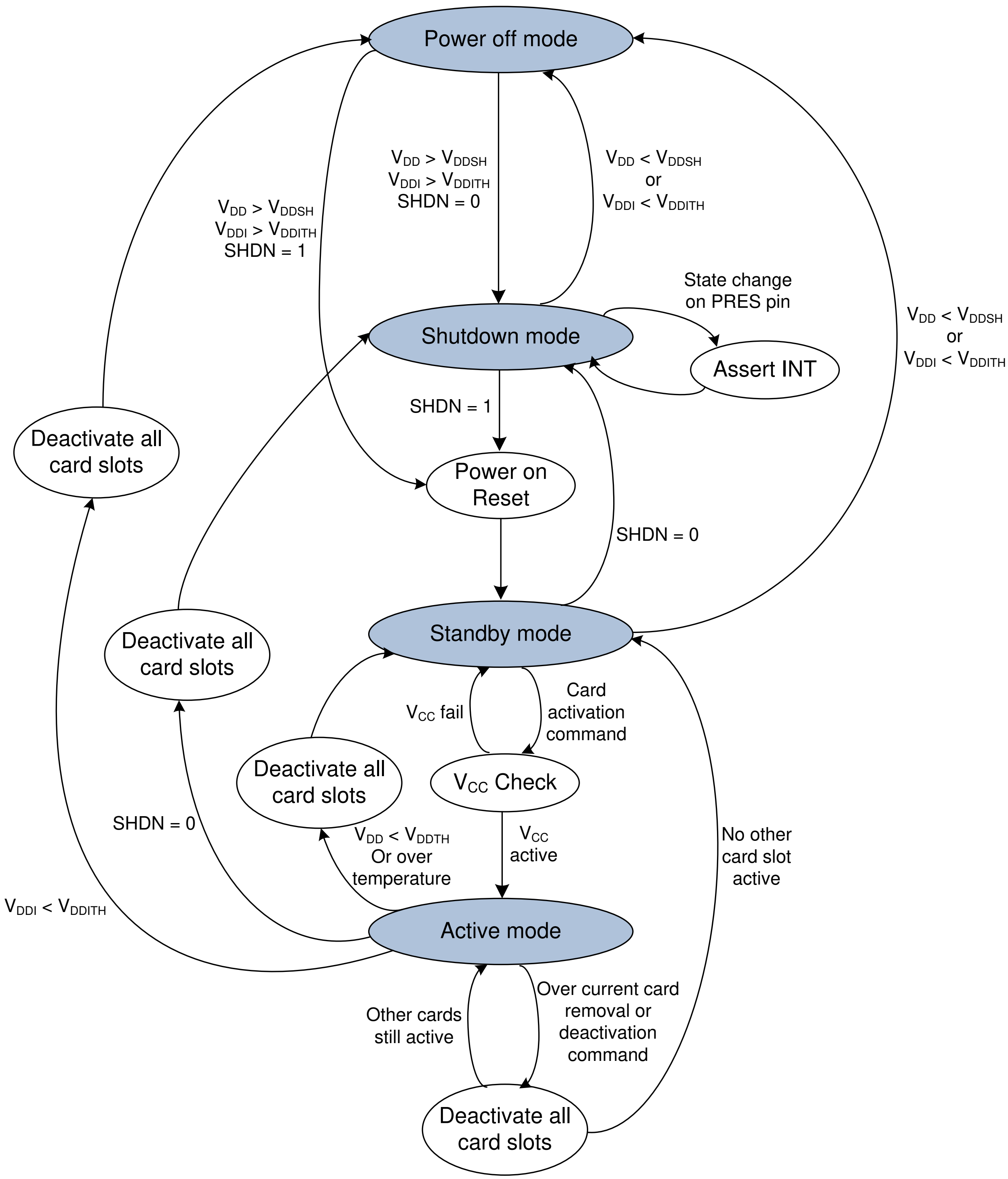


Figure 3. Device Operating Modes

Device Functional Modes (continued)

8.4.1 Power Off Mode

The TCA5013 is in power off mode when $V_{DD} < V_{DDSH}$ or $V_{DDI} < V_{DDITH}$. In power off mode none of the device features are functional and available for use.

8.4.2 Shutdown Mode

TCA5013 is in shutdown mode when all the below conditions are true.

- $V_{DD} > V_{DDSH}$
- $V_{DDI} > V_{DDITH}$
- SHDN = 0

Shutdown mode is a low power mode where all circuits except card insertion detection circuitry are shutdown. Even I2C communication is disabled in shutdown mode. The only active circuit in the device is card insertion detection circuit on the PRES pin (see *User Card Insertion / Removal Detection*). Shutdown mode is entered from *Active Mode* or *Standby Mode* by asserting the SHDN pin. When entering shutdown mode from *Active Mode* all active card interfaces are automatically deactivated.

8.4.3 Standby Mode

The TCA5013 is in standby mode when all the below conditions are true.

- $V_{DD} > V_{DDSH}$
- $V_{DDI} > V_{DDITH}$
- SHDN = 1
- No card interfaces are activated.

In standby mode, the device I^2C and card detection circuits are fully functional. All other circuits are ready to be activated based on I^2C commands received from the microcontroller. Standby mode is entered from shutdown mode by releasing the SHDN pin or from power down mode by powering up the device or from active mode by deactivating all card interfaces.

8.4.4 Active Mode

The TCA5013 is in active mode when all the below conditions are true.

- $V_{DD} > V_{DDSH}$
- $V_{DDI} > V_{DDITH}$
- SHDN = 1
- At least one card interface is activated

  In active mode, the device is fully functional with at least one of the card interfaces activated. The DC-DC Boost and card LDOs are active and provide power to the card VCC pins of the active card interfaces. Active mode can only be entered from standby mode by activating one of the card interfaces. When the device is in active mode, the individual card interfaces can be active in different operating modes. The user card supports *Asynchronous Operating Mode*, *Synchronous Type 1 Operating Mode*,*Synchronous Type 2 Operating Mode*, or *Manual Operating Mode*. The SAM card interfaces can only be activated in asynchronous activation mode.

Device Functional Modes (continued)

8.4.4.1 User Card Operating Mode Selection

The user card interface in the TCA5013 can be activated in different operating modes. When the START_ASYNC bit (bit [0]; Reg 0x01) is set the user card interface is activated in asynchronous operating mode. When START_SYNC bit (bit[0]; Reg 0x09) is set the user card interface is activated in synchronous type1, synchronous type 2 or manual operating mode. When the START_SYNC bit is set, the operating mode is determined by the ACTIVATION_TYPE bit (bit [6]; Reg 0x09) and CARD_TYPE bit (bit [7] Reg 0x09).

If ACTIVATION_TYPE bit (bit [6]; Reg 0x09) is set to ‘0’, the user card interface is activated in manual operating mode. If the ACTIVATION_TYPE bit is set to’1’, the user card interface is set for automatic activation, where it will be activated in synchronous type 1 or synchronous type 2 operating mode based on CARD_TYPE bit (bit [7] Reg 0x09). If CARD_TYPE bit is set to ‘1’, the card interface is activated in synchronous type 2 operating mode. If CARD_TYPE bit is set to ‘0’ the card interface is activated in synchronous type 1 operating mode.

Any changes made to the START_SYNC, START_ASYNC, CARD_TYPE or ACTIVATION_TYPE bits when the user card interface is active, will be ignored and will have no effect on the device. These new settings will take effect only on the next card interface activation following deactivation (see *Deactivation Sequence*).

8.4.4.2 Synchronous Type 1 Operating Mode

Synchronous type 1 operating mode is only supported on the user card interface. To enter synchronous operating mode, the user card interface goes through the synchronous type 1 activation sequence. Figure 4 shows the synchronous type 1 activation sequence.

CLKIN1 shall be low before the synchronous type 1 activation sequence is initiated. The following bit settings are required to initiate a synchronous type 1 activation sequence.

- ACTIVATION_TYPE (bit [6]; Reg 0x09) = 1
- CARD_TYPE (bit [7]; Reg 0x09) = 0
- START_SYNC (bit [0]; Reg 0x09) = 1

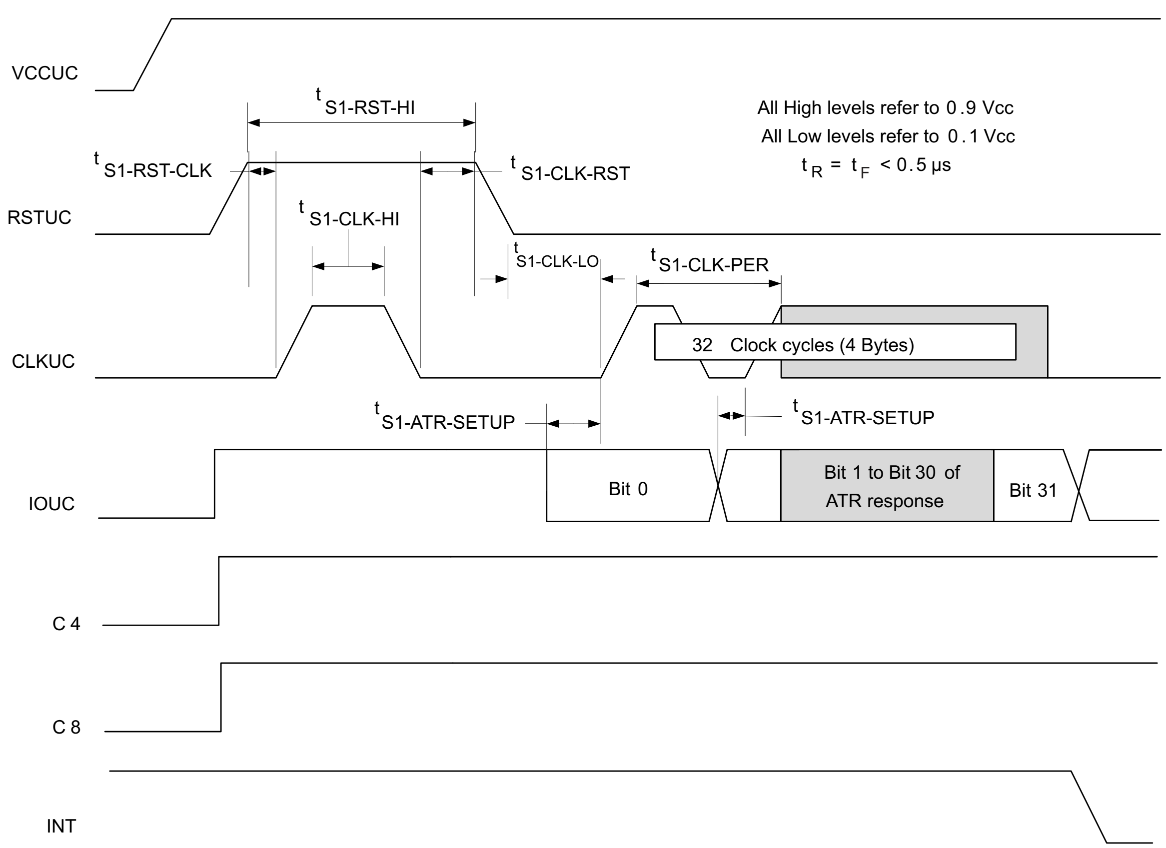


Figure 4. Synchronous Type 1 Activation Sequence

Device Functional Modes (continued)

Once synchronous type 1 activation has been initiated, the following sequence of events occurs on the user card interface:

- VCCUC, RSTUC, CLKUC, C4, C8 and IOUC are all default low.
- V_{CC} is applied to the VCCUC pin per the SET_VCC_UC bit (bit[7:6]; Reg 0x01).
- After V_{CC} is stable RSTUC and CLKUC pulses are applied per $t_{S1\text{-}RST\text{-}HI}$ and $t_{S1\text{-}CLK\text{-}HI}$ defined in Table 2.
- After V_{CC} is stable, the IOUC line is pulled up to V_{CC} .
- After V_{CC} is stable C4 and C8 reflect the value in their corresponding I2C register bits (bit[5] and bit[4]; Reg 0x09).
- RSTUC is held low while the CLKUC line starts oscillating with a frequency of ~40Khz (generated from internal oscillator).
- The IO line is sampled on the 32 rising or falling (based on bit[1]; Reg 0x09) edges of CLK and stored in the FIFO registers 0AH to 0DH.
- At the end of the 32nd CLK pulse, the CLKUC is held low and the CLKUC pin is controlled by the clock settings register (Reg 0x02).
- IOUC is connected to IOMC1 if IO_EN_UC bit (bit[5] Reg 0x01) is set to 1.
- INT_SYNC_COMPLETE bit (Bit[1]; REG 0x41) is set and the INT line is asserted low.
- IOMC1 shall stay pulled up to V_{DDI} i.e. IOMC1 shall not be pulled low until INT is asserted.
- CLKIN1 shall toggle only after INT is asserted.
- RSTUC is controllable by I^2C after INT is asserted.

Table 2. Synchronous Type 1 Card Activation Timing Characteristics

	MIN	TYP	MAX	UNIT
$t_{S1\text{-}RST\text{-}HI}$	60	70	80	µs
$t_{S1\text{-}CLK\text{-}HI}$	10	12.5	15	µs
$t_{S1\text{-}RST\text{-}CLK}$	25	28	32	µs
$t_{S1\text{-}CLK\text{-}RST}$	25	28	32	µs
$t_{S1\text{-}CLK\text{-}LO}$	70	80	90	µs
$t_{S1\text{-}CLK\text{-}PER}$	22.5	25	27.5	µs
Duty cycle	45	50	55	%

8.4.4.3 Synchronous Type 2 Operating Mode

Synchronous type 2 operating mode is only supported on the user card interface. To enter synchronous operating mode, the user card interface goes through the synchronous type 2 activation sequence. Figure 5 shows the synchronous type 2 activation sequence.

CLKIN1 shall be low before the synchronous type 2 activation sequence is initiated. The following bit settings are required to initiate a synchronous type 1 activation sequence.

- ACTIVATION_TYPE (bit [6]; Reg 0x09) = 1
- CARD_TYPE (bit [7]; Reg 0x09) = 1
- START_SYNC (bit [0]; Reg 0x09) = 1

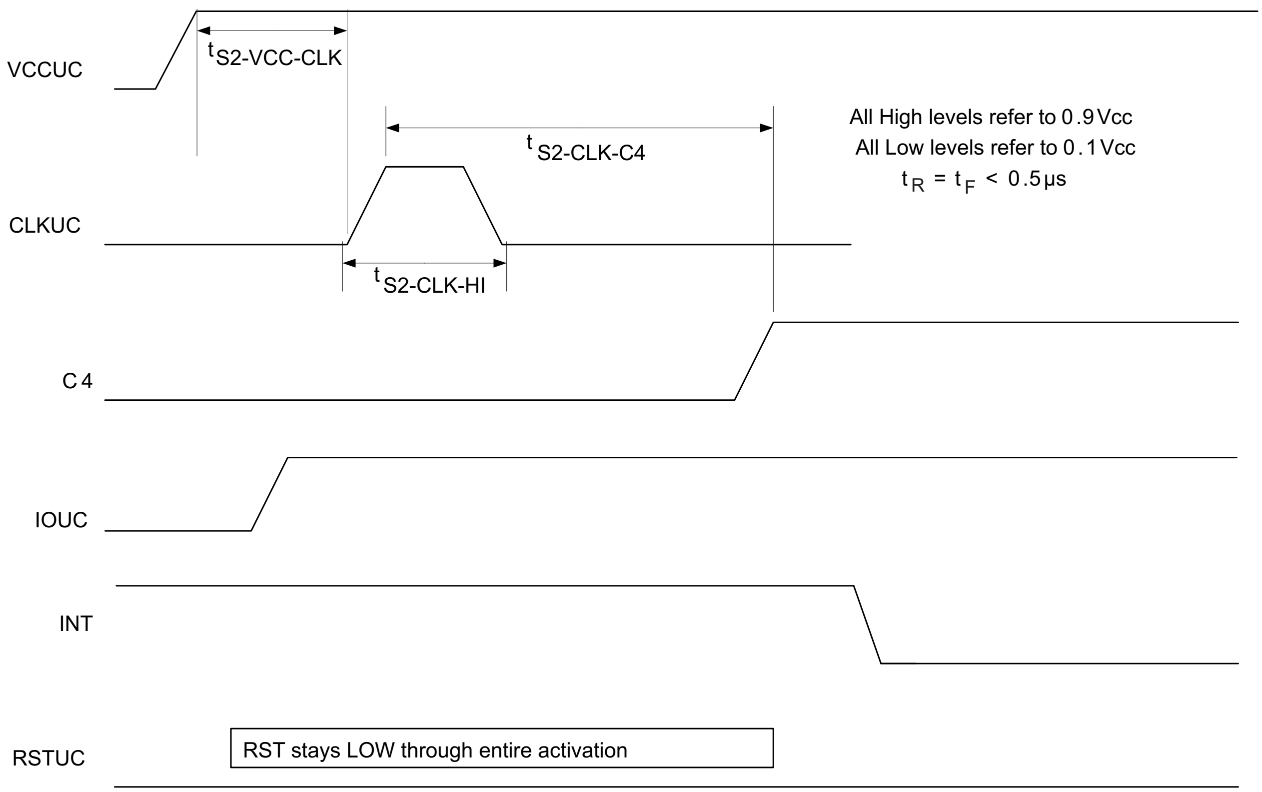


Figure 5. Synchronous Type 2 Activation Sequence

Once synchronous type 2 activation has been initiated, the following sequence of events occur on the user card interface:

- VCCUC, RSTUC, CLKUC, C4, C8 and IOUC are all default low.
- V_{CC} is applied to the VCCUC pin per the SET_VCC_UC bit (bit[7:6]; Reg 0x01).
- A single pulse is applied to CLKUC per the $t_{S2-CLK-HI}$ timing defined in Table 3.
- The C4 line is held low through the V_{CC} ramp.
- The C4 line is released high per the $t_{S2-CLK-C4}$ timing defined in Table 3.
- After C4 is released CLKUC is controlled by clock settings register (Reg 0x02).
- After V_{CC} is stable, the IOUC line is pulled up to V_{CC}.
- After V_{CC} is stable, C8 reflects value in bit [4] Reg 0x09.
- IOUC is connected to IOMC1 if IO_EN_UC bit (bit[5] Reg 0x01) is set to 1.
- INT_SYNC_COMPLETE bit (Bit[1]; REG 0x41) is set and the INT line is asserted low.
- IOMC1 shall stay pulled up to V_{DDI} , that is, IOMC1 shall not be pulled low until INT is asserted.
- CLKIN1 shall toggle only after INT is asserted.
- RSTUC is controllable by I^2C after INT is asserted.

Table 3. Synchronous Type 2 Card Activation Timing Characteristics

	MIN	TYP	MAX	UNIT
$t_{S2-VCC-CLK}$	5	20		µs
$t_{S2-CLK-C4}$	14	18	22	µs
$t_{S2-CLK-HI}$	7	9	11	µs

8.4.4.4 Manual Operating Mode

Manual operating mode is only supported on the user card interface. Unlike the other operating modes, the manual operating mode does not have a defined activation sequence. CLKIN1 shall be low before the manual activation sequence is initiated. The following bit settings are required to initiate a synchronous type 1 activation sequence.

- ACTIVATION_TYPE (bit [6]; Reg 0x09) = 0
- START_SYNC (bit [0]; Reg 0x09) = 1

Once manual activation has been initiated the following sequence of events occur on the user card interface.

- VCCUC, RSTUC, CLKUC, C4, C8 and IOUC are all default low.
- V_{CC} is applied to the VCCUC pin per the SET_VCC_UC bit (bit[7:6]; Reg 0x01)
- After V_{CC} is stable, the IOUC line is pulled up to V_{CC}
- After V_{CC} is stable C4 and C8 reflect the value in their corresponding I^2C register bits (bit[5] and bit[4]; Reg 0x09)
- IOUC is connected to IOMC1 if IO_EN_UC bit (bit[5] Reg 0x01) is set to 1.
- INT_SYNC_COMPLETE bit (Bit[1]; REG 0x41) is set and the INT line is asserted low.
- IOMC1 shall stay pulled up to V_{DDI} i.e. IOMC1 shall not be pulled low until INT is asserted.
- CLKIN1 shall toggle only after INT is asserted.
- RSTUC is controllable by I2C after INT is asserted.

8.4.4.5 Asynchronous Operating Mode

Asynchronous operating mode is supported on all card interfaces. To enter asynchronous operating mode, the user card interface goes through the asynchronous activation sequence. Figure 6 shows the asynchronous activation sequence. CLKIN1 shall be toggling before the asynchronous activation sequence is initiated. The asynchronous activation sequence is initiated by setting the START_ASYNC bit (bit[0]) of the card interface settings register (Reg 0x01 for User card, Reg 0x11 for SAM1, Reg 0x21 for SAM1, Reg 0x31 for SAM3) to '1'.

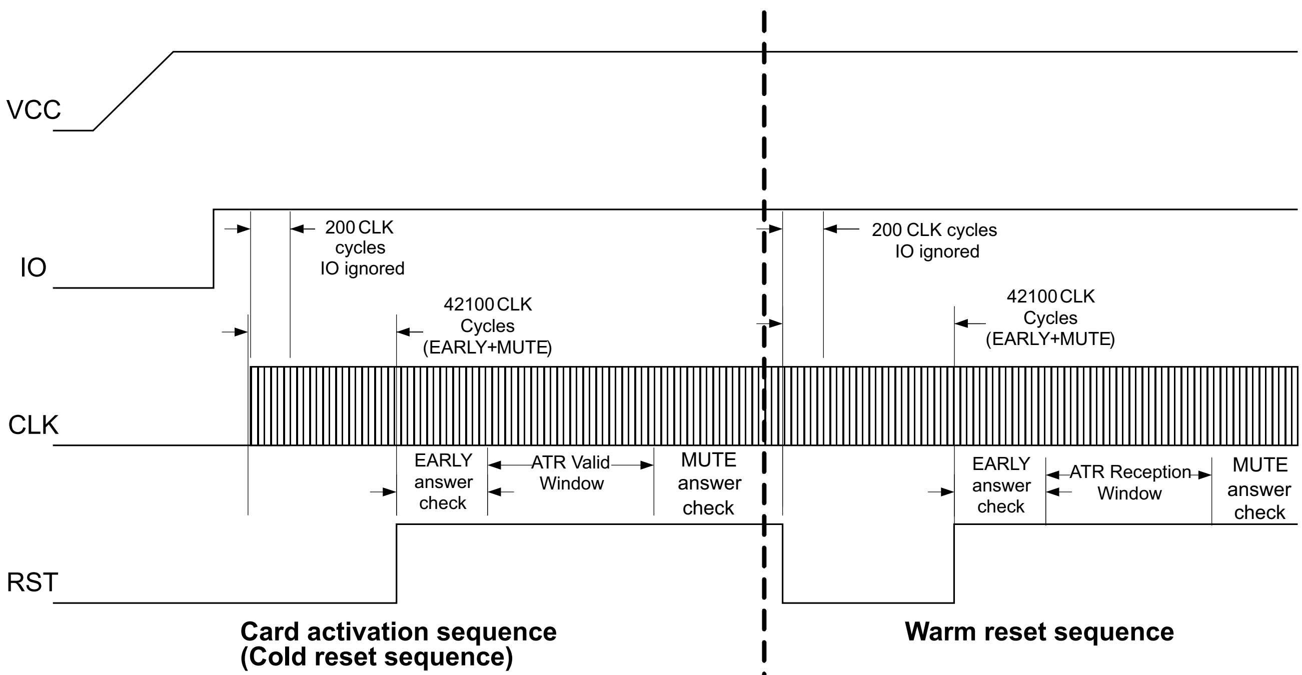


Figure 6. Asynchronous Activation and Warm Reset Sequence

Once asynchronous activation has been initiated, the following sequence of events takes place on the card interface:

- VCC, RST, CLK, C4, C8 and IO are all default low.
- V_{CC} is applied to the VCC pin per the SET_VCC bits (bit [7:6] of card interface settings register).
- After V_{CC} is stable, the IO line is pulled up to V_{CC}.
- After V_{CC} is stable C4 and C8 reflect the value in their corresponding I^2C register bits (bit[5] and bit[4]; Reg 0x09).
- IO is connected to IOMC if IO_EN bit (bit[5] of card interface settings register) is set to 1.
- The CLK line starts to oscillate based on the card clock settings register. Any change on the IO line during the first 200 card clock cycles on the CLK pin is ignored.
- After the first 42100 CLK cycles, the RST line is driven high.
- If there is a high to low transition on the IO line before RST is high, the EARLY bit (bit[6]) and MUTE bit (bit[5]) of the card interface status register (Reg 0x00 for user card, Reg 0x10 for SAM1, Reg 0x20 for SAM2 and Reg 0x30 for SAM3) is set and the INT pin is asserted low.
- After RST is high, an internal counter starts counting CLK cycles. If there is a high to low transition on IO pin before the internal counter reaches the value defined by in the EARLY_COUNT_HI register (Reg 0x03 for user card, Reg 0x13 for SAM1, Reg 0x23 for SAM2, Reg 0x33 for SAM3) and EARLY_ COUNT_LO Register (Reg 0x04 for user card, Reg 0x14 for SAM1, Reg 0x24 for SAM2, Reg 0x34 for SAM3) then the EARLY bit in the card interface status register is set and INT is asserted.
- If the internal counter reaches the value defined by MUTE_COUNT_HI register (Reg 0x05 for user card, Reg 0x15 for SAM1, Reg 0x25 for SAM2, Reg 0x35 for SAM3) and MUTE_COUNT_LO (Reg 0x06 for user card, Reg 0x16 for SAM1, Reg 0x26 for SAM2, Reg 0x36 for SAM3) registers without a high to low transition on the IO line, then the MUTE bit in the card interface status registers is set and INT pin is asserted low.

If the first high to low transition on IO pin happens very close to the clock edges (within ~10 ns) that defines the ATR VALID window (see Figure 6), the TCA5013 response would be non-deterministic, that is, it may not be able to identify whether the transition happened before or after the edge. This implies that the MUTE bit may or may not be set if the IO transition happens very close to the clock edge defining the end of the ATR VALID window. Likewise, if the IO transition happens very close to the clock edge defining the beginning of the EARLY window, it may or may not set the EARLY bit.

8.4.4.6 Warm Reset Sequence

When a card interface is active in asynchronous mode, it is possible to initiate a warm reset sequence on the card interface. The warm reset sequence is initiated by setting the WARM bit (bit [3]) of the card interface settings register to ‘1’. Once warm reset is initiated the below sequence of events takes place on the card interface.

- V_{CC} is already ramped and stable per the SET_VCC bits (bit[7:6] of card interface settings register).
- CLK continues to oscillate per the card clock settings register.
- RST pin is pulled low (high before warm reset was initiated).
- C4 and C8 continue to reflect the value in their corresponding I^2C register bits (bit[5] and bit[4]; Reg 0x09).
- IO stays connected to IOMC if IO_EN bit (bit5 of card interface settings register) is set to 1.
- Any change on the IO line during the first 200 card clock cycles after RST goes low is ignored.
- After the first 42100 CLK cycles, the RST line is driven high.
- If there is a high tow low transition on the IO line before RST is high, the EARLY bit (bit6) and MUTE bit (bit5) of the card interface status register (Reg 0x00 for user card, Reg 0x10 for SAM1, Reg 0x20 for SAM2 and Reg 0x30 for SAM3) is set and the INT pin is asserted low.
- After RST is high, an internal counter starts counting CLK cycles. If there is a high to low transition on IO pin before the internal counter reaches the value defined by in the EARLY_COUNT_HI register (Reg 0x03 for user card, Reg 0x13 for SAM1, Reg 0x23 for SAM2, Reg 0x33 for SAM3) and EARLY_ COUNT_LO Register (Reg 0x04 for user card, Reg 0x14 for SAM1, Reg 0x24 for SAM2, Reg 0x34 for SAM3) then the EARLY bit in the card interface status register is set and INT is asserted.
- If the internal counter reaches the value defined by MUTE_COUNT_HI register (Reg 0x05 for user card, Reg 0x15 for SAM1, Reg 0x25 for SAM2, Reg 0x35 for SAM3) and MUTE_COUNT_LO (Reg 0x06 for user card, Reg 0x16 for SAM1, Reg 0x26 for SAM2, Reg 0x36 for SAM3) registers without a high to low transition on the IO line, then the MUTE bit in the card interface status registers is set and INT pin is asserted low.

8.4.4.7 Deactivation Sequence

After a card interface has been activated in a certain operating mode, it can be deactivated by I²C command or certain interrupt events (see *Interrupt Operation*). The deactivation sequence is the same regardless of what operating mode the card interface is in.

Figure 7 shows the deactivation sequence initiated by card extraction on the user card interface. It is to be noted that the deactivation sequence starts 100 µs after the transition on PRES. This delay is intended to provide a debounce period that provides unintended deactivation due to any glitch on the PRES pin. As mentioned previously any of the card interfaces may be deactivated due to a supervisor fault, over current fault or over temperature fault. In these cases there is no debounce period and the deactivation sequence is initiated as soon as the internal fault signal is asserted.

Figure 8 shows the deactivation of any card interface initiated by I²C command. If the card interface is activated in asynchronous mode, it can be deactivated by clearing (writing '0') the START_ASYNC bit in the card interface settings register. To deactivate the user card interface when it is activated in synchronous mode, the START_SYNC bit should be cleared (write '0').

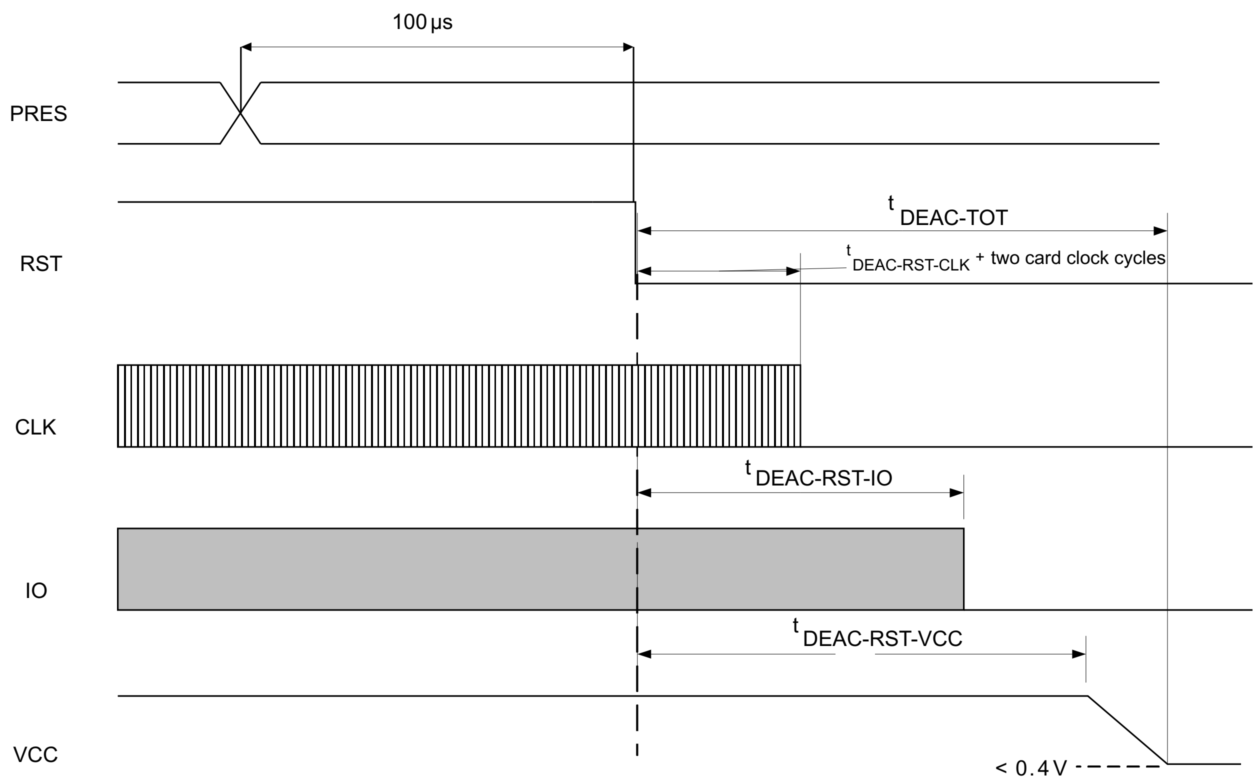


Figure 7. Deactivation Sequence

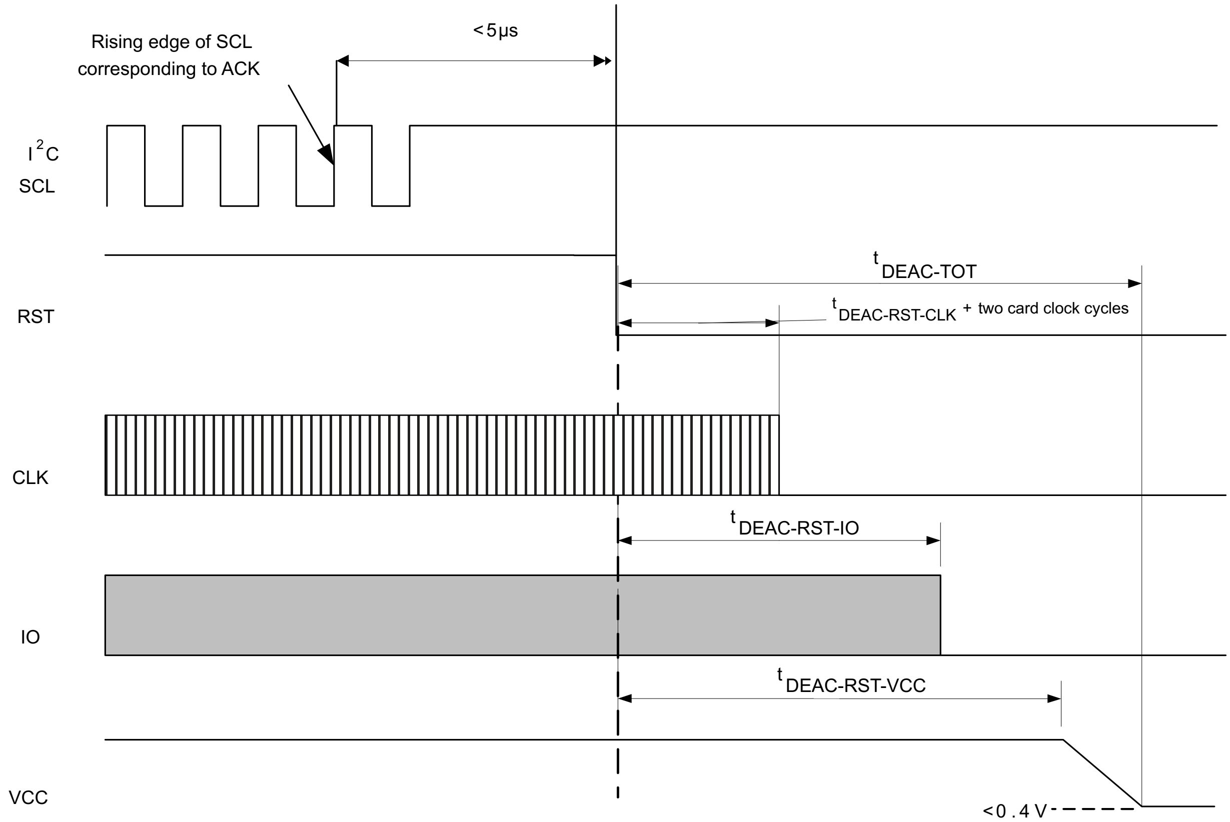


Figure 8. Card Deactivation Sequence Initiated by I^2C Command

Table 4. Card Deactivation Timing Characteristics

	MIN	TYP	MAX	UNIT
$t_{DEAC\text{-}TOT}$	0.4	0.5	0.6	ms
$t_{DEAC\text{-}RST\text{-}CLK}$	10	12	15	µs
$t_{DEAC\text{-}RST\text{-}IO}$	22	24	26	µs
$t_{DEAC\text{-}RST\text{-}VCC}$	33	36	39	µs

8.4.5 User Card Insertion / Removal Detection

User card interface module in the TCA5013 has a PRES pin that is used to detect the presence of a card in that interface. In normal application the signal is connected to a switch that opens or closes when a card is inserted. Whenever a transition is seen on the PRES pin, the PRESL bit (Reg 0x00, bit 2) will be set and INT pin is asserted. Because this transition is associated with a mechanical switch, there is an internal debounce of ~20 ms before the PRESL bit is set and the INT is asserted. If the device sees a transition on the PRESL pin when the card interface is active, the device initiates a card deactivation sequence (see *Deactivation Sequence*). TCA5013 is capable of detecting card insertion even when it is in shutdown mode (see *Shutdown Mode*).

In addition to the PRESL_UC bit mentioned above, there is also a PRES_UC bit (Reg 0x00, bit 2), which indicates to the host whether or not a card is present in the user card slot. In order to accommodate different card cage topologies, the TCA5013 can be configured to detect card presence with a low to high or high to low, transition on the PRES pin. The CARD_DETECT_UC bit (Reg 0x01, bit 2) is used to configure the device for different card detection topologies. If CARD_DETECT_UC = 0 indicates to the TCA5013 that when a card is inserted in the slot, the PRES pin shall be low. CARD_DETECT_UC = 1 indicates to the host that when a card is inserted in the slot the PRES pin shall be high. The status of the PRES_UC bit is based on the status of the PRES pin and the CARD_DETECT_UC bit. The truth table in Table 1 shows the PRES_UC bit status based on the CARD_DETECT_UC bit and the PRES pin. When coming out of power off mode (see *Power Off Mode*) or shutdown mode (see *Shutdown Mode*) the CARD_DETECT_UC = 0. If there is a state transition on the PRES pin when the device is in shutdown mode, the INT pin asserted (after the 20 ms debounce).

Table 5. Truth Table Defining Status of PRES Bit

CARD DETECT BIT	PRES PIN	PRES BIT
0	0	1
0	1	0
1	0	0
1	1	1

Figure 9 to Figure 14 show timing waveforms of device power up and coming out of shutdown with and without a card inserted in the system. In below figures' low to high PRES topology' means that a high level on the PRES pin indicates a card is present. In below figures high to low PRES topology' means that a low level on the PRES pin indicates a card is present. The below figures also show operation of INT pin and interrupt status register. For detailed description of the interrupt operation, refer to *Interrupt Operation* section.

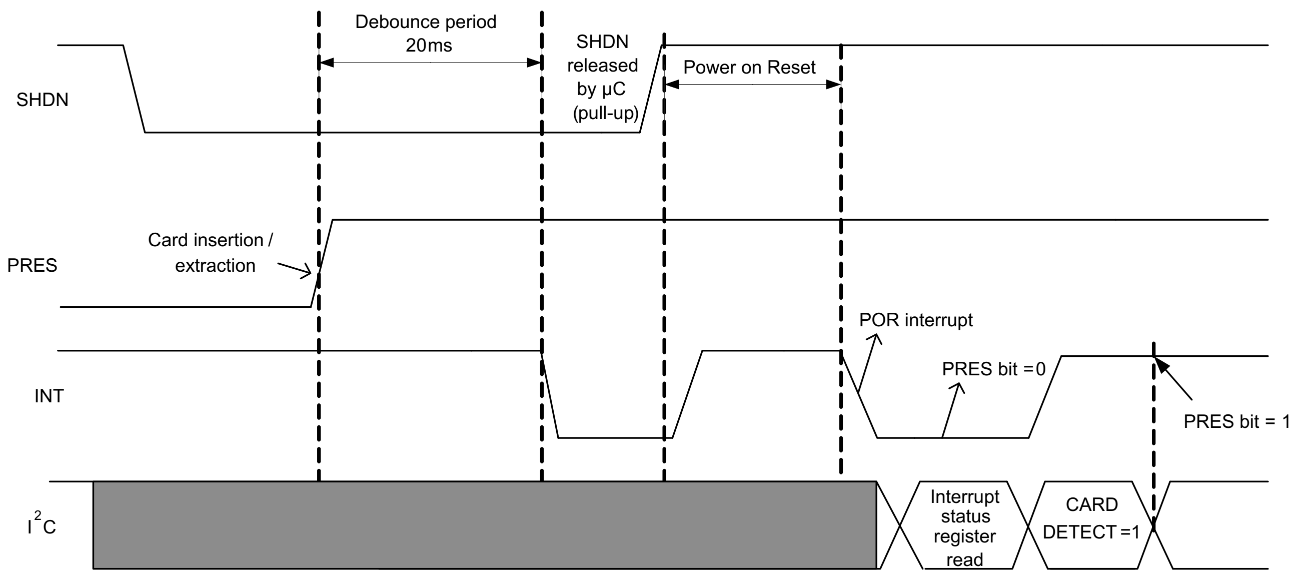


Figure 9. Card detection in shutdown mode - Low to High PRES Topology

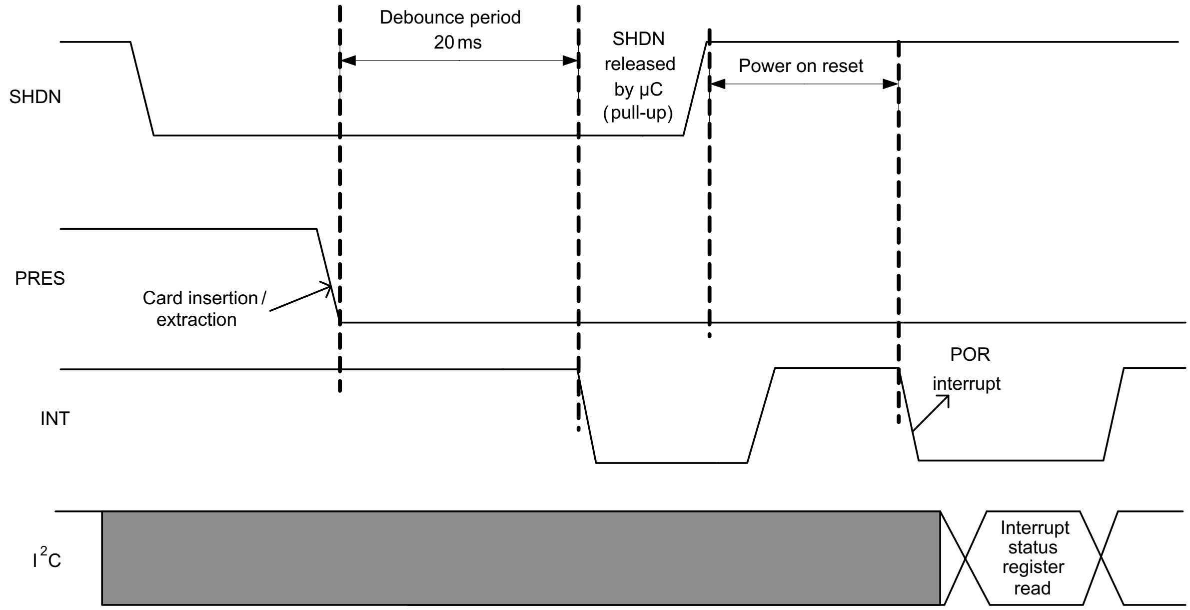


Figure 10. Card detection in shutdown mode - High to Low PRES Topology

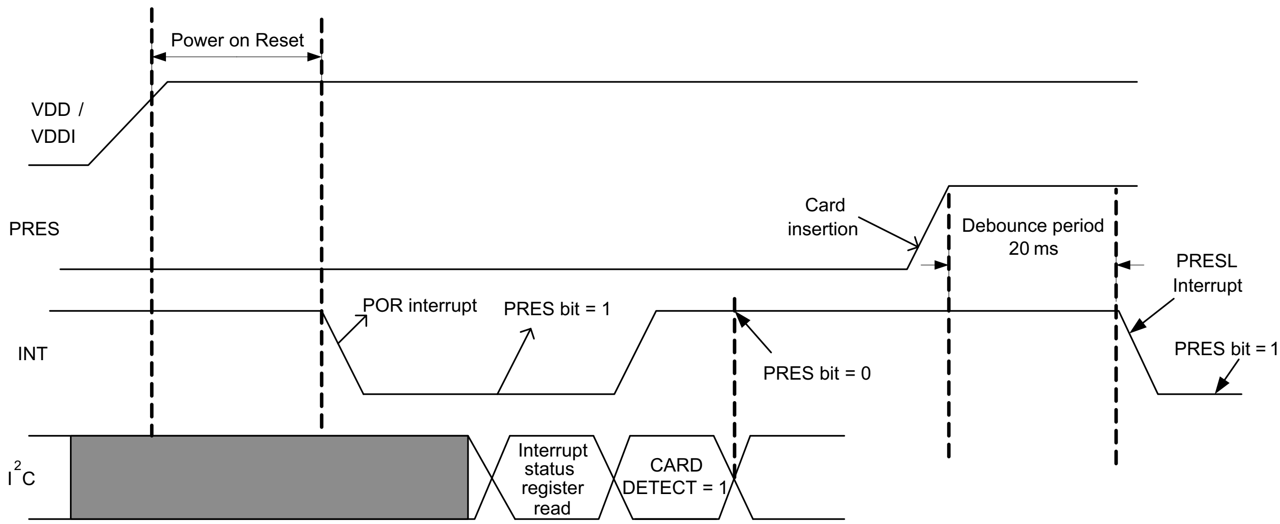


Figure 11. Device power up without card inserted in system - Low to High PRES Topology

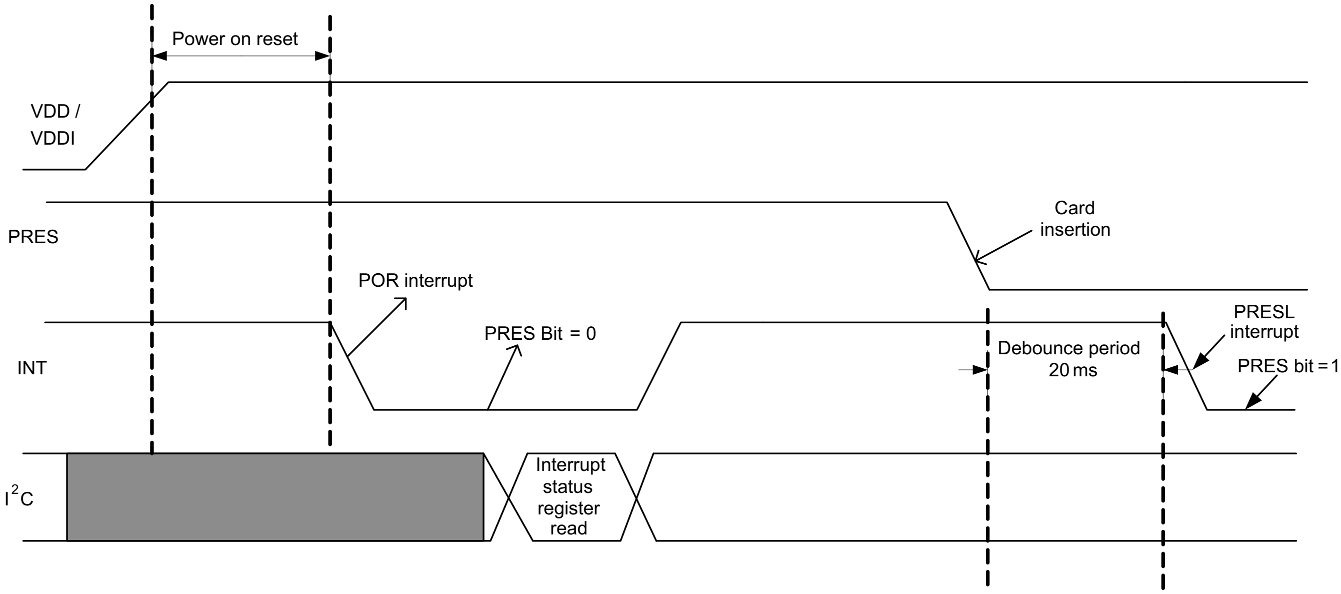


Figure 12. Device power up without card inserted in system - High to Low PRES Topology

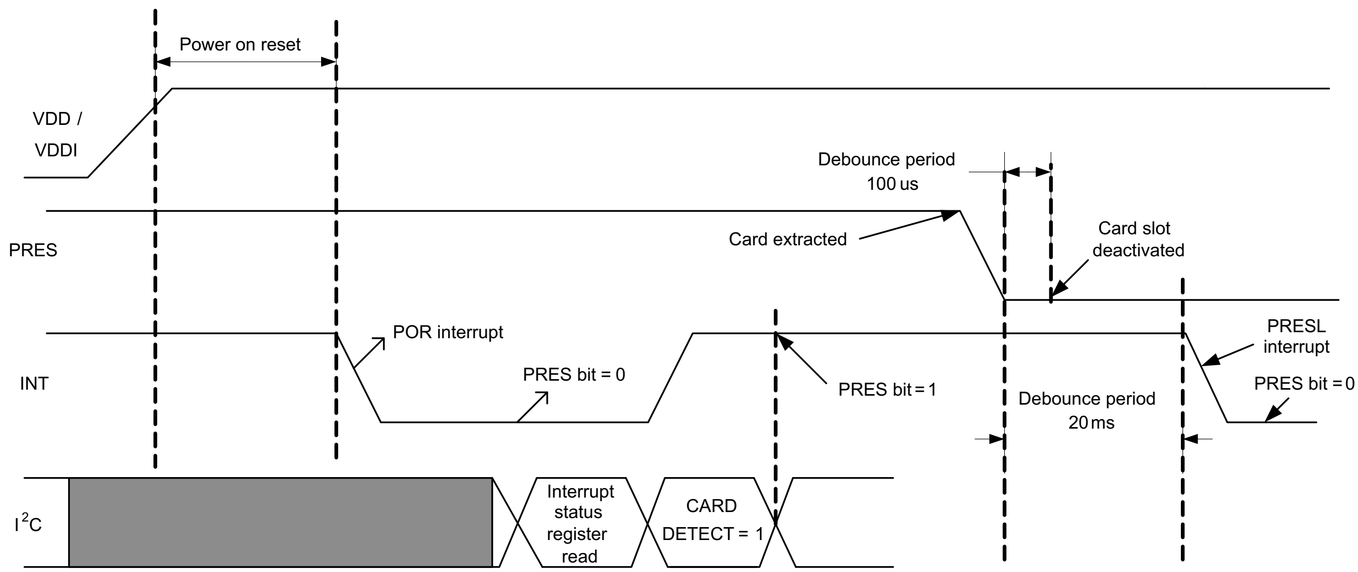


Figure 13. Device Power Up With Card Inserted in System - Low to High PRES Topology

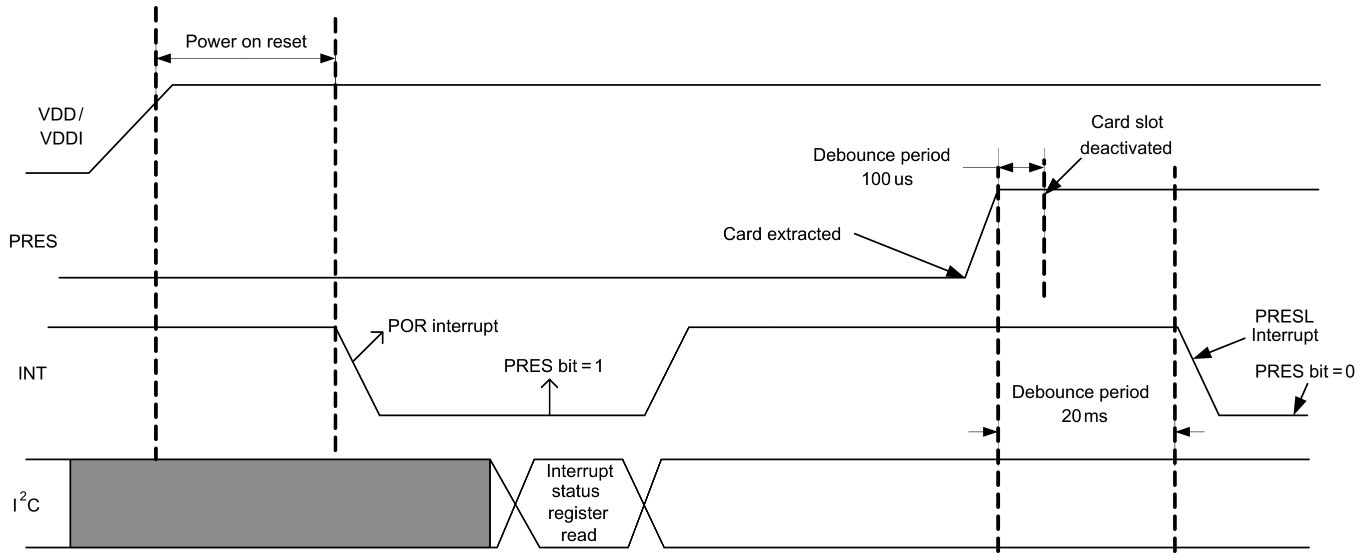


Figure 14. Device Power up with Card Inserted In System - High to Low PRES Topology

8.4.6 IO Operation

All card interfaces in the TCA5013 have an IO pin that connects data, to and from the microcontroller, with the smartcard. The TCA5013 provides automatic level translation from IOMC pin operating voltage (V_{DDI}) to the voltage at which the card is activated (V_{CC}).

8.4.6.1 IO Switching Control

The card interface IOs (IOUC, IOS1, IOS2 and IOS3) connect to the IOMC1 and IOMC2 through switches inside the TCA5013.

The IOUC pin is connected to IOMC1 through an SPST (single-pole single-throw) switch. The switch is controlled by the IO_EN_UC bit (Reg 0x01, Bit 5).The IO_EN_UC bit shall be set to 1 before card activation is started to ensure that the host processor is able to receive the ATR response from the smartcard. When an I2C command is received to open or close the switch, it is immediately implemented regardless of the status of IOUC or IOMC1 pins. It is therefore possible that the switch opens or closes during a rising or falling edge, which could result in a glitch on the IOUC or IOMC1 pins.

The IOS1, IOS2 and IOS3 all are connected to IOMC2 through a SP3T (single-pole triple-throw) switch, such that only one of the SAM interfaces can be connected to IOMC2 at any one time. The connection between the IOMC2 and the SAM card IO pins is controlled by IO_EN_S1 (Reg 0x11, Bit 5), IO_EN_S2 (Reg 0x21, Bit 5), IO_EN_S3 (Reg 0x31, Bit 5). If any one of the IO_EN bits is set for example, if SAM1 is initially connected by setting IO_EN of the SAM1 interface settings register to 1. When the IO_EN bit of the SAM2 or SAM3 is set to 1, the SAM1 gets disconnected and its IO_EN bit will be set to 0. Only one SAM can be connected to the IOUC2 at one time and whenever the IO_EN bit of any SAM interface settings register is set to 1, all other IO_EN bits get cleared (set to 0). Similar to the user card, the SAM IO mux can also result in a short duration pulse, if IOUC2 is not in the same state as the SAMs being switched to/from. Also when making the switch, the TCA5013 uses a break –before-make switch topology in order to avoid any glitches on the lines due to the switching itself.

8.4.6.2 IO Rise Time and Fall Time control

The rise time and fall time of the card interface IO pins can be controlled using the IO slew rate settings register (Reg 0x07 for user card and Reg 0x17 for SAMs). The EMV4.3 specification, has strict restrictions on signal perturbations (overshoot and undershoot during transition). Controlling the rise time and fall time of the signals can help to meet these requirements.

Table 6 shows the typical IO rise time for different register settings (based on a typical 30 pF load).

Table 6. IO Rise Time Register Settings

IO SLEW RATE SETTINGS REGISTER BIT [7:5]	TYPICAL RISE TIME (ns)
000	60
001	60
010	80
011	80
100	100
101	100
110	120
111	120

Table 7 shows the typical IO fall time for different register settings (based on a typical 30 pF load). It should also be noted that the output low logic level (V_{OL}) is affected by the fall time settings. As the fall time becomes slower (higher value of fall time) the V_{OL} will be higher. Therefore, it is recommended that the fastest fall time setting (smallest fall time value) for IO be used whenever possible. Table 7 also shows which settings are usable for the different V_{CC} voltages, without risk of violating the V_{OL} levels required by the EMV4.3 and ISO7816 specifications.

Table 7. IO Fall Time Register Settings

IO SLEW RATE SETTINGS REGISTER BIT [4:3]	TYPICAL FALL TIME (ns)	V_{CC} = 5 V	V_{CC} = 3 V	V_{CC} = 1.8 V
00	68	Usable	Not usable	Not usable
01	51	Usable	Not usable	Not usable
10	34	Usable	Usable	Not usable
11	17	Usable	Usable	Usable

8.4.6.3 Current Limiting on IO Pin

The card IO pins have a current limiting feature that prevents excess current from being drawn on them. The actual current limit can vary based on the fall time setting used for the IO pin, but it is always within the limits defined in *Electrical Characteristics—Fault Condition Detection*. When an external load tries to draw a current higher than the limit, the device responds by adjusting the V_{OH} or V_{OL} to limit the current. The device does not deactivate the card interface when over current limit of the IO pins are reached.

8.4.7 CLK Operation

All card interfaces in the TCA5013 have a CLK pin that provides a clock signal to the smartcard. The TCA5013 provides automatic level translation of the CLK signal from the CLKIN1/CLKIN2 operating voltage (V_{DDI}) to the voltage at which the card is activated (V_{CC}).

8.4.7.1 CLK Switching

The CLK output on each of the smartcard interfaces can be controlled by the corresponding clock settings register (Reg 0x02 for user card, Reg 0x12 for SAM1, Reg 0x22 for SAM2, Reg 0x32 for SAM3). The CLKIN1 pin is dedicated for the user card interface while The CLKIN2 is shared between the SAM interfaces. The clock settings register allows the CLK output to be configured in one of 4 different modes.

A. CLK 0 mode - The CLK output of the card interface is static low.
B. CLK 1 mode - The CLK output of the card interface is static high.
C. CLK div mode - The CLK output is a divided down frequency of the CLKIN1 or CLKIN2 frequency. Bit [4:2] of clock settings register defines the division ratio.
D. Internal CLK mode - The CLK output is at a fixed frequency (~1.2 MHz) based off the internal oscillator.

The allowable changes in CLK output can vary depending on the mode in which the interface has been activated. In asynchronous mode (see *Asynchronous Operating Mode*), The CLK output can be dynamically switched from one state to another. Table 8 shows the permitted frequency transitions on CLK pin in asynchronous mode. Any I²C command that attempts to switch the CLK frequency outside of these state transitions can result in the change not happening on the output or other unpredictable behavior that could cause device to lock up. If the device enters such a locked state, it can be reset by toggling SHDN pin.

Table 8. Permitted CLK Switching Operations in Asynchronous Mode

FROM	TO	
Internal CLK	CLK div	Permitted
Internal CLK	**CLK 0**	**Not Permitted**
Internal CLK	**CLK 1**	**Not Permitted**
CLK div	Internal CLK	Permitted
CLK div	CLK 0	Permitted
CLK div	CLK 1	Permitted
CLK 0	CLK div	Permitted
CLK 0	**Internal CLK**	**Not Permitted**
CLK 0	**CLK1**	**Not Permitted**
CLK 1	CLK div	Permitted
CLK 1	**Internal CLK**	**Not Permitted**
CLK 1	**CLK 0**	**Not Permitted**

When command sets the device in Internal clock mode or CLK 0 mode or CLK 1 mode, the division ratio is locked out, that is, when an I²C transaction that sets either one of the bits [7:5] of the card clock settings register to 1, the remaining bits in the register (bit [4:2]) will not not be updated. It is to be noted that an asynchronous activation cannot be performed with the internal clock. At the start of the asynchronous activation, if the internal CLK mode is selected in the clock settings register, then the device shall begin activation based on divide ratio defined by bit [4:2] of clock settings register. After the activation is completed, the CLK output will switch to Internal CLK mode. When switching to/from a CLK div mode from/to CLK 0 mode or CLK 1 mode, the device waits for the input clock (CLKIN1 or CLKIN2) phase to match the static level it will switch to/from and then makes the transition to ensure that no partial pulses or glitches are seen on the output clock. Similarly, when switching from one division ratio to another the change happens on the rising clock edges to ensure no glitch on the output. Figure 15 shows how the change in divide ratio is seen on the CLK pin.

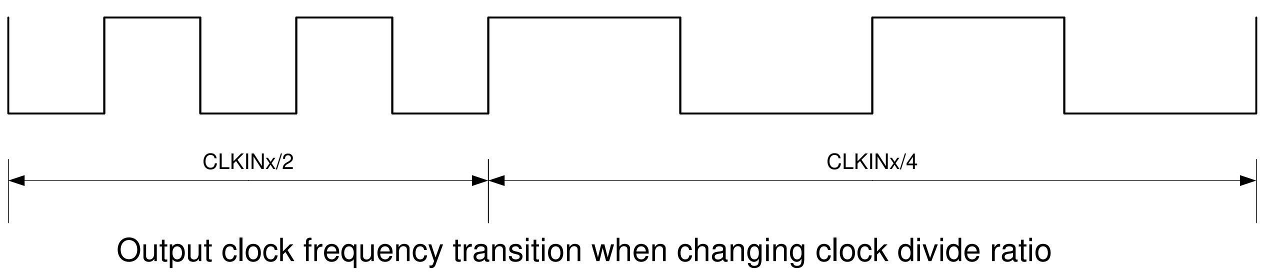


Figure 15. CLK Divide Ratio Change on Card CLK Output

When switching from CLK divide mode to the Internal CLK mode, the device waits for the edges of the internal and external clock to line up (fall within ~10 ns of each other) and makes the switch on that edge. If the external clock is close to an exact harmonic of 1.2 MHz, there could be a situation where the rising edges of the two clocks take very long (milliseconds or seconds) to line up and this would mean the frequency switch at the output would happen long after the I²C command to make the switch is issued. The CLKSW bit (bit [3]) in the card interface status register (Reg 0x01 for user card, Reg 0x11 for SAM1, Reg 0x21 for SAM2, Reg 0x31for SAM3) is set when the internal clock frequency is seen on the CLK pin.

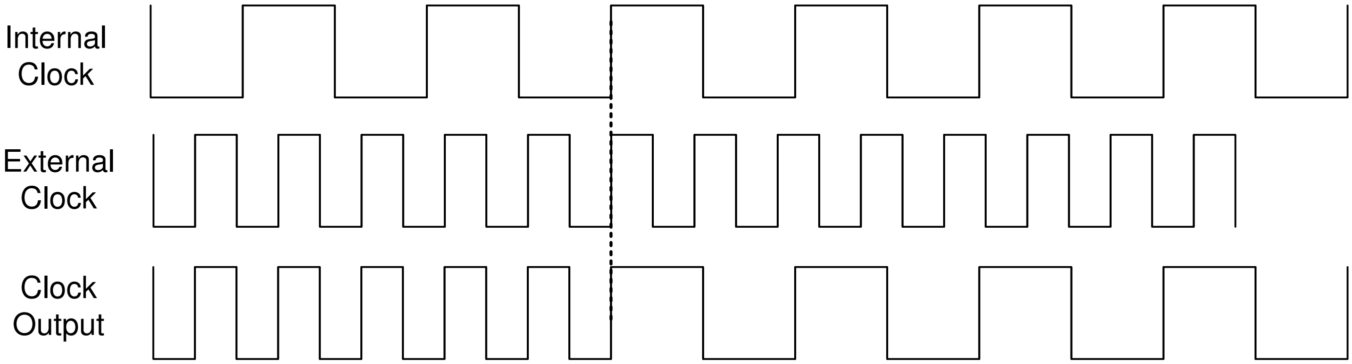


Figure 16. Output CLK Frequency Transition When Switching From External Clock to Internal Clock

In CLK divide mode, when CLKIN/2, CLKIN/4 or CLKIN/8 division ratios are used, the output duty cycle is not affected by the duty cycle of the input clock on CLKIN. When the CLKIN/1 and CLKIN/5 division ratios are used, the output clock duty cycle is a function of the CLKIN1/CLKIN2 duty cycle. For CLKIN/1 the output duty cycle will be equal to the input duty cycle. For CLKIN/5 the output CLK duty cycle is given by (n+2) / 5, where n is the duty cycle of the input clk; for example, if the input clk has a 40% duty cycle (n = 0.4) the CLKIN/5 output will have a (0.4+2) / 5 = 0.48 or 48% duty cycle. In addition to asynchronous mode, the user card interface can also operate in synchronous mode (see *Synchronous Type 1 Operating Mode* and *Synchronous Type 2 Operating Mode*).When in synchronous mode the user card CLK pin output is controlled by CLK_ENABLE_SYNC (bit [2], Reg 0x09) in addition to the clock settings register. Figure 17 shows a simplified logical representation of the user card clock muxing circuit.

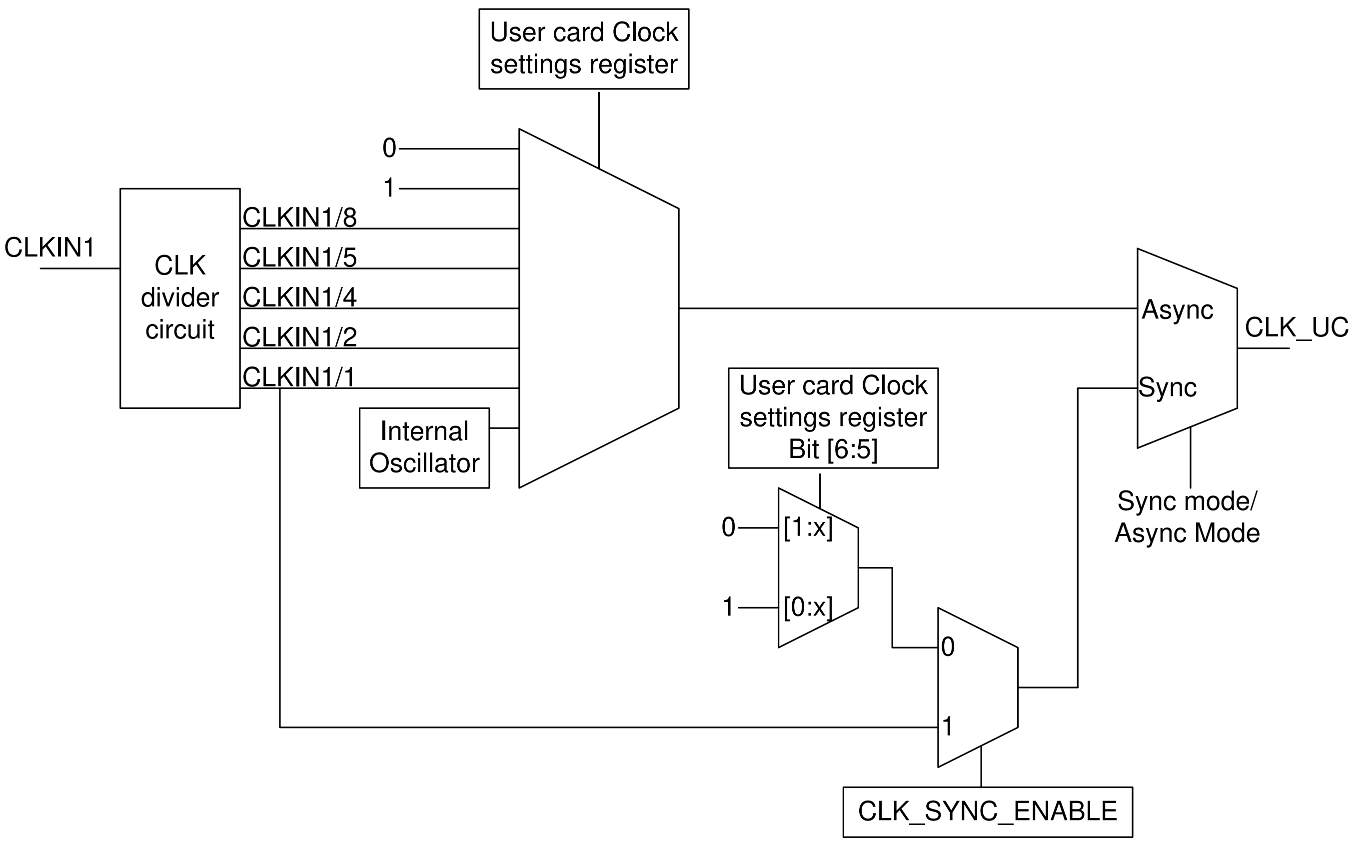


Figure 17. Clock Muxing Logic in Synchronous Mode

Unlike all the other bits that control the CLK, the CLK_ENABLE_SYNC can cause the CLK state to transition instantly. This means that when switching from a static level to a toggling CLK (or vice-versa), there can be partial pulses (glitches) on the CLK output when CLK_ENABLE_SYNC is switched. In sync mode, the CLK output can be switched directly from one static level to another, by using the CLK settings register (when CLK_SYNC_ENABLE = 0).

Table 9. Card CLK Truth Table in Synchronous Mode

CLK_ENABLE_SYNC	CARD CLOCK SETTINGS REGISTER						CARD CLK OUTPUT
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	
0	X	1	X	X	X	X	1
0	X	0	X	X	X	X	0
1	X	X	X	X	X	X	CLKIN1

8.4.7.2 CLK Rise Time and Fall Time Control

The clock slew rate setting register (Reg 0x08 for user card and Reg 0x18 for SAM) is used to control the rise and fall time of the CLK pin. Table 10 shows the rise and fall time corresponding to each register setting. The EMV4.3 specification, has strict restrictions on signal perturbations (overshoot and undershoot during transition). Controlling the rise time and fall time of the CLK signals can help to meet these requirements.

Table 10. CLK Rise and Fall Time Settings

CLOCK SLEW RATE SETTINGS REGISTER	TYPICAL RISE TIME and FALL RATE
0000	6
0001	7
0010	9
0011	11
0100	13
0101	14
0110	15
0111	16
1000	17
1001	18
1010	19
1011	20
1100	21
1101	22
1110	23
1111	25

8.4.7.3 Current Limiting On CLK Pin

The card CLK pins have a current limiting feature that prevents excess current from being drawn on them. When an external load tries to draw a current higher than the limit, the device responds by adjusting the V_{OH} or V_{OL} to limit the current. The device does not deactivate the card interface when over current limit of the CLK pins are reached.

8.4.8 RST Operation

The RST pin operation depends on the mode in which the card interface has been activated. For user card interface and all the SAM card interfaces, in asynchronous mode (see *Asynchronous Operating Mode*) the RST pin status is automatically controlled by the TCA5013 internal state machine.

In synchronous mode (*Synchronous Type 1 Operating Mode* and *Synchronous Type 2 Operating Mode*) the RST pin status is controlled by the TCA5013 internal state machine, until the activation sequence is complete. After activation is complete, the RST pin status is controlled by RST bit (bit [3]) in the user card synchronous mode settings register (Reg 0x09). This operation is described in further detail in *Synchronous Type 1 Operating Mode* and *Synchronous Type 2 Operating Mode*.

8.4.8.1 Current Limiting On RST

The card RST pins have a current limiting feature that prevents excess current from being drawn on them. When an external load tries to draw a current higher than the limit, the device responds by adjusting the V_{OH} or V_{OL} to limit the current. The device does not deactivate the card interface when over current limit of the RST pins are reached.

8.4.9 Interrupt Operation

The INT pin is an open drain active low output pin that needs to be pulled up to V_{DDI} with an external pull-up resistor. The pull-up resistor shall be sized such that the rise time of the INT pin is < 100 µs. This is important since slower rise time could cause *POR Interrupt* to not be detected by the processor during TCA5013 startup. Generally speaking faster rise times on the INT line will reduce the chances of missing interrupts. There various interrupt events in the TCA5013 that can cause the INT pin to be asserted low. These interrupt events are described in the below sections.

8.4.9.1 Card Insertion And Removal

When card insertion or removal is detected on the user card interface (see *User Card Insertion / Removal Detection*) the INT_UC bit (bit[7]) of interrupt status register (Reg 0x41) and the PRESL_UC bit (bit[2]) of User card interface status register (Reg 0x00) are both set to 1 and the INT pin is asserted low. INT_UC is cleared and the INT pin is released when the interrupt status register is read. PRESL_UC is cleared only when the user card interface status register is read.

8.4.9.2 Over Current Fault

When the current drawn on the VCC pin of any of the card interfaces exceeds the over current limit (see *Electrical Characteristics—Fault Condition Detection*) the PROT bit (bit[4]) of the card interface status register (Reg 0x00 for user card, Reg 0x10 for SAM1, Reg 0x20 for SAM2 and Reg 0x30 for SAM3) is set. The interrupt bit corresponding to the card interface in the interrupt status register (Reg 0x41) is also set and the INT pin is asserted low. The interrupt bit is cleared and the INT pin is released, when the interrupt status register is read. The PROT bit is cleared only when the corresponding card interface status register is read.

8.4.9.3 Supervisor Fault

When the voltage on the VDD pin falls below the V_{DDTH} the INT_SUPL bit (bit[2] of Reg 0x41) and The STAT_SUPL bit (bit[1], Reg 0x10) are both set to 1 and the INT pin is asserted low. The INT_SUPL bit is cleared and the INT pin is released when the interrupt status register is read. The STAT_SUPL bit clears when the fault condition goes away, that is, $V_{DD} > V_{DDTH}$

8.4.9.4 Over Temperature Fault

When the die temperature exceeds a safe operating temperature (typ. 125°C) INT_OTP bit (bit[3], Reg 0x41) and The STAT_OTP bit (bit[2], Reg 0x10) are both set to 1 and the INT pin is asserted low. The INT_OTP bit is cleared and the INT pin is released when the interrupt status register is read. The STAT_OTP clears when the fault condition goes away.

8.4.9.5 EARLY Fault

In *Asynchronous Operating Mode* when the ATR response from the smartcard is received before the 'ATR valid window' (see Figure 6) the EARLY bit (bit [6]) of card interface status register (Reg 0x00 for user card, Reg 0x10 for SAM1, Reg 0x20 for SAM2 and Reg 0x30 for SAM3) is set and the INT pin is asserted low. The interrupt bit corresponding to the card interface in the interrupt status register (Reg 0x41) is also set. The interrupt bit is cleared and the INT pin is released, when the interrupt status register is read. The EARLY bit is cleared only when the corresponding card interface status register is read.

8.4.9.6 MUTE Fault

In *Asynchronous Operating Mode* when the ATR response from the smartcard is received after the 'ATR valid window' (refer to Figure 6) the MUTE bit (bit [5]) of card interface status register (Reg 0x00 for user card, Reg 0x10 for SAM1, Reg 0x20 for SAM2 and Reg 0x30 for SAM3) is set and the INT pin is asserted low. The interrupt bit corresponding to the card interface in the interrupt status register (Reg 0x41) is also set. The interrupt bit is cleared and the INT pin is released, when the interrupt status register is read. The EARLY bit is cleared only when the corresponding card interface status register is read.

8.4.9.7 Synchronous Activation Complete

In synchronous activation mode (see *Synchronous Type 1 Operating Mode* and *Synchronous Type 2 Operating Mode*) once the activation sequence is completed, the INT_SYNC_COMPLETE bit (bit[1]) of interrupt status register (Reg 0x41) is set and the INT pin is asserted low. The INT_SYNC_COMPLETE bit is cleared and the INT pin is released when the interrupt status registers is read.

8.4.9.8 V_{CC} Ramp Fault

During any activation sequence if the V_{CC} voltage fails to ramp to programmed value within 5 ms (typ), then the VCC_FAIL bit (bit[0]) of card interface status register (Reg 0x00 for user card, Reg 0x10 for SAM1, Reg 0x20 for SAM2 and Reg 0x30 for SAM3) is set and the INT pin is asserted low. The interrupt bit corresponding to the card interface in the interrupt status register (Reg 0x41) is also set. The interrupt bit is cleared and the INT pin is released, when the interrupt status register is read. The VCC_FAIL bit is cleared only when the corresponding card interface status register is read.

8.4.9.9 GPIO Input State Transition

When there is a state change on a GPIO pin configured as an input the INT_GPIO bit (bit[0]) of the interrupt status register (Reg 0x41) is set and the INT pin is asserted low. The INT_GPIO bit is cleared and the INT pin is released when the interrupt status register is read.

8.4.9.10 POR Interrupt

Whenever the device comes out of *Power Off Mode* or *Shutdown Mode* it goes through a power-on-reset (POR). Once the device internal power up sequence is completed the INT pin is asserted low without any of the bits in the interrupt status register (Reg 0x41) being set. Once the interrupt status register is read, the INT pin is released. When the device is coming out of shutdown mode of power off mode, none of the device functions will be available until the POR interrupt is asserted.

8.4.10 Power Management

The TCA5013 has power management features that enable the device to generate the appropriate card activation voltages and monitor the device power supplies for safe and secure system operation.

8.4.10.1 Voltage Supervisor

The TCA5013 has internal voltage supervisors that monitor V_{DD} and V_{DDI} voltages. When V_{DD} falls below V_{DDTH} all card interfaces are deactivated and the supervisor fault (see *Supervisor Fault*) is asserted.

The V_{DDI} supervisor monitors the voltage on the V_{DDI} pin. When V_{DDI} falls below V_{DDITH} all card interfaces are deactivated and the device enters power off mode (see *Power Off Mode*). When V_{DDI} falls below V_{DDITH} the supervisor fault is not asserted.

It is possible that the supervisor fault is asserted during power up If V_{DDI} ramps before V_{DD} (depending on the V_{DD} ramp rate). If V_{DD} is ramped and stable before V_{DDI} is ramped, the supervisor fault will not be asserted. Figure 18 shows the operation of voltage supervisor for various combinations of V_{DD} and V_{DDI}.

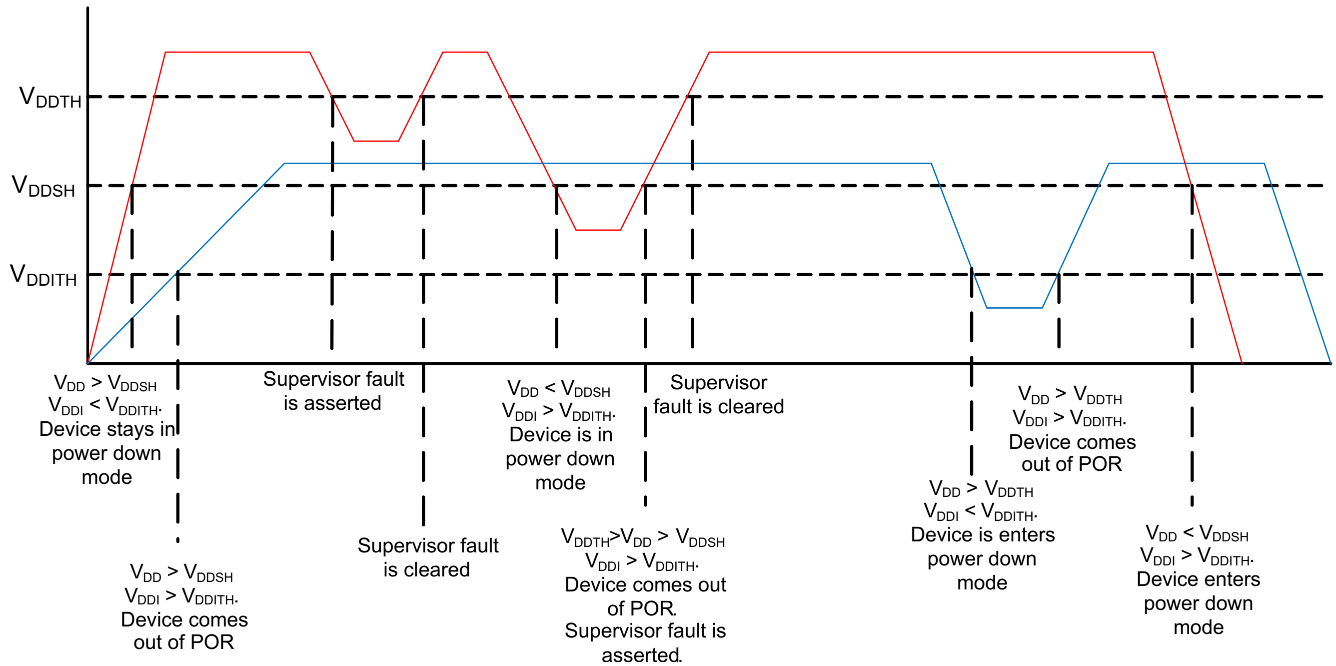


Figure 18. Voltage Supervisor Operation

8.4.10.2 DC-DC Boost

TCA5013 contains a DC-DC boost circuit that can step up V_{DD} voltage to generate the required card V_{CC}. The boost requires an external diode (D_{VUP}) as a high side switch. It also requires an external inductor (L_{VDD}) in series with the VDD pin. The normal switching frequency of the boost is ~2.4 Mhz. The boost is rated for 180 mA. This implies that the sum of the current drawn on individual card VCC pins cannot exceed 180 mA. If exceeded it could result in the card V_{CC} falling out of the operating range defined in *Electrical Characteristics—Power Supply and ESD*.

The DC_DC bit (Reg 0x42; Bit [7]) can be used to disable the DC-DC boost circuit. The DC-DC boost should be disabled only in systems where the supply is always guaranteed to be at least 0.25V greater than maximum card V_{CC} supported on that system, for example, if 5 V cards need to be supported in a system the DC-DC boost can be disabled if V_{DD} is guaranteed to be above 5.25 V. In systems where DC-DC is not used, the VDD pin shall be shorted to VUP pin. The LX pin should shorted to GNDP. Shorting to GNDP is recommended to prevent switching noise from impacting rest of system. Note that LX shall not be connected to anything other than GNDP in order to prevent excess power loss and/or damage to the part. If DC-DC boost is disabled and the V_{DD} is not sufficient to activate a card interface at the voltage set by SET_VCC (Reg 0x01, Reg 0x11, Reg 0x21, Reg 0x31; bit [7:6]), it will result in a V_{CC} ramp fault (See *V_{CC} Ramp Fault*).

The DC-DC boost is always disabled in standby mode (See *Standby Mode*). When a card activation command is received, the DC-DC boost circuit is enabled by the digital core. The boost output voltage depends on voltage at which the card needs to be activated, that is, based on SET_VCC (Reg 0x01, Reg 0x11, Reg 0x21, Reg 0x31; bit [7:6]). For 1.8-V and 3-V card activation, the boost output voltage will be ~3.5 V. For 5-V card activations the boost output voltage will be ~5.5 V. In a scenario where a 3 V or 1.8 V card is active and an I^2C command is received to activate another card with 5 V, the boost output voltage will go up to 5.5 V and the card LDOs (See *LDOs and Load Transient Response*) on the already active card interface, will keep the card V_{CC} within regulation.

Under light load conditions, the DC-DC boost can enter pulse skipping mode in order to improve efficiency. In pulse skipping mode, the switching frequency is not constant and will be much lower than the normal switching frequency of 2.4 MHz.

8.4.10.3 LDOs and Load Transient Response

The TCA5013 has an internal LDO that generates a stable supply for the internal circuits. The input to the internal LDO is V_{DD}. The output of the internal LDO is connected to the LDOCAP pin. A 1 uF decoupling capacitor shall be connected to the LDOCAP pin to ensure proper device operation. The internal LDO voltage is typically 2.65 V but can be lower if V_{DD} is not sufficient.

In addition to the internal LDO, the TCA5013 has a dedicated LDO per card interface to generate the V_{CC} for that card interface (here on forth, these LDOs are referred to as card LDOs). The card LDOs provide the power supply for smartcard operation. During the normal operation of the smartcard, the LDO output is subject to load transients. The EMV4.3 standard defines a load transient envelope shown in Figure 19. The card LDOs are able to handle these transients, while keeping V_{CC} within limits defined in *Electrical Characteristics—Card V_{CC}*. An external 200 nF capacitor shall be connected to their card VCC pins (VCCUC, VCCCS1, VCCS2, VCCS3) to ensure proper load transient response by the card LDOs.

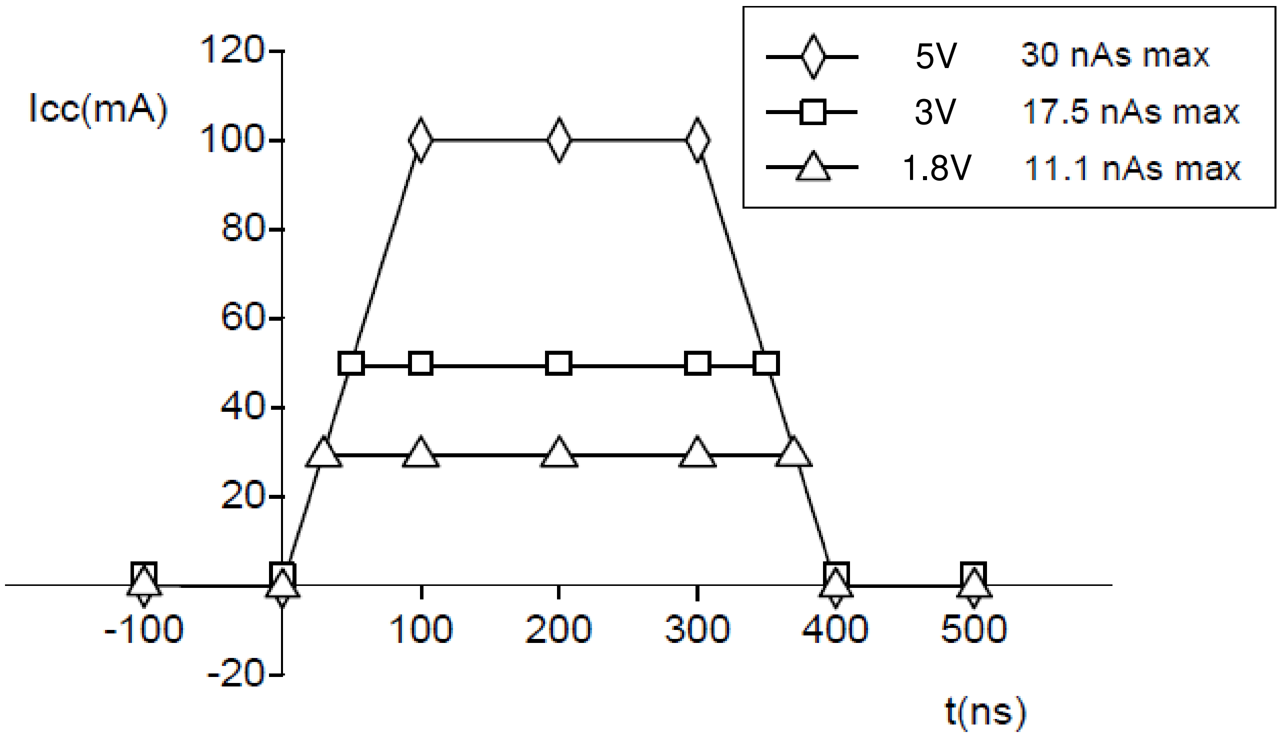


Figure 19. Load Transients defined by EMV4.3

The card LDOs are enabled only when the card interface is activated (see *Active Mode*). The output voltage is determined by the card interface settings registers (Reg 0x01, Reg 0x11, Reg 0x21, Reg 0x31). At the start of the activation sequence, the card LDO is enabled and starts to ramp to the voltage defined in the corresponding card interface settings register. Once the LDO has been enabled, any changes to the card interface settings registers will not have any effect on the LDO output voltage. The card also LDOs also have short circuit protection. When the current drawn exceeds ~150 mA (typ.) the LDO automatically shuts down and the card interface is deactivated (see *Deactivation Sequence*).

8.5 Programming

8.5.1 I²C Interface Operation

The device has a standard bidirectional I²C that is used by the microcontroller to access the device *Register Maps* that is used to configure the device and read the status of various fault flags in the device. The interface consists of the serial clock (SCL) and serial data (SDA) lines and is capable of MHz operation. Both SDA and SCL must be connected to V_{DDI} through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the I²C lines (for further details refer to I²C standard specification).

I²C communication with this device is initiated by a master (microcontroller) sending a START condition, a high-to-low transition on the SDA input/output, while the SCL input is high. Only one data bit is transferred during each clock pulse. A STOP condition is a low-to-high transition on the SDA input/output while the SCL input is high. A STOP condition shall be sent by the master to indicate to the slave that a particular transaction has been completed. The data on the SDA line must remain stable during the high phase of the clock period, as changes in the data line when SCL is high are interpreted as control commands (START or STOP).

Figure 20 shows the definition of an I²C START condition and Figure 21 shows timing of a bit transfer on the I²C bus. I²C

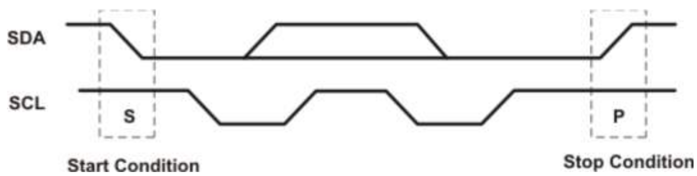


Figure 20. Definition of Start and Stop Conditions

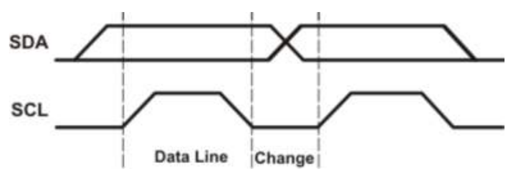


Figure 21. Bit Transfer

Any number of data bytes can be transferred from the master to slave (TCA5013) between the START and STOP conditions. Each byte of eight bits is followed by one ACK bit. The master must release the SDA line before the slave can send an ACK bit. To send an ACK bit the slave pulls down the SDA line during the low phase of ACK-related clock period, so that the SDA line is stable low during the high phase of the ACK-related clock period. When the slave is addressed, it generates an ACK after each byte is received. The master is not required to generate an ACK after each byte that it receives from the slave transmitter

Figure 22 shows the timing diagram for generation of the ACK bit on the I²C interface of the TCA5013

Programming (continued)

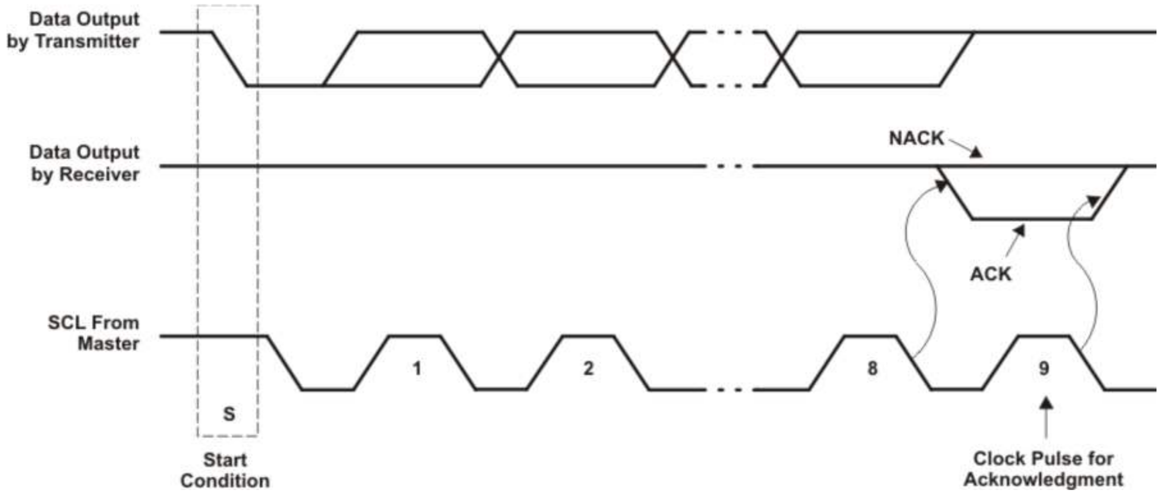
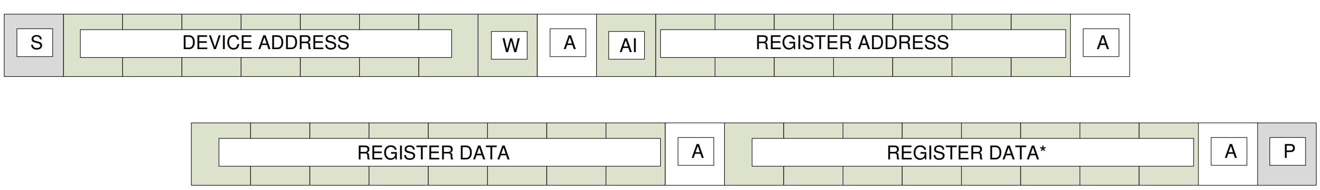


Figure 22. Acknowledgment on I²C Bus

8.5.1.1 I²C Read and Write Procedures

Following the successful acknowledgment of the I²C address byte, the bus master shall send one register address byte indicating the address of the register on which the read or write operation needs to be performed. This register address is stored in an internal register and used by the device for subsequent read/write to the device. After the device address is acknowledged by the slave, all register addresses will be acknowledged even if an actual register is not defined for that address

The TCA5013 supports an auto increment feature by which multiple bytes can be written to consecutive registers without requiring the master to send the device address and register address for each data byte. Auto increment is enabled by setting the MSB of the register address to a 1 (see Figure 23). If auto increment is used to write the entire register map, the gaps in the register address map need to be written with dummy bytes. If auto increment is used to read the entire register map then data read from gaps in the register map will be 8'hFF



2nd and subsequent bytes of Register data are written to next register if Auto increment is enabled (AI=1)
2nd and subsequent bytes of register data are ignored if auto increment is disabled (AI=0).

SDA line is controlled by Master **SDA line is controlled by Slave**

Figure 23. I²C Write Procedure

Programming (continued)

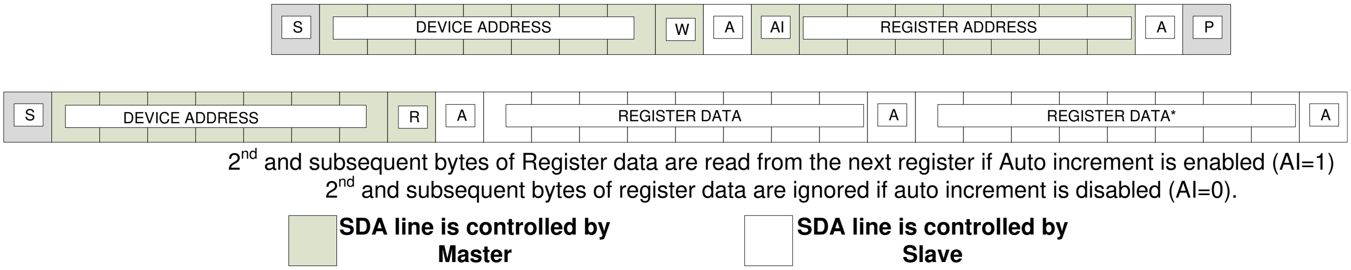


Figure 24. I²C Read Procedure

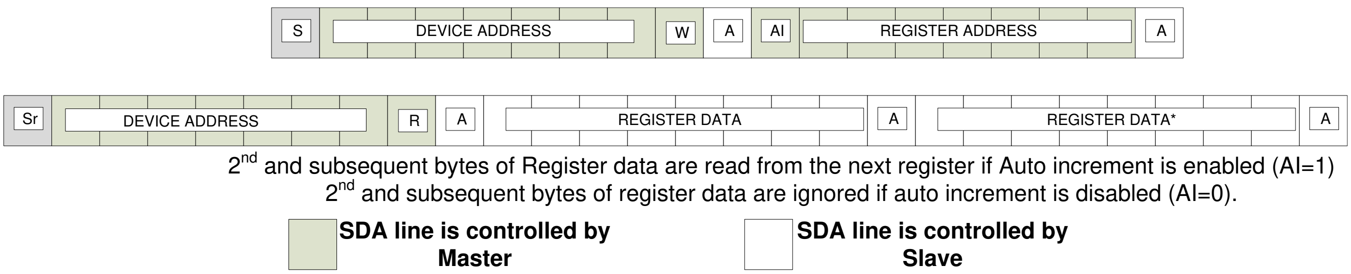


Figure 25. I²C Read Procedure with Repeated Start

8.5.1.2 I²C Address Configuration

The I²C address of the TCA5013 can be configured using the A0. The A0 pin shall be connected to VDDI or GND to select one of the addresses, as shown in Table 11. The last bit in the address byte defines the operation (read or write)

Table 11. TCA5013 I²C address selection

A0	SLAVE ADDRESS								I²C BUS SLAVE ADDRESS
	B7	B6	B5	B4	B3	B2	B1	B0	
GND	0	1	1	1	0	0	1	W/R	Write - 72(h), Read – 73(h)
VDDI	0	1	1	1	1	1	0	W/R	Write - 7C(h), Read – 7D(h)

8.6 Register Maps

Memory Map

Address (Hex)	Register Description	Type	Reset (Hex)	Reset (Binary)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	User Card Interface Status	R	00	0000 0000	ACTIVE_UC	EARLY_UC	MUTE_UC	PROT_UC	CLKSW_UC	PRESL_UC	PRES_UC	VCC_FAIL_UC
01	User Card Interface Settings	R/W	60	0110 0000	SET_VCC_UC		IO_EN_UC		WARM_UC	CARD_DETECT_UC		START_ASYNC_UC
02	User Card Clock Settings	R/W	0C	0000 1100	INTERN_CLK_UC	CLK0_UC	CLK1_UC	CLK_DIV_UC				
03	Asynchronous Mode ATR EARLY Counter MSB for User Card	R/W	AA	1010 1010	EARLY_COUNT_HI_UC							
04	Asynchronous Mode ATR EARLY Counter LSB for User Card	R/W	00	0000 0000	EARLY_COUNT_LO_UC							
05	Asynchronous Mode ATR MUTE Counter MSB for User Card	R/W	A4	1010 0100	MUTE_COUNT_HI_UC							
06	Asynchronous Mode ATR MUTE Counter LSB for User Card	R/W	74	0111 0100	MUTE_COUNT_LO_UC							
07	User Card IO Slew Rate Settings	R/W	80	1000 0000	IO_TR_UC			IO_TF_UC				
08	User Card Clock Slew Rate Settings	R/W	A0	1010 0000	CLK_SR_UC							
09	User Card Synchronous Mode Settings	R/W	76	0111 0110	CARD_TYPE	ACTIVATION_TYPE	C4	C8	RST	CLK_ENABLE_SYNC	EDGE	START_SYNC
0A	Synchronous Mode ATR Byte 1	R	00	0000 0000	BYTE1_UC							
0B	Synchronous Mode ATR Byte 2	R	00	0000 0000	BYTE2_UC							
0C	Synchronous Mode ATR Byte 3	R	00	0000 0000	BYTE3_UC							
0D	Synchronous Mode ATR Byte 4	R	00	0000 0000	BYTE4_UC							
10	SAM1 Interface Status	R	00	0000 0000	ACTIVE_SAM1	EARLY_SAM1	MUTE_SAM1	PROT_SAM1	CLKSW_SAM1	STAT_OTP	STAT_SUPL	VCC_FAIL_SAM1
11	SAM1 Interface Settings	R/W	40	0100 0000	SET_VCC_SAM1		IO_EN_SAM1		WARM_SAM1			START_ASYNC_SAM1
12	SAM1 Clock Settings	R/W	0C	0000 1100	INTERN_CLK_SAM1	CLK0_SAM1	CLK1_SAM1	CLK_DIV_SAM1				
13	Asynchronous Mode ATR EARLY Counter MSB for SAM1	R/W	AA	1010 1010	EARLY_COUNT_HI_SAM1							
14	Asynchronous Mode ATR EARLY Counter LSB for SAM1	R/W	00	0000 0000	EARLY_COUNT_LO_SAM1							
15	Asynchronous Mode ATR MUTE Counter MSB for SAM1	R/W	A4	1010 0100	MUTE_COUNT_HI_SAM1							
16	Asynchronous Mode ATR MUTE Counter LSB for SAM1	R/W	74	0111 0100	MUTE_COUNT_LO_SAM1							
17	SAM IO Slew Rate Settings	R/W	80	1000 0000	IO_TR_SAM			IO_TF_SAM				
18	SAM Clock Slew Rate Settings	R/W	A0	1010 0000	CLK_SR_SAM							

Register Maps (continued)

Memory Map (continued)

Address (Hex)	Register Description	Type	Reset (Hex)	Reset (Binary)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20	SAM2 Interface Status	R	00	0000 0000	ACTIVE_SAM2	EARLY_SAM2	MUTE_SAM2	PROT_SAM2	CLKSW_SAM2			VCC_FAIL_SAM2
21	SAM2 Interface Settings	R/W	40	0100 0000	SET_VCC_SAM2		IO_EN_SAM2		WARM_SAM2			START_ASYNC_SAM2
22	SAM2 Clock Settings	R/W	0C	0000 1100	INTERN_CLK_SAM2	CLK0_SAM2	CLK1_SAM2	CLK_DIV_SAM2				
23	Asynchronous Mode ATR EARLY Counter MSB for SAM2	R/W	AA	1010 1010	EARLY_COUNT_HI_SAM2							
24	Asynchronous Mode ATR EARLY Counter LSB for SAM2	R/W	00	0000 0000	EARLY_COUNT_LO_SAM2							
25	Asynchronous Mode ATR MUTE Counter MSB for SAM2	R/W	A4	1010 0100	MUTE_COUNT_HI_SAM2							
26	Asynchronous Mode ATR MUTE Counter LSB for SAM2	R/W	74	0111 0100	MUTE_COUNT_LO_SAM2							
30	SAM3 Interface Status	R	00	0000 0000	ACTIVE_SAM3	EARLY_SAM3	MUTE_SAM3	PROT_SAM3	CLKSW_SAM3			VCC_FAIL_SAM3
31	SAM3 Interface Settings	R/W	40	0100 0000	SET_VCC_SAM3		IO_EN_SAM3		WARM_SAM3			START_ASYNC_SAM3
32	SAM3 Clock Settings	R/W	0C	0000 1100	INTERN_CLK_SAM3	CLK0_SAM3	CLK1_SAM3	CLK_DIV_SAM3				
33	Asynchronous Mode ATR EARLY Counter MSB for SAM3	R/W	AA	1010 1010	EARLY_COUNT_HI_SAM3							
34	Asynchronous Mode ATR EARLY Counter LSB for SAM3	R/W	00	0000 0000	EARLY_COUNT_LO_SAM3							
35	Asynchronous Mode ATR MUTE Counter MSB for SAM3	R/W	A4	1010 0100	MUTE_COUNT_HI_SAM3							
36	Asynchronous Mode ATR MUTE Counter LSB for SAM3	R/W	74	0111 0100	MUTE_COUNT_LO_SAM3							
40	Product Version	R	00	0000 0000	PRODUCT_VER							
41	Interrupt Status Register	R	00	0000 0000	INT_UC	INT_SAM1	INT_SAM2	INT_SAM3	INT_OTP	INT_SUPL	INT_SYNC_COMPLETE	INT_GPIO
42	Device Settings	R/W	80	1000 0000	DC_DC		GPIO4	GPIO3	GPIO2	GPIO1		
43	GPIO Settings	R/W	xF	xxxx 1111	GPIO4_INPUT	GPIO3_INPUT	GPIO2_INPUT	GPIO1_INPUT	GPIO4_OUTPUT	GPIO3_OUTPUT	GPIO2_OUTPUT	GPIO1_OUTPUT
44	User Card Interrupt Mask Register	R/W	00	0000 0000	EARLY_UC_MASK	MUTE_UC_MASK	PROT_UC_MASK	SYNC_COMPLETE_MASK	OTP_MASK	SUPL_MASK	GPIO_INT_MASK	PRESL_INT_MASK
45	SAM1 and SAM2 Interrupt Mask Register	R/W	00	0000 0000	EARLY_SAM1_MASK	MUTE_SAM1_MASK	PROT_SAM1_MASK	EARLY_SAM2_MASK	MUTE_SAM2_MASK	PROT_SAM2_MASK	VCC_FAIL_SAM_MASK	VCC_FAIL_UC_MASK
46	SAM3 and GPIO Interrupt Mask Register	R/W	00	0000 0000	EARLY_SAM3_MASK	MUTE_SAM3_MASK	PROT_SAM3_MASK	GPIO4_INT_MASK	GPIO3_INT_MASK	GPIO2_INT_MASK	GPIO1_INT_MASK	

Table 12.

REGISTER ADDRESS	DESCRIPTION	FIELD NAME	BIT	R/W	DEFAULT
0x00	**User Card Interface Status**				
0x00	1: Card interface is active (V_{CC} is ramped and stable) 0: Card interface is inactive	ACTIVE_UC	7	R	1'b0
0x00	1: Indicates card ATR was received before the ATR valid window. INT_UC bit is set in interrupt register. Bit is cleared when the register is read	EARLY_UC	6	R	1'b0
0x00	1: Indicates card ATR was not received within the ATR valid window. INT_UC bit is set in interrupt register. Bit is cleared when the register is read.	MUTE_UC	5	R	1'b0
0x00	1: Indicates over current condition on the card interface. INT_UC bit is set in interrupt register. Bit clears when the register is read	PROT_UC	4	R	1'b0
0x00	1: Indicates the card interface is in internal CLK mode i.e frequency on CLK pin is ~1.2 Mhz 0: Indicates the card interface is not in internal clock mode.	CLKSW_UC	3	R	1'b0
0x00	1: indicates the card has been inserted or extracted. INT_UC bit is set in interrupt register. Bit is cleared when the register is read	PRESL_UC	2	R	1'b0
0x00	1: indicates a card is present 0: indicates a card is not present	PRES_UC	1	R	1'b0
0x00	1: indicates V_{CC} ramp fault on card interface. INT_UC bit is set in interrupt register. Bit is cleared when register is read	VCC_FAIL_UC	0	R	1'b0

Table 13.

REGISTER ADDRESS	DESCRIPTION	FIELD NAME	BIT	R/W	DEFAULT
0x01	**User Card Interface Settings**				
0x01	00 : set V_{CC} to 1.8 V 01 : set V_{CC} to 1.8 V 10 : set V_{CC} to 3 V 11 : set V_{CC} to 5 V	SET_VCC_UC	[7:6]	R/W	2'b01
0x01	1: IOMC1 is connected IOUC 0: IOMC1 is disconnected from IOUC	IO_EN_UC	5	R/W	1'b1
0x01	1: Warm reset sequence is started on user card interface Bit is clears when warm reset sequence starts. Bit is ignored if card interface is in synchronous type 1 operating mode, synchronous type 2 operating mode or manual operating mode.	WARM_UC	3	R/W	1'b0
0x01	1 :Low to high transition on PRES pin indicates card insertion 0 : High to low transition on PRES pin indicates card insertion	CARD_DETECT_UC	2	R/W	1'b0
0x01	1: Starts asynchronous activation sequence 0: Starts deactivation sequence Bit clears when automatic deactivation occurs Bit is ignored if card interface is in synchronous type 1 operating mode, synchronous type 2 operating mode or manual operating mode.	START_ASYNC_UC	0	R/W	1'b0

Table 14.

REGISTER ADDRESS	DESCRIPTION	FIELD NAME	BIT	R/W	DEFAULT
0x02	**User Card Clock Settings**				
0x02	**In asynchronous operating mode (START_ASYNC=1)** 1: CLKUC is set to ~1.2 MHz 0: CLKUC is set by Bit[6] or Bit[5] or Bit[4:2] **In synchronous operating mode (START_SYNC=1)** Bit is ignored in Sync mode	INTERN_CLK_UC	7	R/W	1'b0
0x02	**In asynchronous operating mode (START_ASYNC=1)** 1: CLKUC is set to 0 0: CLKUC is set by Bit[5] or Bit[4:2] **In synchronous operating mode (START_SYNC=1)** 1: CLKUC is set to 0 0: CLKUC is set by Bit5.	CLK0_UC	6	R/W	1'b0
0x02	**In asynchronous operating mode (START_ASYNC=1)** 1: CLKUC is set to 1 0: CLKUC is set by Bit[4:2] **In synchronous operating mode (START_SYNC=1)** **Usable only is CLK_ENABLE_SYNC=0** 1: CLKUC is set to 1 0: CLKUC is set to 1	CLK1_UC	5	R/W	1'b0
0x02	**In asynchronous operating mode (START_ASYNC=1)** 000: CLKUC frequency = CLKIN1 001: CLKUC frequency = CLKIN1/2. 010: CLKUC frequency = CLKIN1/4. 011: CLKUC frequency = CLKIN1/5. 100: CLKUC frequency = CLKIN1/8. 101: CLKUC frequency = CLKIN1/8. 110: CLKUC frequency = CLKIN1/8. 111: CLKUC frequency = CLKIN1/8. **In synchronous operating mode (START_SYNC=1)** **Usable only is CLK_ENABLE_SYNC=1** [111:000] : CLKUC = CLKIN1	CLK_DIV_UC	[4:2]	R/W	3'b011
0x03	**Asynchronous Mode ATR EARLY Counter MSB for User Card**				
0x03	MSB (8-bits) of programmable 10-bit clock counter value.	EARLY_COUNT_HI_UC	[7:0]	R/W	8'b10101010
0x04	**Asynchronous Mode ATR EARLY Counter LSB for User Card**				
0x04	LSB (2-bits) of programmable 10-bit clock counter value.	EARLY_COUNT_LO_UC	[7:6]	R/W	2'b00
0x05	**Asynchronous Mode ATR MUTE Counter MSB for User Card**				
0x05	MSB (8-bits) of programmable 16-Bit clock counter value.	MUTE_COUNT_HI_UC	[7:0]	R/W	8'b10100100
0x06	**Asynchronous Mode ATR MUTE Counter LSB for User Card**				
0x06	LSB (8-bits) of programmable 16-Bit clock counter value.	MUTE_COUNT_LO_UC	[7:0]	R/W	8'b01110100
0x07	**User Card IO Slew Rate Settings**				
0x07	3 Bit value defining the rise time of IOUC	IO_TR_UC	[7:5]	R/W	3'b100
0x07	2 Bit value defining the fall time of IOUC	IO_TF_UC	[4:3]	R/W	2'b00
0x08	**User Card Clock Slew Rate Settings**				
0x08	4 Bit value defining the rise time and fall time of the CLKUC	CLK_SR_UC	[7:4]	R/W	4'b1010

Table 15.

REGISTER ADDRESS	DESCRIPTION	FIELD NAME	BIT	R/W	DEFAULT
0x09	**User Card Synchronous Mode Settings**				
0x09	0: Synchronous Type 1 card activation is selected 1: Synchronous Type 2 card activation is selected	CARD_TYPE	7	R/W	1'b0
0x09	1: Automatic activation per bit[7] is selected 0: Manual operating mode is selected	ACTIVATION_TYPE	6	R/W	1'b1
0x09	0 :Llow level is driven on C4 or C4 is being driven low externally 1 : C4 is pulled up high by internal pull-up Bit has no effect if card interface is not active	C4	5	R/W	1'b1
0x09	0 : Low level is driven on C8 or C8 is being driven low externally 1 : C8 is pulled up high by internal pull-up Bit has no effect if card interface is not active	C8	4	R/W	1'b1
0x09	0 : Low level is driven on RSTUC 1 : High level is driven on RSTUC Bit has no effect when card interface is not active. Bit has no effect if card interface is activated in asynchronous operating mode	RST	3	R/W	1'b0
0x09	0 : CLKUC is driven low or high based on the clock settings register (Reg 0x02, Bit [6:5]) 1 : CLK output is controlled by CLKIN1 Bit has no effect when card interface is not active. Bit has no effect if card interface is activated in asynchronous operating mode	CLK_ENABLE_SYNC	2	R/W	1'b1
0x09	1 : IO line is sampled on rising edge during synchronous type 1 activation sequence 0 : IO line sampled on falling edge during synchronous type 1 activation sequence Bit has no effect when card interface is not active. Bit has no effect if card interface is activated in asynchronous operating mode	EDGE	1	R/W	1'b1
0x09	1 : Start card interface activation based on bit[7:6] 0: Start deactivation sequence bit clears when automatic deactivation occurs.	START_SYNC	0	R/W	1'b0

REGISTER ADDRESS	DESCRIPTION	FIELD NAME	BIT	R/W	DEFAULT
0x0A	**Synchronous Mode ATR Byte1**				
0x0A	Bit 7 to Bit 0 of ATR response	BYTE1_UC	[7:0]	R	8'b00000000
0x0B	**Synchronous Mode ATR Byte2**				
0x0B	Bit 15 to Bit 8 of ATR response	BYTE2_UC	[7:0]	R	8'b00000000
0x0C	**Synchronous Mode ATR Byte3**				
0x0C	Bit 23 to Bit 16 of ATR response	BYTE3_UC	[7:0]	R	8'b00000000
0x0D	**Synchronous Mode ATR Byte4**				
0x0D	Bit 31 to Bit 24 of ATR response	BYTE4_UC	[7:0]	R	8'b00000000

Table 16.

REGISTER ADDRESS	DESCRIPTION	FIELD NAME	BIT	R/W	DEFAULT
0x10	**SAM1 Interface Status**				
0x10	1: Card interface is active (V_{CC} is ramped and stable) 0: Card interface is inactive	ACTIVE_SAM1	7	R	1'b0
0x10	1: Indicates card ATR was received before the ATR valid window. INT_SAM1 bit is set in interrupt register. Bit is cleared when the register is read	EARLY_SAM1	6	R	1'b0
0x10	1: Indicates card ATR was not received within the ATR valid window. INT_SAM1 bit is set in interrupt register. Bit is cleared when the register is read.	MUTE_SAM1	5	R	1'b0
0x10	1: Indicates over current condition on the card interface. INT_SAM1 bit is set in interrupt register. Bit clears when the register is read	PROT_UC_SAM1	4	R	1'b0
0x10	1: Indicates the card interface is in internal CLK mode i.e frequency on CLK pin is ~1.2 Mhz 0: Indicates the card interface is not in internal clock mode.	CLKSW_SAM1	3	R	1'b0
0x10	1: Indicates that an over temperature fault condition exists 0: Over temperature fault doesn't exist	STAT_OTP	2	R	1'b0
0x10	1: Indicates a supervisor fault condition exists. 0: Supervisor fault condition doesn't exist.	STAT_SUPL	1	R	1'b0
0x10	1: Indicates V_{CC} ramp fault on card interface. INT_SAM1 bit is set in interrupt register. Bit is cleared when register is read	VCC_FAIL_SAM1	0	R	1'b0
0x11	**SAM1 Interface Settings**				
0x11	00 : Set V_{CC} to 1.8 V 01 : Set V_{CC} to 1.8 V 10 : Set V_{CC} to 3 V 11 : Set V_{CC} to 5 V	SET_VCC_SAM1	[7:6]	R/W	2'b01
0x11	1: IOMC2 is connected to IOS1 0: IOMC2 is disconnected from IOS1	IO_EN_SAM1	5	R/W	1'b0
0x11	1: Warm reset sequence is started on SAM1 Bit is clears when warm reset sequence starts.	WARM_SAM1	3	R/W	1'b0
0x11	1: Starts activation sequence 0: Starts deactivation sequence Bit clears when automatic deactivation occurs	START_ASYNC_SAM1	0	R/W	1'b0

REGISTER ADDRESS	DESCRIPTION	FIELD NAME	BIT	R/W	DEFAULT
0x12	**SAM1 Clock Settings**				
0x12	1 : Card CLK is set to ~1.2 MHz 0 : Card CLK is set by Bit[6], Bit[5] or Bit[4:2]	INTERN_CLK_SAM1	7	R/W	1'b0
0x12	1 : Card CLK is set to 0 0 : Card CLK is set by Bit[5] or Bit[4:2]	CLK0_SAM1	6	R/W	1'b0
0x12	1 : Card CLK is set to 1 0 : Card CLK is set by Bit[4:2]	CLK1_SAM1	5	R/W	1'b0
0x12	000 : CLKS1 frequency = CLKIN2 001 : CLKS1 frequency = CLKIN2/2 010 : CLKS1 frequency = CLKIN2/4 011 : CLKS1 frequency = CLKIN2/5 100: CLKS1 frequency = CLKIN2/8 101: CLKS1 frequency = CLKIN2/8 110: CLKS1 frequency = CLKIN2/8 111: CLKS1 frequency = CLKIN2/8	CLK_DIV_SAM1	[4:2]	R/W	3'b011
0x13	**Asynchronous Mode ATR EARLY Counter MSB for SAM1**				
0x13	MSB (8-bits) of programmable 10-bit clock counter value	EARLY_COUNT_HI_SAM1	[7:0]	R/W	8'b10101010
0x14	**Asynchronous Mode ATR EARLY Counter LSB for SAM1**				
0x14	LSB (2-bits) of programmable 10-bit clock counter value	EARLY_COUNT_LO_SAM1	[7:6]	R/W	2'b00

Table 17.

REGISTER ADDRESS	DESCRIPTION	FIELD NAME	BIT	R/W	DEFAULT
0x15	**Asynchronous Mode ATR MUTE counter MSB for SAM1**				
0x15	MSB (8-bits) of programmable 16-bit clock counter value	MUTE_COUNT_HI_SAM1	[7:0]	R/W	8'b10100100
0x16	**Asynchronous Mode ATR MUTE counter LSB for SAM1**				
0x16	MSB (8-bits) of programmable 16-bit clock counter value	MUTE_COUNT_LO_SAM1	[7:0]	R/W	8'b01110100
0x17	**SAM IO Slew Rate Settings**				
0x17	3-Bit value defining the rise time of IO pin for all SAM interfaces	IO_TR_SAM	[7:5]	R/W	3'b100
0x17	2-Bit value defining the rise time of IO pin for all SAM interfaces	IO_TF_SAM	[4:3]	R/W	2'b00
0x18	**SAM Clock Slew Rate Settings**				
0x18	4-Bit value defining the rise time and fall time of CLK for all SAM interfaces	CLK_SR_SAM1	[7:4]	R/W	4'b1010

Table 18.

REGISTER ADDRESS	DESCRIPTION	FIELD NAME	BIT	R/W	DEFAULT
0x20	**SAM2 Interface Status**				
0x20	1: Card interface is active (V_{CC} is ramped and stable) 0: Card interface is inactive	ACTIVE_SAM2	7	R	1'b0
0x20	1: Indicates card ATR was received before the ATR valid window. INT_SAM2 bit is set in interrupt register. Bit is cleared when the register is read	EARLY_SAM2	6	R	1'b0
0x20	1: Indicates card ATR was not received within the ATR valid window. INT_SAM2 bit is set in interrupt register. Bit is cleared when the register is read.	MUTE_SAM2	5	R	1'b0
0x20	1: Indicates over current condition on the card interface. INT_SAM2 bit is set in interrupt register. Bit clears when the register is read	PROT_UC_SAM2	4	R	1'b0
0x20	1: Indicates the card interface is in internal CLK mode i.e frequency on CLK pin is ~1.2Mhz 0: Indicates the card interface is not in internal clock mode.	CLKSW_SAM2	3	R	1'b0
0x20	1: indicates V_{CC} ramp fault on card interface. INT_SAM2 bit is set in interrupt register. Bit is cleared when register is read	VCC_FAIL_SAM2	0	R	1'b0
0x21	**SAM2 Interface Settings**				
0x21	00 : set V_{CC} to 1.8 V 01 : set V_{CC} to 1.8 V 10 : set V_{CC} to 3 V 11 : set V_{CC} to 5 V	SET_VCC_SAM2	[7:6]	R/W	2'b01
0x21	1: IOMC2 is connected to IOS2 0: IOMC2 is disconnected from IOS2	IO_EN_SAM2	5	R/W	1'b0
0x21	1: Warm reset sequence is started on SAM2 Bit is clears when warm reset sequence starts.	WARM_SAM2	3	R/W	1'b0
0x21	1: Starts activation sequence 0: Starts deactivation sequence Bit clears when automatic deactivation occurs	START_ASYNC_SAM2	0	R/W	1'b0

Table 19.

REGISTER ADDRESS	DESCRIPTION	FIELD NAME	BIT	R/W	DEFAULT
0x22	**SAM2 Clock Settings**				
0x22	1 : Card CLK is set to ~1.2MHz 0 : CLKS2 is set by Bit[6] or Bit [5] or Bit[4:2]	INTERN_CLK_SAM2	7	R/W	1'b0
0x22	1 : Card CLK is set to 0 0 : CLKS2 is set by Bit[5] or Bit[4:2]	CLK0_SAM2	6	R/W	1'b0
0x22	1 : Card CLK is set to 1 0 : CLKS2 is set by Bit[4:2]	CLK1_SAM2	5	R/W	1'b0
0x22	000 : CLKS2 frequency = CLKIN2 001 : CLKS2 frequency = CLKIN2/2 010 : CLKS2 frequency = CLKIN2/4 011 : CLKS2 frequency = CLKIN2/5 100: CLKS2 frequency = CLKIN2/8 101: CLKS2 frequency = CLKIN2/8 110: CLKS2 frequency = CLKIN2/8 111: CLKS2 frequency = CLKIN2/8	CLK_DIV_SAM2	[4:2]	R/W	3'b011
0x23	**Asynchronous Mode ATR EARLY Counter MSB for SAM2**				
0x23	MSB (8-bits) of programmable 10-bit clock counter value.	EARLY_COUNT_HI_SAM2	[7:0]	R/W	8'b10101010
0x24	**Asynchronous Mode ATR EARLY Counter LSB for SAM2**				
0x24	LSB (2-bits) of programmable 10-bit clock counter value.	EARLY_COUNT_LO_SAM2	[7:6]	R/W	2'b00
0x25	**Asynchronous Mode ATR MUTE Counter MSB for SAM2**				
0x25	MSB (8-bits) of programmable 16-bit clock counter value.	MUTE_COUNT_HI_SAM2	[7:0]	R/W	8'b10100100
0x26	**Asynchronous Mode ATR MUTE Counter LSB for SAM2**				
0x26	MSB (8-bits) of programmable 16-bit clock counter value.	MUTE_COUNT_LO_SAM2	[7:0]	R/W	8'b01110100

Table 20.

REGISTER ADDRESS	DESCRIPTION	FIELD NAME	BIT	R/W	DEFAULT
0x30	**SAM3 Interface Status**				
0x30	1: Card interface is active (V_{CC} is ramped and stable) 0: Card interface is inactive	ACTIVE_SAM3	7	R	1'b0
0x30	1: Indicates card ATR was received before the ATR valid window. INT_SAM3 bit is set in interrupt register. Bit is cleared when the register is read	EARLY_SAM3	6	R	1'b0
0x30	1: Indicates card ATR was not received within the ATR valid window. INT_SAM3 bit is set in interrupt register. Bit is cleared when the register is read.	MUTE_SAM3	5	R	1'b0
0x30	1: Indicates over current condition on the card interface. INT_SAM3 bit is set in interrupt register Bit clears when the register is read	PROT_UC_SAM3	4	R	1'b0
0x30	1: Indicates the card interface is in internal CLK mode i.e frequency on CLK pin is ~1.2Mhz 0: Indicates the card interface is not in internal clock mode.	CLKSW_SAM3	3	R	1'b0
0x30	1: Indicates V_{CC} ramp fault on card interface. INT_SAM3 bit is set in interrupt register. Bit is cleared when register is read	VCC_FAIL_SAM3	0	R	1'b0
0x31	**SAM3 Interface Settings**				
0x31	00 : set V_{CC} to 1.8 V 01 : set V_{CC} to 1.8 V 10 : set V_{CC} to 3V 11 : set V_{CC} to 5V	SET_VCC_SAM3	[7:6]	R/W	2'b01
0x31	1: IOMC2 is connected to IOS3 0: IOMC2 is disconnected from IOS3	IO_EN_SAM3	5	R/W	1'b0
0x31	1: Warm reset sequence is started on SAM3 Bit is clears when warm reset sequence starts.	WARM_SAM3	3	R/W	1'b0
0x31	1: Starts activation sequence 0: Starts deactivation sequence Bit clears when automatic deactivation occurs	START_ASYNC_SAM3	0	R/W	1'b0

Table 21.

REGISTER ADDRESS	DESCRIPTION	FIELD NAME	BIT	R/W	DEFAULT
0x32	**SAM3 Clock Settings**				
0x32	1 : CLKS3 is set to ~1.2 Mhz 0 : CLKS3 is set by Bit[6] or Bit [5] or Bit[4:2]	INTERN_CLK_SAM3	7	R/W	1'b0
0x32	1 : CLKS3 is set to 0 0 : CLKS3 is set by Bit[5] or Bit[4:2]	CLK0_SAM3	6	R/W	1'b0
0x32	1 : CLKS3 is set to 1 0 : CLKS3 is set by Bit[4:2]	CLK1_SAM3	5	R/W	1'b0
0x32	000 : CLKS3 frequency = CLKIN2 001 : CLKS3 frequency = CLKIN2/2 010 : CLKS3 frequency = CLKIN2/4 011 : CLKS3 frequency = CLKIN2/5 100: CLKS3 frequency = CLKIN2/8 101: CLKS3 frequency = CLKIN2/8 110: CLKS3 frequency = CLKIN2/8 111: CLKS3 frequency = CLKIN2/8	CLK_DIV_SAM3	[4:2]	R/W	3'b011
0x33	**Asynchronous Mode ATR EARLY Counter MSB for SAM3**				
0x33	MSB (8-bits) of programmable 10-bit clock counter value.	EARLY_COUNT_HI_SAM3	[7:0]	R/W	8'b10101010
0x34	**Asynchronous Mode ATR EARLY Counter LSB for SAM3**				
0x34	LSB (2-bits) of programmable 10-bit clock counter value.	EARLY_COUNT_LO_SAM3	[7:6]	R/W	2'b00
0x35	**Asynchronous Mode ATR MUTE Counter MSB for SAM3**				
0x35	MSB (8-bits) of programmable 16-bit clock counter value.	MUTE_COUNT_HI_SAM3	[7:0]	R/W	8'b10100100
0x36	**Asynchronous Mode ATR MUTE Counter LSB for SAM3**				
0x36	MSB (8-bits) of programmable 16-bit clock counter value.		[7:0]	R/W	8'b01110100

Table 22.

REGISTER ADDRESS	DESCRIPTION	FIELD NAME	BIT	R/W	DEFAULT
0x40	**Product Version**				
0x40	Product Version	PRODUCT_VER	[7:0]	R	8'b00000000
0x41	**Interrupt Status Register**				
0x41	1: PROT, MUTE, EARLY, VCC_FAIL or PRESL bit set in User card. INT pin is asserted low when this bit is set. 0 : Bit clears when Register is read	INT_UC	7	R	1'b0
0x41	1: PROT, VCC_FAIL, MUTE or EARLY bit set in SAM1. INT is asserted low when this bit is set. 0 : Bit clears when Register is read	INT_SAM1	6	R	1'b0
0x41	1: PROT, VCC_FAIL, MUTE or EARLY bit set in SAM2. INT is asserted low when this bit is set. 0 : Bit clears when Register is read	INT_SAM2	5	R	1'b0
0x41	1: PROT, VCC_FAIL, MUTE or EARLY bit set in SAM3. INT is asserted low when this bit is set. 0 : Bit clears when Register is read	INT_SAM3	4	R	1'b0
0x41	1: All card interfaces deactivated due to over temperature fault. INT is asserted low when this bit is set. 0 : Bit clears when Register is read	INT_OTP	3	R	1'b0
0x41	1: All card interfaces deactivated due to Supervisor fault. INT is asserted low when this bit is set. 0 : Bit clears when register is read	INT_SUPL	2	R	1'b0
0x41	1: Sync card activation sequence complete. INT is asserted low when this bit is set. 0 : Bit clears when register is read	INT_SYNC_COMPLETE	1	R	1'b0
0x41	1: One of the GPIO inputs has changes state. INT is asserted low when this bit is set. 0 : Bit clears when register is read	INT_GPIO	0	R	1'b0
0x42	**Device Settings**				
0x42	1: DC-DC boost is enabled 0: DC-DC boost is disabled	DC_DC	7	R/W	1'b1
0x42	1: GPIO4 is configured as input 0: GPIO4 is configured as output	GPIO4	5	R/W	1'b0
0x42	1: GPIO3 is configured as input 0: GPIO3 is configured as output	GPIO3	4	R/W	1'b0
0x42	1: GPIO2 is configured as input 0: GPIO2 is configured as output	GPIO2	3	R/W	1'b0
0x42	1: GPIO1 is configured as input 0: GPIO1 is configured as output	GPIO1	2	R/W	1'b0

Table 23.

REGISTER ADDRESS	DESCRIPTION	FIELD NAME	BIT	R/W	DEFAULT
0x43	**GPIO Settings**				
0x43	Reflects level on GPIO4 (read only)	GPIO4_INPUT	7	R	1'b0
0x43	Reflects level on GPIO3 (read only)	GPIO3_INPUT	6	R	1'b0
0x43	Reflects level on GPIO2 (read only)	GPIO2_INPUT	5	R	1'b0
0x43	Reflects level on GPIO1 (read only)	GPIO1_INPUT	4	R	1'b0
0x43	Sets level on GPIO4 (Bit is ignored if pin is configured as input)	GPIO4_OUTPUT	3	R/W	1'b1
0x43	Sets level on GPIO3 (Bit is ignored if pin is configured as input)	GPIO3_OUTPUT	2	R/W	1'b1
0x43	Sets level on GPIO2 (Bit is ignored if pin is configured as input)	GPIO2_OUTPUT	1	R/W	1'b1
0x43	Sets level on GPIO1 (Bit is ignored if pin is configured as input)	GPIO1_OUTPUT	0	R/W	1'b1
0x44	**User Card Interrupt Mask Register**				
0x44	1: Mask User card EARLY Interrupt 0: Unmask User card EARLY interrupt	EARLY_UC_MASK	7	R/W	1'b0
0x44	1: Mask User Card MUTE Interrupt 0: Unmask User Card MUTE interrupt	MUTE_UC _MASK	6	R/W	1'b0
0x44	1: Mask User Card PROT Interrupt 0: Unmask User Card PROT interrupt	PROT_UC_MASK	5	R/W	1'b0
0x44	1: Mask sync card activation complete Interrupt 0: Unmask sync card activation complete interrupt	SYNC_COMPLETE_MASK	4	R/W	1'b0
0x44	1: Mask thermal shutdown Interrupt 0: Unmask thermal shutdown interrupt	OTP_MASK	3	R/W	1'b0
0x44	1: Mask supervisor fault Interrupt 0: Unmask supervisor fault interrupt	SUPL_MASK	2	R/W	1'b0
0x44	1: Mask all GPIO Interrupt 0: Unmask all GPIO interrupt	GPIO_INT_MASK	1	R/W	1'b0
0x44	1: Mask PRESL Interrupt 0: Unmask PRESL interrupt	PRESL_INT_MASK	0	R/W	1'b0

Table 24.

REGISTER ADDRESS	DESCRIPTION	FIELD NAME	BIT	R/W	DEFAULT
0x45	**SAM1 and SAM2 Interrupt Mask Register**				
0x45	1: Mask SAM1 EARLY Interrupt 0: Unmask SAM1 EARLY interrupt	EARLY_SAM1_MASK	7	R/W	1'b0
0x45	1: Mask SAM1 MUTE Interrupt 0: Unmask SAM1 MUTE interrupt	MUTE_SAM1 _MASK	6	R/W	1'b0
0x45	1: Mask SAM1 PROT Interrupt 0: Unmask SAM1 PROT interrupt	PROT_SAM1_MASK	5	R/W	1'b0
0x45	1: Mask SAM2 EARLY Interrupt 0: Unmask SAM2 EARLY interrupt	EARLY_SAM2_MASK	4	R/W	1'b0
0x45	1: Mask SAM2 MUTE Interrupt 0: Unmask SAM2 MUTE interrupt	MUTE_SAM2 _MASK	3	R/W	1'b0
0x45	1: Mask SAM2 PROT Interrupt 0: Unmask SAM2 PROT interrupt	PROT_SAM2_MASK	2	R/W	1'b0
0x45	1: Mask VCC_FAIL Interrupt on all SAMs 0: Unmask VCC_FAIL Interrupt on all SAMs	VCC_FAIL_SAM_MASK	1	R/W	1'b0
0x45	1: Mask VCC_FAIL Interrupt on all User Card 0: Unmask VCC_FAIL Interrupt on all User Card	VCC_FAIL_UC_MASK	0	R/W	1'b0
0x46	**SAM3 and GPIO Interrupt Mask Register**				
0x46	1: Mask SAM3 EARLY Interrupt 0: Unmask SAM3 EARLY interrupt	EARLY_SAM3_MASK	7	R/W	1'b0
0x46	1: Mask SAM3 MUTE Interrupt 0: Unmask SAM3 MUTE interrupt	MUTE_SAM3 _MASK	6	R/W	1'b0
0x46	1: Mask SAM3 PROT Interrupt 0: Unmask SAM3 PROT interrupt	PROT_SAM3_MASK	5	R/W	1'b0
0x46	1: Mask GPIO4 Interrupt 0: Unmask GPIO4 interrupt	GPIO4_INT_MASK	4	R/W	1'b0
0x46	1: Mask GPIO3 Interrupt 0: Unmask GPIO3 interrupt	GPIO3_INT_MASK	3	R/W	1'b0
0x46	1: Mask GPIO2 Interrupt 0: Unmask GPIO2 interrupt	GPIO2_INT_MASK	2	R/W	1'b0
0x46	1: Mask GPIO1 Interrupt 0: Unmask GPIO1 interrupt	GPIO1_INT_MASK	1	R/W	1'b0

9 Application and Implementation

9.1 Application Information

TCA5013 is a smartcard interface IC that is used in POS terminals that support EMV 4.3, ISO7816 - 3 and ISO 7816 - 10 smartcards. The below application note provides general guidelines for implementing the device in a POS terminal.

9.2 Typical Application

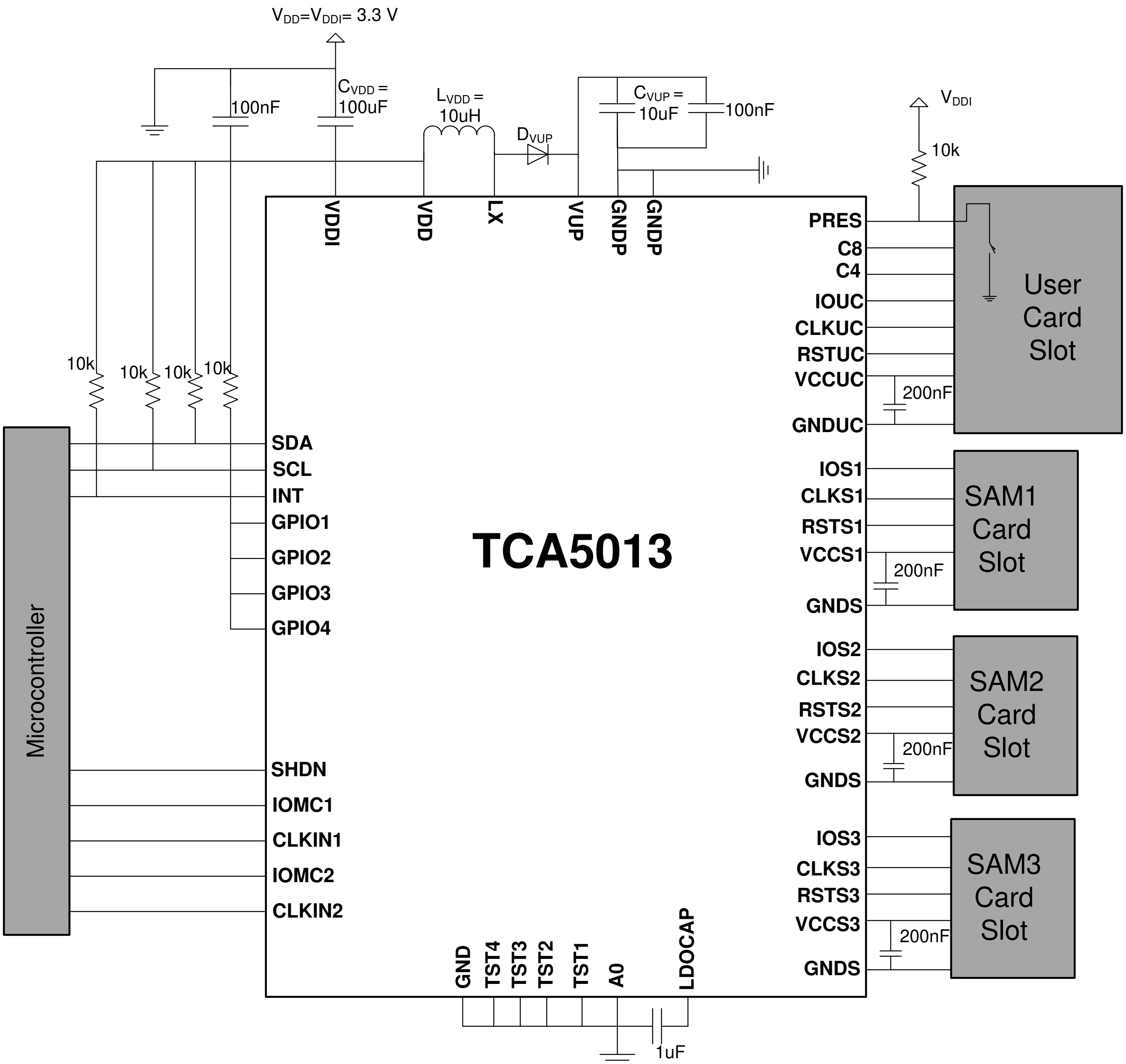


Figure 26. POS Terminal Typical Application

Typical Application (continued)

9.2.1 Design Requirements

For this design example shown below, Table 25 shows the input parameters.

Table 25. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{DD} input Voltage range	2.7 V to 4.2 V
V_{DDI} input Voltage range	2.7 V to 4.2 V
V_{CC} output Voltage range	1.8 V, 3 V, 5 V
Sum of all ICC currents	180 mA (max)
V_{CC} output ripple voltage	90 mV (max)
Max load transient supported on V_{CC}	As defined in the *Electrical Characteristics—Card V_{CC}*

9.2.2 Detailed Design Procedure

9.2.2.1 IO Pin Fall Time Setting

The V_{OL} on the IO pin depends on the IO fall time setting shown in Table 7. It also shows the different IO fall time settings that are usable for different V_{CC} voltage. Care should be taken to select a register setting such that V_{OL} meets the system requirements.

9.2.2.2 CLK Pin Rise Time And Fall Time Settings

Electrical Characteristics—Card CLK shows the typical rise and fall time of the clock signal for a 30 pF load. Because most applications will not have a typical 30 pF load, the rise and fall time of the clock signal will need to be calibrated for the board. EMV 4.3 specifies that the rise/fall time on the clock signal shall not be more than 8% of the clock period. It is recommended that the slowest fall time setting that meets the EMV requirement be selected. For systems where multiple clock frequencies will be used, it is recommended that a different fall time setting be used for each clock frequency.

9.2.3 Application Curves

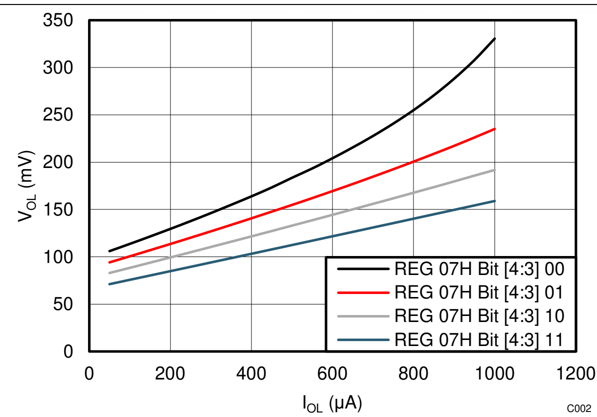


Figure 27. V_{OL} vs I_{OL} for User Card

10 Power Supply Recommendations

The TCA5013 has two power supplies V_{DD} and V_{DDI}. When the device is powering up, the ramp rates of V_{DD} and V_{DDI} can cause the supervisor fault to be asserted. The supervisor fault at power up can be avoided if V_{DD} is ramped and stable before V_{DDI} is ramped.

10.1 Power-On-Reset

When the voltage on these pins ramps an internal power-on-reset circuit holds the device in reset condition unless the voltage on both pins rises above the VPORR voltage defined Table 26. Values in Table 26 are ensured by design, but are not tested in production.

Table 26. Power On Reset Thresholds

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{PORF}	Voltage trip point of POR on falling V_{DD}	1.8	1.85	1.95	V
	Voltage trip point of POR on falling V_{DDI}	1.4	1.5	1.55	V
V_{PORR}	Voltage trip point of POR on rising V_{DD}	1.9	1.95	2	V
	Voltage trip point of POR on rising V_{DDI}	1.45	1.5	1.55	V

11 Layout

11.1 Layout Guidelines

11.1.1 DC-DC Boost Layout Recommendation

Some key guidelines are listed here to be followed for the layout of the DC-DC boost in the TCA5013:

- The inductor must be placed close to the LX pin such that the trace resistance between the LX pin and the inductor terminal is as small as possible.
- The 10 µF input capacitor on VDD shall be placed close to the inductor terminal and the two shall be connected by a copper pour to minimize resistance as much as possible.
- The other terminal of the 10 µF capacitor should be connected to GNDP plane by multiple vias to provide a low resistance path to ground.
- The 100 nF capacitor should be placed as close to VDD pin as possible.
- The anode of the schottky diode shall be placed as close as possible to the inductor and shall be connected to it by a copper pour to minimize resistance as much as possible.
- The 10 µF output capacitor on VUP should have a very low resistive connection to VUP and GNDP.

11.1.2 Card Interface Layout Recommendations

The card interface layout is important for proper operation of the device and for meeting EMV4.3 electrical requirements:

- If possible two 100 nF capacitors should be connected to VCC. One near the TCA5013 and one close to the card slot.
- If only one 200 nF capacitor is used it should be placed close to the TCA5013.
- If possible the CLK trace should be routed on a separate signal layer different from the layer on which the other card interface traces (IO and RST) are routed. It is also recommended that the two signal layers be separated by a ground plane if possible.
- The GNDS, GNDUC and GND pins should be connected to the ground plane with the shortest trace possible to reduce inductance from the device ground to the ground plane. This is critical in order for the device to meet the 8 kV IEC protection level on the card interface pins.

11.2 Layout Example

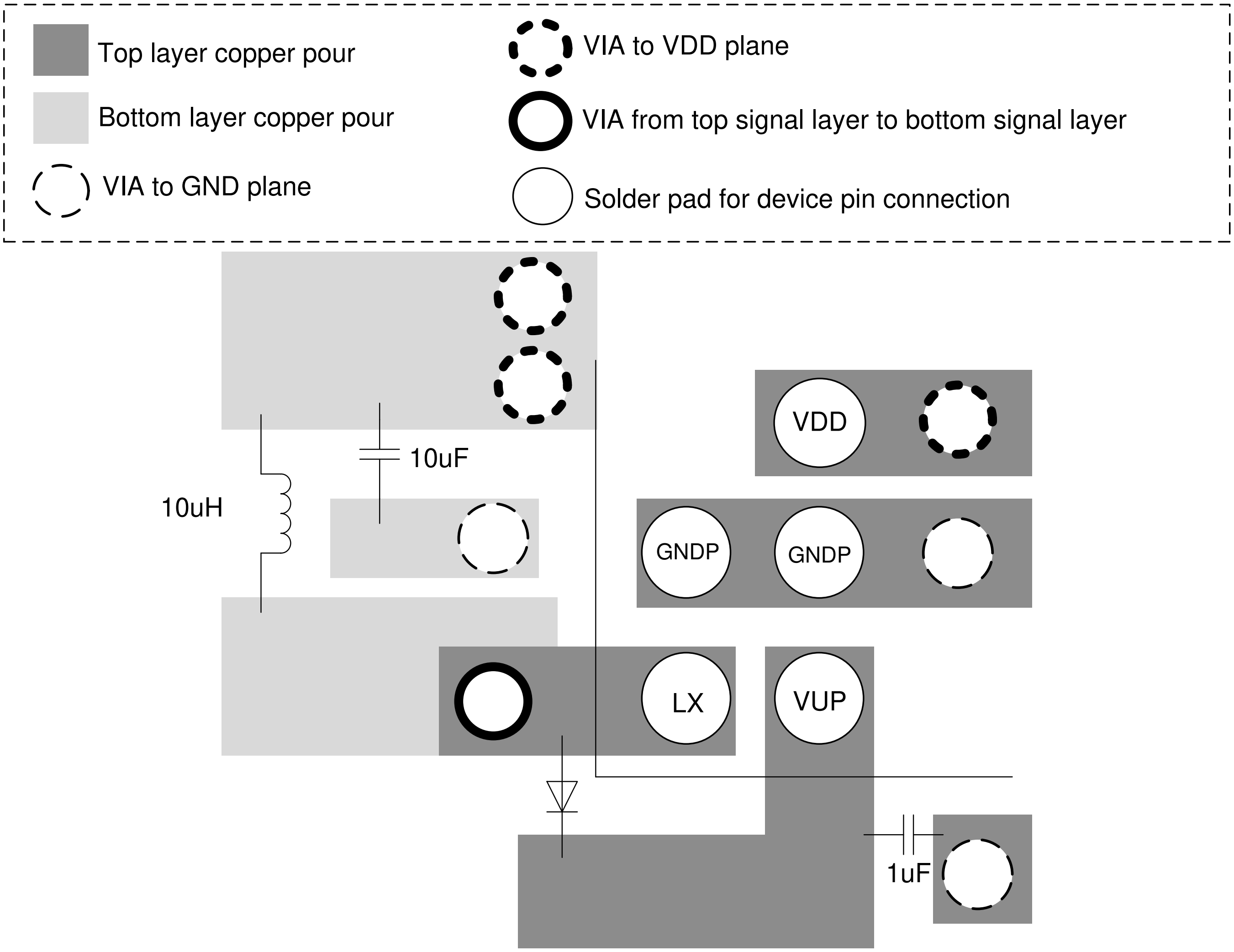


Figure 28. Example Layout of DC-DC Boost Section of TCA5013

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA5013ZAHR	ACTIVE	NFBGA	ZAH	48	3000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	RN013	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

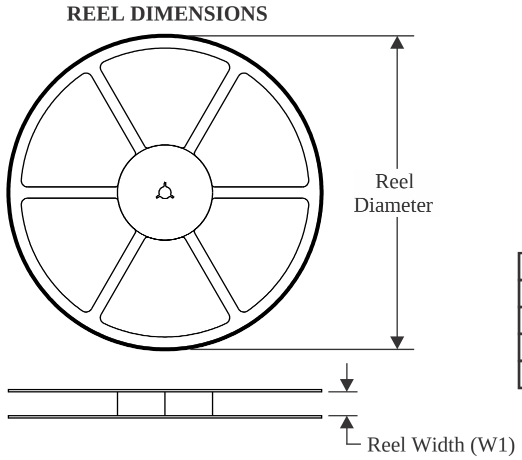
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

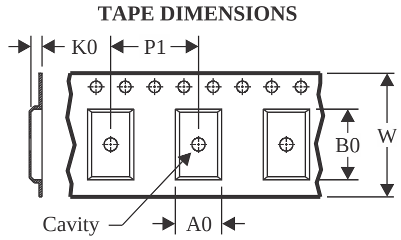
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

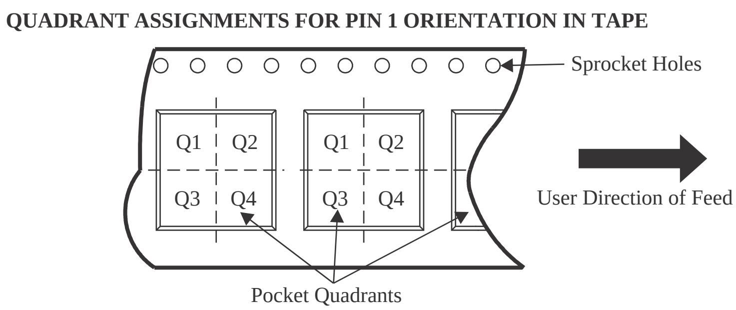
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





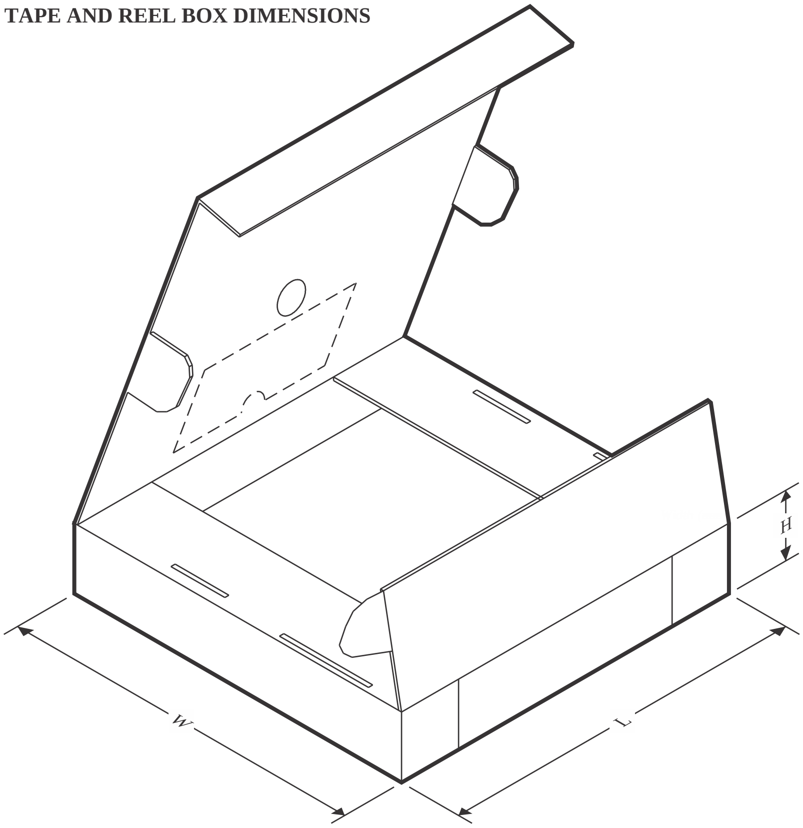
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

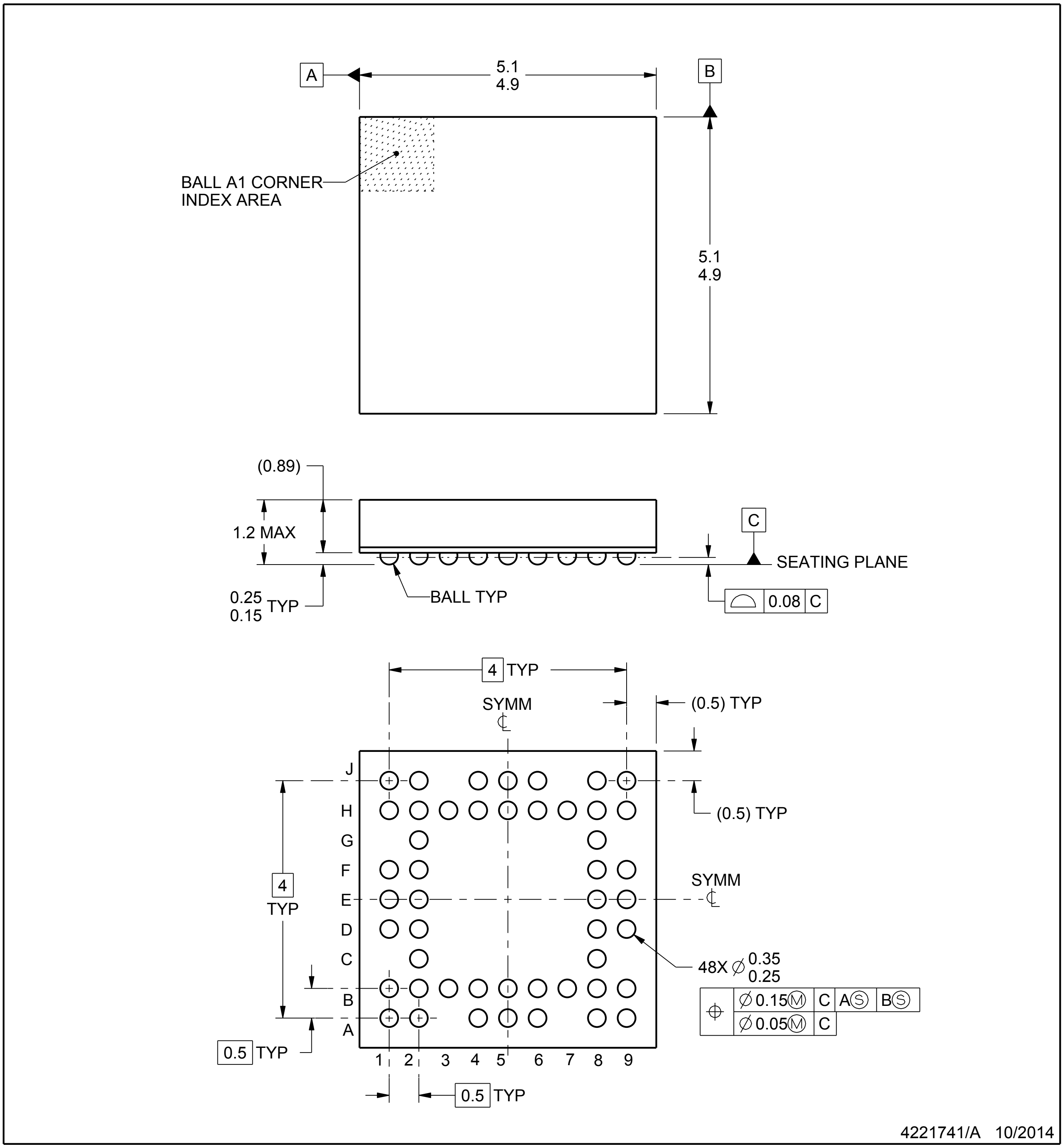
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA5013ZAHR	NFBGA	ZAH	48	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



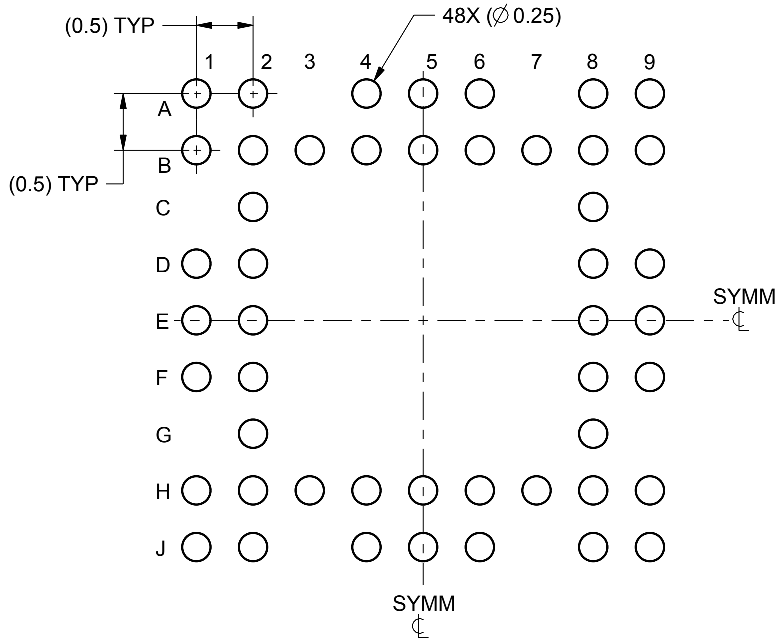
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA5013ZAHR	NFBGA	ZAH	48	3000	336.6	336.6	31.8

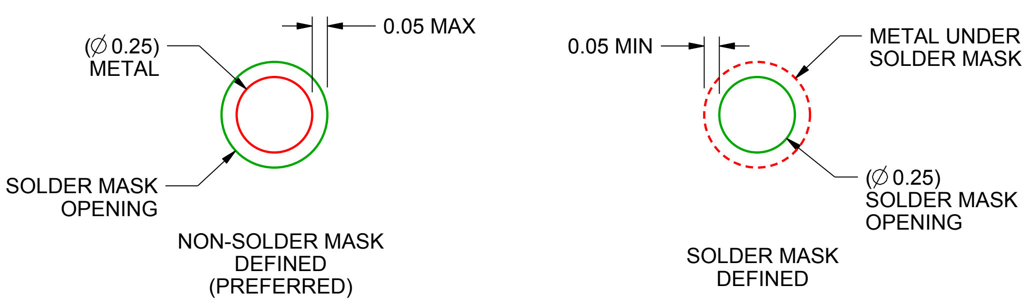


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS
NOT TO SCALE

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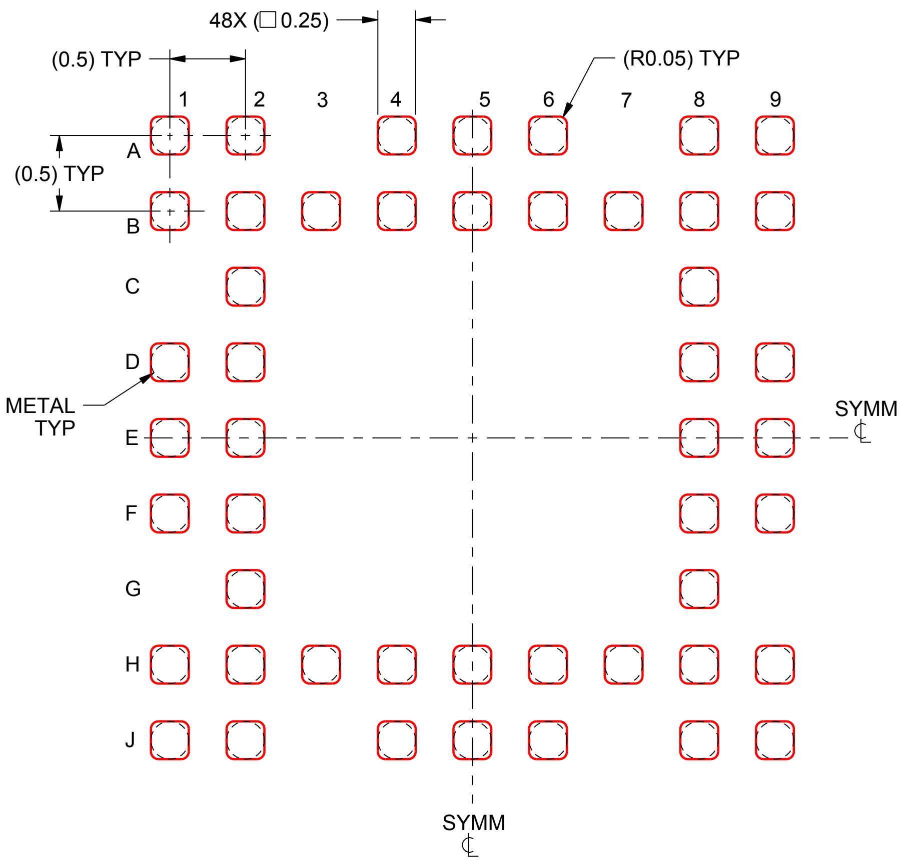
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SSYZ015 (www.ti.com/lit/ssyz015).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.