UM11596

PTN3944 linear equalizer application board user manual

Rev. 1 — 14 July 2021 User manual

Document information

Information	Content
Keywords	PTN3944, PCIe, linear redriver
Abstract	UM11596 demonstrates application board capability, interfacing an PCIe device with a host computer on a x16 slot. The application board is intended for use as an evaluation board, customer demonstration tool, and a reference design.

Revision history

Rev	Date	Description
1	20210714	Initial release

Important notice

NXP provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

1 Introduction

The PTN3944 is a high-performance, multi-channel, linear equalizer optimized for PCIe 4.0, UPI, and similar high-speed interfaces. Using multiple components of the PTN3944 supports redriving PCIe signals on x1, x2, x4, x8, or x16 devices installed in a PCIe slot.

This document details how to properly connect the evaluation board in a system in order to interface a chipset and a PCIe device. The document also illustrates; the Graphical User Interface (GUI) to configure the equalizer settings of transmitters and receivers; LPCUSBSIO module operation; and configuration with the PTN3944 application board.

2 PTN3944 PCIe Add-In-Card

The PTN3944 PCIe Add-In-Card (AIC) is designed for use in an available PCIe x16 slot on a PC or server computer. In addition, using the CEM connector on the top, a PCIe device can be attached. On the front side of the AIC, there are four PTN3944 that redrive PCIe signals from motherboard side (from CPU/chipset) to the PCIe device. On the back side of the AIC, another 4 PTN3944 redrive PCIe signals from a PCIe device to the motherboard side (to CPU/chipset). The PTN3944 equalizer, output swing level, or flat gain settings can be configured through either an I^2C bus, or using the onboard pull-up/down DIP switches.

The AIC power is supplied from either gold finger 3.3 V, or from an external 5.0 V power supply. Each redriver consumes up to 250 mA of current at 1.8 V. With all 8 components of the PTN3944 active at the same time, the AIC consumes up to 2 A of current at 1.8 V. NXP recommends using an external 5.0 V, 1 A power supply instead of using power from the PCIe gold finger. An onboard DC-to-DC power converter converts 5.0 V input to 1.8 V.

2.1 Block diagram

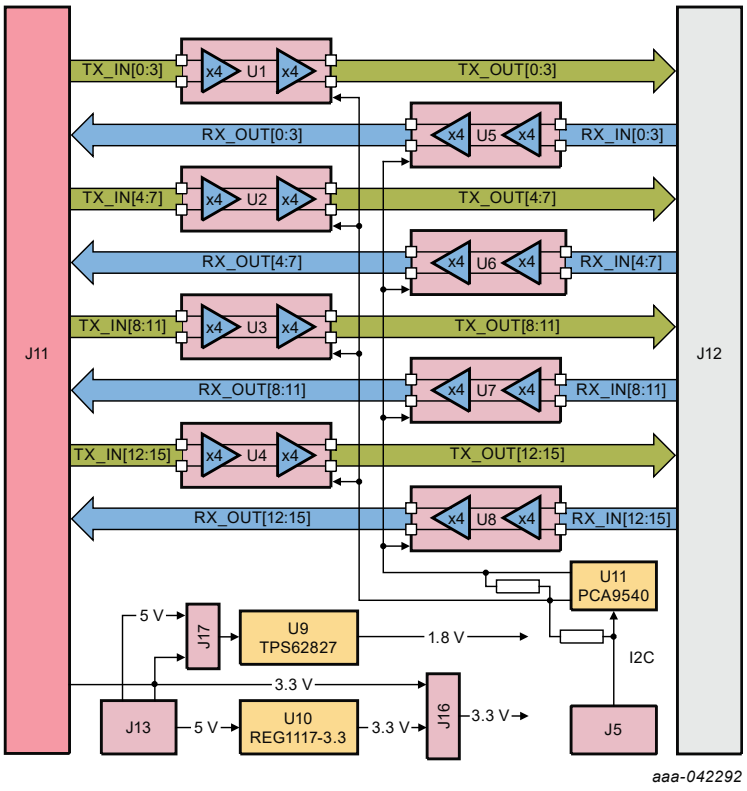


Figure 1. Block diagram

2.2 PCB photographs

Figure 2. PTN3944 PCIe add-in-card front side

Figure 3. PTN3944 PCIe add-in-card back side

2.3 PTN3944 PCIe Add-In-Card schematics

2.3.1 Front side redrivers

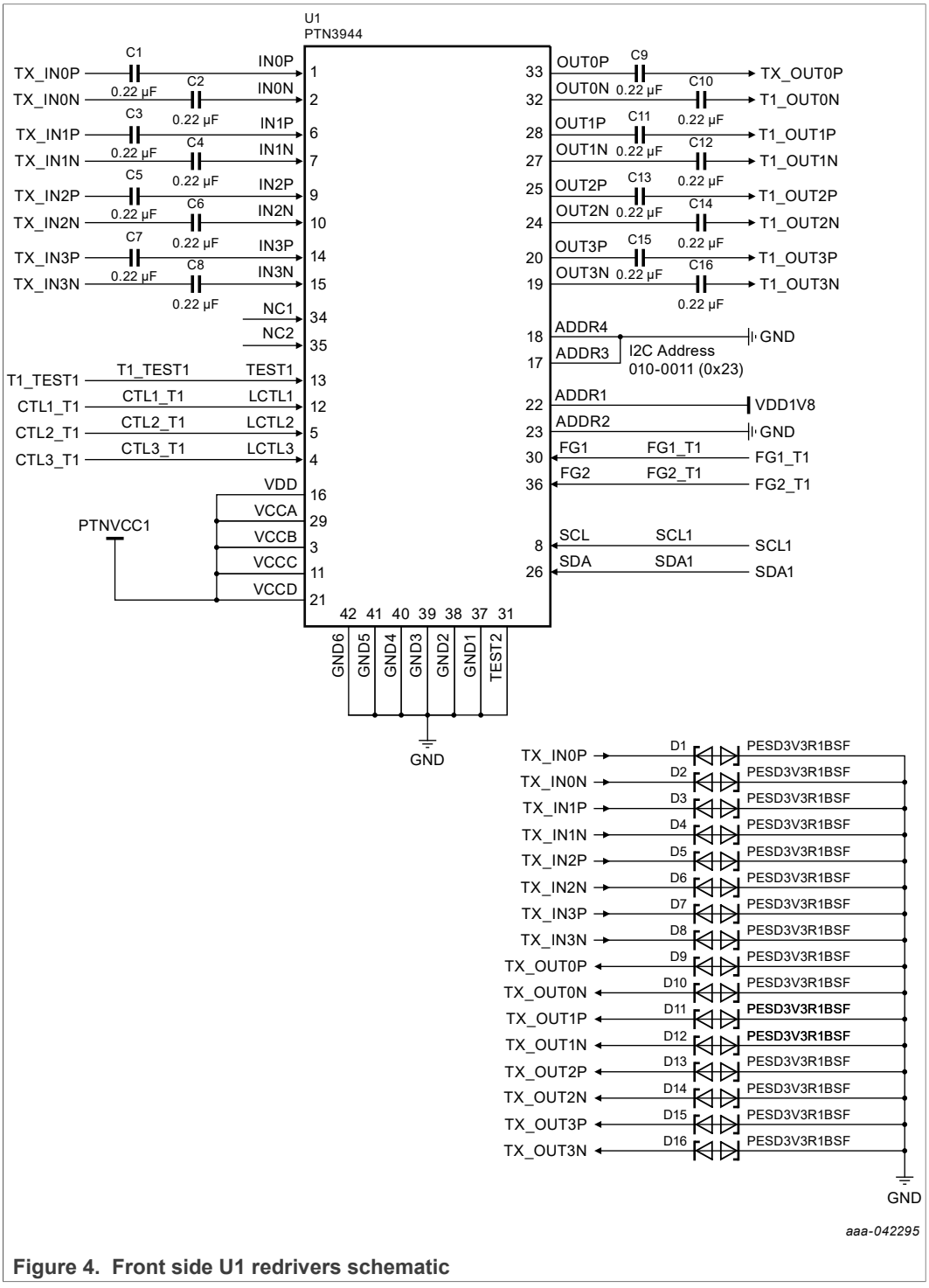


Figure 4. Front side U1 redrivers schematic

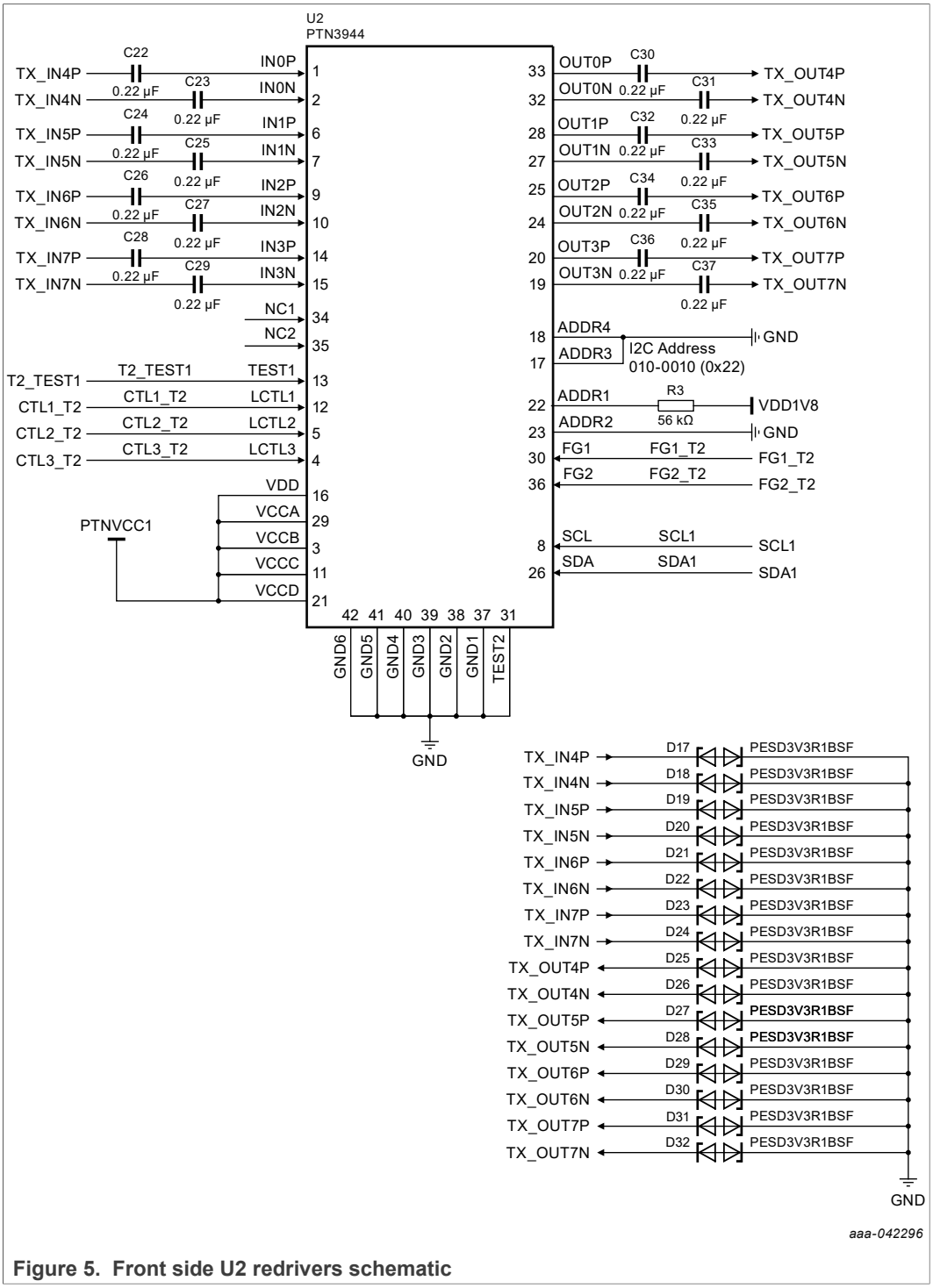


Figure 5. Front side U2 redrivers schematic

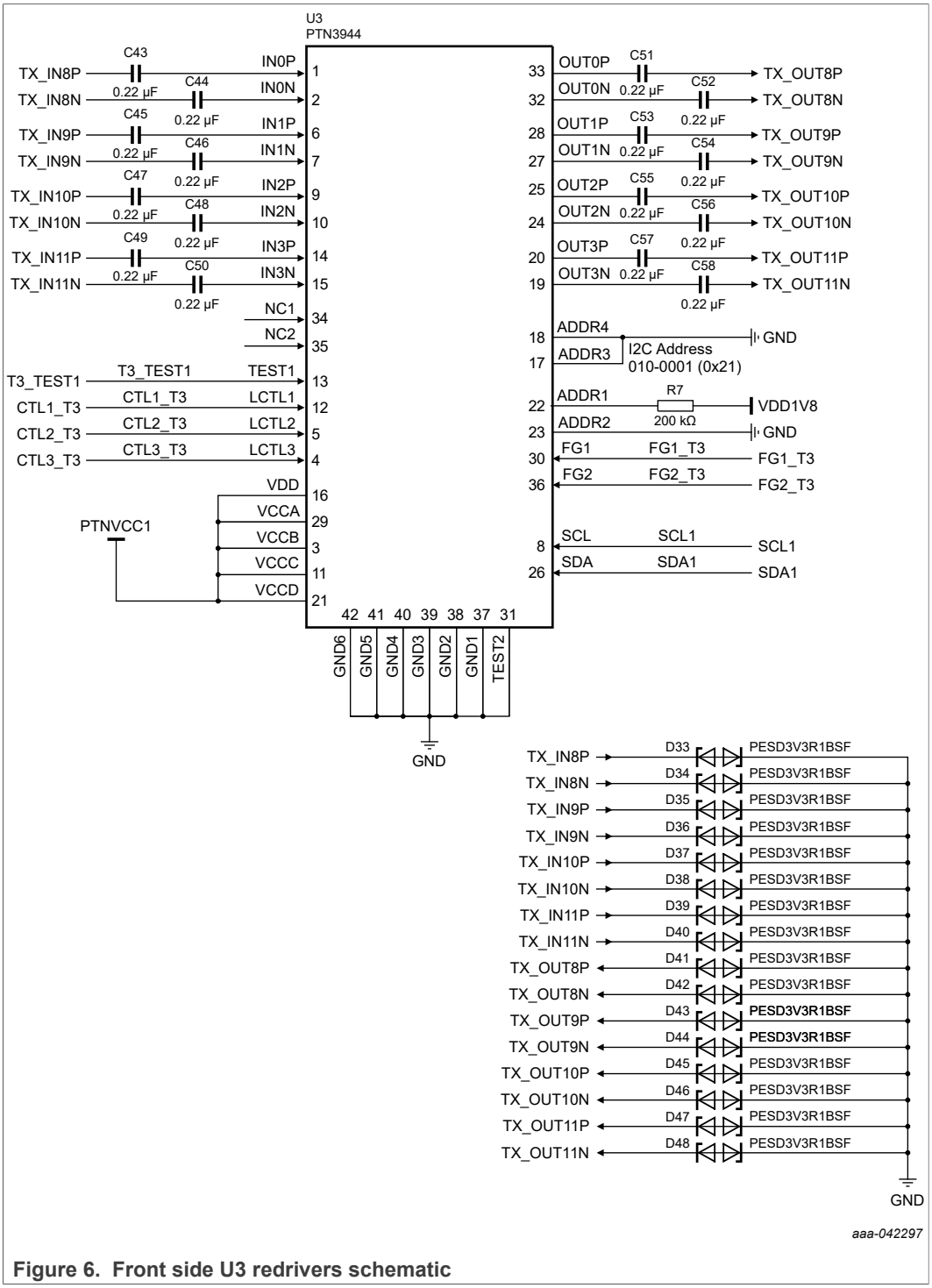


Figure 6. Front side U3 redrivers schematic

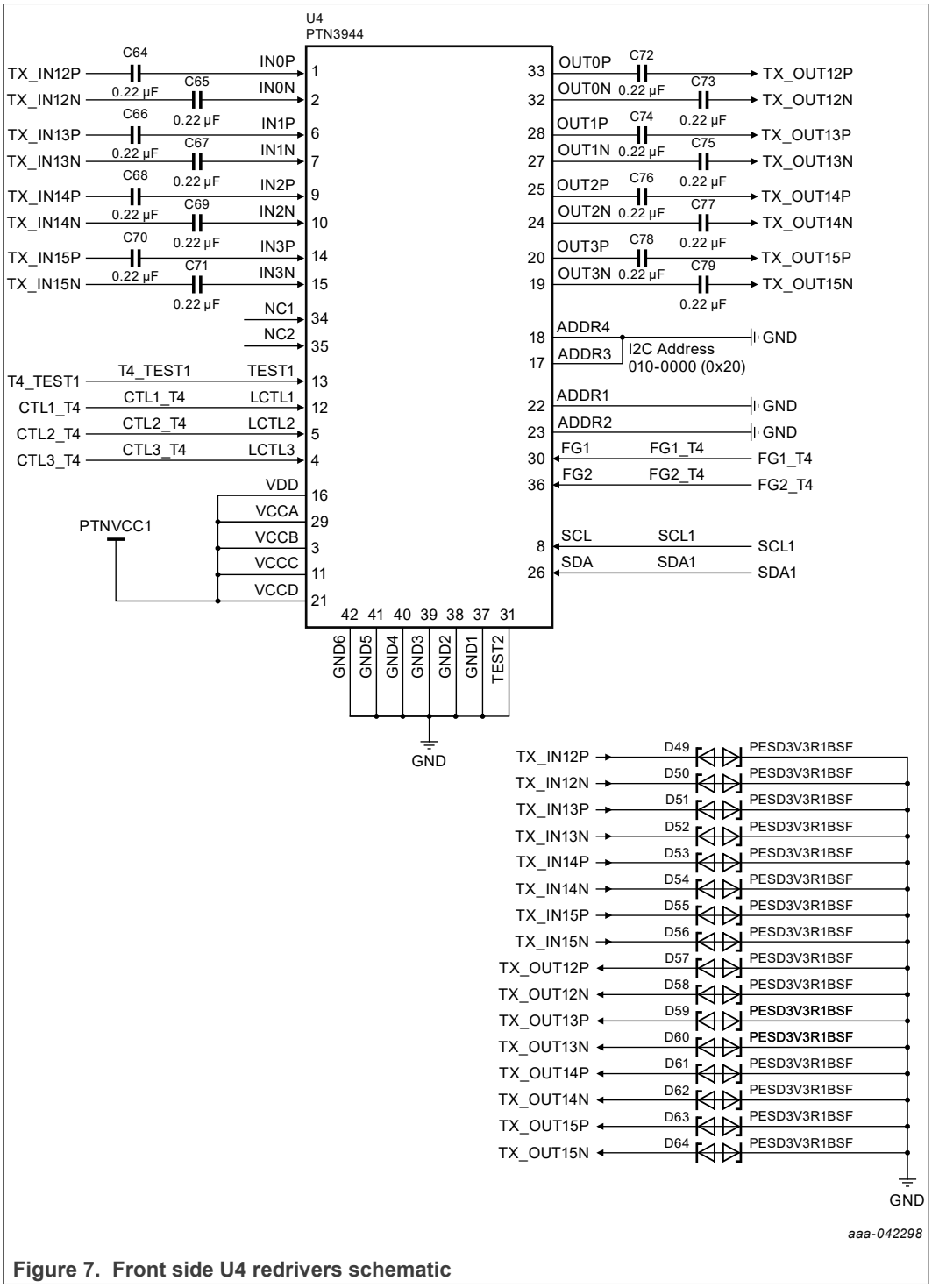


Figure 7. Front side U4 redrivers schematic

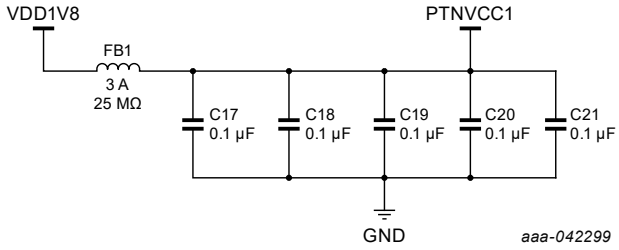


Figure 8. Schematic - front side

There are four PTN3944 on the front side of the AIC. Each PTN3944 component is responsible for 4 lanes of transmitters from the motherboard side to PCIe device side. Each PTN3944 is assigned a unique I^2C address. See Table 1.

Table 1. Front side redrivers U1 – U4 I^2C addresses and corresponding TX lanes

Designator	I^2C Address	Corresponding PCIe TX Lanes
U1	0x23	CH[0] – PCIe TX[0] CH[1] – PCIe TX[1] CH[2] – PCIe TX[2] CH[3] – PCIe TX[3]
U2	0x22	CH[0] – PCIe TX[4] CH[1] – PCIe TX[5] CH[2] – PCIe TX[6] CH[3] – PCIe TX[7]
U3	0x21	CH[0] – PCIe TX[8] CH[1] – PCIe TX[9] CH[2] – PCIe TX[10] CH[3] – PCIe TX[11]
U4	0x20	CH[0] – PCIe TX[12] CH[1] – PCIe TX[13] CH[2] – PCIe TX[14] CH[3] – PCIe TX[15]

2.3.2 Back side redrivers

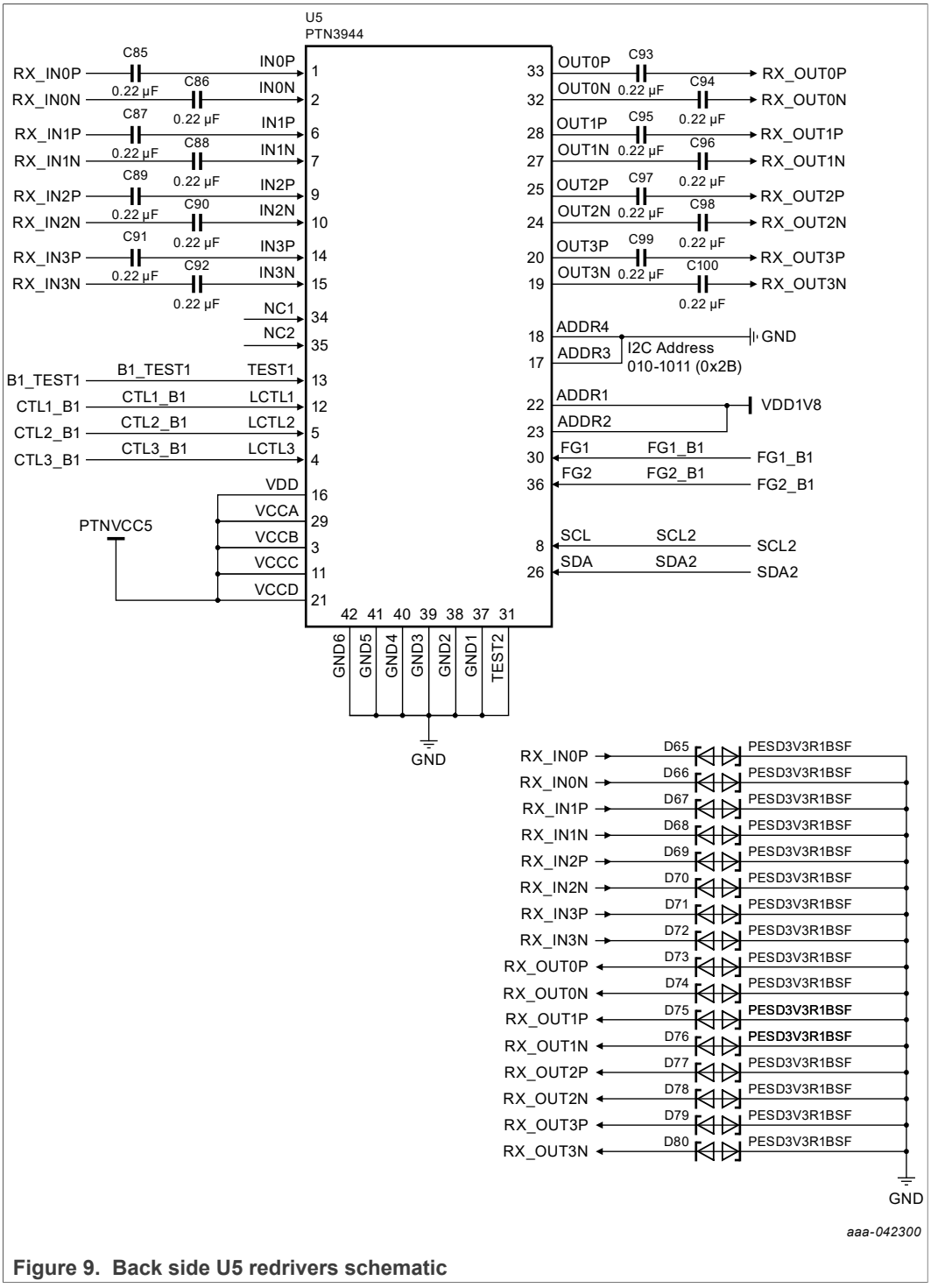


Figure 9. Back side U5 redrivers schematic

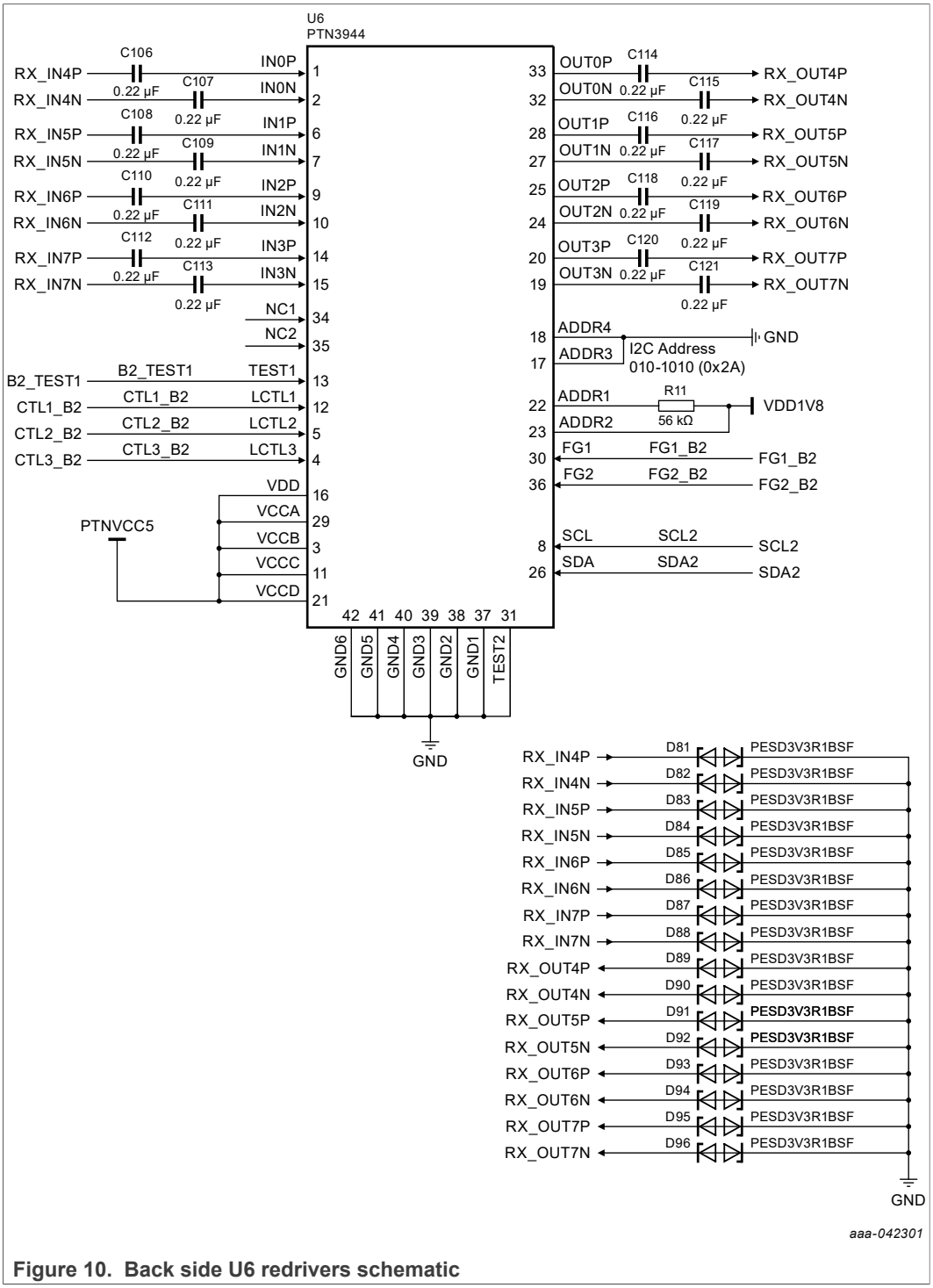


Figure 10. Back side U6 redrivers schematic

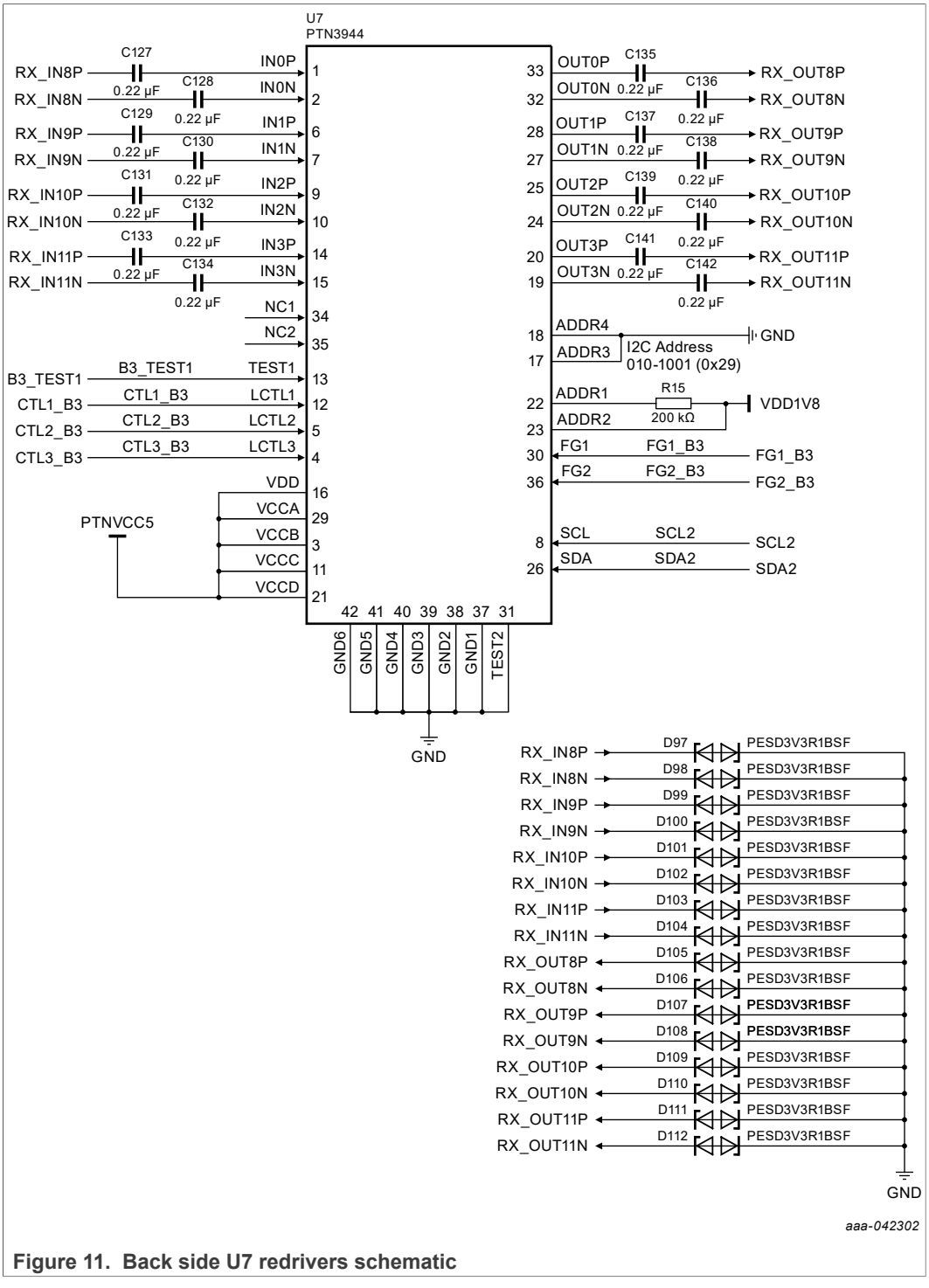


Figure 11. Back side U7 redrivers schematic

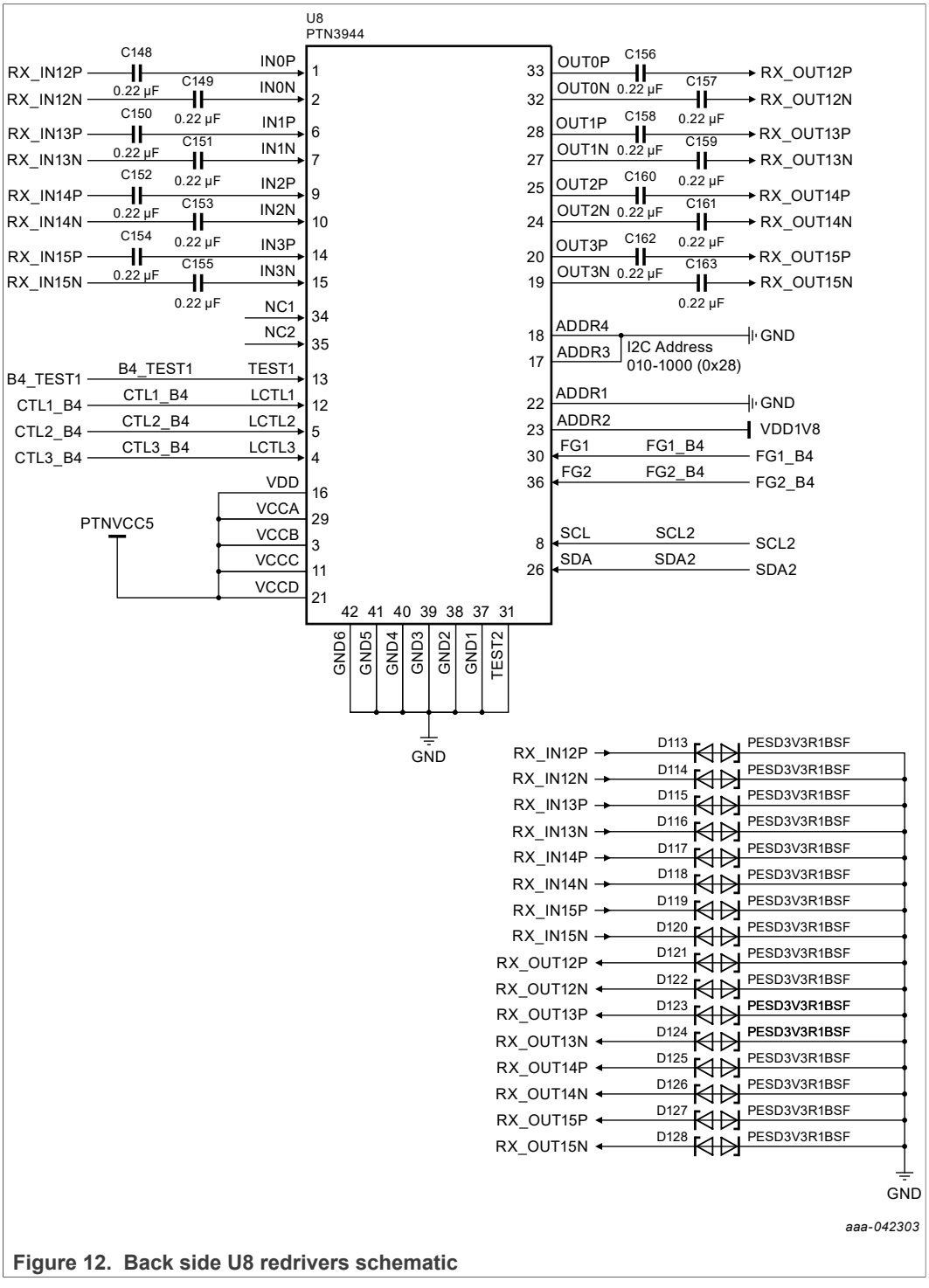


Figure 12. Back side U8 redrivers schematic

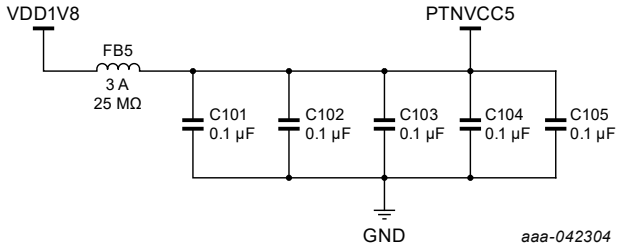


Figure 13. Schematic - back side

There are four PTN3944 on the back side of the AIC. Each PTN3944 component is responsible for 4 lanes of receivers from PCIe device side to the motherboard side. Each PTN3944 component is assigned a unique I^2C address. See Table 2.

Table 2. Back side redrivers U5 – U8 I^2C addresses and corresponding TX lanes

Designator	I^2C Address	Corresponding PCIe TX Lanes
U5	0x2B	CH[0] – PCIe RX[0] CH[1] – PCIe RX[1] CH[2] – PCIe RX[2] CH[3] – PCIe RX[3]
U6	0x2A	CH[0] – PCIe RX[4] CH[1] – PCIe RX[5] CH[2] – PCIe RX[6] CH[3] – PCIe RX[7]
U7	0x29	CH[0] – PCIe RX[8] CH[1] – PCIe RX[9] CH[2] – PCIe RX[10] CH[3] – PCIe RX[11]
U8	0x28	CH[0] – PCIe RX[12] CH[1] – PCIe RX[13] CH[2] – PCIe RX[14] CH[3] – PCIe RX[15]

2.3.3 Front side redriver control switches

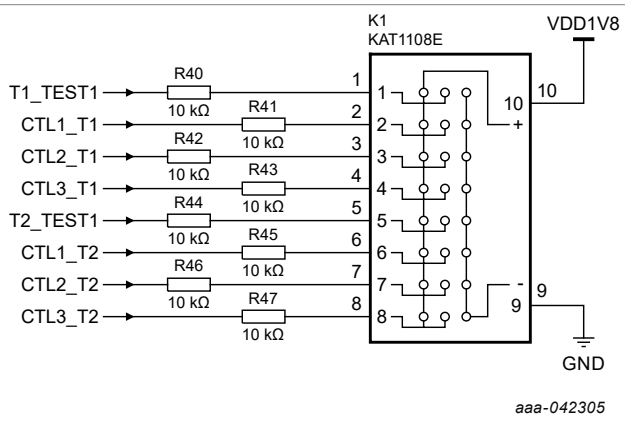


Figure 14. Front side K1 control switch schematic

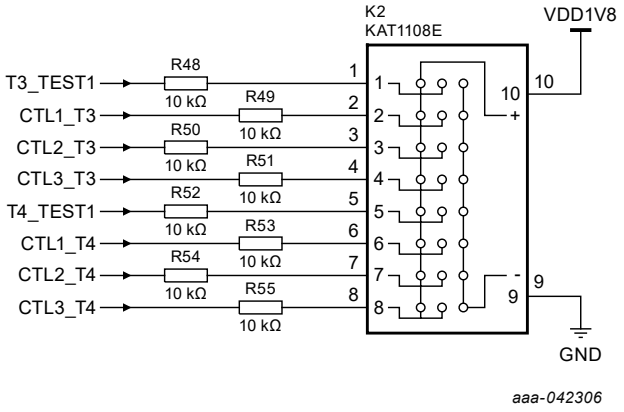


Figure 15. Front side K2 control switch schematic

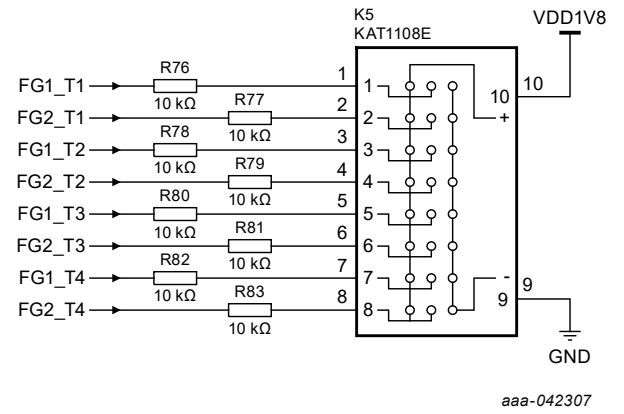


Figure 16. Front side K5 control switch schematic

Table 3. Front side redriver K1, K2, and K5 control switch positions and descriptions

Switch	Switch Position	Description
K1	1	U1 (Top/Front) Test Pin, Connect To GND
	2	U1 (Top/Front) LCTL1, Peaking Gain Setting
	3	U1 (Top/Front) LCTL2, Peaking Gain Setting
	4	U1 (Top/Front) LCTL3, Output Linear Swing Setting
	5	U2 (Top/Front) Test Pin, Connect To GND
	6	U2 (Top/Front) LCTL1, Peaking Gain Setting
	7	U2 (Top/Front) LCTL2, Peaking Gain Setting
	8	U2 (Top/Front) LCTL3, Output Linear Swing Setting

Table 3. Front side redriver K1, K2, and K5 control switch positions and descriptions*...continued*

Switch	Switch Position	Description
K2	1	U3 (Top/Front) Test Pin, Connect To GND
	2	U3 (Top/Front) LCTL1, Peaking Gain Setting
	3	U3 (Top/Front) LCTL2, Peaking Gain Setting
	4	U3 (Top/Front) LCTL3, Output Linear Swing Setting
	5	U4 (Top/Front) Test Pin, Connect To GND
	6	U4 (Top/Front) LCTL1, Peaking Gain Setting
	7	U4 (Top/Front) LCTL2, Peaking Gain Setting
	8	U4 (Top/Front) LCTL3, Output Linear Swing Setting
K5	1	U1 (Top/Front) FG1, Flat Gain Control Setting
	2	U1 (Top/Front) FG2, Flat Gain Control Setting
	3	U2 (Top/Front) FG1, Flat Gain Control Setting
	4	U2 (Top/Front) FG2, Flat Gain Control Setting
	5	U3 (Top/Front) FG1, Flat Gain Control Setting
	6	U3 (Top/Front) FG2, Flat Gain Control Setting
	7	U4 (Top/Front) FG1, Flat Gain Control Setting
	8	U4 (Top/Front) FG2, Flat Gain Control Setting

2.3.4 Back side redriver control switches

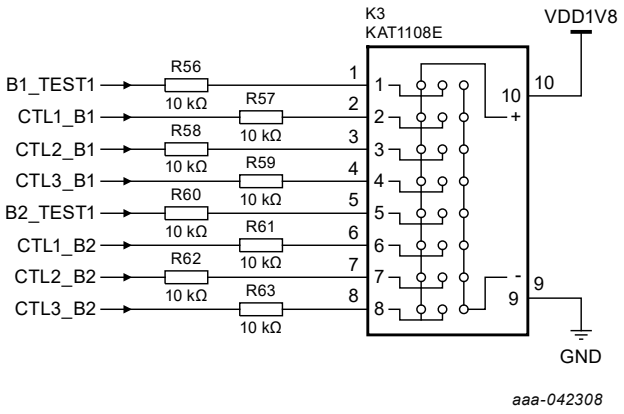


Figure 17. Back side K3 control switch schematic

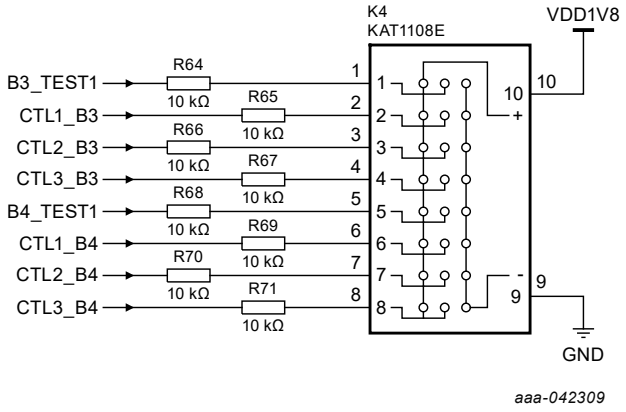


Figure 18. Back side K4 control switch schematic

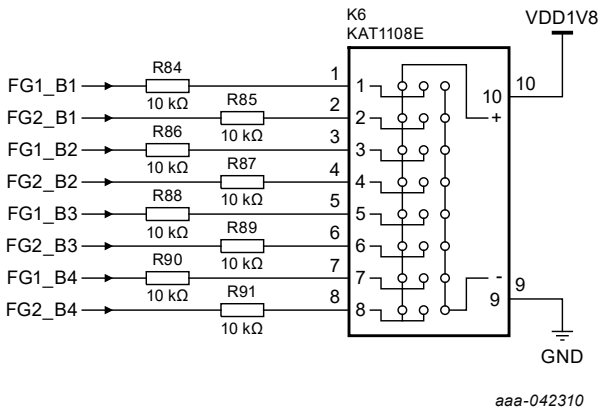


Figure 19. Back side K6 control switch schematic

Table 4. Back side redrivers K3, K4, and K6 control switch positions and descriptions

Switch	Switch Position	Description
K3	1	U5 (Bottom/Back) Test Pin, Connect To GND
	2	U5 (Bottom/Back) LCTL1, Peaking Gain Setting
	3	U5 (Bottom/Back) LCTL2, Peaking Gain Setting
	4	U5 (Bottom/Back) LCTL3, Output Linear Swing Setting
	5	U6 (Bottom/Back) Test Pin, Connect To GND
	6	U6 (Bottom/Back) LCTL1, Peaking Gain Setting
	7	U6 (Bottom/Back) LCTL2, Peaking Gain Setting
	8	U6 (Bottom/Back) LCTL3, Output Linear Swing Setting

Table 4. Back side redrivers K3, K4, and K6 control switch positions and descriptions*...continued*

Switch	Switch Position	Description
K4	1	U7 (Bottom/Back) Test Pin, Connect To GND
	2	U7 (Bottom/Back) LCTL1, Peaking Gain Setting
	3	U7 (Bottom/Back) LCTL2, Peaking Gain Setting
	4	U7 (Bottom/Back) LCTL3, Output Linear Swing Setting
	5	U8 (Bottom/Back) Test Pin, Connect To GND
	6	U8 (Bottom/Back) LCTL1, Peaking Gain Setting
	7	U8 (Bottom/Back) LCTL2, Peaking Gain Setting
	8	U8 (Bottom/Back) LCTL3, Output Linear Swing Setting
K6	1	U5 (Bottom/Back) FG1, Flat Gain Control Setting
	2	U5 (Bottom/Back) FG2, Flat Gain Control Setting
	3	U6 (Bottom/Back) FG1, Flat Gain Control Setting
	4	U6 (Bottom/Back) FG2, Flat Gain Control Setting
	5	U7 (Bottom/Back) FG1, Flat Gain Control Setting
	6	U7 (Bottom/Back) FG2, Flat Gain Control Setting
	7	U8 (Bottom/Back) FG1, Flat Gain Control Setting
	8	U8 (Bottom/Back) FG2, Flat Gain Control Setting

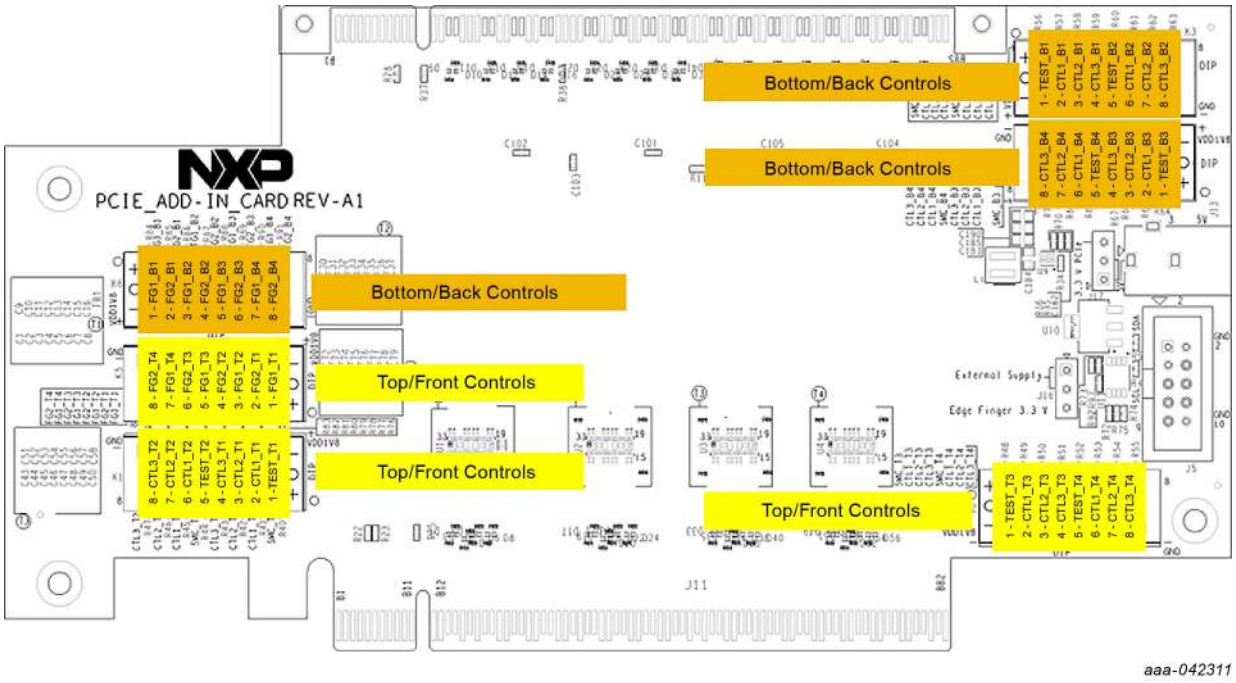


Figure 20. Board control locations

2.3.5 PCIe x16 edge finger

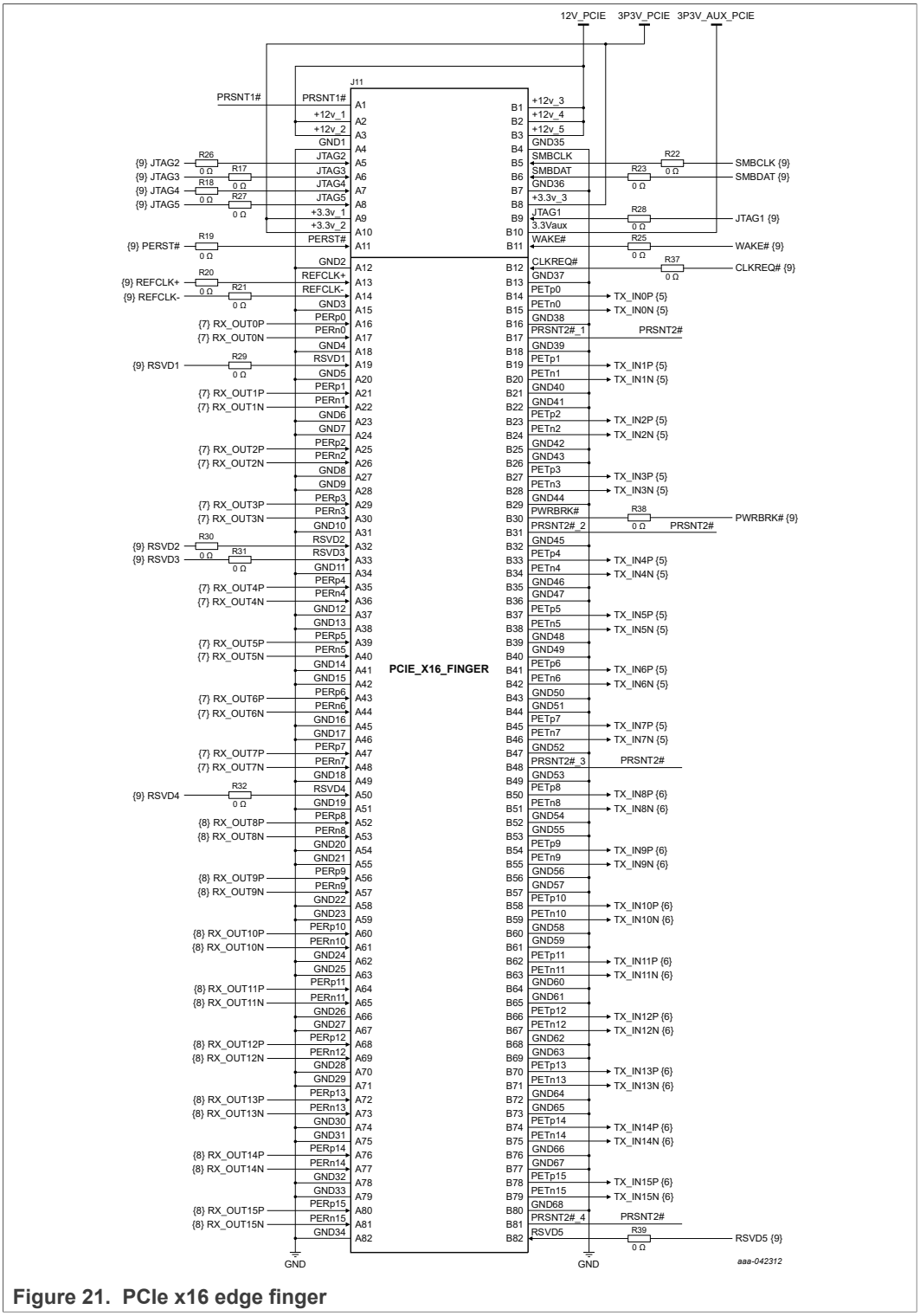


Figure 21. PCIe x16 edge finger

2.3.6 PCIe x16 straddle mount connector

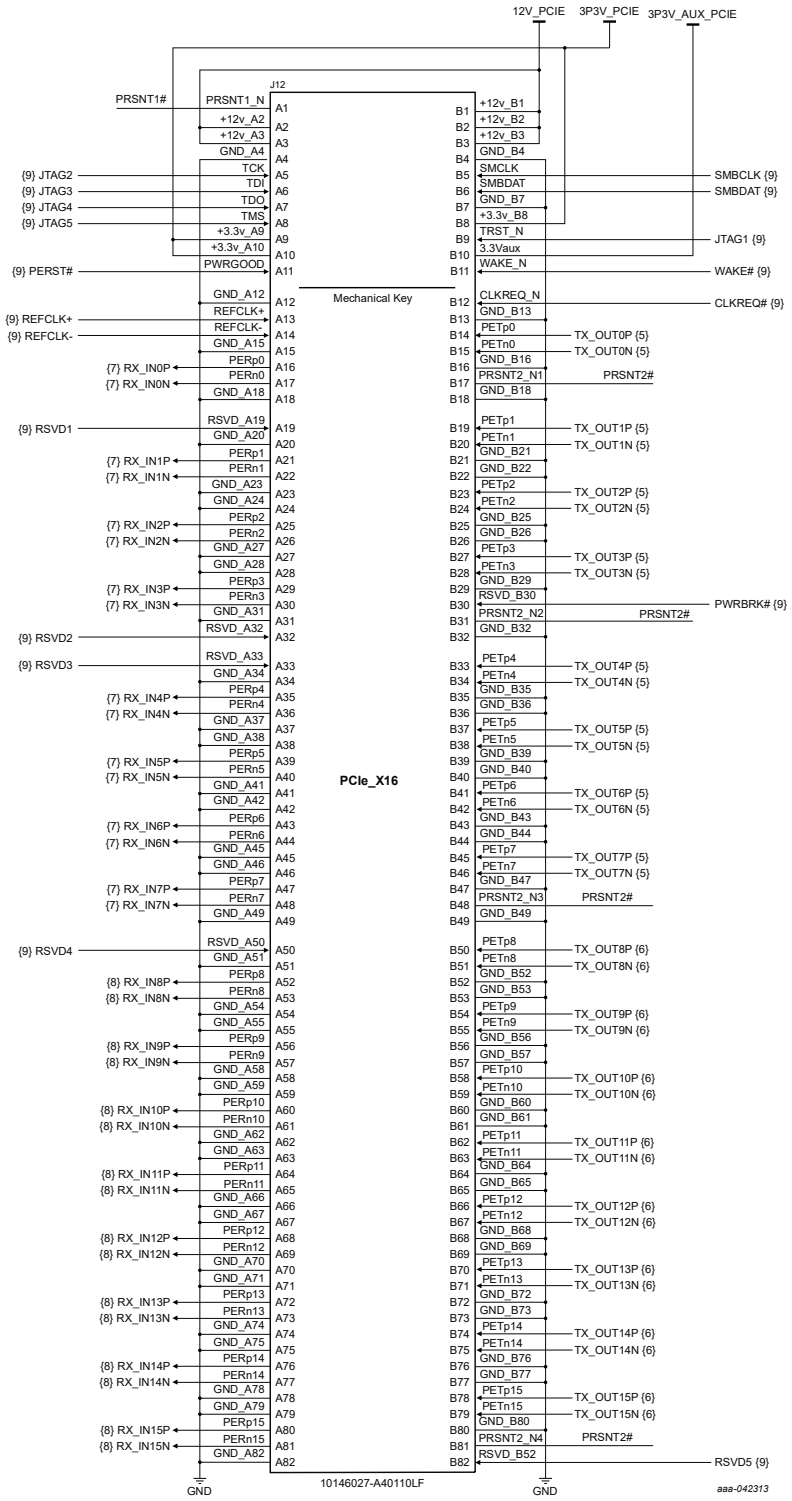


Figure 22. PCIe straddle mount connector

2.3.7 I²C controls

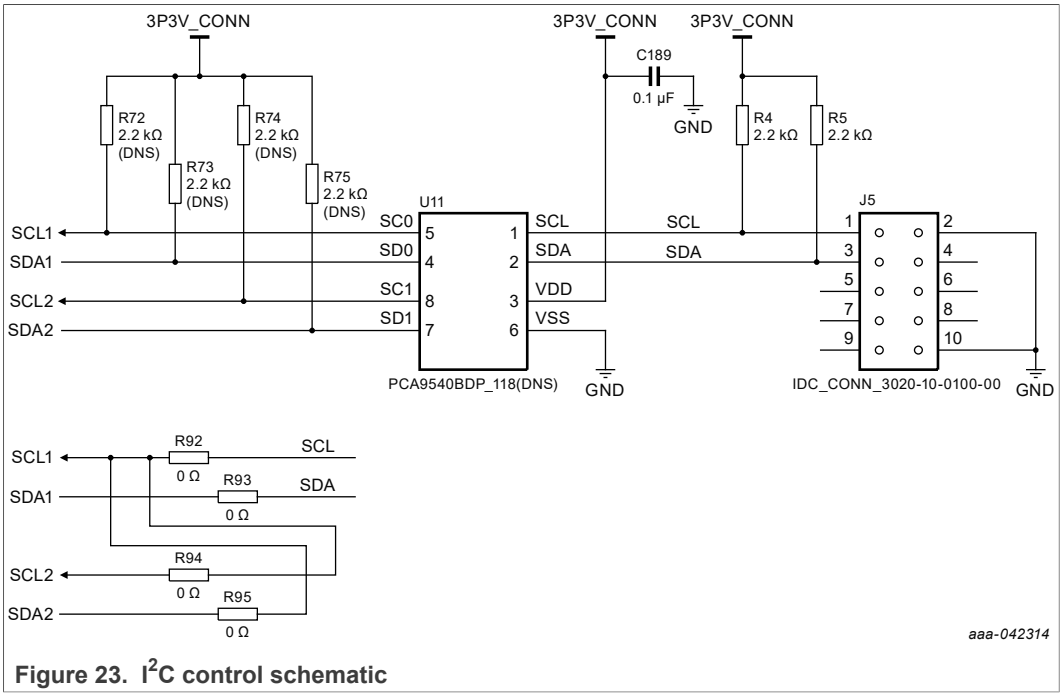


Figure 23. I²C control schematic

To configure the equalizer and output swing level settings on an 8x PTN3944 using the same I²C bus, connect an I²C bus connector to the USB-to-I²C tool (NXP LPCUSBSIO). An I²C MUX (U11) on the board is not populated. U11 was used to control the previous generation of the device (PTN38006) which supported only four I²C addresses. Since PTN3944 supports up to 32 I²C addresses, the I²C MUX is no longer needed.

2.3.8 Power supplies

Power to the AIC is supplied from either the PCIe gold finger 3.3 V connection, or from an external 5 V barrel input. When all 8 pieces of PTN3944 are active, the AIC consumes up to 2 A of current at 1.8 V. NXP recommends using an external 5 V, 1 A supply (close J17 pin 1-2) for evaluation.

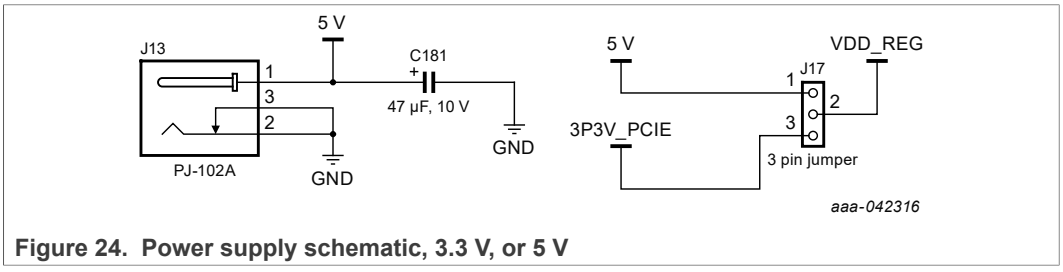


Figure 24. Power supply schematic, 3.3 V, or 5 V

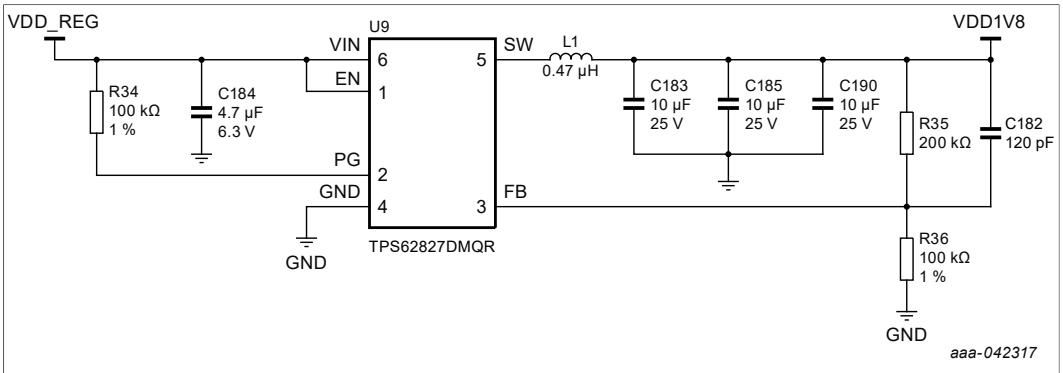


Figure 25. Power supply schematic

A 3.3 V LDO provides power to I^2C MUX and I^2C pull-up resistors. As previously mentioned, the I^2C MUX is not populated. The 3.3 V power supplies only the I^2C pull-up resistors. The 3.3 V LDO is not populated, and uses 3.3 V from the PCIe gold finger (close J16 pin 2-3).

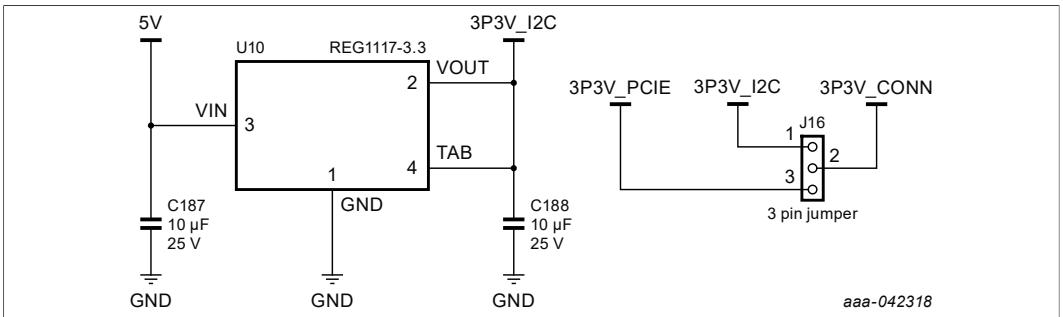


Figure 26. Power schematic

3 LPCUSBSIO module

To demonstrate the programmability of PTN3944 through the I^2C interface, use the LPCUSBSIO module with PTN3944 PCIe AIC. The main function of the LPCUSBSIO module is to provide a USB-to-I^2C bridge. Using a USB2 interface, the bridge allows users to connect the module to a PC and exercise the I^2C interface with each PTN3944 on the AIC. A GUI monitors and/or configures the settings for each PTN3944.

3.1 PCB photographs

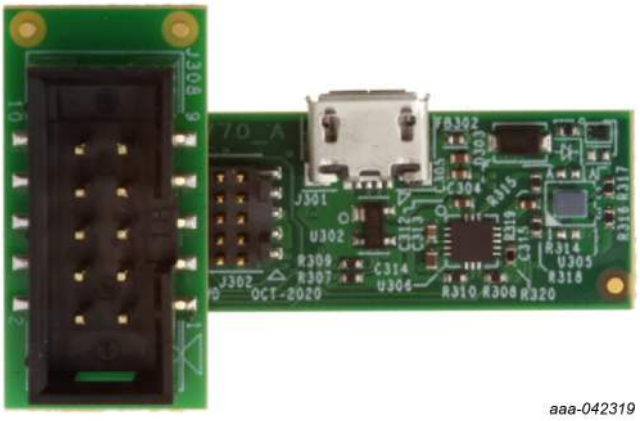


Figure 27. USB-to-I²C tool (NXP LPCUSBSIO) front side

Figure 28. USB-to-I²C tool (NXP LPCUSBSIO) back side

3.2 Connection

The PTN3944 PCIe AIC and LPCUSBSIO module are connected by a 10-pin ribbon cable. First, attach a 50 mil to 100 mil adapter to the LPCUSBSIO J303 connector. Then connect the ribbon cable between the adapter and the J5 connector of the AIC. In order to provide power and USB2 communication to the PC, attach a micro USB cable to the J301 connector on the LPCUSBSIO module.

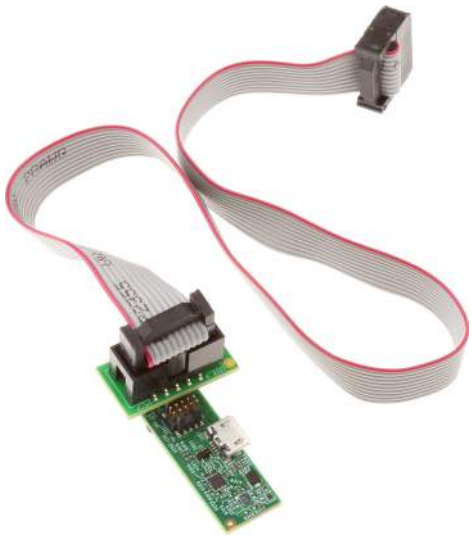


Figure 29. LPCUSBSIO base board with attached cable

3.3 Firmware update

From time to time, NXP provides the latest firmware update for the EVM to fix issues found in the code. To perform the firmware upgrade, follow these steps:

1. Download the firmware update to the local PC from the NXP.com website.
2. Connect a Micro USB Cable on the J301 connector. Do not attach the cable into the PC until instructed.
3. Locate SW302 ISP switch on the Sniffer Based Board, and hold it down while plug in the micro USB cable to the PC. See Figure 30.
4. Locate the SW302 ISP switch on the LPCUSBSIO board.
5. While holding the SW302 ISP switch, plug in the micro USB cable to the PC. See Figure 30.

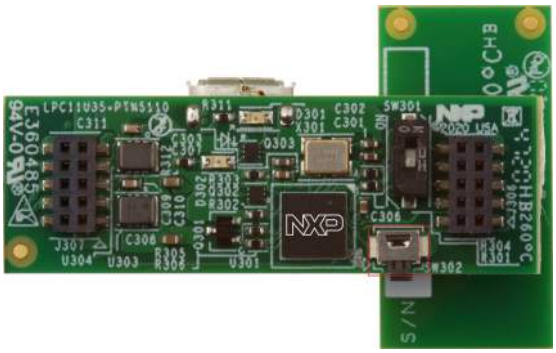


Figure 30. SW302 ISP switch identified on an assembled PTN3944 PCIe/LPCUSBSIO module

6. Release SW302 switch.

7. On the PC, a disk drive named “CRP DISABLD” appears under “computer in the left window as shown.”

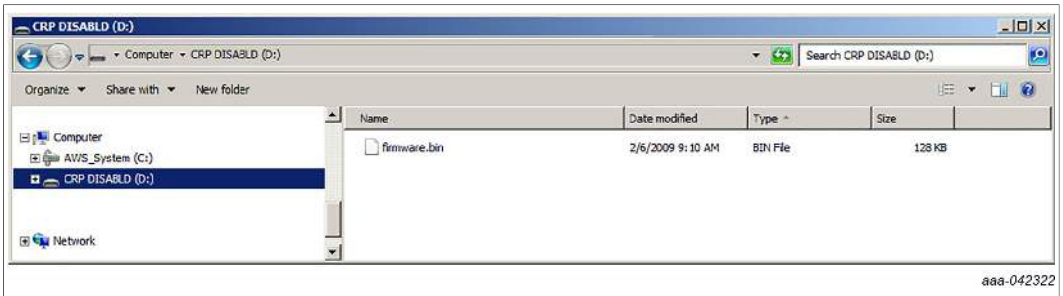


Figure 31. CRP DISABLD drive added after releasing SW302 switch

8. Right-click the prior version of “firmware.bin” in the “CRP DISABLD” driver window.
9. Select "Delete". When prompted to delete the file, click “Yes” as shown to confirm that the file should be deleted as shown.

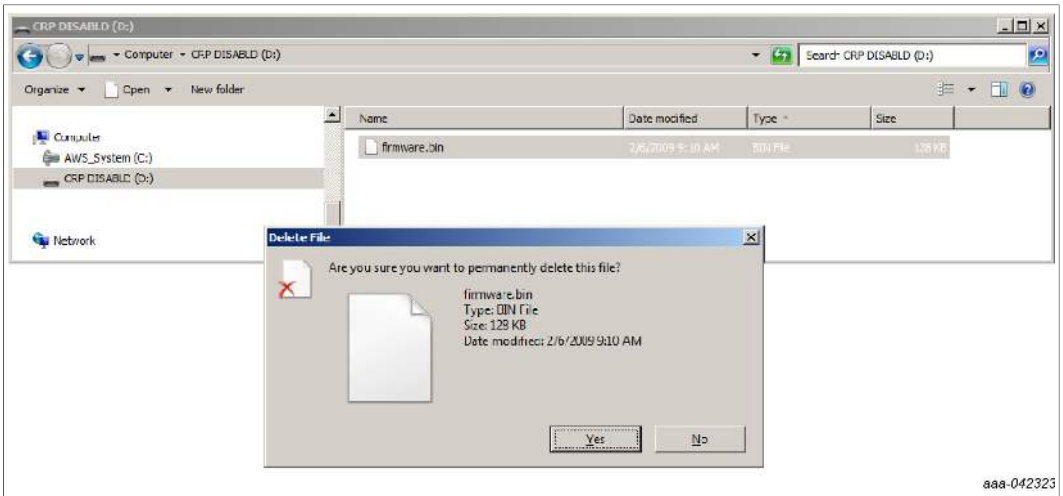


Figure 32. Deleting the current firmware.bin

10. Locate the updated firmware file with a .bin extension from the first step. Drag and drop the file into “CRP DISABLD” folder. A copy dialog displays showing the progress.

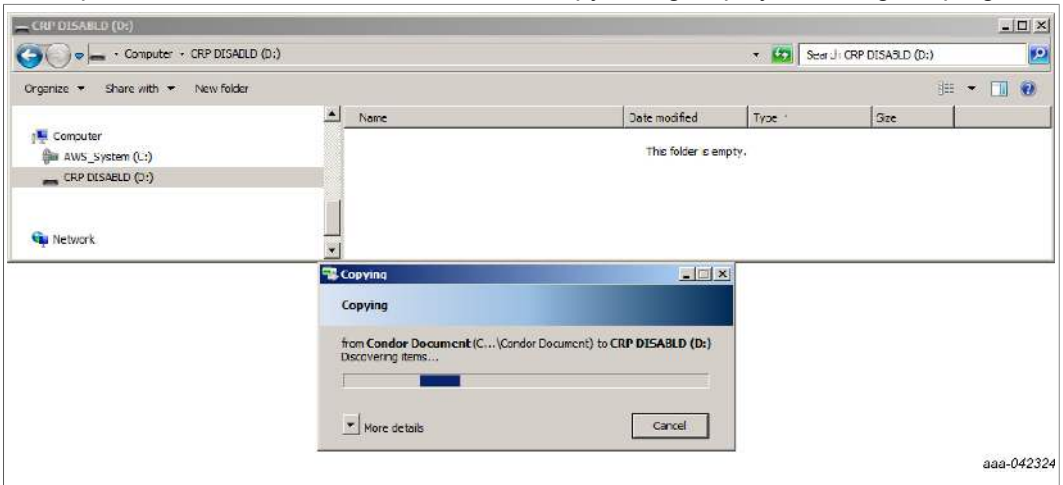


Figure 33. Adding the new firmware.bin file

11. You should see the new binary file appear in the “CRP DISABLD” drive. The firmware update is completed. Now you can remove the Micro USB cable from your computer and insert into computer again to emulate power-on reset condition.
12. After copying the new binary file completes, the updated binary file appears in the “CRP DISABLD” drive. This completes the firmware update.

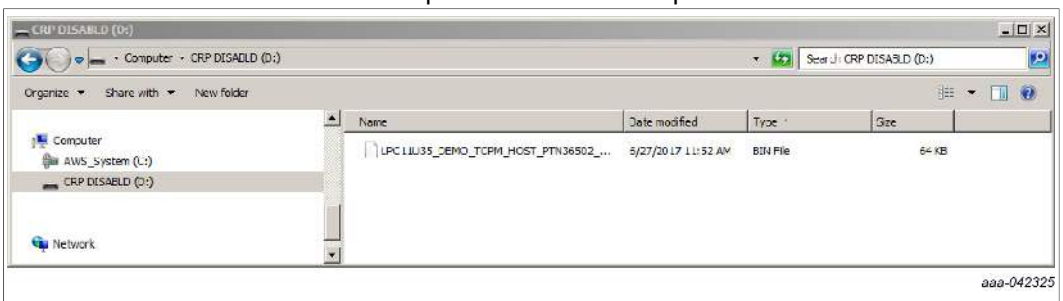


Figure 34. Update firmware added to CRP DISABLD drive

13. Detach the Micro USB cable from your computer
14. To emulate a power-on-reset condition, insert the EVM into the computer.
15. The new firmware is now running on the LPCUSBSIO module.

4 GUI introduction

The I^2C GUI control interface enables users to monitor and change the PTN3944 registers. The GUI can be used in standalone mode, or used concurrently with the LPCUSBSIO module plug-in.

4.1 List of files

The GUI zip file contains the following files:

Table 5. GUI zip file contents

File	Description
`Columbus.exe`	GUI executable. Click this file to run the GUI.
`liblpcusbsio.dll`	LPCUSBSIO library
`Script_File.txt`	A default list of script files loads when the GUI opens. Users may edit this file to revise the default scripts loaded at startup.
`PTN3944.txt`	Default product script file(s). If the file exists, for each matched product type found during the I^2C address search, a corresponding product script is executed once. These script files are useful to set up default equalizer settings.
`PTN3944_AIC_TX.txt` `PTN3944_AIC_RX.txt`	Script files for PTN3944 AIC board

4.2 Editing Script_File.txt

To load up to eight script files in the GUI, users can edit the file "Script_File.txt". The GUI refreshes the contents of this file when the GUI is first executed, or when **I2C Reset** button is clicked. Note that the following rules apply when editing the file.

- One entry per line.
- A blank line is counted as an entry without any filename loaded.

- Only the first eight lines/entries are loaded, entries after the eighth line discarded.
- When populating entries in the script file, users should ensure that the entries exist as files in the current directory. The GUI checks whether an entry is valid when the script filename is clicked in the GUI.

4.3 GUI Fields

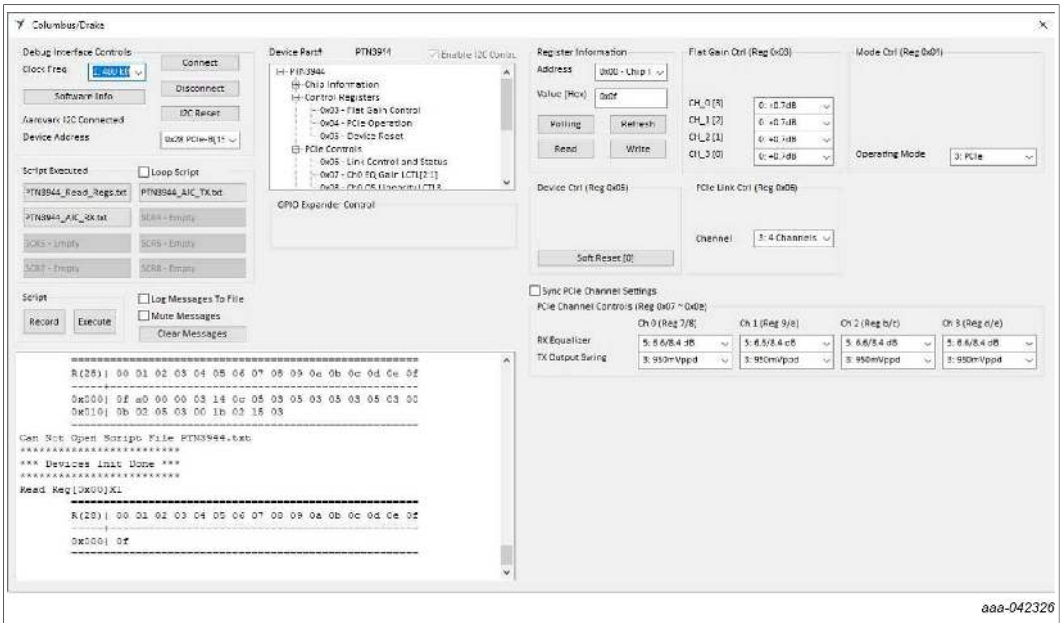


Figure 35. Graphical user interface (GUI)

4.4 Interface

Table 6. GUI debug interface controls

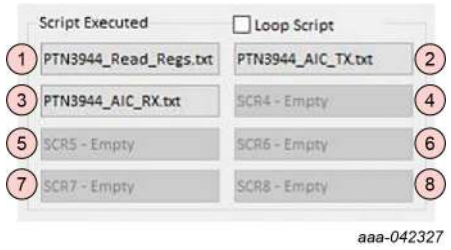
Control	Description
Connect / **Disconnect**	When the LPCUSBSIO module is disconnected from the PC (in the event of an evaluation board power cycle, or to remove USB2 cable from the module), click the **Disconnect** button then click the **Connect** button to re-initialize the LPCUSBSIO module.
I2C Reset	Clicking the **I2C Reset** button, all possible I^2C addresses in the product family are re-scanned, the evaluation board type is determined, the default product script (if it exists) is executed, and respective register values are updated onscreen.
Clock Freq	I^2C Interface clock frequency. The default value is set to 400 kHz. Users can change the interface frequency at any time, providing the clock speed is supported.

Table 6. GUI debug interface controls*...continued*

Control	Description
Device Address	The **Device Address** field shows the evaluation board type and/or a list of product I^2C addresses found in the current setup. • PCIe AIC: – 0x23 PCIe-F[3:0] – Front side, TX from motherboard to AIC – 0x22 PCIe-F[7:4] – 0x21 PCIe-F[11:8] – 0x20 PCIe-F[15:12] – 0x2B PCIe-B[3:0] – Back side, RX from AIC to motherboard – 0x2A PCIe-B[7:4] – 0x29 PCIe-B[11:8] – 0x28 PCIe-B[15:12]

4.5 Script Files

Table 7. GUI script controls

Control	Description
Script Executed	Up to eight default scripts are populated in order as shown.  **Figure 36. Default script population order into the GUI** **Script #1** **Script #2** **Script #3** **Script #4** **Script #5** **Script #6** **Script #7** **Script #8**
Loop Script	Checked: Scripts are executed in the order described (#1, #2, #3, #4, #5, #6, #7, #8), and going back to #1. If a specific script file entry is empty, that entry is skipped. Unchecked: Script execution stops.
Execute	Click **Execute** **button to load a script not currently populated in the script fields. New script files names are populated and executed in the order #1, #2, #3, #4, #5, #6, #7, #8, returning back to #1.**
Record	Use **Record** button to record current I^2C register reads/writes into a script file.

4.6 Messages

Table 8. Message controls

Control	Description
Log Messages To File	Checked: Creates a log file with current date/time stamp. All messages are logged in the file. Unchecked: Cancel file logging activity.

Table 8. Message controls...*continued*

Control	Description
Mute Messages	Checked: Most I^2C read/write messages are not displayed in the message window. I^2C read/write errors are always displayed, and cannot be turned off. Checking this option reduces the time gap between I^2C read/write transactions. Unchecked: All I^2C read/write messages display in the message window
Clear Messages	Clears all messages in the message window.
Message Window	Displays script generate messages.

4.7 Register Information

Table 9. Register controls

Control	Description
Address	The **Address** pull-down identifies the specific register address to access. Users can either select the value from the pulldown menu, or click a register address from the pull-down. a
Value (Hex)	The **Value (Hex)** register value field presents the read out or the value to be written to/from the register address field.
Read	The **Read** button performs a read operation from the register address field. The read out value is populated in the **Value (Hex)** field.
Write	The **Write** button performs a write operation to the register address field. The write value is loaded from the **Value (Hex)** field.
Polling	The **Polling** button performs a repetitive read operation from the register address. The read out value populates the **Value (Hex)** field. The repetitive read operation continues until the **Polling** is pressed again, terminating the repetitive read.
Refresh	The **Refresh** button performs a repetitive read operation across all registers. The read out values are populated in the GUI directly. The repetitive read operation continues until the **Refresh** button is pressed again, terminating the repetitive read across all registers.

4.8 PTN3944 Register Fields Setup

To view the Graphical User Interface, refer to Section 4.3 "GUI Fields", Figure 35.

4.8.1 Suggested Scrpt_File.txt content

Table 10. Examples of script file content

File	Description
PTN3944_AIC_TX.txt	Example EQ/OSL settings for PCIe Gen 4 TX Compliance Test

Table 10. Examples of script file content*...continued*

File	Description
Equivalent Jumper Setting	

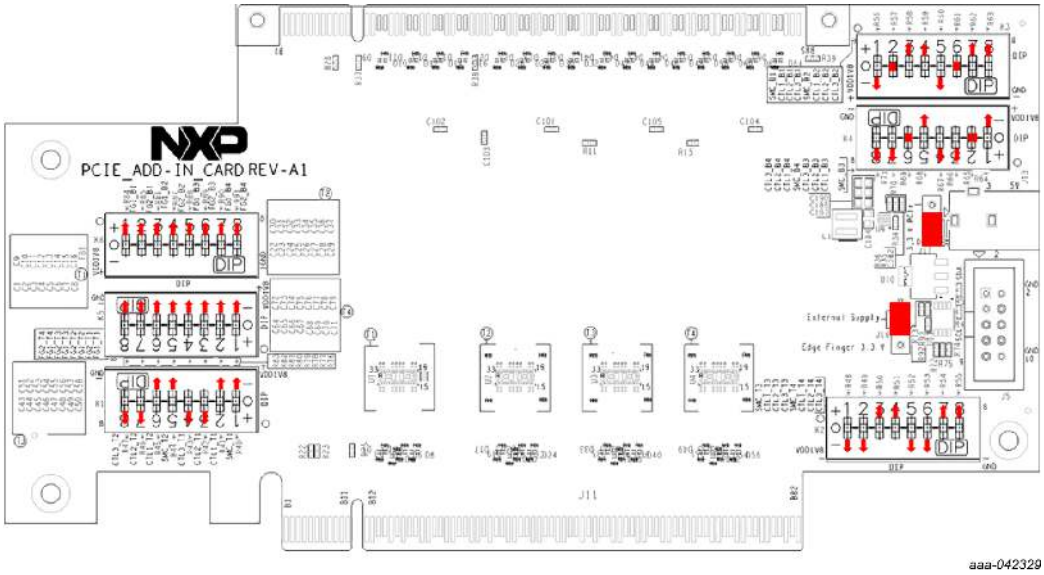


Figure 37. Example EQ/OSL settings for PCIe Gen 4 TX compliance test

```
%Top LCTRL[2:1]=[1,0] {EQ=11.5dB@8GHz}
%Top LCTRL[3]=1 {OSL=950mVppd}
%Top FG[2:1]=[0,0] {+0.7dB on All Channels}
DUT[0x23-20][0x07] = 0x07 0x03 0x07 0x03 0x07 0x03 0x07 0x03;
DUT[0x23-20][0x03] = 0x00;
%Bottom LCTRL[2:1]=[1,z] {EQ=9.1dB@8GHz}
%Bottom LCTRL[3]=1 {OSL=950mVppd}
%Bottom FG[2:1]=[1,1] {-0.7dB on All Channels}
DUT[0x2b-28][0x07] = 0x05 0x03 0x05 0x03 0x05 0x03 0x05 0x03;
DUT[0x2b-28][0x03] = 0x0f;
```

PTN3944_AIC_RX.txt	Example EQ/OSL settings for PCIe Gen 4 RX Compliance Test

Table 10. Examples of script file content*...continued*

File	Description
Example Jumper Setting	

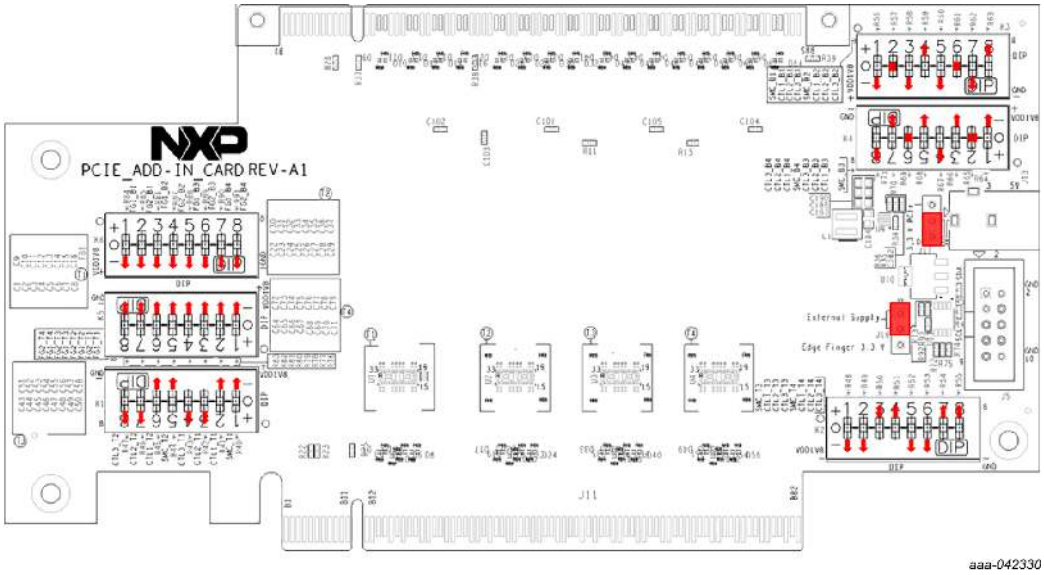


Figure 38. Example EQ/OSL settings for PCIe Gen 4 RX compliance test

```
%Top LCTRL[2:1]=[1,0] {EQ=11.5dB@8GHz}
%Top LCTRL[3]=1 {OSL=950mVppd}
%Top FG[2:1]=[0,0] {+0.7dB on All Channels}
DUT[0x23-20][0x07] = 0x07 0x03 0x07 0x03 0x07 0x03 0x07 0x03;
DUT[0x23-20][0x03] = 0x00;
%Bottom LCTRL[2:1]=[0,z] {EQ=3.0dB@8GHz}
%Bottom LCTRL[3]=1 {OSL=950mVppd}
%Bottom FG[2:1]=[0,0] {+0.7dB on All Channels}
DUT[0x2b-28][0x07] = 0x00 0x03 0x00 0x03 0x00 0x03 0x00 0x03;
DUT[0x2b-28][0x03] = 0x00;
```

4.8.2 Other Controls

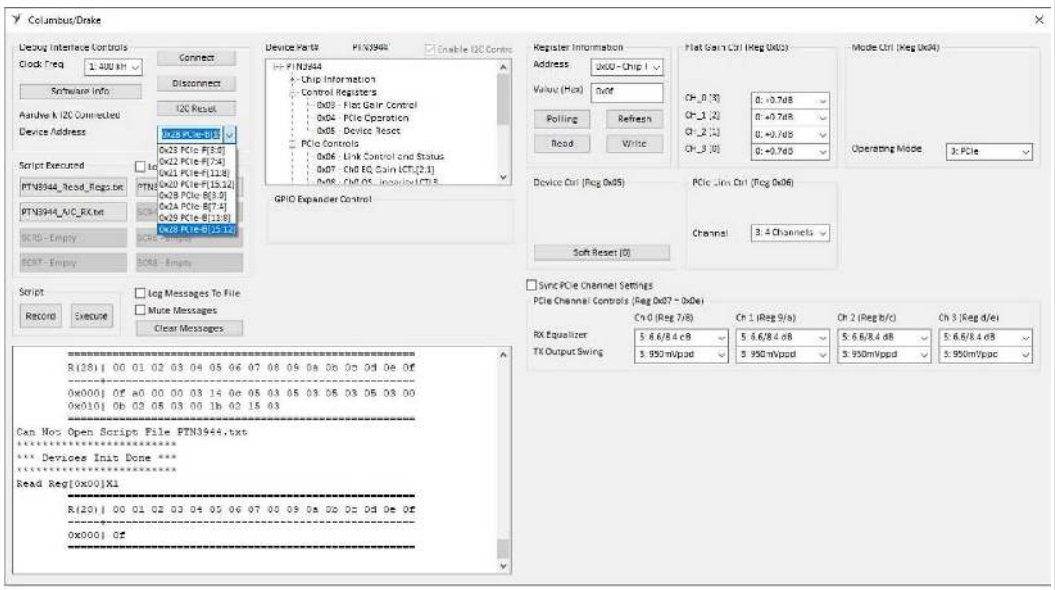


Figure 39. Device address and Sync PCIe channel settings

4.8.2.1 Device Address pulldown menu

When a PTN3944 PCIe Add-In-Card (AIC) is detected, the device address pull-down displays all detected devices (with their respective I^2C device addresses). If less than 8 PTN3944 devices are detected, a connection or soldering issue may exist. Contact NXP for a new evaluation board. See Figure 39.

Table 11. Device address pulldown menu

Pulldown menu displays:	I^2C Address	Lanes on IC Mapped to AIC's Lane	TX/RX direction
0x23 PCIe-F[3:0]	0x23	IC_LANE[3:0] = PCIe_TX[3:0]	Front Side Chipset TX to AIC Direction
0x22 PCIe-F[7:4]	0x22	IC_LANE[3:0] = PCIe_TX[7:4]	
0x21 PCIe-F[11:8]	0x21	IC_LANE[3:0] = PCIe_TX[11:8]	
0x20 PCIe-F[15:12]	0x20	IC_LANE[3:0] = PCIe_TX[15:12]	
0x2B PCIe-B[3:0]	0x2B	IC_LANE[3:0] = PCIe_RX[3:0]	Back Side Chipset RX from AIC Direction
0x2A PCIe-B[7:4]	0x2A	IC_LANE[3:0] = PCIe_RX[7:4]	
0x29 PCIe-B[11:8]	0x29	IC_LANE[3:0] = PCIe_RX[11:8]	
0x28 PCIe-B[15:12]	0x28	IC_LANE[3:0] = PCIe_RX[15:12]	

4.8.2.2 Sync PCIe Channel Settings checkbox

When the Sync PCIe Channel Settings checkbox is selected, if either the EQ or Output Swing Level (OSL) is changed, the same values for both EQ and OL are applied to other lanes in the same IC. The values are also applied to other lanes/ICs of the same TX/RX function. For example, if the EQ/OSL settings on PCIe_TX[13] are changed, the same EQ/OSL settings are updated for PCIe_TX[15, 14, 12] (on the same IC, I^2C address 0x20), and also for PCIe_TX[3:0] (I^2C address 0x23), PCIe_TX[7:4] (I^2C address 0x22) and PCIe_TX[11:8] (I^2C address 0x21).

5 Legal information

5.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

5.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer. In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages. Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

5.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Figures

Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 14 July 2021
Document identifier: UM11596