TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7W240FU

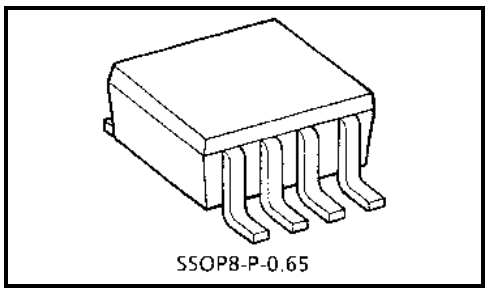
Inverted, 3-State Outputs

The TC7W240FU is a high speed C^2MOS Dual Bus Buffers fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the C^2MOS low power dissipation.

It is an inverting 3-state buffer having two active-low output enables.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



Weight: 0.02 g (typ.)

Features

- High speed: t_{pd} = 10 ns (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 2 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Output drive capability: 15 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 6 mA (min)
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V

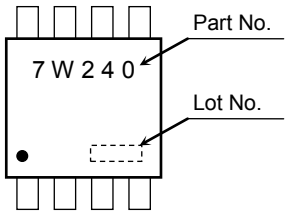
Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±35	mA
DC V_{CC}/ground current	I_{CC}	±37.5	mA
Power dissipation	P_D	300	mW
Storage temperature range	T_{stg}	−65 to 150	°C
Lead temperature (10 s)	T_L	260	°C

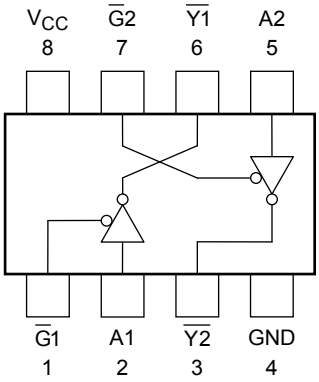
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production
1993-04

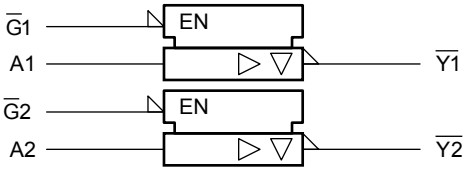
Marking



Pin Configuration (top view)



Logic Diagram



Truth Table

Inputs		Output
$\overline{G}$	A	$\overline{Y}$
L	L	H
L	H	L
H	X	Z

X: Don't care
Z: High impedance

Operating Ranges

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature range	T_{opr}	−40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 (V_{CC} = 2.0 V)	ns
		0 to 500 (V_{CC} = 4.5 V)	
		0 to 400 (V_{CC} = 6.0 V)	

Electrical Characteristics

DC Electrical Characteristics

Characteristics		Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = –40 to 85°C Min	Ta = –40 to 85°C Max	Unit
Input voltage	High level	V_{IH}	—		2.0	1.5	—	—	1.5	—	V
					4.5	3.15	—	—	3.15	—	
					6.0	4.2	—	—	4.2	—	
	Low level	V_{IL}	—		2.0	—	—	0.5	—	0.5	
					4.5	—	—	1.35	—	1.35	
					6.0	—	—	1.8	—	1.8	
Output voltage	High level	V_{OH}	$V_{IN} = V_{IL}$	I_{OH} = –20 μA	2.0	1.9	2.0	—	1.9	—	V
					4.5	4.4	4.5	—	4.4	—	
					6.0	5.9	6.0	—	5.9	—	
				I_{OH} = –6 mA	4.5	4.18	4.31	—	4.13	—	
				I_{OH} = –7.8 mA	6.0	5.68	5.80	—	5.63	—	
	Low level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0	0.1	—	0.1	
					4.5	—	0	0.1	—	0.1	
					6.0	—	0	0.1	—	0.1	
				I_{OL} = 6 mA	4.5	—	0.17	0.26	—	0.33	
				I_{OL} = 7.8 mA	6.0	—	0.18	0.26	—	0.33	
3-state output off-state current		I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND		6.0	—	—	±0.5	—	±5.0	μA
Input leakage current		I_{IN}	$V_{IN} = V_{CC}$ or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current		I_{CC}	$V_{IN} = V_{CC}$ or GND		6.0	—	—	2.0	—	20.0	μA

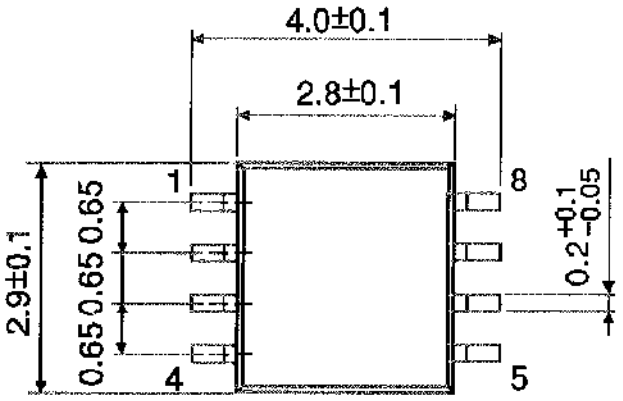
AC Electrical Characteristics (input $t_r = t_f = 6$ ns)

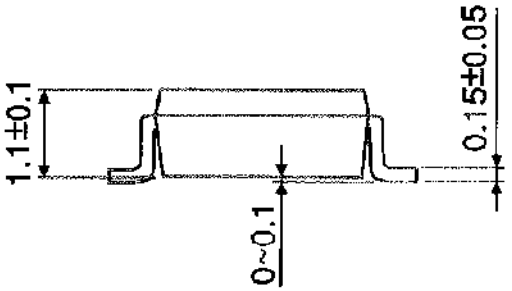
Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			$C_{L(pF)}$	V_{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time	t_{TLH} t_{THL}	—	50	2.0	—	25	60	—	75	ns
				4.5	—	7	12	—	15	
				6.0	—	6	10	—	13	
Propagation delay time	t_{pLH} t_{pHL}	—	50	2.0	—	36	90	—	115	ns
				4.5	—	12	18	—	23	
				6.0	—	10	15	—	20	
			150	2.0	—	51	130	—	165	ns
				4.5	—	17	26	—	33	
				6.0	—	14	22	—	28	
Output enable time	t_{pZL} t_{pZH}	R_L = 1 kΩ	50	2.0	—	48	125	—	155	ns
				4.5	—	16	25	—	31	
				6.0	—	14	21	—	26	
			150	2.0	—	63	165	—	205	ns
				4.5	—	21	33	—	41	
				6.0	—	18	28	—	35	
Output disable time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	50	2.0	—	32	125	—	155	ns
				4.5	—	15	25	—	31	
				6.0	—	14	21	—	26	
Input capacitance	C_{IN}	—	—	—	—	5	10	—	10	pF
Output capacitance	C_{OUT}	—	—	—	—	10	—	—	—	pF
Power dissipation capacitance	C_{PD}	(Note)	—	—	—	31	—	—	—	pF

Note: C_{PD} is defined as the value of internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per gate)

Package Dimensions

SSOP8-P-0.65 Unit : mm





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