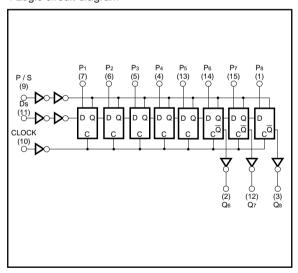
8-bit static shift register BU4021B / BU4021BF

The BU4021B and BU4021BF are 8-bit static shift registers consisting of 8 register cells, each of which has parallel input. Control of the parallel / serial control input (P / S) enables serial input / serial output with clock synchronization, as well as parallel input / serial output conversions.

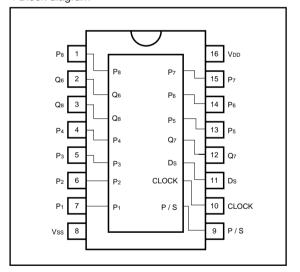
● Absolute maximum ratings (Vss = 0V, Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V _{DD}	- 0.3 ~ + 18	V
Power dissipation	Pd	1000 (DIP), 500 (SOP)	mW
Operating temperature	Topr	- 40 ~ + 85	°C
Storage temperature	Tstg	- 55 ~ + 150	°C
Input voltage	Vin	- 0.3 ~ V _{DD} + 0.3	V

■Logic circuit diagram



●Block diagram



Truth tableSerial operation

	•					
t	CLOCK	Ds	P/S	$Q_6 $ (t = n + 6)	Q_7 $(t = n + 7)$	$Q_8 $ $(t = n + 8)$
n	<u>_</u>	L	L	0	?	?
n + 1		Н	L	1	0	?
n + 2	ⅎ	L	L	0	1	0
n + 3		Н	L	1	0	1
	¬L	Χ	L	Q ₆	Q ₇	Q ₈

Parallel operation

CLOCK	Ds	P/S	Dm	Q _m *
	Χ	Н	L	L
	Χ	Н	Н	Н

X. Irrelevant

^{*:} Q6, Q7, and Q8 are external

Electrical characteristics

DC characteristics (unless otherwise noted, Ta = 25°C, Vss = 0V)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions	
Falailletei						V _{DD} (V)	Conditions
-		3.5	_	_	٧	5	
Input high level voltage	ViH	7.0	_	_		10	_
		11.0	_	_		15	
		_	_	1.5	V	5	
Input low level voltage	VIL	_	_	3.0		10	_
		_	_	4.0		15	
Input high level current	lін	_	_	0.3	μΑ	15	V _{IH} = 15V
Input low level current	lıL	_	_	- 0.3	μΑ	15	VIL = 0V
	Vон	4.95	_	_	V	5	
Output high level voltage		9.95	_	_		10	lo = 0mA
		14.95	_	_		15	
	Vol	_	_	0.05	V	5	lo = 0mA
Output low level voltage		_	_	0.05		10	
		_	_	0.05		15	
	Іон	- 0.16	_	_		5	Voн = 4.6V
Output high level current		- 0.4	_	_	mA	10	Vон = 9.5V
		- 1.2	_	_		15	Voн = 13.5V
Output low level current	Іоь	0.44	_	_	mA	5	Vol = 0.4V
		1.1	_	_		10	Vol = 0.5V
		3.0	_	_		15	Vol = 1.5V
	IDD	_	_	20	μΑ	5	
Static current dissipation		_	_	40		10	VI = VDD, GND
		_	_	80		15	

Switching characteristics (unless otherwise noted, Vss = 0V, Ta = 25°C, CL = 50pF)

Parameter	Symbol	Min.	Typ	Max.	Unit		Conditions	Measurement circuit
			Тур.			V _{DD} (V)	Conditions	
		_	180	_	ns	5		Fig.1
Output rise time	tтьн	_	90	_		10	_	
		_	65	_		15		
		_	100	_	ns	5		Fig.1
Output fall time	tтнL	_	50	_		10	_	
		_	40	_		15		
"L" to "H"		_	400	_		5		Fig.1
propagation delay time	t PLH	_	170	_	ns	10	_	
CLOCK to Q, P / S to Q		_	115	_		15		
"H" to "L"		_	400	_		5		Fig.1
propagation delay time	tрнL	_	170	_	ns	10	_	
CLOCK to Q, P / S to Q		_	115	_		15		
	t su	_	150	_	ns	5		Fig.1
Setup time		_	50	_		10	_	
		_	30	_		15		
	tw (CLK)	_	150	_	ns	5	_	Fig.1
Minimum clock pulse width		_	75	_		10		
		_	40	_		15		
	f (CLK) Max.	_	3.0	_		5		Fig.1
Maximum clock frequency		_	6.0	_	MHz	10	_	
ricquericy		_	8.0	_		15		
Maximum clock rise / fall time	tr (CLK) tr (CLK)	_	_	15	μs	5		Fig.1
		_	_	5.0		10	_	
		_	-	4.0		15		
	t w (P/S)	_	150	_	ns	5		_
Minimum P / S control pulse width		_	75	_		10	_	
Control pulse width		_	40	_		15		
Input capacitance	Cin	_	5	_	pF	_		

Measurement circuit

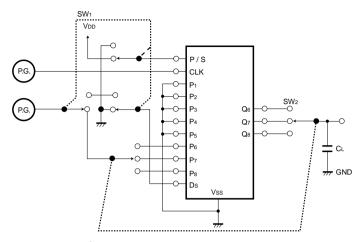


Fig.1 Switching characteristics measurement circuit

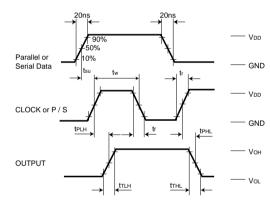


Fig.2 Switching characteristics waveform

•Electrical characteristic curve

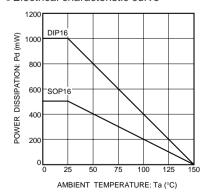
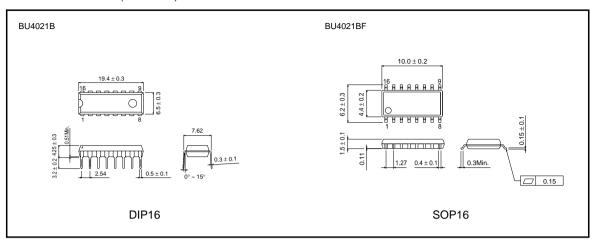


Fig.3 Power dissipation vs. ambient temperature

●External dimensions (Units: mm)



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