

### FEATURES

**Driver, comparator, and active load**  
**500 MHz toggle rate**  
**Inhibit mode function**  
**Dynamic clamps**  
**Operating voltage range:  $-1.5\text{ V}$  to  $6.5\text{ V}$**   
**Output voltage swing:  $200\text{ mV}$  to  $8\text{ V}$**   
**Four range adjustable slew rate**  
**True/complement data mode bit**  
**100-lead TQFP package, exposed pad**  
**Low per channel power**  
      **$1.4\text{ W}$  with load off**  
      **$1.75\text{ W}$  with load programmed at  $20\text{ mA}$  nominal**  
**Low leakage ( $<10\text{ nA}$ ) in High-Z mode**  
**Driver**  
      **$50\ \Omega$  output resistance**  
      **$1\text{ ns}$  minimum pulse width for a  $3\text{ V}$  step**  
**Load:  $-35\text{ mA}$  to  $+35\text{ mA}$  maximum current range**

### APPLICATIONS

**Automatic test equipment**  
**Semiconductor test systems**  
**Board test systems**  
**Instrumentation and characterization equipment**

### GENERAL DESCRIPTION

The ADATE206 is a complete, single-chip solution that performs the pin electronics functions of driver, comparator, and active load (DCL) for ATE applications. The active load can be powered down if not used.

The driver is a proprietary design that features three active modes: data high mode, data low mode, and term mode, as well as an inhibit state. The driver has low leakage ( $<10\text{ nA}$ ) in High-Z mode. The output voltage range is  $-1.5\text{ V}$  to  $+6.5\text{ V}$  to accommodate a wide variety of test devices.

The ADATE206 supports four programmable  $T_r/T_f$  times for applications where slower edge rates are required. The edge rate selection is done via two static digital CMOS select bits. The input data to the driver can be inverted using a single CMOS logic bit. This feature can be used for system calibration or applications where complement input data is needed.

### FUNCTIONAL BLOCK DIAGRAM

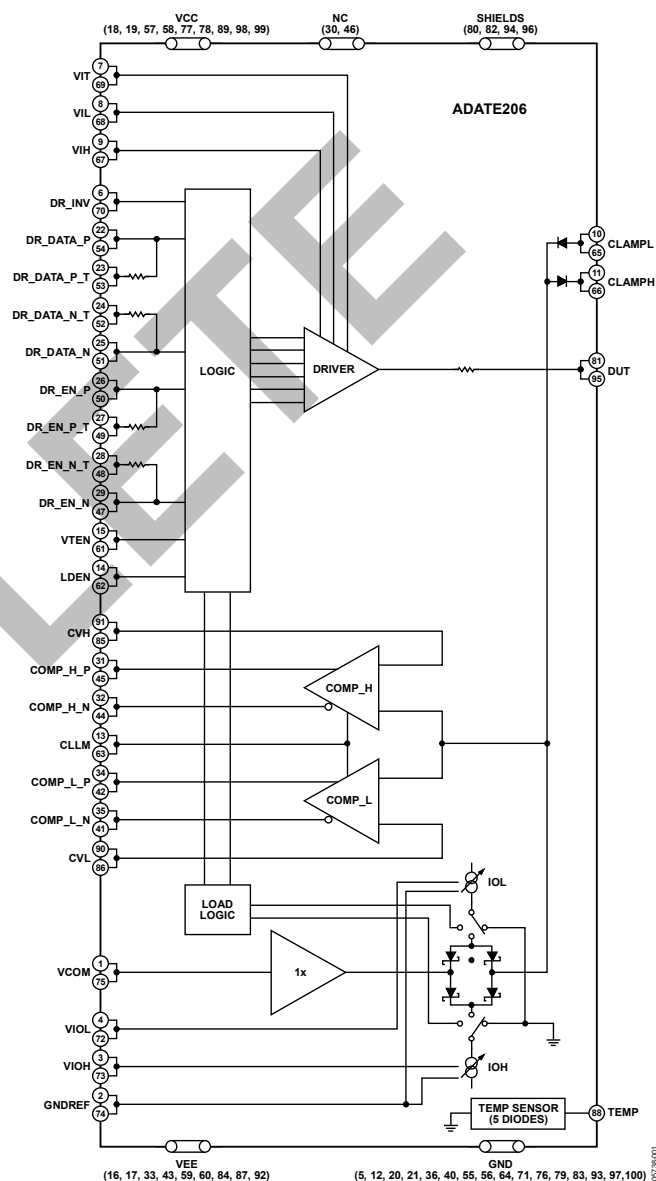


Figure 1.

#### Rev. A

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

|                                  |   |                                                  |    |
|----------------------------------|---|--------------------------------------------------|----|
| Features .....                   | 1 | Absolute Maximum Ratings .....                   | 8  |
| Applications.....                | 1 | ESD Caution.....                                 | 8  |
| General Description .....        | 1 | Pin Configuration and Function Descriptions..... | 9  |
| Functional Block Diagram .....   | 1 | Typical Performace Characteristics .....         | 12 |
| Table of Contents .....          | 2 | Theory of Operation .....                        | 15 |
| Revision History .....           | 2 | Outline Dimensions .....                         | 16 |
| Specifications.....              | 3 | Ordering Guide .....                             | 16 |
| Electrical Characteristics ..... | 3 |                                                  |    |

REVISION HISTORY

- 10/08— Rev. 0 to Rev. A**  
Changes to the VCOM Buffer Offset Parameter, Table 1..... 7
- 1/06— Revision 0: Initial Version**

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

$V_{CC} = 10.0\text{ V}$ ,  $V_{EE} = -5.0\text{ V}$ ,  $T_J = 75^\circ\text{C}$ , unless otherwise noted.

**Table 1.**

| Parameter                                                                         | Min       | Typ            | Max  | Unit          | Test Conditions/Comments                                                                                                    |
|-----------------------------------------------------------------------------------|-----------|----------------|------|---------------|-----------------------------------------------------------------------------------------------------------------------------|
| <b>DRIVER</b>                                                                     |           |                |      |               |                                                                                                                             |
| Single-Ended Logic Input Characteristics (VTEN, DRV_INV)                          |           |                |      |               |                                                                                                                             |
| Threshold Voltage                                                                 |           | CMOS_VDD/2     |      | V             |                                                                                                                             |
| Voltage Range                                                                     | 0         |                | 5.5  | V             |                                                                                                                             |
| Bias Current                                                                      | -10       |                | +10  | $\mu\text{A}$ | $V_{IN} = 0\text{ V}, 3.3\text{ V}$                                                                                         |
| Single-Ended Logic Input Characteristics (SLEW0, SLEW1)                           |           |                |      |               |                                                                                                                             |
| Threshold Voltage                                                                 |           | CMOS_VDD/2     |      | V             |                                                                                                                             |
| Voltage Range                                                                     | 0         |                | 5.5  | V             |                                                                                                                             |
| Bias Current                                                                      | -10       | +600 (@ 3.3 V) | +800 | $\mu\text{A}$ | $V_{IN} = 0\text{ V}, 3.3\text{ V}$                                                                                         |
| Bias Current                                                                      |           | 1              |      | mA            | $V_{IN} = 5.5\text{ V}$                                                                                                     |
| Differential Logic Input Characteristics (DR_DATA_N, DR_DATA_P, DR_EN_N, DR_EN_P) |           |                |      |               |                                                                                                                             |
| Voltage Range                                                                     | -2.0      |                | +3.5 | V             |                                                                                                                             |
| Differential Voltage with LVPECL Levels                                           | $\pm 250$ | $\pm 300$      |      | mV            |                                                                                                                             |
| Bias Current                                                                      | -10       | +2             | +10  | $\mu\text{A}$ | $V_{IN} = 3.24\text{ V}, 3.495\text{ V}$                                                                                    |
| VIH, VIL Reference Inputs                                                         |           |                |      |               |                                                                                                                             |
| Input Bias Current                                                                | -10       | -2             | +10  | $\mu\text{A}$ | Maximum value bias of reference sweep                                                                                       |
| VIT Reference Inputs                                                              |           |                |      |               |                                                                                                                             |
| Input Bias Current                                                                | -25       | +12            | +25  | $\mu\text{A}$ | Maximum value bias of reference sweep                                                                                       |
| DC Output Characteristics                                                         |           |                |      |               |                                                                                                                             |
| Logic Range, VIL, VIH, VIT                                                        | -1.5      |                | +6.5 | V             |                                                                                                                             |
| Amplitude [VH to VL]                                                              |           |                | 8    | V             |                                                                                                                             |
| Output Resistance                                                                 | 47.5      |                | 52.5 | $\Omega$      |                                                                                                                             |
| PSRR, Drive or Term Mode                                                          |           | 10             |      | mV/V          | $V_{CC}, V_{EE} \pm 1\%$                                                                                                    |
| Static Current Limit                                                              | -125      | $\pm 110$      | +125 | mA            | Output to -1.5 V, $V_H = 6.5\text{ V}$ , $V_T = 0\text{ V}$                                                                 |
| Absolute Accuracy—VIH, VIL, VIT                                                   |           |                |      |               |                                                                                                                             |
| VIH Offset                                                                        | -100      | +30            | +100 | mV            | Data = H, $V_H = 0\text{ V}$ , $V_L = -1.5\text{ V}$ , $V_T = 3\text{ V}$                                                   |
| VIH Gain Error                                                                    | 0.98      |                | 1.02 | V/V           | Data = H, $V_H = 0\text{ V}$ to $5\text{ V}$ , $V_L = -1.5\text{ V}$ , $V_T = 3\text{ V}$                                   |
| VIH Linearity Error                                                               | -15       | +5             | +15  | mV            | Data = VH relative to line between $0\text{ V}$ to $5\text{ V}$ ; full range of $V_{IH} = -1.4\text{ V}$ to $+6.5\text{ V}$ |
| VIL Offset                                                                        | -100      | +30            | +100 | mV            |                                                                                                                             |
| VIL Gain Error                                                                    | 0.98      |                | 1.02 | V/V           | Data = L, $V_L = 0\text{ V}$ to $5\text{ V}$ , $V_H = 6.5\text{ V}$ , $V_T = 3\text{ V}$                                    |
| VIL Linearity Error                                                               | -15       | +5             | +15  | mV            | Data = VH relative to line between $0\text{ V}$ to $5\text{ V}$ ; full range of $V_{IH} = -1.4\text{ V}$ to $+6.5\text{ V}$ |
| VIT Offset                                                                        | -100      | +30            | +100 | mV            | Data = VT, $V_T = 0\text{ V}$ , $V_L = 0\text{ V}$ , $V_H = 3\text{ V}$                                                     |
| VIT Gain Error                                                                    | 0.98      |                | 1.02 | V/V           | Data = VT, $V_T = 0\text{ V}$ to $5\text{ V}$ , $V_L = 0\text{ V}$ , $V_H = 3\text{ V}$                                     |

# ADATE206

| Parameter                                     | Min | Typ | Max | Unit  | Test Conditions/Comments                                                                     |
|-----------------------------------------------|-----|-----|-----|-------|----------------------------------------------------------------------------------------------|
| VIT Linearity Error                           | -15 | +5  | +15 | mV    | Data = VH relative to line between 0 V to 5 V; full range of VIH = -1.4 V to +6.5 V          |
| Offset Tempco                                 |     | 80  |     | μV/°C | 65°C to 105°C                                                                                |
| Driver Interaction                            |     |     |     |       |                                                                                              |
| VH Interaction to VL                          | -2  |     | +2  | mV    | VIH = 5.0 V; VIL = -1.5 V, +4.7 V, +4.8 V, +4.9 V                                            |
| VH Interaction to VT                          | -2  |     | +2  | mV    | VIH = 3.0 V; VIT = -1.5 V, +2.9 V, +3.1 V, +6.5 V                                            |
| VL Interaction to VH                          | -2  |     | +2  | mV    | VIL = 0.0 V; VIH = 0.1 V, 0.2 V, 0.3 V, 6.5 V                                                |
| VL Interaction to VT                          | -2  |     | +2  | mV    | VIL = 0.0 V; VIT = -1.5 V, -0.1 V, +0.1 V, +6.5 V                                            |
| VT Interaction to VH                          | -2  |     | +2  | mV    | VIT = 1.5 V, VIL = -1.0 V; VIH = -0.8 V, +1.4 V, +1.6 V, +6.5 V                              |
| VT Interaction to VL                          | -2  |     | +2  | mV    | VIT = 1.5 V, VIH = 6.0 V; IL = -1.5 V, +1.4 V, +1.6 V, +5.8 V                                |
| Rise/Fall Times at Device Under Testing (DUT) |     |     |     |       |                                                                                              |
| 0.2 V Swing: Rise/Fall Time                   |     | 300 |     | ps    | Terminated 20% to 80%, VIH = 400 mV, VIL = 0 V, VIT = 0 V                                    |
| 0.5 V Swing: Rise/Fall Time                   |     | 350 |     | ps    | Terminated 10% to 90%, VIH = 1.0 V, VIL = 0 V, VIT = 0 V                                     |
| 1 V Swing: Rise/Fall Time                     |     | 500 |     | ps    | Terminated 10% to 90%, VIH = 2.0 V, VIL = 0 V, VIT = 0 V                                     |
| 3 V Swing: Rise/Fall Time                     |     | 650 |     | ps    | Unterminated 10% to 90%, VIH = 3.0 V, VIL = 0 V, VIT = 0 V                                   |
| 3 V Swing: Rise/Fall Time                     | 350 | 450 | 550 | ps    | Terminated 20% to 80%, VIH = 3.0 V, VIL = 0 V, VIT = 0 V using DUT comparator                |
| 5 V Swing: Rise/Fall Time                     |     | 1.1 |     | ns    | Unterminated 10% to 90%, VIH = 5.0 V, VIL = 0 V, VIT = 0 V                                   |
| Minimum Pulse Width at DUT                    |     |     |     |       |                                                                                              |
| 500 mV Swing <sup>1</sup>                     |     | 500 |     | ps    | Terminated, VIH = 1.0 V, VIL = 0 V, VIT = 0 V                                                |
| 1.5 V Swing <sup>1</sup>                      |     | 800 |     | ps    | Terminated, VIH = 3.0 V, VIL = 0 V, VIT = 0 V                                                |
| Toggle Rate @ 3 V                             |     | 500 |     | MHz   | Unterminated, 50/50 dc measured frequency when amplitude drops 10%                           |
| Dynamic Performance, Drive (VH and VL)        |     |     |     |       |                                                                                              |
| Propagation Delay Time <sup>2</sup>           |     | 1.4 |     | ns    | Terminated, VIH = 3.0 V, VIL = 0.0 V, VIT = 0.0 V                                            |
| Propagation Delay Tempco <sup>2</sup>         |     | 2.0 |     | ps/°C | Terminated, VIH = 3.0 V, VIL = 0.0 V, VIT = 0.0 V, 65°C to 85°C                              |
| Delay Matching, Edge-to-Edge                  |     | 20  |     | ps    |                                                                                              |
| Delay Change vs. Pulse Width <sup>2</sup>     |     | 30  |     | ps    | Terminated, VIH = 3.0 V, VIL = 0.0 V, VIT = 0.0 V, 1 μs period, pulse width = 50 ns to 1 ns  |
| Delay Change vs. Duty Cycle <sup>2</sup>      |     | 5   |     | ps    | Terminated, VIH = 3.0 V, VIL = 0.0 V, VIT = 0.0 V, 1 μs period; 10%, 50%, and 90% duty cycle |

| Parameter                                                  | Min    | Typ | Max    | Unit          | Test Conditions/Comments                                                                                                  |
|------------------------------------------------------------|--------|-----|--------|---------------|---------------------------------------------------------------------------------------------------------------------------|
| Settling Time to 15 mV                                     |        | 8   |        | ns            | Terminated, $V_{IH} = 3\text{ V}$ , $V_{IL} = 0.0\text{ V}$ , $V_{IT} = 0.0\text{ V}$                                     |
| Settling Time to 4 mV                                      |        | 32  |        | ns            | Terminated, $V_{IH} = 3\text{ V}$ , $V_{IL} = 0.0\text{ V}$ , $V_{IT} = 0.0\text{ V}$                                     |
| Rise and Fall Time Temperature Coefficient<br>500 mV Swing |        | 2   |        | ps/°C         | Terminated 10% to 90%,<br>$V_{IH} = 1.0\text{ V}$ , $V_{IL} = 0.0\text{ V}$ ,<br>$V_{IT} = 0.0\text{ V}$ , 65°C to 85°C   |
| 1 V Swing                                                  |        | 2   |        | ps/°C         | Terminated 10% to 90%,<br>$V_{IH} = 2.0\text{ V}$ , $V_{IL} = 0.0\text{ V}$ ,<br>$V_{IT} = 0.0\text{ V}$ , 65°C to 85°C   |
| 3 V Swing                                                  |        | 2   |        | ps/°C         | Unterminated 10% to 90%,<br>$V_{IH} = 3.0\text{ V}$ , $V_{IL} = 0.0\text{ V}$ ,<br>$V_{IT} = 0.0\text{ V}$ , 65°C to 85°C |
| 5 V Swing                                                  |        | 2   |        | ps/°C         | Unterminated 10% to 90%,<br>$V_{IH} = 5.0\text{ V}$ , $V_{IL} = 0.0\text{ V}$ ,<br>$V_{IT} = 0.0\text{ V}$ , 65°C to 85°C |
| Overshoot and Preshoot 200 mV swing                        |        | 1   |        | %             | Terminated, $V_{IH} = 400\text{ mV}$                                                                                      |
| Overshoot and Preshoot 1 V swing                           |        | 1   |        | %             | Terminated, $V_{IH} = 2\text{ V}$                                                                                         |
| Overshoot and Preshoot 3 V swing                           |        | 2   |        | %             | Unterminated                                                                                                              |
| Overshoot and Preshoot 5 V swing                           |        | 2   |        | %             | Unterminated                                                                                                              |
| Dynamic Performance, Inhibit                               |        |     |        |               |                                                                                                                           |
| Delay Time, Active High to Inhibit <sup>3</sup>            |        | 3.1 |        | ns            | Terminated, $V_{IH} = 3.0\text{ V}$ ,<br>$V_{IL} = -1.0\text{ V}$                                                         |
| Delay Time, Active Low to Inhibit <sup>3</sup>             |        | 2.1 |        | ns            | $V_H = 3.0\text{ V}$ , $V_L = -1.0\text{ V}$ ,<br>terminated 50 $\Omega$                                                  |
| Delay Time, Inhibit to Active High <sup>3</sup>            |        | 2.5 |        | ns            | Terminated, $V_{IH} = 3.0\text{ V}$ ,<br>$V_{IL} = -1.0\text{ V}$                                                         |
| Delay Time, Inhibit to Active Low <sup>3</sup>             |        | 3.9 |        | ns            | Terminated, $V_{IH} = 3.0\text{ V}$ ,<br>$V_{IL} = -1.0\text{ V}$                                                         |
| I/O Spike                                                  |        | 350 |        | mV            | Terminated, $V_{IH} = 0.0\text{ V}$ ,<br>$V_{IL} = 0.0\text{ V}$ , $V_{IT} = 0.0\text{ V}$                                |
| <b>CLAMPS</b>                                              |        |     |        |               |                                                                                                                           |
| VCPH, VCPL Clamp Inputs                                    |        |     |        |               |                                                                                                                           |
| VCPH Voltage Range                                         | CLAMPL |     | 6.8    | V             |                                                                                                                           |
| VCPL Voltage Range                                         | -1.8   |     | CLAMPH | V             |                                                                                                                           |
| Input Bias Current                                         | -50    | -2  | +50    | $\mu\text{A}$ | Maximum value bias of<br>reference sweep = -1.8 V to<br>+6.8 V                                                            |
| Absolute Accuracy VCPH, VCPL                               |        |     |        |               |                                                                                                                           |
| VCPH Offset                                                | -100   | +55 | +100   | mV            | Driver = INH, VCPH = 0 V                                                                                                  |
| VCPH Gain Error                                            |        | 1   |        | V/V           |                                                                                                                           |
| VCPH Linearity Error                                       |        | +10 |        | mV            | Driver = INH, relative to line<br>between 0 V to 4.5 V,<br>VCPH = -1.5 V to +6.5 V,<br>VCPL = -1.8 V                      |
| VCPL Offset                                                | -100   | +55 | +100   | mV            | Driver = INH, VCPL = 0 V                                                                                                  |
| VCPL Gain Error                                            |        | 1   |        | V/V           |                                                                                                                           |
| VCPL Linearity Error                                       |        | +10 |        | mV            | Driver = INH, relative to line<br>between 0 V to 4.5 V,<br>VCPL = -1.5 V to +6.5 V,<br>VCPH = 6.5 V                       |
| <b>COMPARATOR DC SPECIFICATIONS<sup>4</sup></b>            |        |     |        |               |                                                                                                                           |
| DC Input Characteristics ( $V_{OH}$ , $V_{OL}$ )           |        |     |        |               |                                                                                                                           |
| Bias Current                                               | -10    | +5  | +10    | $\mu\text{A}$ | $V_{OH}$ and $V_{OL} = -1.5\text{ V}$ to +6.5 V                                                                           |
| Voltage Range                                              | -1.5   |     | +6.5   | V             |                                                                                                                           |
| Differential Voltage                                       | -8.0   |     | +8.0   | V             |                                                                                                                           |

# ADATE206

| Parameter                                                     | Min  | Typ        | Max  | Unit                   | Test Conditions/Comments                                                                                                                            |
|---------------------------------------------------------------|------|------------|------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| Offset                                                        | -15  |            | +15  | mV                     | Common mode = 0 V                                                                                                                                   |
| Gain Error                                                    |      | 1          |      | % FSR                  | $V_{IN} = -1.5 \text{ V to } +6.5 \text{ V}$                                                                                                        |
| Linearity Error                                               |      | 3          |      | mV                     | $V_{IN} = -1.5 \text{ V to } +6.5 \text{ V}$                                                                                                        |
| Single-Ended Logic Input Characteristics                      |      |            |      |                        |                                                                                                                                                     |
| Threshold Voltage (CLLM)                                      |      | CMOS_VDD/2 |      | V                      |                                                                                                                                                     |
| Voltage Range                                                 | 0    |            | 5.5  | V                      |                                                                                                                                                     |
| Bias Current                                                  | -10  | +160       | +200 | $\mu\text{A}$          | $V_{IN} = 0 \text{ V}, 3.3 \text{ V}$                                                                                                               |
| Bias Current                                                  |      | 260        |      | $\mu\text{A}$          | $V_{IN} = 5.5 \text{ V}$                                                                                                                            |
| Digital Output Characteristics<br>(VOH, VOL Levels)           |      |            |      |                        |                                                                                                                                                     |
| Logic 1                                                       | 3.1  | 3.26       | 3.4  | V                      | Terminated 50 $\Omega$ to 3.3 V                                                                                                                     |
| Logic 0                                                       | 2.7  | 2.86       | 3.1  | V                      | Terminated 50 $\Omega$ to 3.3 V                                                                                                                     |
| Differential Levels                                           | 350  | 400        | 450  | mV                     | Terminated 50 $\Omega$ to 3.3 V                                                                                                                     |
| COMPARATOR AC SPECIFICATIONS                                  |      |            |      |                        |                                                                                                                                                     |
| Propagation Delay                                             |      |            |      |                        |                                                                                                                                                     |
| Input to Output                                               |      | 500        |      | ps                     | $V_{IN} = 3 \text{ V p-p}, 2 \text{ V/ns}$                                                                                                          |
| Propagation Delay Tempco                                      |      | 1.0        |      | ps/ $^{\circ}\text{C}$ | $V_{IN} = 3 \text{ V p-p}, 2 \text{ V/ns}$                                                                                                          |
| Propagation Delay Change with Respect to<br>PD vs. Duty Cycle |      | 40         |      | ps                     | $V_{IN} = 0 \text{ V to } 3 \text{ V}, 2 \text{ V/ns}$ , driver in<br>VTERM, VIT = 0 V, period = 10 ns;<br>dc = 1 ns, 5 ns, 9 ns                    |
| Slew Rate: 1 V/ns, 2 V/ns, 3 V/ns                             |      | 30         |      | ps                     | $V_{IN} = 0 \text{ V to } 3 \text{ V}$ , driver in VTERM,<br>VIT = 0 V                                                                              |
| Amplitude: 500 mV, 1.0 V, 3.0 V                               |      | 30         |      | ps                     | $V_{IN} = 0 \text{ V to } 500 \text{ mV}, 0 \text{ V to } 1 \text{ V}, 0 \text{ V to } 3 \text{ V}, 2 \text{ V/ns}$ , driver in VTERM,<br>VIT = 0 V |
| Equivalent Input Rise Time                                    |      | 225        |      | ps                     | $V_{IN} = 0 \text{ V to } 1 \text{ V}, <50 \text{ ps}$ , 20% to<br>80% rise time, driver in VTERM =<br>0 V                                          |
| Pulse-Width Linearity                                         |      | 20         |      | ps                     | $V_{IN} = 0 \text{ V to } 3 \text{ V}, 2 \text{ V/ns}$ ; pulse<br>width = 3 ns, 4 ns, 5 ns, 10 ns;<br>driver in VTERM, VIT = 0 V                    |
| Settling Time                                                 |      | 5.5        |      | ns                     | Settling to $\pm 8 \text{ mV}$ , $V_{IN} = 0 \text{ V to } 3 \text{ V}$ , driver in VTERM, VIT = 0 V                                                |
| Minimum Pulse Width                                           |      | 1          |      | ns                     | 2 V terminated, 1 V at the<br>comparator, driver in VTERM,<br>VIT = 0 V, 1 $\mu\text{s}$ period, pulse<br>width = 50 ns to 1 ns                     |
| Hysteresis                                                    |      | 6          |      | mV                     | $V_{IN} = 100 \text{ mV}$ , sweep CVL and<br>CVH                                                                                                    |
| Comparator Propagation Delay Matching,<br>HCOMP to LCOMP      |      | 50         |      | ps                     | HCOMP rise to LCOMP rise,<br>HCOMP fall to LCOMP fall                                                                                               |
| LOAD DC SPECIFICATIONS                                        |      |            |      |                        |                                                                                                                                                     |
| Single-Ended Logic Input Characteristics                      |      |            |      |                        |                                                                                                                                                     |
| Threshold Voltage (LDEN)                                      |      | CMOS_VDD/2 |      | V                      |                                                                                                                                                     |
| Voltage Range                                                 | 0    |            | 5.5  | V                      |                                                                                                                                                     |
| Bias Current                                                  | -10  |            | +10  | $\mu\text{A}$          | $V_{IN} = 0 \text{ V}, 3.3 \text{ V}$                                                                                                               |
| Input Characteristics                                         |      |            |      |                        |                                                                                                                                                     |
| VIOL Current Program Range                                    | 0.0  |            | 3.5  | V                      | VDUT = -1.5 V, +6.5 V;<br>IOL = 0 mA to 35 mA                                                                                                       |
| VIOH Current Program Range                                    | 0.0  |            | 3.5  | V                      | VDUT = -1.5 V, +6.5 V;<br>IOH = 0 mA to 35 mA                                                                                                       |
| VIOH, VIOL Input Bias Current                                 | -10  |            | +10  | $\mu\text{A}$          | VIOL = 0 V, 3.5 V;<br>VIOH = 0 V, 3.5 V                                                                                                             |
| VDUT Range                                                    | -1.5 |            | +6.5 | V                      | $ VDUT - VCOM  > 1.0 \text{ V}$                                                                                                                     |

| Parameter                                              | Min   | Typ   | Max   | Unit  | Test Conditions/Comments                                                        |
|--------------------------------------------------------|-------|-------|-------|-------|---------------------------------------------------------------------------------|
| VDUT Range                                             | −1.5  |       | +6.5  | V     | VDUT − VCOM > 1.0 V;<br>IOH = 0 mA to 35 mA                                     |
| VDUT Range                                             | −1.5  |       | +6.5  | V     | VCOM − VDUT > 1.0 V;<br>IOL = 0 mA to 35 mA                                     |
| Output characteristics                                 |       |       |       |       |                                                                                 |
| Gain                                                   | 9.5   | 10    | 10.5  | mA/V  | Slope of line between 5 mA and 30 mA                                            |
| Load Offset, IOH, IOL <sub>T</sub>                     | −200  |       | +200  | μA    | IOH and IOL programmed at 20 mV (200 μA)                                        |
| Load Nonlinearity, IOH, IOL <sub>T</sub>               | −50   |       | +50   | μA    | Relative to a line from 5 mA to 30 mA; IOL, IOH from 200 μA to 35 mA            |
| Output Current Tempco, IOH, IOL <sub>T</sub>           |       | ±3    |       | μA/C  | Measured at IOH, IOL = 30 mA                                                    |
| VCOM Buffer (Through Bridge)                           |       |       |       |       |                                                                                 |
| VCOM Buffer Offset                                     | −50   | +3    | +50   | mV    | IOL, IOH = 20 mA, VCOM = 0 V                                                    |
| VCOM Buffer Bias Current                               | −10   | +1    | +10   | μA    | VCOM = −1.5 V to +6.5 V                                                         |
| VCOM Buffer Gain                                       | 0.99  | 1     | 1.01  | V/V   | IOL, IOH = 20 mA,<br>VCOM = −1.5 V to +6.5 V                                    |
| VCOM Buffer Linearity Error                            | −10   | +1    | +10   | mV    | IOL, IOH = 20 mA,<br>VCOM = −1.5 V to +6.5 V, relative to a line at 0 V and 5 V |
| Dynamic Performance                                    |       |       |       |       |                                                                                 |
| Propagation Delay—I <sub>MAX</sub> to INHIBIT          |       | 2.3   |       | ns    | V <sub>TT</sub> = 2 V, VCOM = 4 V/0 V,<br>IOL = 20 mA, IOH = 20 mA              |
| INHIBIT to I <sub>MAX</sub>                            |       | 2.3   |       | ns    | V <sub>TT</sub> = 2 V, VCOM = 4 V/0 V,<br>IOL = 20 mA, IOH = 20 mA              |
| <b>TOTAL FUNCTION</b>                                  |       |       |       |       |                                                                                 |
| Output Leakage Current                                 | −1.5  | +0.28 | +1.5  | μA    | Driver = INH, VDUT swept from −1.5 V to +6.5 V                                  |
| Output Leakage Current, Low Leakage Mode               | −200  | +10   | +200  | nA    | Driver = INH, VDUT swept from −1.5 V to +6.5 V                                  |
| Output Capacitance                                     |       | 2     |       | pF    |                                                                                 |
| Power Supplies <sup>5</sup>                            |       |       |       |       |                                                                                 |
| Total Supply Range                                     |       |       | 15.5  | V     |                                                                                 |
| Positive Supply, V <sub>CC</sub>                       | 9.75  | 10.0  | 10.25 | V     |                                                                                 |
| Negative Supply, V <sub>EE</sub>                       | −5.25 | −5.0  | −4.75 | V     |                                                                                 |
| Positive Supply Current, V <sub>CC</sub>               | 190   | 210   | 245   | mA    | Load enabled at 20 mA, driver is set to VIL = 0 V                               |
| Negative Supply Current, V <sub>EE</sub>               | 240   | 270   | 300   | mA    | Load enabled at 20 mA, driver is set to VIL = 0 V                               |
| Total Power Dissipation                                | 2.5   | 3.5   | 4     | W     | Load enabled at 20 mA, driver is set to VIL = 0 V                               |
| Positive Supply Current Load Disabled, V <sub>CC</sub> | 145   | 165   | 200   | mA    | Load enabled at 0 mA, driver is set to VIL = 0 V                                |
| Negative Supply Current Load Disabled, V <sub>EE</sub> | 190   | 220   | 250   | mA    | Load enabled at 0 mA, driver is set to VIL = 0 V                                |
| Total Power Dissipation                                | 1.8   | 2.8   | 3.3   | W     | Load enabled at 0 mA, driver is set to VIL = 0 V                                |
| Temperature Sensor Gain Factor                         |       | 10    |       | mV/°C | Five diodes in series                                                           |

<sup>1</sup> 1 μs period, pulse width = 50 ns to 500 ps, pulse width measured when amplitude drops 10%.

<sup>2</sup> Measured at 50% of input amp to 50% of output amp.

<sup>3</sup> t<sub>PD</sub> measured from the 50% of enable signal to 50% of output.

<sup>4</sup> The low leakage mode of the comparator, controlled by VLLM input, reduces the leakage due to the comparator input. The comparator operates in this mode, but its bandwidth is compromised and is not guaranteed.

<sup>5</sup> Under no circumstances should the input voltages exceed the supply voltages.

## ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter                            | Rating          |
|--------------------------------------|-----------------|
| Maximum Current for VCC              | 245 mA          |
| Maximum Current for VEE              | 300 mA          |
| Positive Supply Voltage (VCC to GND) | +10.5 V         |
| Negative Supply Voltage (VEE to GND) | −5.5 V          |
| Operating Temperature (Junction)     | +150°C          |
| Storage Temperature Range            | −65°C to +150°C |
| ESD (Human Body Model)               | ±1500 V         |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

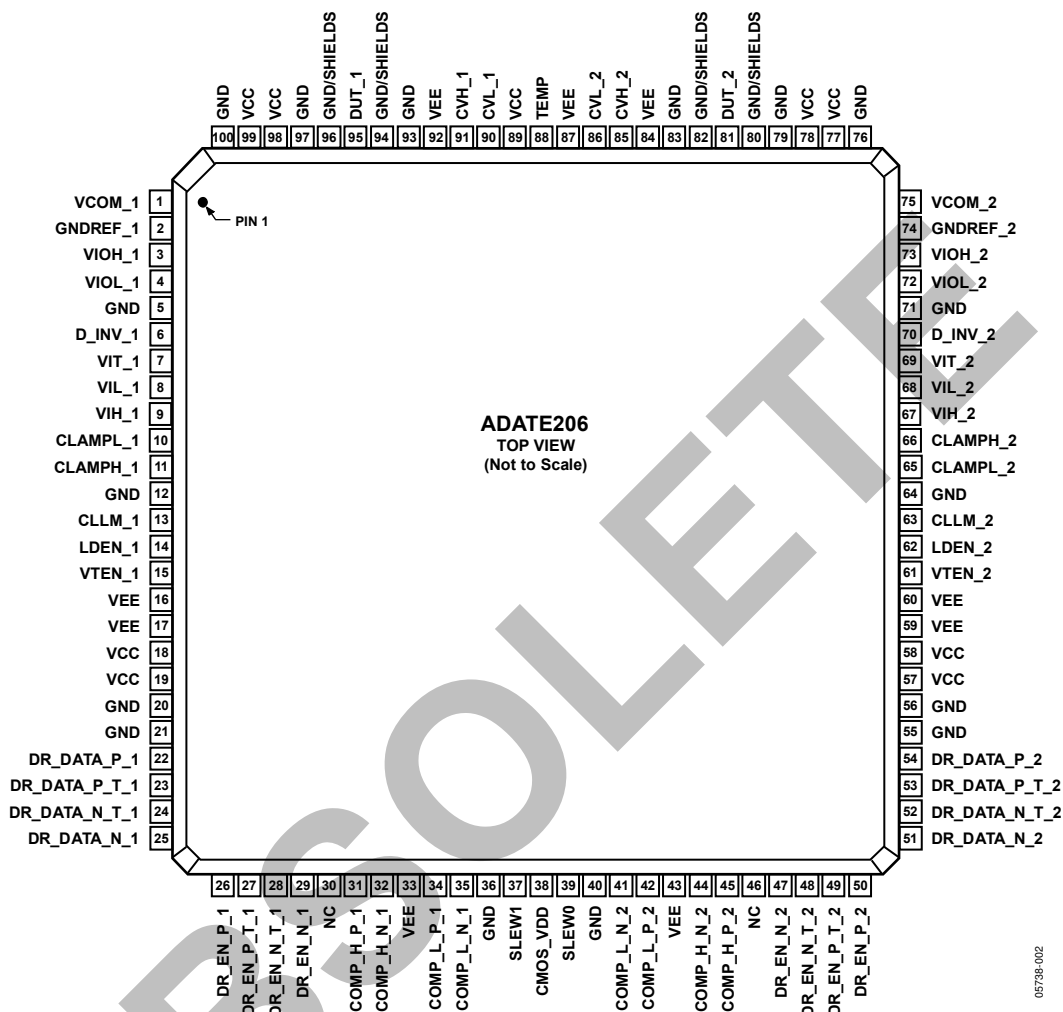


Figure 2. Pin Configuration

05738-002

**Table 3. Pin Function Descriptions**

| Pin No.                                                                 | Mnemonic      | Description                                                                                                                                                                                                |
|-------------------------------------------------------------------------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                                                                       | VCOM_1        | Commutation Reference Voltage.                                                                                                                                                                             |
| 2                                                                       | GNDREF_1      | Reference GND for VIOL, VIOH.                                                                                                                                                                              |
| 3                                                                       | VIOH_1        | Program Voltage for IOH (Sink).                                                                                                                                                                            |
| 4                                                                       | VIOL_1        | Program Voltage for IOL (Source).                                                                                                                                                                          |
| 5, 12, 20, 21, 36,<br>40, 55, 56, 64, 71,<br>76, 79, 83, 93, 97,<br>100 | GND           | Device Ground.                                                                                                                                                                                             |
| 6                                                                       | D_INV_1       | Driver Invert.                                                                                                                                                                                             |
| 7                                                                       | VIT_1         | Driver Term Voltage Reference.                                                                                                                                                                             |
| 8                                                                       | VIL_1         | Driver Low Voltage Reference.                                                                                                                                                                              |
| 9                                                                       | VIH_1         | Driver High Voltage Reference.                                                                                                                                                                             |
| 10                                                                      | CLAMPL_1      | Low Clamp.                                                                                                                                                                                                 |
| 11                                                                      | CLAMPH_1      | High Clamp.                                                                                                                                                                                                |
| 13                                                                      | CLLM_1        | Comparator Low Leakage Mode.                                                                                                                                                                               |
| 14                                                                      | LDEN_1        | Determines Whether LD Responds to DR_EN_1 or is Disabled (see Table 4).                                                                                                                                    |
| 15                                                                      | VTEN_1        | Low Speed Control Signal. When high, DR_EN_1 forces driver output to VIT. Otherwise, DR_EN_1 forces driver to high impedance (see Table 4).                                                                |
| 16, 17, 33, 43, 59,<br>60, 84, 87, 92                                   | VEE           | Negative Power Supply.                                                                                                                                                                                     |
| 18, 19, 57, 58, 77,<br>78, 89, 98, 99                                   | VCC           | Positive Power Supply.                                                                                                                                                                                     |
| 22                                                                      | DR_DATA_P_1   | High Speed Data Inputs. Sets high/low state of driver output (see Table 4).                                                                                                                                |
| 23                                                                      | DR_DATA_P_T_1 | Termination Resistor for HS Inputs. Opposite end of each 50 $\Omega$ termination resistor goes to the appropriate signal.                                                                                  |
| 24                                                                      | DR_DATA_N_T_1 | Termination Resistors for HS Inputs. Opposite end of each 50 $\Omega$ termination resistor goes to the appropriate signal.                                                                                 |
| 25                                                                      | DR_DATA_N_1   | Complement of DR_DATA_P_1.                                                                                                                                                                                 |
| 26                                                                      | DR_EN_P_1     | High Speed Enable Inputs. Multifunction depending on status of VTEN_1 and LDEN_1. Causes driver to enter/leave inhibit; driver to enter/leave termination mode; load to leave/enter inhibit (see Table 4). |
| 27                                                                      | DR_EN_P_T_1   | Termination Resistor for HS Inputs. Opposite end of each 50 $\Omega$ termination resistor goes to the appropriate signal.                                                                                  |
| 28                                                                      | DR_EN_N_T_1   | Termination Resistor for HS Inputs. Opposite end of each 50 $\Omega$ termination resistor goes to the appropriate signal.                                                                                  |
| 29                                                                      | DR_EN_N_1     | Complement of DR_EN_P_1.                                                                                                                                                                                   |
| 30, 46                                                                  | NC            | No Connect.                                                                                                                                                                                                |
| 31                                                                      | COMP_H_P_1    | High Comparator Output.                                                                                                                                                                                    |
| 32                                                                      | COMP_H_N_1    | Complement of COMP_H_P_1.                                                                                                                                                                                  |
| 34                                                                      | COMP_L_P_1    | Low Comparator Output.                                                                                                                                                                                     |
| 35                                                                      | COMP_L_N_1    | Complement of COMP_L_P_1.                                                                                                                                                                                  |
| 37, 39                                                                  | SLEW1, SLEW0  | Logic Signals Controlling Driver Slew Rates for Both Drivers. 00 codes for maximum slew voltage; 11 codes for minimum slew voltage.                                                                        |
| 38                                                                      | CMOS_VDD      | CMOS Supply (Internal $\div 2$ = Single-Ended Logic Reference).                                                                                                                                            |
| 41                                                                      | COMP_L_N_2    | Complement of COMP_L_P_1.                                                                                                                                                                                  |
| 42                                                                      | COMP_L_P_2    | Low Comparator Output.                                                                                                                                                                                     |
| 44                                                                      | COMP_H_N_2    | Complement of COMP_H_P_1.                                                                                                                                                                                  |
| 45                                                                      | COMP_H_P_2    | High Comparator Output.                                                                                                                                                                                    |

| Pin No.        | Mnemonic      | Description                                                                                                                                                                                               |
|----------------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 47             | DR_EN_N_2     | Complement of DR_EN_P_2.                                                                                                                                                                                  |
| 48             | DR_EN_N_T_2   | Complement of DR_EN_P_T_2.                                                                                                                                                                                |
| 49             | DR_EN_P_T_2   | Termination Resistor for HS Inputs. Opposite end of each 50 $\Omega$ termination resistor goes to the appropriate signal.                                                                                 |
| 50             | DR_EN_P_2     | High Speed Enable Input. Multifunction depending on status of VTEN_2 and LDEN_2. Causes driver to enter/leave inhibit; driver to enter/leave termination mode; load to leave/enter inhibit (see Table 4). |
| 51             | DR_DATA_N_2   | Complement of DR_DATA_P_2.                                                                                                                                                                                |
| 52             | DR_DATA_N_T_2 | Complement of DR_DATA_P_T_2.                                                                                                                                                                              |
| 53             | DR_DATA_P_T_2 | Termination Resistor for HS Inputs. Opposite end of each 50 $\Omega$ termination resistor goes to the appropriate signal.                                                                                 |
| 54             | DR_DATA_P_2   | High Speed Data Input. Sets high/low state of driver output (see Table 4).                                                                                                                                |
| 61             | VTEN_2        | Low Speed Control Signal. When high, DR_EN_2 forces driver output to VT; otherwise, DR_EN_2 forces driver to high impedance (see Table 4).                                                                |
| 62             | LDEN_2        | Determines Whether LD Responds to DR_EN_2 or is Disabled (see Table 4).                                                                                                                                   |
| 63             | CLLM_2        | Comp Low Leakage Mode.                                                                                                                                                                                    |
| 65             | CLAMPL_2      | Low Clamp.                                                                                                                                                                                                |
| 66             | CLAMPH_2      | High Clamp.                                                                                                                                                                                               |
| 67             | VIH_2         | Driver High Voltage Reference.                                                                                                                                                                            |
| 68             | VIL_2         | Driver Low Voltage Reference.                                                                                                                                                                             |
| 69             | VIT_2         | Driver Term Voltage Reference.                                                                                                                                                                            |
| 70             | D_INV_2       | Driver Invert.                                                                                                                                                                                            |
| 72             | VIOL_2        | Program Voltage for IOL (Source).                                                                                                                                                                         |
| 73             | VIOH_2        | Program Voltage for IOH (Sink).                                                                                                                                                                           |
| 74             | GNDREF_2      | Reference GND for VIOL, VIOH.                                                                                                                                                                             |
| 75             | VCOM_2        | Commutation Reference Voltage.                                                                                                                                                                            |
| 80, 82, 94, 96 | GND/SHIELDS   | Device Ground or Pin Shield.                                                                                                                                                                              |
| 81             | DUT_2         | Output/Input Pin.                                                                                                                                                                                         |
| 85             | CVH_2         | Window High Reference Level.                                                                                                                                                                              |
| 86             | CVL_2         | Window Low Reference Level.                                                                                                                                                                               |
| 88             | TEMP          | Temperature Sense, Five Diode String, Reference to GND.                                                                                                                                                   |
| 90             | CVL_1         | Window Low Reference Level.                                                                                                                                                                               |
| 91             | CVH_1         | Window High Reference Level.                                                                                                                                                                              |
| 95             | DUT_1         | Output/Input Pin.                                                                                                                                                                                         |

# TYPICAL PERFORMANCE CHARACTERISTICS

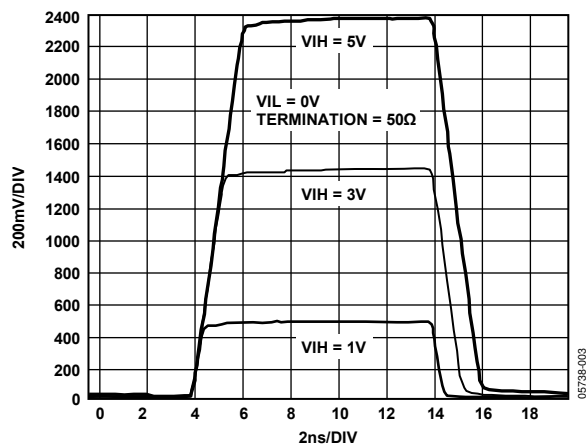


Figure 3. Driver Large Signal Response

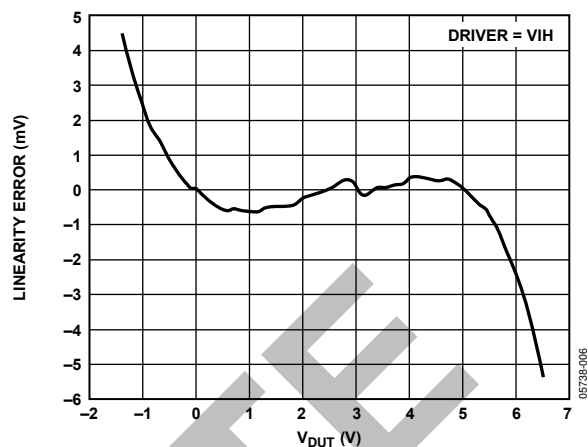


Figure 6. Driver VIH Linearity vs. Output

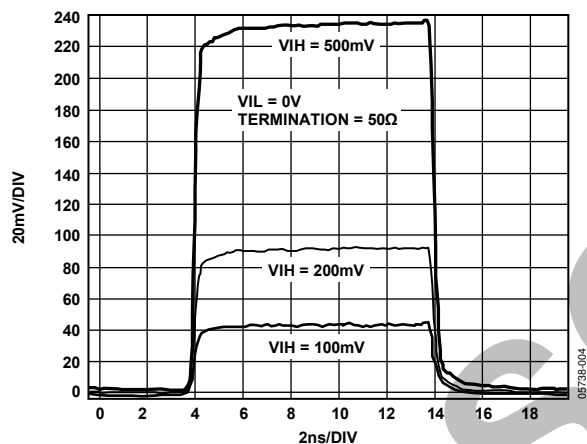


Figure 4. Driver Small Signal Response

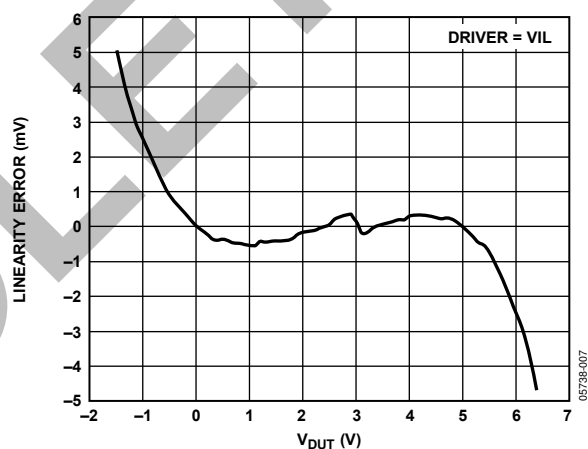


Figure 7. Driver VIL Linearity vs. Output

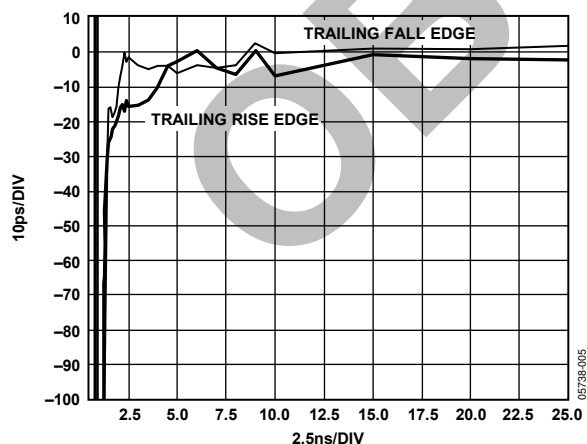


Figure 5. Driver Trailing Edge Timing Error vs. Pulse Width

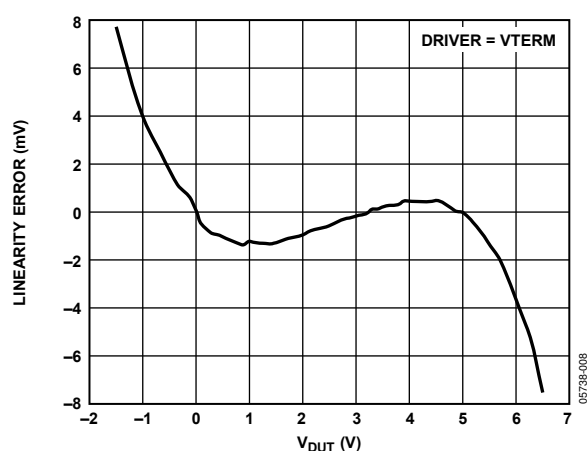


Figure 8. Driver VTERM Linearity vs. Output

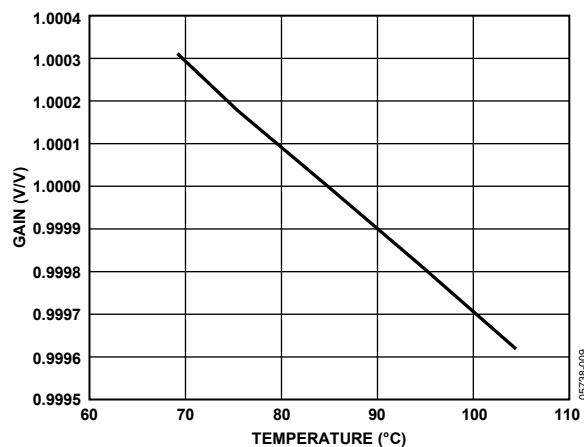


Figure 9. Driver Gain vs. Temperature

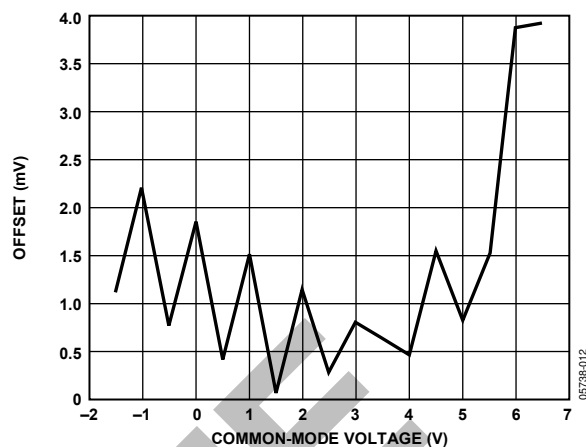


Figure 12. Comparator Offset vs. Common-Mode Voltage

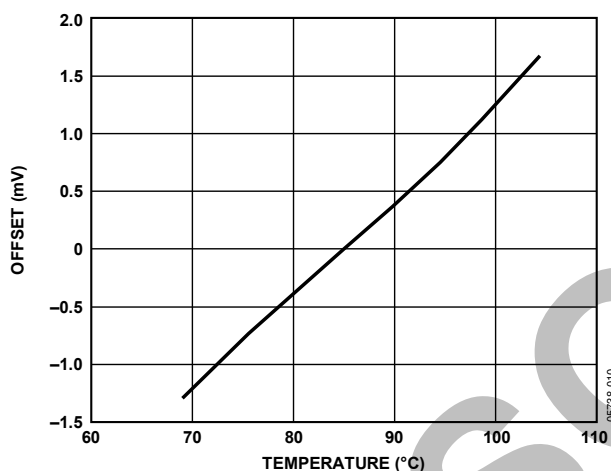


Figure 10. Driver Offset vs. Temperature

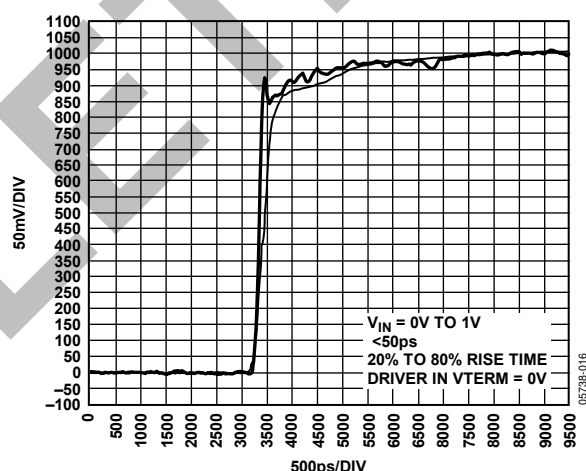


Figure 13. Comparator Schmoos at 1 ns Rise and Fall Time

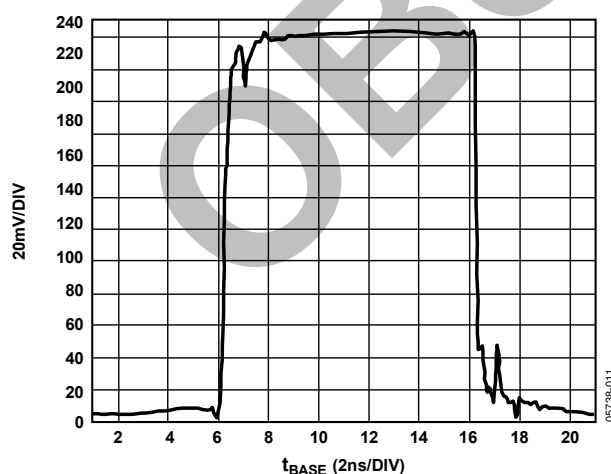


Figure 11. Comparator Differential Output Response

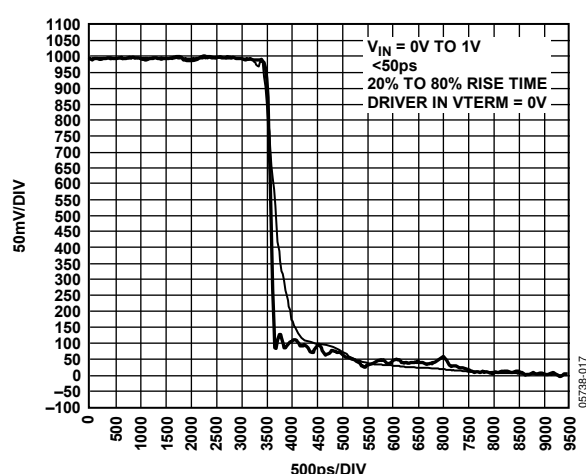


Figure 14. Comparator Schmoos at 600 ps Rise and Fall Time

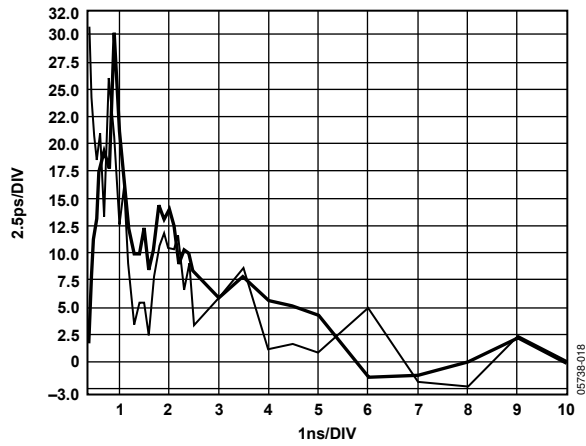


Figure 15. Comparator  $t_{PD}$  vs. Pulse Width

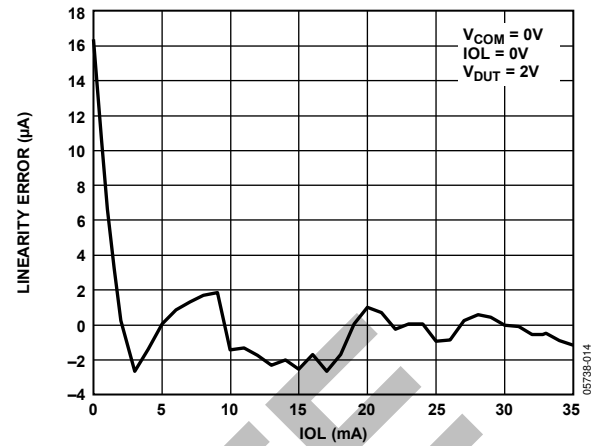


Figure 17. Active Load Linearity vs.  $I_{OH}$

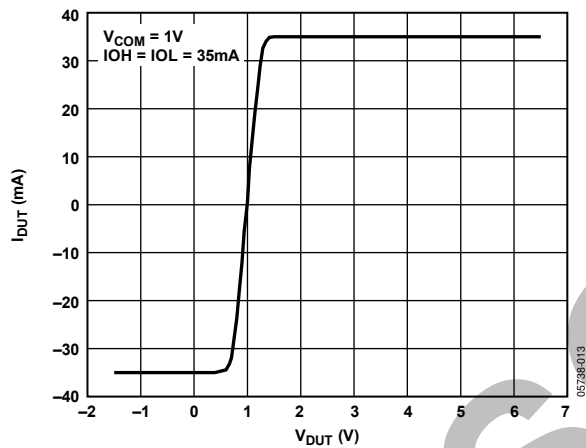


Figure 16. Active Load Commutation Region

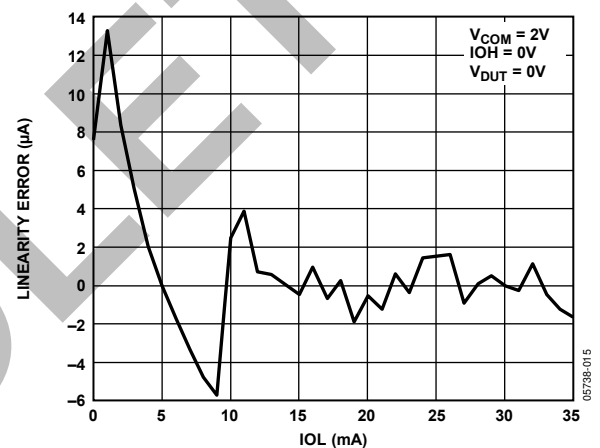


Figure 18. Active Load Linearity vs.  $I_{OL}$

## THEORY OF OPERATION

The ADATE206 has two general classes of logic inputs: differential inputs for controlling functions that generally need to be operated at high speed, and single-ended CMOS inputs for setting operating modes or other low speed functions. The differential inputs have a wide common-mode range that allows them to be used with a variety of logic families. The differential inputs can be used single-ended, with one input from each pair of inputs tied to a fixed reference. However, this makes precise timing more difficult to achieve.

These differential input pins provide 50  $\Omega$  input termination resistors for use as desired. The single-ended inputs have an input range compatible with most logic families and are high impedance to make driving them very easy. The switching threshold for the single-ended inputs is preset to one-half of the voltage at the CMOS\_VDD pin.

**Table 4. Driver and Load Modes**

| <b>LDEN</b><br>(CMOS Single-Ended) | <b>VTEN</b><br>(CMOS Single-Ended) | <b>DR_EN</b><br>(High Speed Differential) | <b>DR_DATA</b><br>(High Speed Differential) | <b>Driver Status</b> | <b>Load Status</b> |
|------------------------------------|------------------------------------|-------------------------------------------|---------------------------------------------|----------------------|--------------------|
| 0                                  | 0                                  | 0                                         | X                                           | High-Z               | High-Z             |
| 0                                  | 0                                  | 1                                         | 0                                           | VIL                  | High-Z             |
| 0                                  | 0                                  | 1                                         | 1                                           | VIH                  | High-Z             |
| 0                                  | 1                                  | 0                                         | X                                           | VIT                  | High-Z             |
| 0                                  | 1                                  | 1                                         | 0                                           | VIL                  | High-Z             |
| 0                                  | 1                                  | 1                                         | 1                                           | VIH                  | High-Z             |
| 1                                  | 0                                  | 0                                         | X                                           | High-Z               | ON                 |
| 1                                  | 0                                  | 1                                         | 0                                           | VIL                  | High-Z             |
| 1                                  | 0                                  | 1                                         | 1                                           | VIH                  | High-Z             |

**Table 5. Comparator Low Leakage Mode**

| <b>CLLM</b><br>(CMOS Single-Ended) | <b>Typical DUT Pin Bias Current</b> |
|------------------------------------|-------------------------------------|
| 0                                  | 1 $\mu$ A                           |
| 1                                  | 10 nA                               |

**Table 6. Rise/Fall Time Selection 3 V, 10% to 90%, Unterminated**

| <b>Slew1</b> | <b>Slew0</b> | <b>Tr/Tf (ns)</b> |
|--------------|--------------|-------------------|
| 0            | 0            | 0.7               |
| 0            | 1            | 0.95              |
| 1            | 0            | 1.4               |
| 1            | 1            | 2.8               |

**Table 7. Comparator Logic Function**

| <b>DUT Pin Voltage</b> |      | <b>Output States</b> |                 |                 |                 |
|------------------------|------|----------------------|-----------------|-----------------|-----------------|
|                        |      | <b>COMP_L_P</b>      | <b>COMP_L_N</b> | <b>COMP_H_P</b> | <b>COMP_H_N</b> |
| >CVL                   | >CVH | 1                    | 0               | 1               | 0               |
| >CVL                   | <CVH | 1                    | 0               | 0               | 1               |
| <CVL                   | >CVH | 0                    | 1               | 1               | 0               |
| <CVL                   | <CVH | 0                    | 1               | 0               | 1               |

## OUTLINE DIMENSIONS

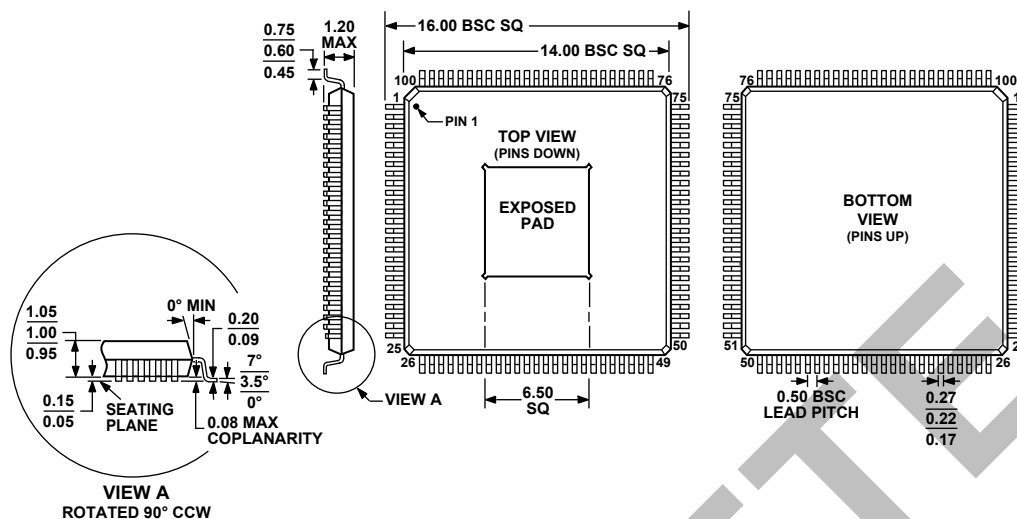


Figure 19. 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP\_EP]  
(SV-100-2)  
Dimensions shown in millimeters

## ORDERING GUIDE

| Model       | Temperature Range | Package Description                                    | Package Option |
|-------------|-------------------|--------------------------------------------------------|----------------|
| ADATE206BSV | -40°C to +85°C    | 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP] | SV-100-2       |