## 400MHz Multiplexing Amplifier

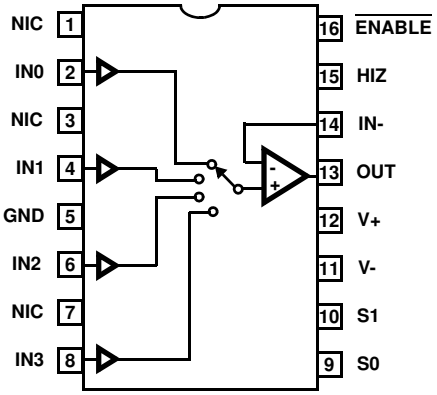
The ISL59440 is a 400MHz bandwidth 4:1 multiplexing amplifier designed primarily for video switching. This Mux-amp has user-settable gain and also features a high speed three-state function to enable the output of multiple devices to be wired together. All logic inputs have pull-downs to ground and may be left floating. The $\overline{\text{ENABLE}}$ pin, when pulled high, sets the ISL59440 to the low current power-down mode for power sensitive applications - consuming just 5mW.

**TABLE 1. CHANNEL SELECT LOGIC TABLE**

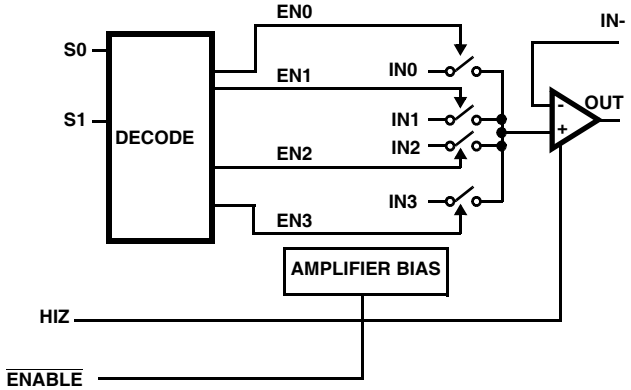
| S1 | S0 | $\overline{\text{ENABLE}}$ | HIZ | OUTPUT |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | IN0 |
| 0 | 1 | 0 | 0 | IN1 |
| 1 | 0 | 0 | 0 | IN2 |
| 1 | 1 | 0 | 0 | IN3 |
| X | X | 1 | X | Power Down |
| X | X | 0 | 1 | High Z |

## Pinout

**ISL59440**
**(16 LD QSOP)**
TOP VIEW




## Functional Diagram




**$\overline{\text{ENABLE}}$ pin must be low in order to activate the HIZ state**

## Features

- 411MHz (-3dB) Bandwidth ($A_V$ = 1, $V_{OUT}$ = 100m$V_{P-P}$)
- 200MHz (-3dB) Bandwidth ($A_V$ = 2, $V_{OUT}$ = 2$V_{P-P}$)
- Slew Rate ($A_V$ = 1, $R_L$ = 500Ω, $V_{OUT}$ = 4V) . . . . .1053V/µs
- Slew Rate ($A_V$ = 2, $R_L$ = 500Ω, $V_{OUT}$ = 5V) . . . . .1470V/µs
- Adjustable Gain
- High Speed Three-state Output (HIZ)
- Low Current Power-down. . . . . .5mW
- Pb-Free Available (RoHS Compliant)

## Applications

- HDTV/DTV Analog Inputs
- Video Projectors
- Computer Monitors
- Set-top Boxes
- Security Video
- Broadcast Video Equipment

## Ordering Information

| PART NUMBER | PART MARKING | PACKAGE | PKG. DWG. # |
|---|---|---|---|
| ISL59440IA* | 59440 IA | 16 Ld QSOP | MDP0040 |
| ISL59440IAZ* (Note) | 59440 IAZ | 16 Ld QSOP (Pb-free) | MDP0040 |

*Add “-T7” or “-T13” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Absolute Maximum Ratings ($T_A$ = 25°C)

Supply Voltage (V+ to V-) . . . . . 11V
Input Voltage . . . . . V- -0.5V, V+ +0.5V
Supply Turn-on Slew Rate . . . . . 1V/µs
IN- Input Current (Note 1) . . . . . 5mA
Digital & Analog Input Current (Note 1) . . . . . 50mA
Output Current (Continuous) . . . . . 50mA
ESD Rating
Human Body Model . . . . . 2.5kV
Machine Model . . . . . 300V

## Thermal Information

Storage Temperature Range . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -40°C to +85°C
Operating Junction Temperature . . . . . -40°C to +125°C
Power Dissipation . . . . . See Curves
$\theta_{JA}$ . . . . . See Curves
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

1. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.
2. Parts are 100% tested at +25°C. Over temperature limits established by characterization and are not production tested.

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$*

## Electrical Specifications

V+ = +5V, V- = -5V, GND = 0V, $T_A$ = +25°C, $R_L$ = 500Ω to GND unless otherwise specified.

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 2) | TYP | MAX (Note 2) | UNIT |
|---|---|---|---|---|---|---|
| **GENERAL** | | | | | | |
| ±$I_S$ Enabled | Supply Current | No load, $V_{IN}$ = 0V, $\overline{\text{ENABLE}}$ Low | 12.5 | 14.5 | 16.5 | mA |
| $I_S$ Disabled | Disabled Supply Current I+ | No load, $V_{IN}$ = 0V, $\overline{\text{ENABLE}}$ High | 0.5 | 1 | 1.5 | mA |
| | Disabled Supply Current I- | No load, $V_{IN}$ = 0V, $\overline{\text{ENABLE}}$ High | | 3 | 10 | µA |
| $V_{OUT}$ | Positive and Negative Output Swing | $V_{IN}$ = ±2V, $R_L$ = 500Ω, $A_V$ = 2 | ±3.5 | ±3.9 | | V |
| $I_{OUT}$ | Output Current | $R_L$ = 10Ω to GND | 80 | 130 | | mA |
| $V_{OS}$ | Output Offset Voltage | | -12 | 4 | +12 | mV |
| Ib+ | Input Bias Current | $V_{IN}$ = 0V | -4 | 2.5 | -1.5 | µA |
| Ib- | Feedback Bias Current | | -15 | 7 | 15 | µA |
| $R_{OUT}$ | Output Resistance | HIZ = logic high, (DC), $A_V$ =1 | | 1.4 | | MΩ |
| | | HIZ = logic low, (DC), $A_V$ =1 | | 0.2 | | Ω |
| $R_{IN}$ | Input Resistance | $V_{IN}$ = 3.5V | | 10 | | MΩ |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 224m$V_{RMS}$, $A_V$ = 1 | | 0.9 | | pF |
| $A_{CL}$ or $A_V$ | Voltage Gain | $R_F$ = $R_G$ = 500Ω, $V_{OUT}$ = ±3V | 1.990 | 2.005 | 2.020 | V/V |
| $I_{TRI}$ | Output Current in Three-state | $V_{OUT}$ = 0V | -20 | 6 | 20 | µA |
| **LOGIC** | | | | | | |
| $V_H$ | Input High Voltage (Logic Inputs) | | 2 | | | V |
| $V_L$ | Input Low Voltage (Logic Inputs) | | | | 0.8 | V |
| $I_{IH}$ | Input High Current (Logic Inputs) | | 55 | 90 | 135 | µA |
| $I_{IL}$ | Input Low Current (Logic Inputs) | | -10 | 0 | 10 | µA |
| **AC GENERAL** | | | | | | |
| - 3dB BW | -3dB Bandwidth | $A_V$ = 1, $R_F$ = 332Ω, $V_{OUT}$ = 200m$V_{P-P}$, $C_L$ = 1.6pF, $C_G$ = 0.6pF | | 400 | | MHz |
| | | $A_V$ = 2, $R_F$ = $R_G$ = 511Ω, $V_{OUT}$ = 2$V_{P-P}$, $C_L$ = 5.5pF, $C_G$ = 0.6pF | | 200 | | MHz |

**Electrical Specifications** $V+ = +5V$, $V- = -5V$, GND = 0V, $T_A = +25°C$, $R_L = 500\Omega$ to GND unless otherwise specified. **(Continued)**

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 2) | TYP | MAX (Note 2) | UNIT |
|---|---|---|---|---|---|---|
| 0.1dB BW | 0.1dB Bandwidth | $A_V = 1$, $R_F = 332\Omega$, $V_{OUT} = 200mV_{P-P}$, $C_L = 1.6pF$, $C_G = 0.6pF$ | | 22 | | MHz |
| | | $A_V = 2$, $R_F = R_G = 511\Omega$, $V_{OUT} = 2V_{P-P}$, $C_L = 5.5pF$, $C_G = 0.6pF$ | | 62 | | MHz |
| dG | Differential Gain Error | NTC-7, $R_L = 150$, $C_L = 1.6pF$, $A_V = 1$ | | 0.01 | | % |
| | | NTC-7, $R_L = 150$, $C_L = 5.5pF$, $A_V = 2$ | | 0.05 | | % |
| dP | Differential Phase Error | NTC-7, $R_L = 150$, $C_L = 1.6pF$, $A_V = 1$ | | 0.02 | | ° |
| | | NTC-7, $R_L = 150$, $C_L = 5.5pF$, $A_V = 2$ | | 0.02 | | ° |
| +SR | Slew Rate | 25% to 75%, $A_V = 1$, $V_{OUT} = 4V$, $R_L = 500\Omega$, $C_L = 1.6pF$ | | 1053 | | V/µs |
| | | 25% to 75%, $A_V = 2$, $V_{OUT} = 5V$, $R_L = 500\Omega$, $C_L = 5.5pF$ | | 1470 | | V/µs |
| -SR | Slew Rate | 25% to 75%, $A_V = 1$, $V_{OUT} = 4V$, $R_L = 500\Omega$, $C_L = 1.6pF$ | | 925 | | V/µs |
| | | 25% to 75%, $A_V = 2$, $V_{OUT} = 5V$, $R_L = 500\Omega$, $C_L = 5.5pF$ | | 1309 | | V/µs |
| PSRR | Power Supply Rejection Ratio | DC, PSRR V+ and V- combined | -50 | -58 | | dB |
| ISO | Channel Isolation | f = 10MHz, Ch-Ch crosstalk and off-isolation, $C_L = 5.5pF$ | | 75 | | dB |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| $V_{GLITCH}$ | Channel-to-Channel Switching Glitch | $V_{IN} = 0V$, $C_L = 5.5pF$, $A_V = 2$ | | 1 | | $mV_{P-P}$ |
| | $\overline{ENABLE}$ Switching Glitch | $V_{IN} = 0V$, $C_L = 5.5pF$, $A_V = 2$ | | 800 | | $mV_{P-P}$ |
| | HIZ Switching Glitch | $V_{IN} = 0V$, $C_L = 5.5pF$, $A_V = 2$ | | 375 | | $mV_{P-P}$ |
| $t_{SW-L-H}$ | Channel Switching Time Low to High | 1.2V logic threshold to 10% movement of analog output | | 25 | | ns |
| $t_{SW-H-L}$ | Channel Switching Time High to Low | 1.2V logic threshold to 10% movement of analog output | | 20 | | ns |
| **TRANSIENT RESPONSE** | | | | | | |
| $t_R$, $t_F$ | Rise and Fall Time, 10% to 90% | $A_V = 1$, $R_F = 332\Omega$, $V_{OUT} = 100mV_{P-P}$, $C_L = 1.6pF$, $C_G = 0.6pF$ | | 0.65 | | ns |
| | | $A_V = 2$, $R_F = R_G = 511\Omega$, $V_{OUT} = 2V_{P-P}$, $C_L = 5.5pF$, $C_G = 0.6pF$ | | 1.51 | | ns |
| $t_S$ | 0.1% Settling Time | $A_V = 2$, $R_F = R_G = 511\Omega$, $V_{OUT} = 2V_{P-P}$, $C_L = 5.5pF$, $C_G = 0.6pF$ | | 9.0 | | ns |
| $O_S$ | Overshoot | $A_V = 1$, $R_F = 332\Omega$, $V_{OUT} = 100mV_{P-P}$, $C_L = 1.6pF$, $C_G = 0.6pF$ | | 17.85 | | % |
| | | $A_V = 2$, $R_F = R_G = 511\Omega$, $V_{OUT} = 2V_{P-P}$, $C_L = 5.5pF$, $C_G = 0.6pF$ | | 12.65 | | % |
| $t_{PLH}$ | Propagation Delay - Low to High, 10% to 10% | $A_V = 1$, $R_F = 332\Omega$, $V_{OUT} = 100mV_{P-P}$, $C_L = 1.6pF$, $C_G = 0.6pF$ | | 0.54 | | ns |
| | | $A_V = 2$, $R_F = R_G = 511\Omega$, $V_{OUT} = 2V_{P-P}$, $C_L = 5.5pF$, $C_G = 0.6pF$ | | 0.99 | | ns |
| $t_{PHL}$ | Propagation Delay- High to Low, 10% to 10% | $A_V = 1$, $R_F = 332\Omega$, $V_{OUT} = 100mV_{P-P}$, $C_L = 1.6pF$, $C_G = 0.6pF$ | | 0.57 | | ns |
| | | $A_V = 2$, $R_F = R_G = 511\Omega$, $V_{OUT} = 2V_{P-P}$, $C_L = 5.5pF$, $C_G = 0.6pF$ | | 1.02 | | ns |

## Typical Performance Curves $V_S = \pm5V$, $R_L = 500\Omega$ to GND, $T_A = 25°C$, unless otherwise specified.

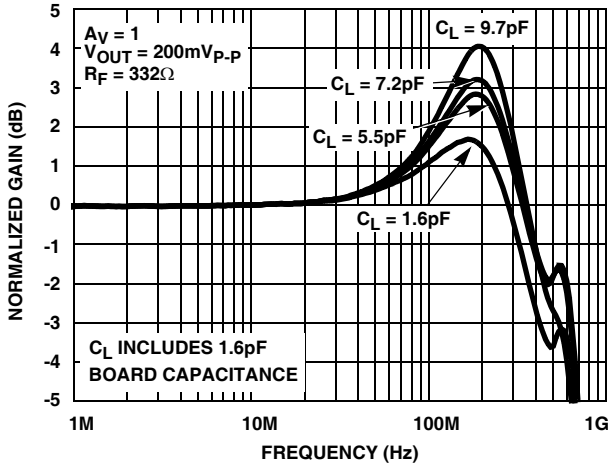



FIGURE 1. SMALL SIGNAL GAIN vs FREQUENCY vs $C_L$

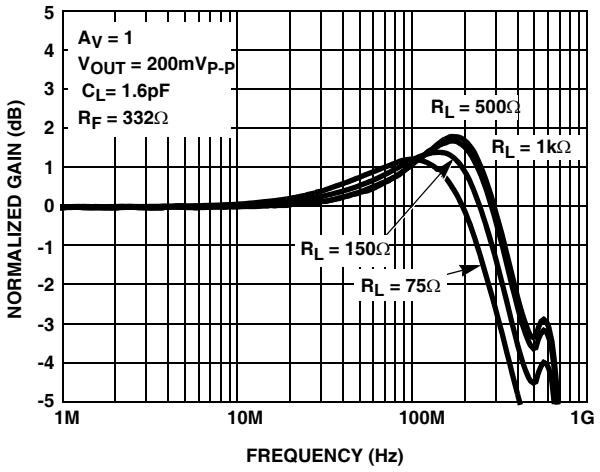



FIGURE 2. SMALL SIGNAL GAIN vs FREQUENCY vs $R_L$

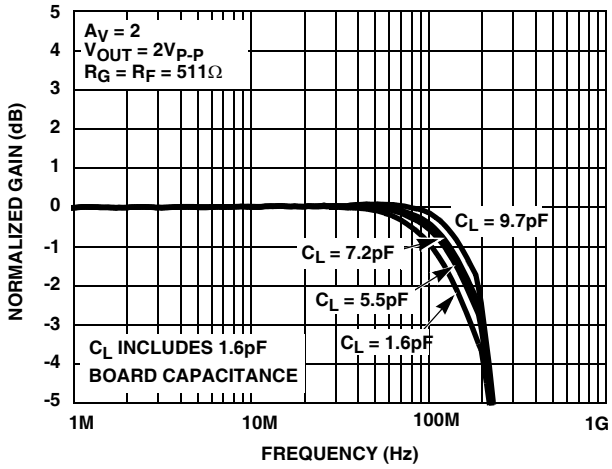



FIGURE 3. LARGE SIGNAL GAIN vs FREQUENCY vs $C_L$

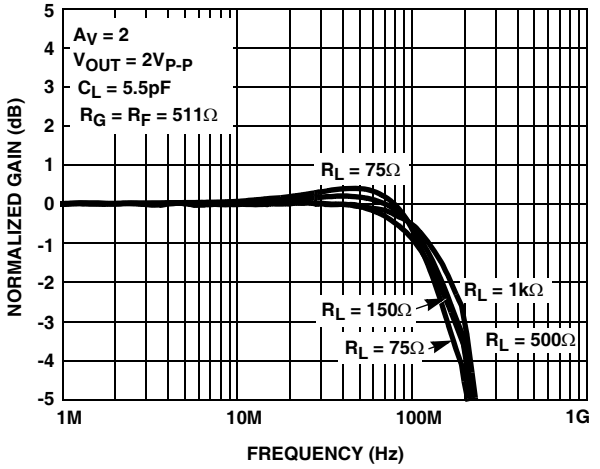



FIGURE 4. LARGE SIGNAL GAIN vs FREQUENCY vs $R_L$

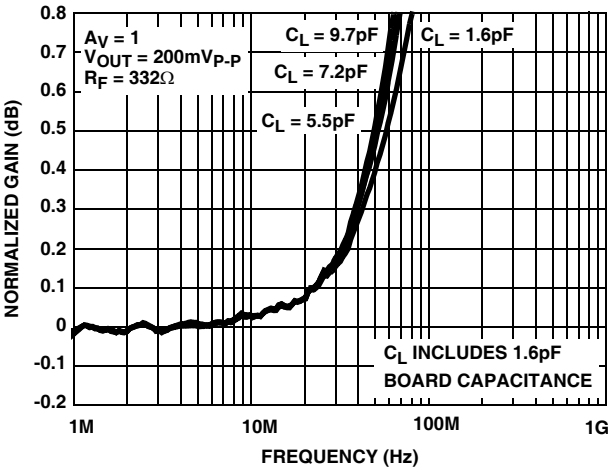



FIGURE 5. SMALL SIGNAL 0.1dB GAIN vs FREQUENCY vs $C_L$

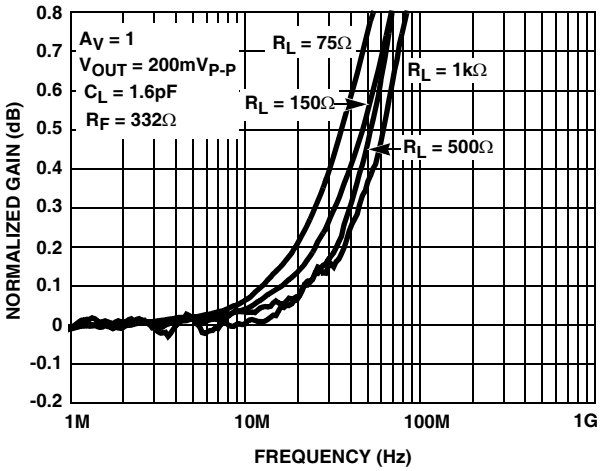



FIGURE 6. SMALL SIGNAL 0.1dB GAIN vs FREQUENCY vs $R_L$

## Typical Performance Curves $V_S = \pm5V$, $R_L = 500\Omega$ to GND, $T_A = 25°C$, unless otherwise specified. **(Continued)**

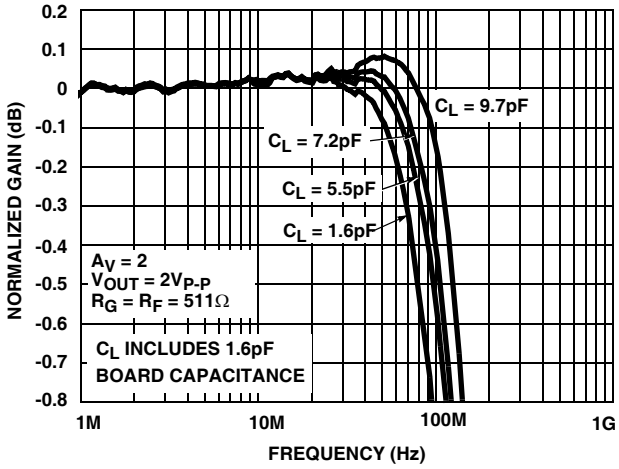



FIGURE 7. LARGE SIGNAL 0.1dB GAIN vs FREQUENCY vs $C_L$

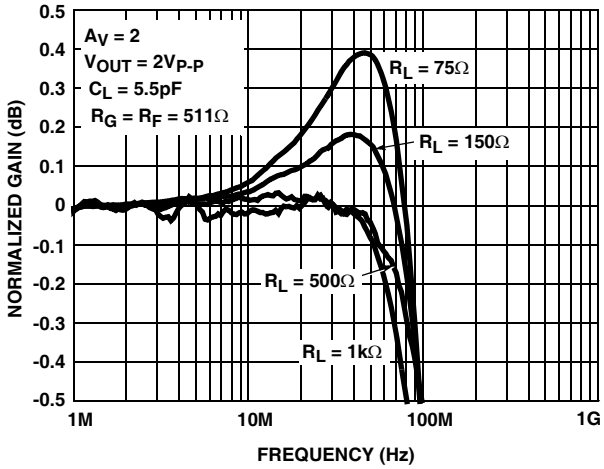



FIGURE 8. LARGE SIGNAL 0.1dB GAIN vs FREQUENCY vs $R_L$

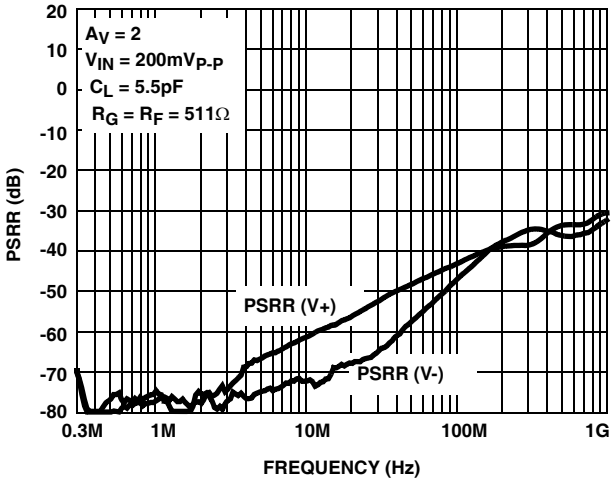



FIGURE 9. PSRR CHANNELS

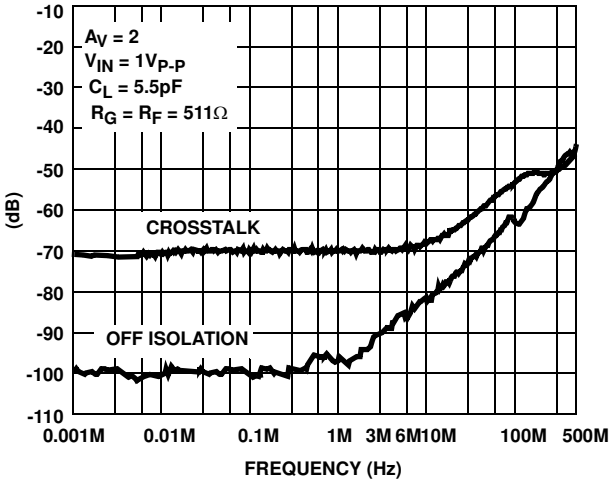



FIGURE 10. CROSSTALK AND OFF ISOLATION

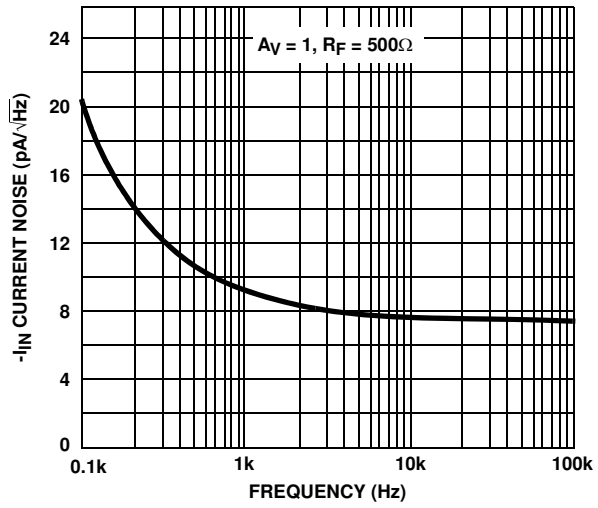



FIGURE 11. INPUT NOISE vs FREQUENCY

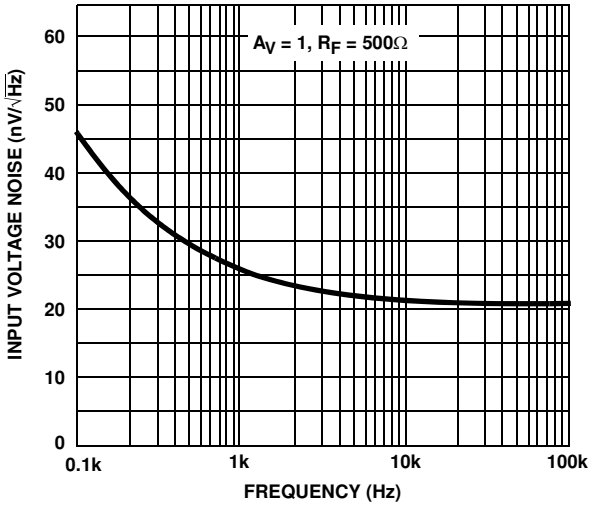



FIGURE 12. INPUT NOISE vs FREQUENCY

## Typical Performance Curves $V_S = \pm5V$, $R_L = 500\Omega$ to GND, $T_A = 25°C$, unless otherwise specified. **(Continued)**

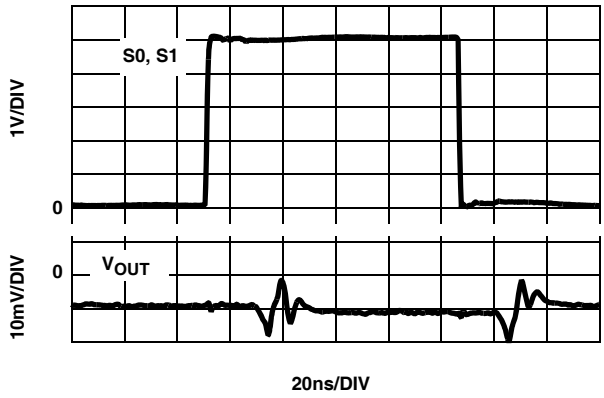



FIGURE 13. CHANNEL TO CHANNEL SWITCHING GLITCH $V_{IN} = 0V$, $A_V = 2$

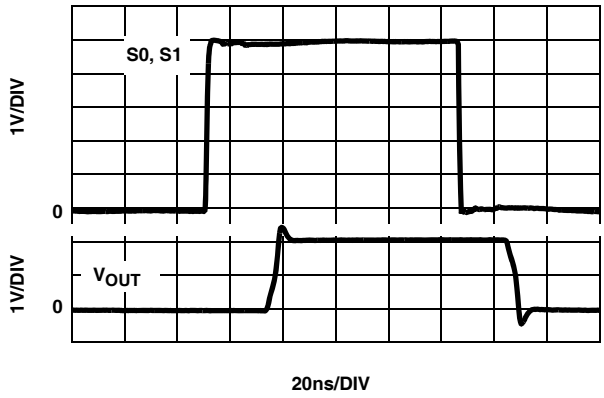



FIGURE 14. CHANNEL TO CHANNEL TRANSIENT RESPONSE $V_{IN} = 1V$, $A_V = 2$

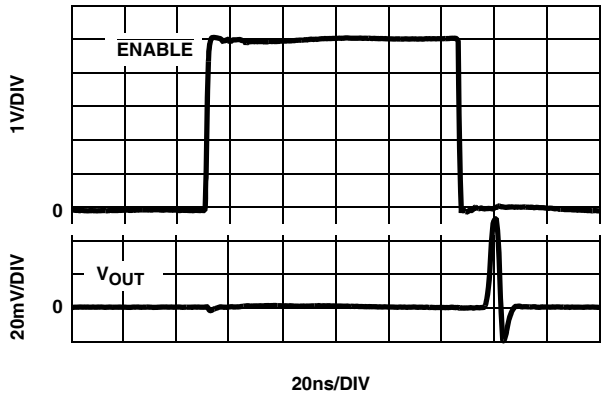



FIGURE 15. $\overline{\text{ENABLE}}$ SWITCHING GLITCH $V_{IN} = 0V$, $A_V = 2$

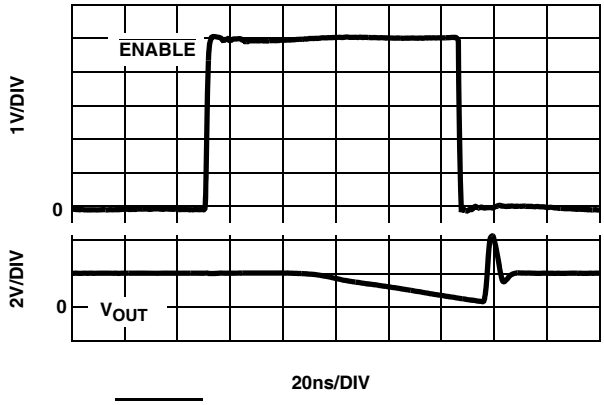



FIGURE 16. $\overline{\text{ENABLE}}$ TRANSIENT RESPONSE $V_{IN} = 1V$, $A_V = 2$

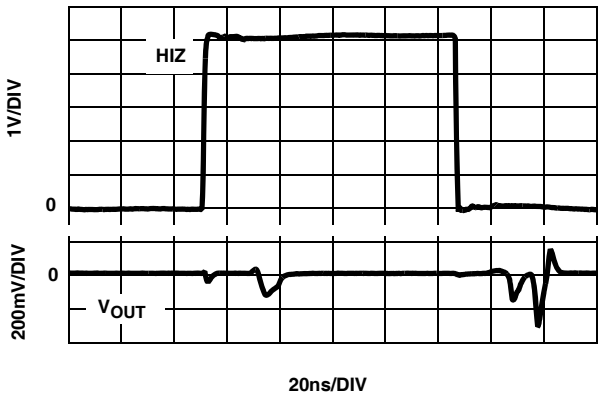



FIGURE 17. HIZ SWITCHING GLITCH $V_{IN} = 0V$, $A_V = 2$

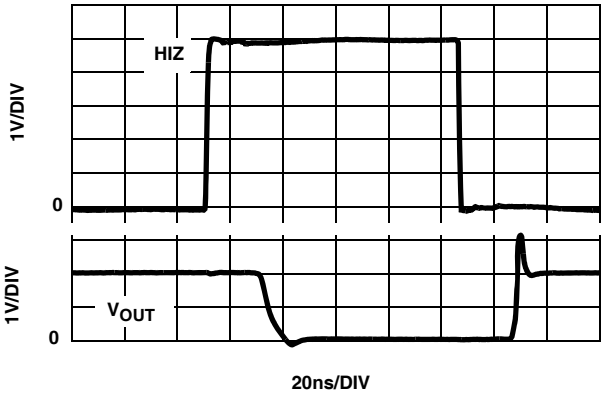



FIGURE 18. HIZ TRANSIENT RESPONSE $V_{IN} = 1V$, $A_V = 2$

## Typical Performance Curves $V_S = \pm5V$, $R_L = 500\Omega$ to GND, $T_A = 25°C$, unless otherwise specified. **(Continued)**

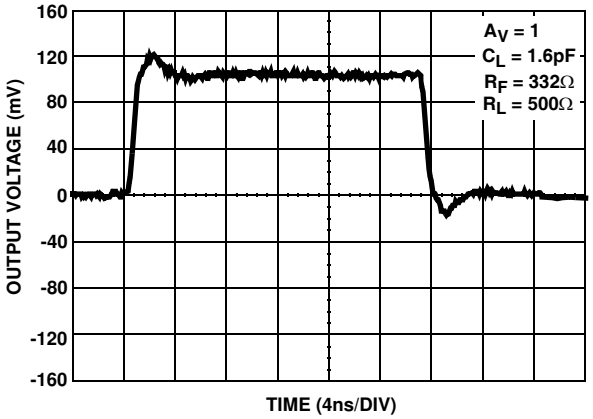



FIGURE 19. SMALL SIGNAL TRANSIENT RESPONSE

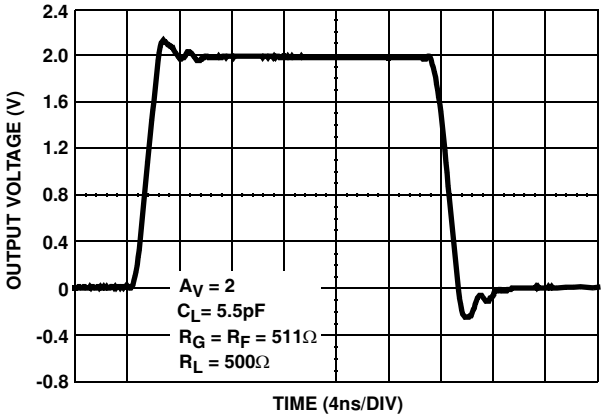



FIGURE 20. LARGE SIGNAL TRANSIENT RESPONSE

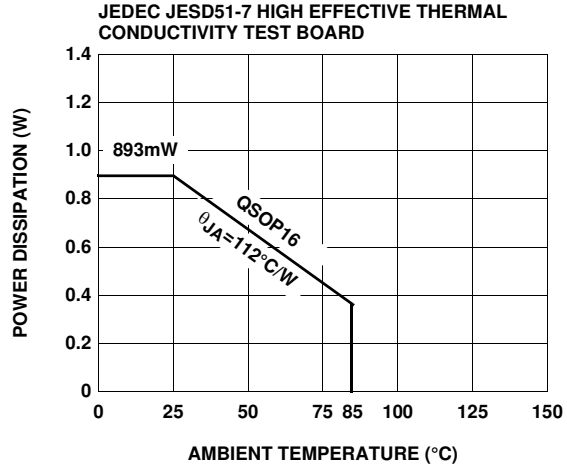



FIGURE 21. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

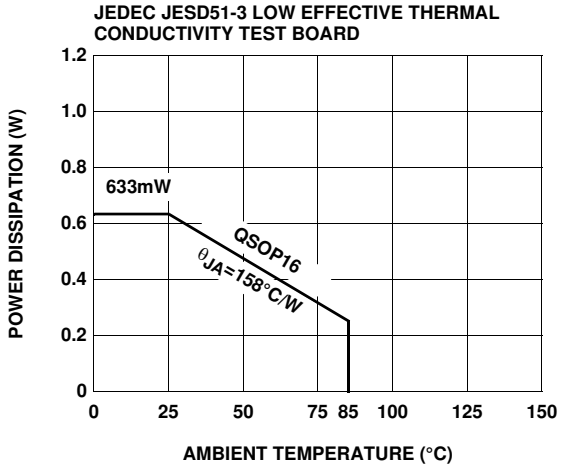



FIGURE 22. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

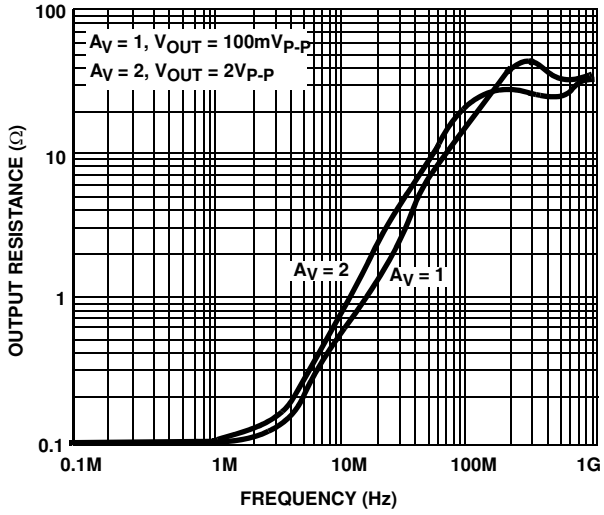
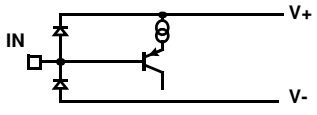


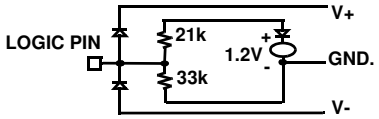

FIGURE 23. $R_{OUT}$ vs FREQUENCY

## Pin Descriptions

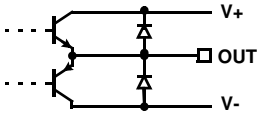
| PIN NUMBER | PIN NAME | EQUIVALENT CIRCUIT | DESCRIPTION |
|---|---|---|---|
| 1, 3, 7 | NIC | | **N**ot **I**nternally **C**onnected; it is recommended this pin be tied to ground to minimize crosstalk. |
| 2 | IN0 | Circuit 1 | Input for Channel 0 |
| 4 | IN1 | Circuit 1 | Input for Channel 1 |
| 5 | GND | Circuit 4 | Ground pin |
| 6 | IN2 | Circuit 1 | Input for Channel 2 |
| 8 | IN3 | Circuit 1 | Input for Channel 3 |
| 9 | S0 | Circuit 2 | Channel selection pin LSB (binary logic code) |
| 10 | S1 | Circuit 2 | Channel selection pin MSB (binary logic code) |
| 11 | V- | Circuit 4 | Negative power supply |
| 12 | V+ | Circuit 4 | Positive power supply |
| 13 | OUT | Circuit 3 | Output |
| 14 | IN- | Circuit 1 | Inverting input of output amplifier |
| 15 | HIZ | Circuit 2 | Output disable (active high); there are internal pull-down resistors, so the device will be active with no connection; “HI” puts the output in high impedance state. |
| 16 | $\overline{\text{ENABLE}}$ | Circuit 2 | Device enable (active low); there are internal pull-down resistors, so the device will be active with no connection; "HI" puts device into power-down mode. |



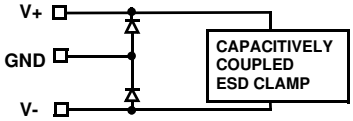

CIRCUIT 1.




CIRCUIT 2.




CIRCUIT 3.




CIRCUIT 4.

## AC Test Circuits

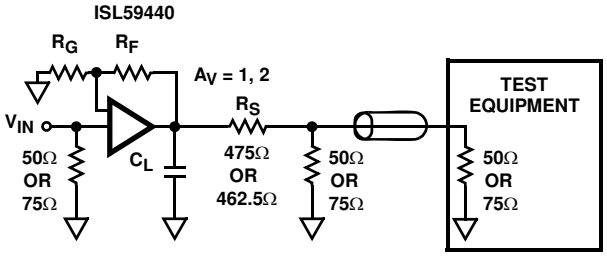



**FIGURE 24A. TEST CIRCUIT FOR MEASURING WITH A 50Ω OR 75Ω INPUT TERMINATED EQUIPMENT**

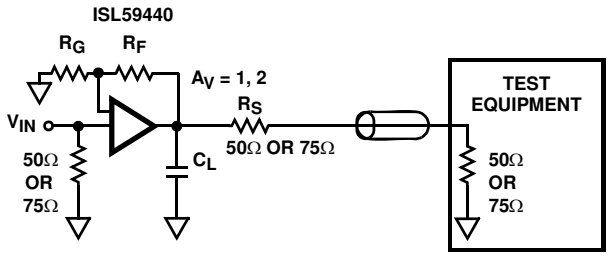



**FIGURE 24B. BACKLOADED TEST CIRCUIT FOR VIDEO CABLE APPLICATION. BANDWIDTH AND LINEARITY FOR $R_L$ LESS THAN 500Ω WILL BE DEGRADED.**

NOTE: Figure 24A illustrates the optimum output load when connecting to input terminated equipment. Figure 24B illustrates backloaded test circuit for video cable applications.

## Application Circuits

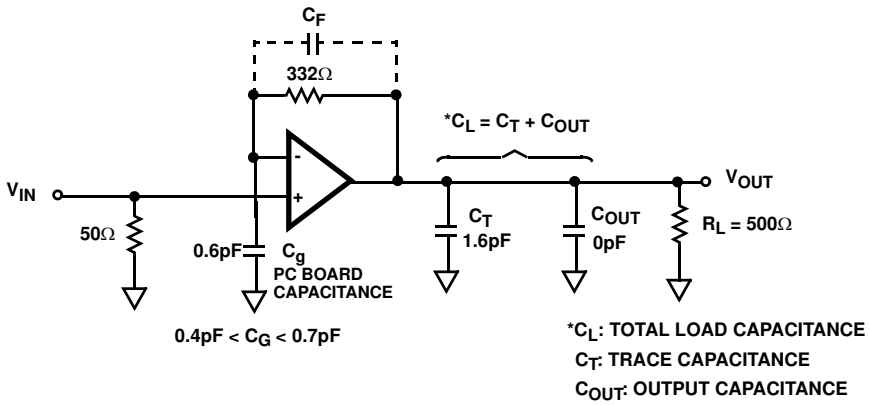



FIGURE 25A. GAIN OF 1 APPLICATION CIRCUIT

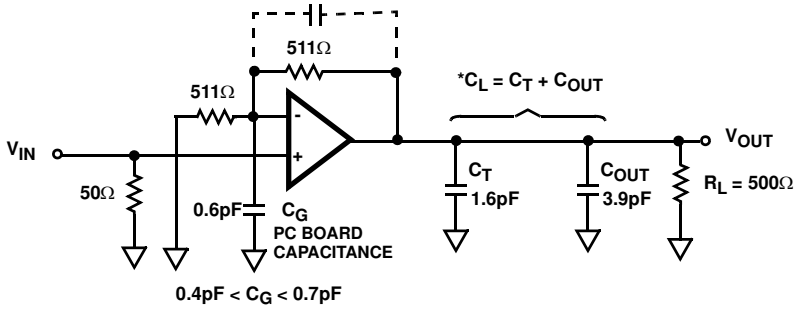



FIGURE 25B. GAIN OF 2 APPLICATION CIRCUIT

## Application Information

### General

The ISL59440 is a 4:1 mux that is ideal as a matrix element in high performance switchers and routers. The ISL59440 is optimized to drive 5pF in parallel with a 500Ω load. The capacitance can be split between the PCB capacitance and an external load capacitance. Its low input capacitance and high input resistance provides excellent 50Ω or 75Ω terminations.

### Parasitic Effects on Frequency Performance

#### CAPACITANCE AT THE INVERTING INPUT

The AC performance of current-feedback amplifiers in the non-inverting gain configuration is strongly effected by stray capacitance at the inverting input. Stray capacitance from the inverting input pin to the output ($C_F$), and to ground ($C_G$), increase gain peaking and bandwidth. Large values of either capacitance can cause oscillation. The ISL59440 has been optimized for a 0.4pF to 0.7pF capacitance ($C_G$). Capacitance ($C_F$) to the output should be minimized. To achieve optimum performance the feedback network resistor(s) must be placed as close to the device as possible. Trace lengths greater than 1/4 inch combined with resistor pad capacitance can result in inverting input to ground capacitance approaching 1pF. Inverting input and output traces should not run parallel to each other. Small size surface mount resistors (604 or smaller) are recommended.

#### CAPACITANCE AT THE OUTPUT

The output amplifier is optimized for capacitance to ground ($C_L$) directly on the output pin. Increased capacitance causes higher peaking with an increase in bandwidth. The optimum range for most applications is ~1.0pF to ~6pF. The optimum value can be achieved through a combination of PC board trace capacitance ($C_T$) and an external capacitor ($C_{OUT}$). A good method to maintain control over the output pin capacitance is to minimize the trace length ($C_T$) to the next component, and include a discrete surface mount capacitor ($C_{OUT}$) directly at the output pin.

#### FEEDBACK RESISTOR VALUES

The AC performance of the output amplifier is optimized with the feedback resistor network ($R_F$, $R_G$) values recommended in the application circuits. The amplifier bandwidth and gain peaking are directly effected by the value(s) of the feedback resistor(s) in unity gain and gain >1 configurations. Transient response performance can be tailored simply by changing these resistor values. Generally, lower values of $R_F$ and $R_G$ increase bandwidth and gain peaking. This has the effect of decreasing rise/fall times and increasing overshoot.

## GROUND CONNECTIONS

For the best isolation and crosstalk rejection, the GND pin and NIC pins must connect to the GND plane.

## CONTROL SIGNALS

S0, S1, $\overline{\text{ENABLE}}$, HIZ - These pins are TTL/CMOS compatible control inputs. The S0 pin selects which one of the inputs connect to the output. The $\overline{\text{ENABLE}}$, HIZ pins are used to disable the part to save power and three-state the output amplifiers, respectively. For control signal rise and fall times less than 10ns the use of termination resistors close to the part will minimize transients coupled to the output.

## POWER-UP CONSIDERATIONS

The ESD protection circuits use internal diodes from all pins the V+ and V- supplies. In addition, a dV/dT- triggered clamp is connected between the V+ and V- pins, as shown in the Equivalent Circuits 1 through 4 section of the “Pin Descriptions” on page 8. The dV/dT triggered clamp imposes a maximum supply turn-on slew rate of 1V/µs. Damaging currents can flow for power supply rates-of-rise in excess of 1V/µs, such as during hot plugging. Under these conditions, additional methods should be employed to ensure the rate of rise is not exceeded.

Consideration must be given to the order in which power is applied to the V+ and V- pins, as well as analog and logic input pins. Schottky diodes (Motorola MBR0550T or equivalent) connected from V+ to ground and V- to ground (Figure 26) will shunt damaging currents away from the internal V+ and V- ESD diodes in the event that the V+ supply is applied to the device before the V- supply.

If positive voltages are applied to the logic or analog video input pins before V+ is applied, current will flow through the internal ESD diodes to the V+ pin. The presence of large decoupling capacitors and the loading effect of other circuits connected to V+, can result in damaging currents through the ESD diodes and other active circuits within the device. Therefore, adequate current limiting on the digital and analog inputs is needed to prevent damage during the time the voltages on these inputs are more positive than V+.

## HIZ STATE

An internal pull-down resistor connected to the HIZ pin ensures the device will be active with no connection to the HIZ pin. The HIZ state is established within approximately 30ns (Figure 18) by placing a logic high (> 2V) on the HIZ pin. If the HIZ state is selected, the output is a high impedance 1.4MΩ. Use this state to control the logic when more than one mux shares a common output.

In the HIZ state the output is three-stated, and maintains its high Z even in the presence of high slew rates. The supply current during this state is basically the same as the active state.

## $\overline{\text{ENABLE}}$ AND POWER DOWN STATES

The enable pin is active low. An internal pull-down resistor ensures the device will be active with no connection to the $\overline{\text{ENABLE}}$ pin. The Power Down state is established when a logic high (>2V) is placed on the $\overline{\text{ENABLE}}$ pin. In the Power Down state, the output has no leakage but has a large capacitance (on the order of 15pF), and is capable of being back-driven. Under this condition, large incoming slew rates can cause fault currents of tens of mA. **Do not use this state as a high Z state for applications driving more than one mux on a common output.**

## LIMITING THE OUTPUT CURRENT

No output short circuit current limit exists on this part. All applications need to limit the output current to less than 50mA. Adequate thermal heat sinking of the parts is also required.

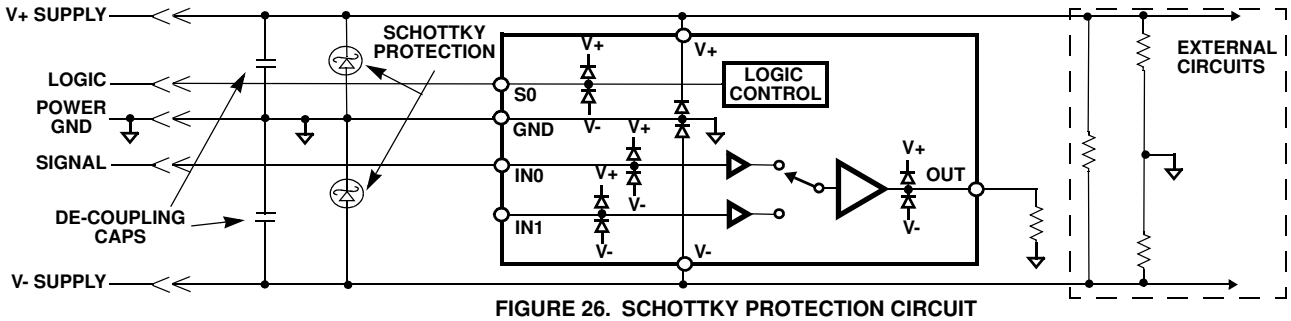


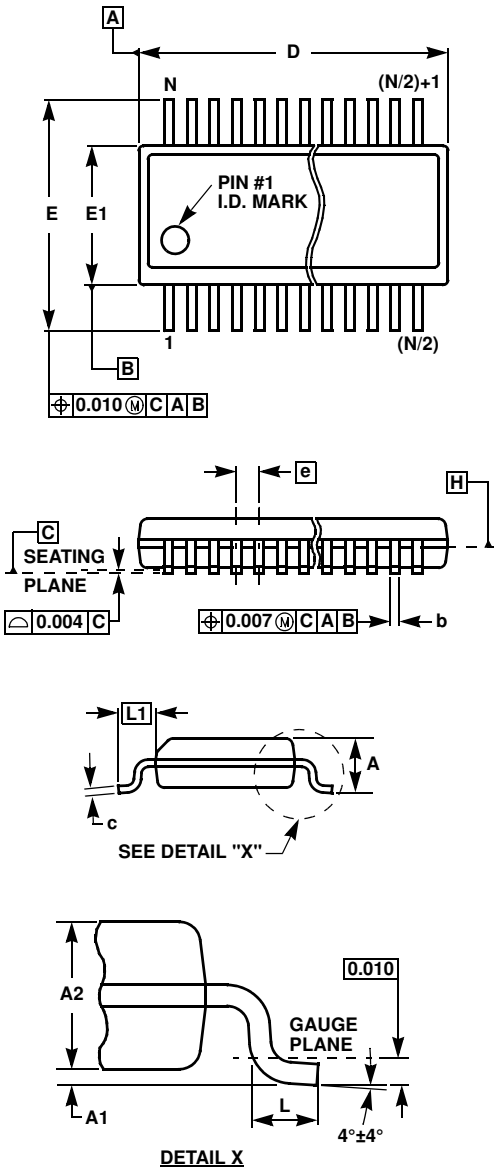

FIGURE 26. SCHOTTKY PROTECTION CIRCUIT

## PC Board Layout

The frequency response of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high frequency performance from your PC board.

- The use of low inductance components such as chip resistors and chip capacitors is strongly recommended.
- Match channel-channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches.
- Maximize use of AC de-coupled PCB layers. All signal I/O lines should be routed over continuous ground planes (i.e. no split planes or PCB gaps under these lines). Avoid vias in the signal I/O lines.
- Use proper value and location of termination resistors. Termination resistors should be as close to the device as possible.
- When testing use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.
- Minimum of 2 power supply de-coupling capacitors are recommended (1000pF, 0.01µF) as close to the device as possible - Avoid vias between the cap and the device because vias add unwanted inductance. Larger caps can be farther away. When vias are required in a layout, they should be routed as far away from the device as possible.
- The NIC pins are placed on both sides of the input pins. These pins are not internally connected to the die. It is recommended these pins be tied to ground to minimize crosstalk.

## Quarter Size Outline Plastic Packages Family (QSOP)




### MDP0040

**QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY**

| SYMBOL | INCHES | | | TOLERANCE | NOTES |
|---|---|---|---|---|---|
| | QSOP16 | QSOP24 | QSOP28 | | |
| A | 0.068 | 0.068 | 0.068 | Max. | - |
| A1 | 0.006 | 0.006 | 0.006 | ±0.002 | - |
| A2 | 0.056 | 0.056 | 0.056 | ±0.004 | - |
| b | 0.010 | 0.010 | 0.010 | ±0.002 | - |
| c | 0.008 | 0.008 | 0.008 | ±0.001 | - |
| D | 0.193 | 0.341 | 0.390 | ±0.004 | 1, 3 |
| E | 0.236 | 0.236 | 0.236 | ±0.008 | - |
| E1 | 0.154 | 0.154 | 0.154 | ±0.004 | 2, 3 |
| e | 0.025 | 0.025 | 0.025 | Basic | - |
| L | 0.025 | 0.025 | 0.025 | ±0.009 | - |
| L1 | 0.041 | 0.041 | 0.041 | Basic | - |
| N | 16 | 24 | 28 | Reference | - |

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.006” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.