

2.5-V TO 3.3-V HIGH-PERFORMANCE CLOCK BUFFER

Check for Samples: [CDCVF2310-EP](#)

FEATURES

- High-Performance 1:10 Clock Driver
- Operates up to 200 MHz at V_{DD} 3.3 V
- Pin-to-Pin Skew < 100 ps at V_{DD} 3.3 V
- V_{DD} Range: 2.3 V to 3.6 V
- Output Enable Glitch Suppression
- Distributes One Clock Input to Two Banks of Five Outputs
- 25- Ω On-Chip Series Damping Resistors
- Packaged in 24-Pin TSSOP

APPLICATIONS

- General-Purpose Applications

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site
- Available in Military (-55°C to 125°C) Temperature Range ⁽¹⁾
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

(1) Custom temperature ranges available

DESCRIPTION

The CDCVF2310 is a high-performance, low-skew clock buffer that operates up to 200 MHz. Two banks of five outputs each provide low-skew copies of CLK. After power up, the default state of the outputs is low regardless of the state of the control pins. For normal operation, the outputs of bank 1Y[0:4] or 2Y[0:4] can be placed in a low state when the control pins (1G or 2G, respectively) are held low and a negative clock edge is detected on the CLK input. The outputs of bank 1Y[0:4] or 2Y[0:4] can be switched into the buffer mode when the control pins (1G and 2G) are held high and a negative clock edge is detected on the CLK input. The device operates in a 2.5-V and 3.3-V environment. The built-in output enable glitch suppression ensures a synchronized output enable sequence to distribute full period clock signals.

The CDCVF2310 is characterized for operation from -55°C to 125°C .

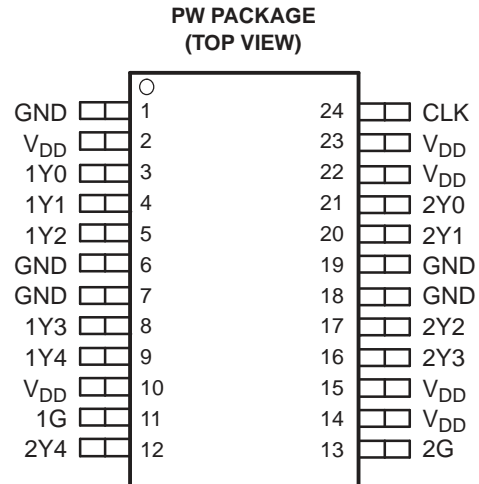
Table 1. ORDERING INFORMATION⁽¹⁾

T_J	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
-55°C to 125°C	TSSOP - PW	CDCVF2310MPWREP	CKV2310EP	V62/13603-01XE
		CDCVF2310MPWEP	CKV2310EP	V62/13603-01XE-T

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM

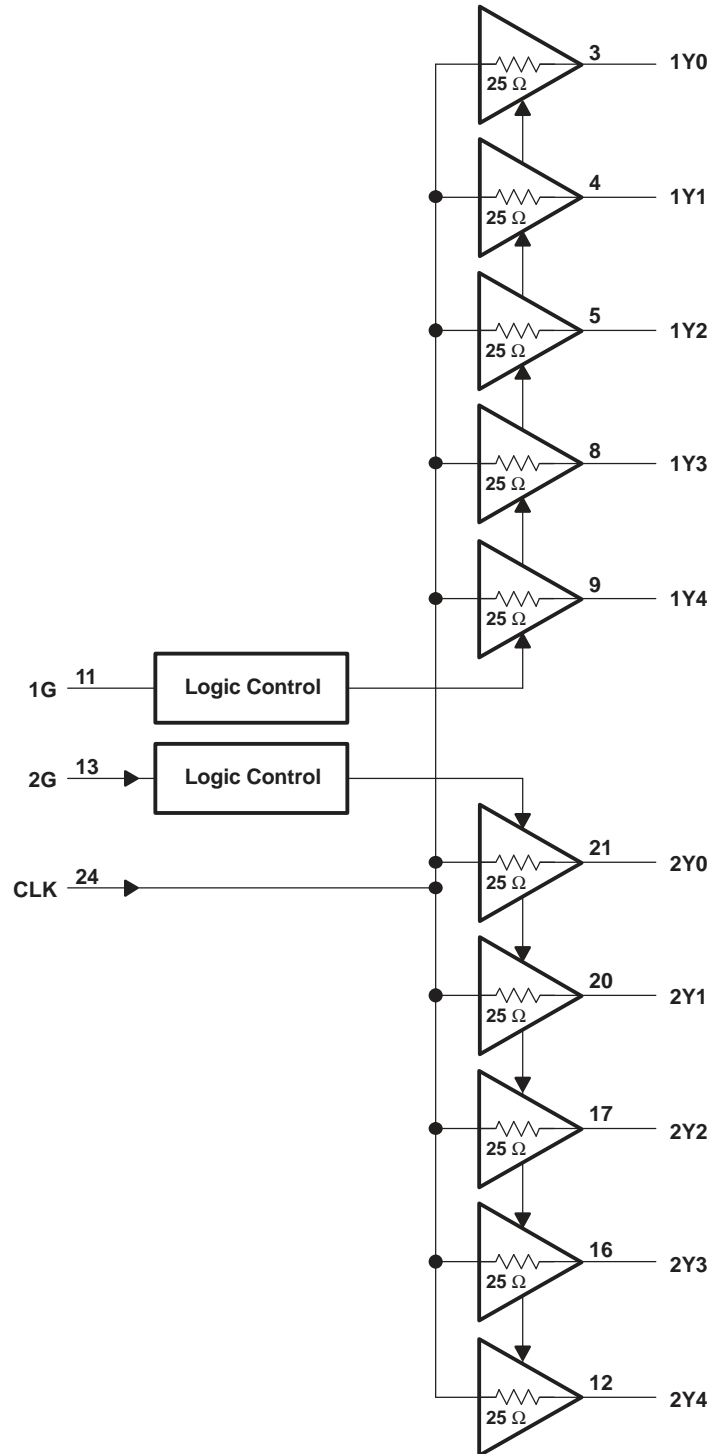


Table 2. FUNCTION TABLE

INPUT			OUTPUT	
1G	2G	CLK	1Y[0:4]	2Y[0:4]
L	L	↓	L	L
H	L	↓	CLK ⁽¹⁾	L
L	H	↓	L	CLK ⁽¹⁾
H	H	↓	CLK ⁽¹⁾	CLK ⁽¹⁾

- (1) After detecting one negative edge on the CLK input, the output follows the input CLK if the control pin is held high.

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
1G	11	I	Output enable control for 1Y[0:4] outputs. This output enable is active-high, meaning the 1Y[0:4] clock outputs follow the input clock (CLK) if this pin is logic high.
2G	13	I	Output enable control for 2Y[0:4] outputs. This output enable is active-high, meaning the 2Y[0:4] clock outputs follow the input clock (CLK) if this pin is logic high.
1Y[0:4]	3, 4, 5, 8, 9	O	Buffered output clocks
2Y[0:4]	21, 20, 17, 16, 12	O	Buffered output clocks
CLK	24	I	Input reference frequency
GND	1, 6, 7, 18, 19		Ground
V _{DD}	2, 10, 14, 15, 22, 23		DC power supply, 2.3 V – 3.6 V

ABSOLUTE MAXIMUM RATINGS

over operating junction temperature range (unless otherwise noted) ⁽¹⁾

Supply voltage range, V _{DD}	–0.5 V to 4.6 V
Input voltage range, V _I ⁽²⁾ ⁽³⁾	–0.5 V to V _{DD} + 0.5 V
Output voltage range, V _O ⁽²⁾ ⁽³⁾	–0.5 V to V _{DD} + 0.5 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD})	±50 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD})	±50 mA
Continuous total output current, I _O (V _O = 0 to V _{DD})	±50 mA
Storage temperature range T _{stg}	–65°C to 150°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This value is limited to 4.6 V maximum.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		CDCVF2310		UNITS
		PW		
		24 PINS		
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	91.7		°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance ⁽³⁾	31.2		
θ_{JB}	Junction-to-board thermal resistance ⁽⁴⁾	46.4		
ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	1.5		
ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	45.8		
θ_{JCbott}	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	N/A		

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.3	2.5		V
			3.3	3.6	
Low-level input voltage, V_{IL}	$V_{DD} = 3\text{ V to }3.6\text{ V}$			0.8	V
	$V_{DD} = 2.3\text{ V to }2.7\text{ V}$			0.7	
High-level input voltage, V_{IH}	$V_{DD} = 3\text{ V to }3.6\text{ V}$	2			V
	$V_{DD} = 2.3\text{ V to }2.7\text{ V}$	1.7			
Input voltage, V_i		0		V_{DD}	V
High-level output current, I_{OH}	$V_{DD} = 3\text{ V to }3.6\text{ V}$			12	mA
	$V_{DD} = 2.3\text{ V to }2.7\text{ V}$			6	
Low-level output current, I_{OL}	$V_{DD} = 3\text{ V to }3.6\text{ V}$			12	mA
	$V_{DD} = 2.3\text{ V to }2.7\text{ V}$			6	
Operating junction temperature, T_J		-55		125	°C

- (1) Unused inputs must be held high or low to prevent them from floating.

ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IK}	Input voltage	V _{DD} = 3 V,	I _I = -18 mA			-1.2	V
I _I	Input current	V _I = 0 V or V _{DD}				±5	μA
I _{DD} ⁽²⁾	Static device current	CLK = 0 V or V _{DD} ,	I _O = 0 mA			100	μA
C _I	Input capacitance	V _{DD} = 2.3 V to 3.6 V,	V _I = 0 V or V _{DD}		2.5		pF
C _O	Output capacitance	V _{DD} = 2.3 V to 3.6 V,	V _I = 0 V or V _{DD}		2.8		pF
V_{DD} = 3.3 V ±0.3 V							
V _{OH}	High-level output voltage	V _{DD} = min to max,	I _{OH} = -100 μA	V _{DD} - 0.2			V
		V _{DD} = 3 V	I _{OH} = -12 mA I _{OH} = -6 mA	2.1	2.4		
V _{OL}	Low-level output voltage	V _{DD} = min to max,	I _{OL} = -100 μA			0.2	V
		V _{DD} = 3 V	I _{OL} = 12 mA I _{OL} = 6 mA			0.8 0.55	
I _{OH}	High-level output current	V _{DD} = 3 V,	V _O = 1 V	-28			mA
		V _{DD} = 3.3 V,	V _O = 1.65 V	-36			
		V _{DD} = 3.6 V,	V _O = 3.135 V	-14			
I _{OL}	Low-level output current	V _{DD} = 3 V,	V _O = 1.95 V	28			mA
		V _{DD} = 3.3 V,	V _O = 1.65 V	36			
		V _{DD} = 3.6 V,	V _O = 0.4 V	14			
V_{DD} = 2.5 V ±0.2 V							
V _{OH}	High-level output voltage	V _{DD} = min to max,	I _{OH} = -100 μA	V _{DD} - 0.2			V
		V _{DD} = 2.3 V	I _{OH} = -6 mA	1.8			
V _{OL}	Low-level output voltage	V _{DD} = min to max,	I _{OL} = 100 μA			0.2	V
		V _{DD} = 2.3 V	I _{OL} = 6 mA			0.55	
I _{OH}	High-level output current	V _{DD} = 2.3 V,	V _O = 1 V	-15			mA
		V _{DD} = 2.5 V,	V _O = 1.25 V	-25			
		V _{DD} = 2.7 V,	V _O = 2.375 V	-10			
I _{OL}	Low-level output current	V _{DD} = 2.3 V,	V _O = 1.2 V	15			mA
		V _{DD} = 2.5 V,	V _O = 1.25 V	25			
		V _{DD} = 2.7 V,	V _O = 0.3 V	10			

 (1) All typical values are at respective nominal V_{DD}.

 (2) For I_{CC} over frequency, see [Figure 6](#).

TIMING REQUIREMENTS

over recommended ranges of supply voltage and operating junction temperature

		MIN	NOM	MAX	UNIT	
f _{clk}	Clock frequency	V _{DD} = 3 V to 3.6 V		0	200	MHz
		V _{DD} = 2.3 V to 2.7 V		0	170	

JITTER CHARACTERISTICS

Characterized using CDCVF2310 Performance EVM when V_{DD}=3.3 V. Outputs not under test are terminated to 50 Ω.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{jitter}	Additive phase jitter from input to output 1Y0	12 kHz to 5 MHz, f _{out} = 30.72 MHz		52	fs rms
		12 kHz to 20 MHz, f _{out} = 125 MHz		45	

SWITCHING CHARACTERISTICS

over recommended operating junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V_{DD} = 3.3 V ±0.3 V (see Figure 2)						
t _{PLH}	CLK to Yn	f = 0 MHz to 200 MHz For circuit load, see Figure 2.		1.3	3.3	ns
t _{PHL}						
t _{sk(o)}	Output skew (Ym to Yn) ⁽¹⁾ (see Figure 4)			100	ps	
t _{sk(p)}	Pulse skew (see Figure 5)			570	ps	
t _{sk(pp)}	Part-to-part skew			500	ps	
t _r	Rise time (see Figure 3)	V _O = 0.4 V to 2 V		0.7	2.2	V/ns
t _f	Fall time (see Figure 3)	V _O = 2 V to 0.4 V		0.7	2.2	V/ns
t _{su(en)}	Enable setup time, G_high before CLK ↓			0.1		ns
t _{su(dis)}	Disable setup time, G_low before CLK ↓			0.1		ns
t _{h(en)}	Enable hold time, G_high after CLK ↓			0.4		ns
t _{h(dis)}	Disable hold time, G_low after CLK ↓			0.4		ns
V_{DD} = 2.5 V ±0.2 V (see Figure 2)						
t _{PLH}	CLK to Yn	f = 0 MHz to 170 MHz For circuit load, see Figure 2.		1.5	4	ns
t _{PHL}						
t _{sk(o)}	Output skew (Ym to Yn) ⁽¹⁾ (see Figure 4)			170	ps	
t _{sk(p)}	Pulse skew (see Figure 5)			680	ps	
t _{sk(pp)}	Part-to-part skew			600	ps	
t _r	Rise time (see Figure 3)	V _O = 0.4 V to 1.7 V		0.5	1.4	V/ns
t _f	Fall time (see Figure 3)	V _O = 1.7 V to 0.4 V		0.5	1.4	V/ns
t _{su(en)}	Enable setup time, G_high before CLK ↓			0.1		ns
t _{su(dis)}	Disable setup time, G_low before CLK ↓			0.1		ns
t _{h(en)}	Enable hold time, G_high after CLK ↓			0.4		ns
t _{h(dis)}	Disable hold time, G_low after CLK ↓			0.4		ns

(1) The t_{sk(o)} specification is only valid for equal loading of all outputs.

DETAILED DESCRIPTION

Output Enable Glitch Suppression Circuit

The purpose of the glitch suppression circuitry is to ensure the output enable sequence is synchronized with the clock input such that the output buffer is enabled or disabled on the next full period of the input clock (negative edge triggered by the input clock) (see Figure 1).

The G input must fulfill the timing requirements (t_{su} , t_h) according to the *Switching Characteristics* table for predictable operation.

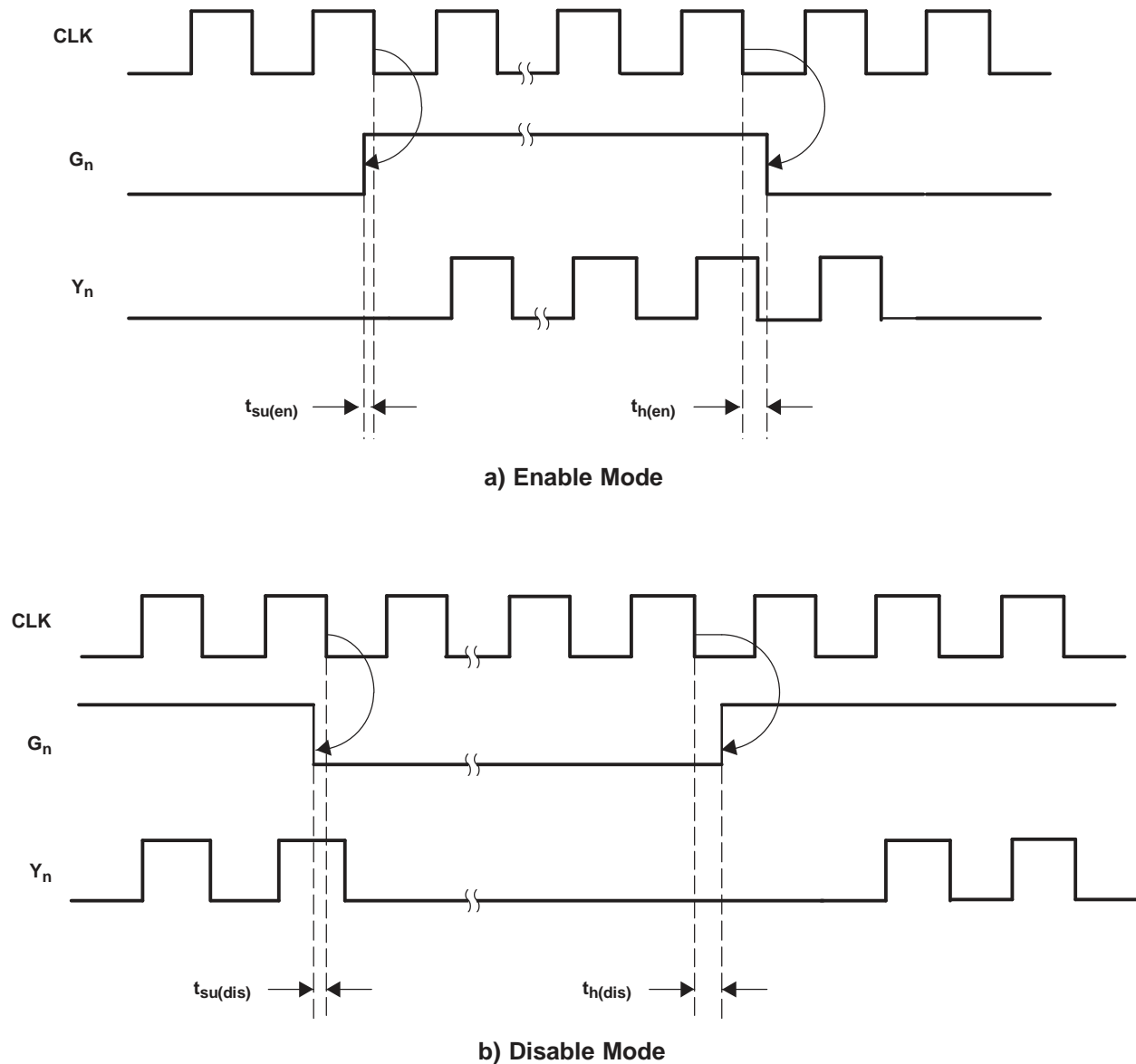
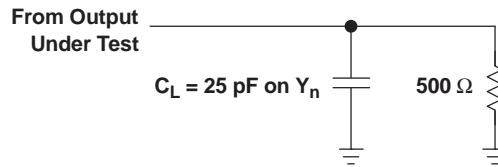


Figure 1. Enable and Disable Mode Relative to CLK↓

PARAMETER MEASUREMENT INFORMATION



- A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 200 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r < 1.2 \text{ ns}$, $t_f < 1.2 \text{ ns}$.

Figure 2. Test Load Circuit

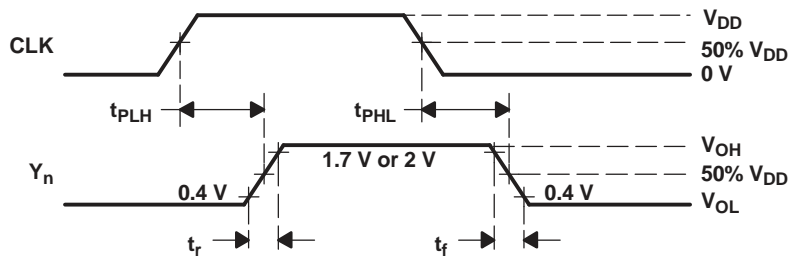


Figure 3. Voltage Waveforms Propagation Delay Times

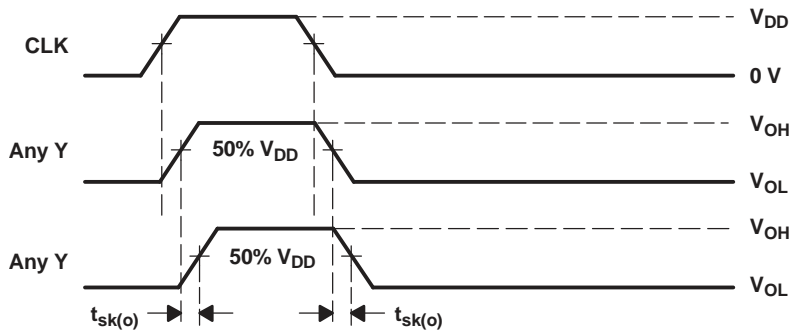
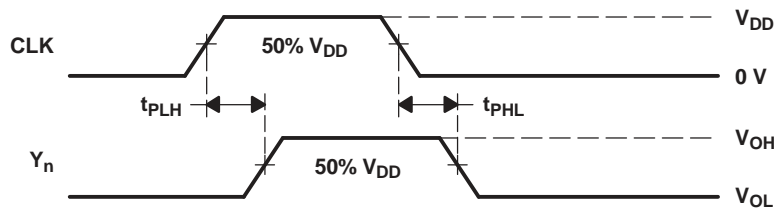


Figure 4. Output Skew



NOTE: $t_{sk(p)} = |t_{PLH} - t_{PHL}|$

Figure 5. Pulse Skew

PARAMETER MEASUREMENT INFORMATION (continued)

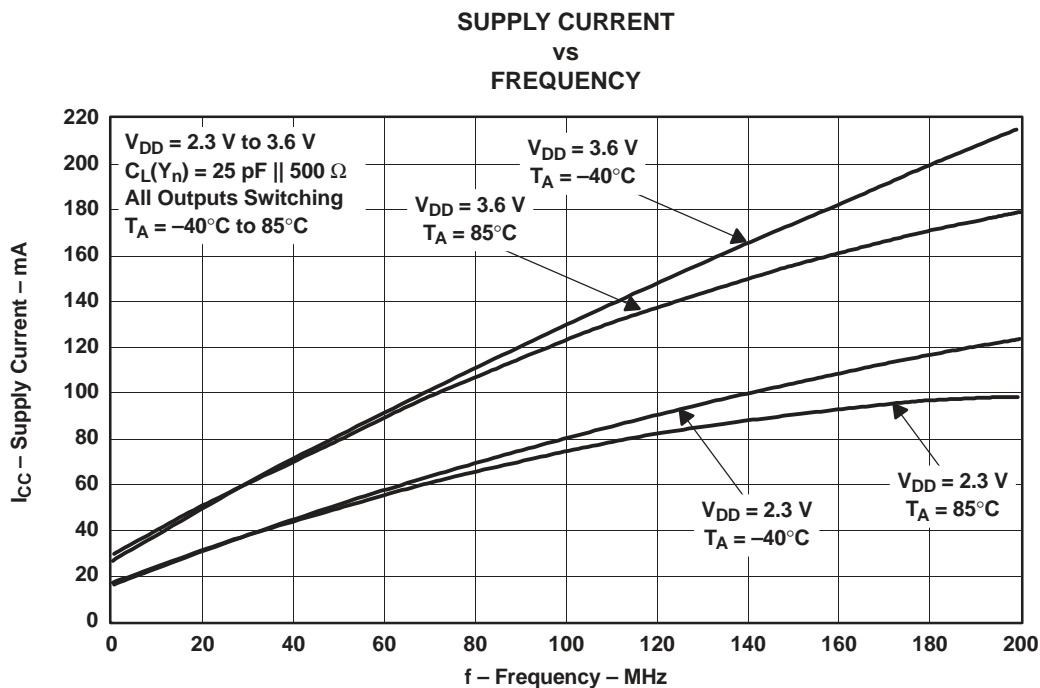


Figure 6.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCVF2310MPWEP	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CKV2310EP	Samples
CDCVF2310MPWREP	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CKV2310EP	Samples
V62/13603-01XE	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CKV2310EP	Samples
V62/13603-01XE-T	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CKV2310EP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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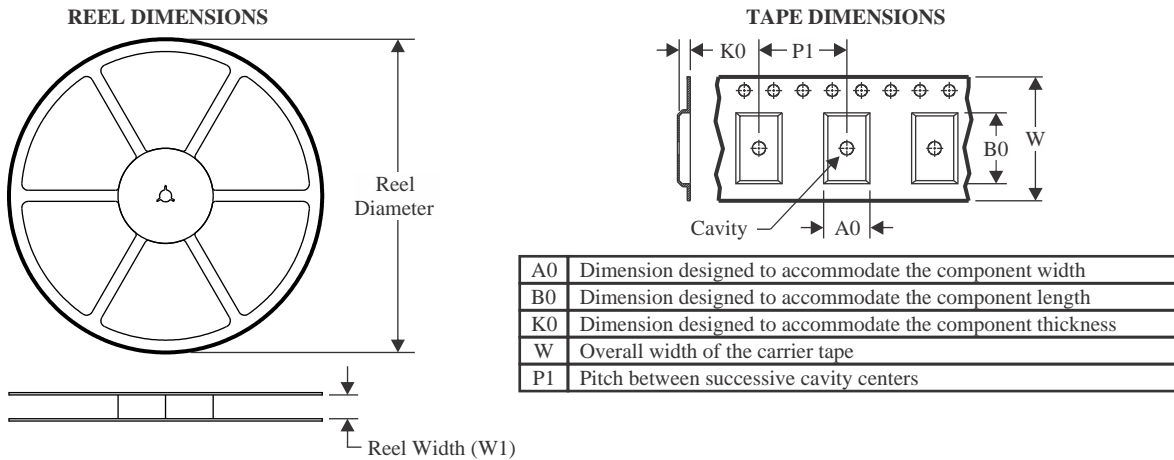
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OTHER QUALIFIED VERSIONS OF CDCVF2310-EP :

- Catalog: [CDCVF2310](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

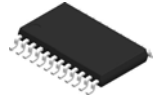
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF2310MPWREP	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF2310MPWREP	TSSOP	PW	24	2000	356.0	356.0	35.0

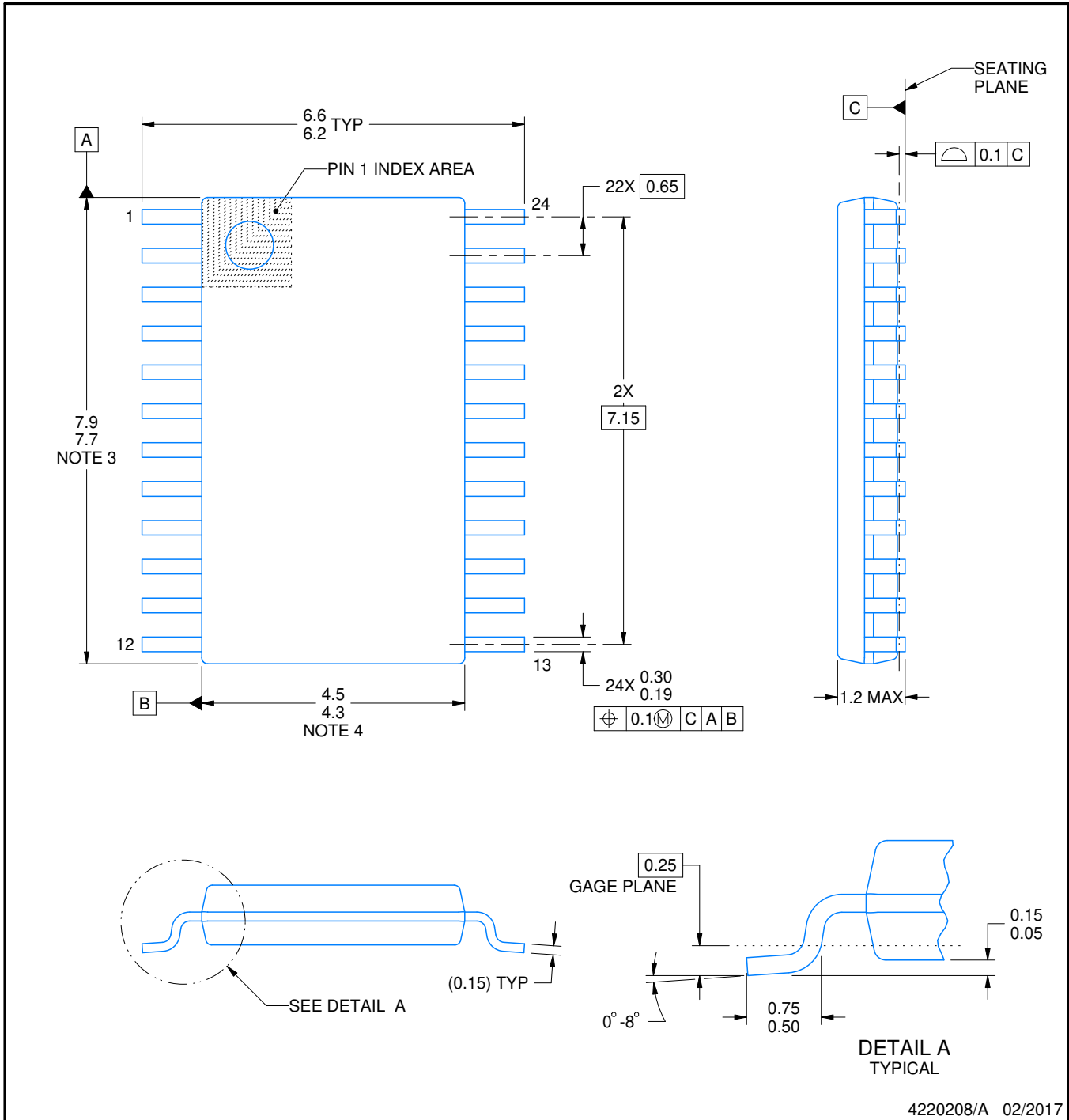
PW0024A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

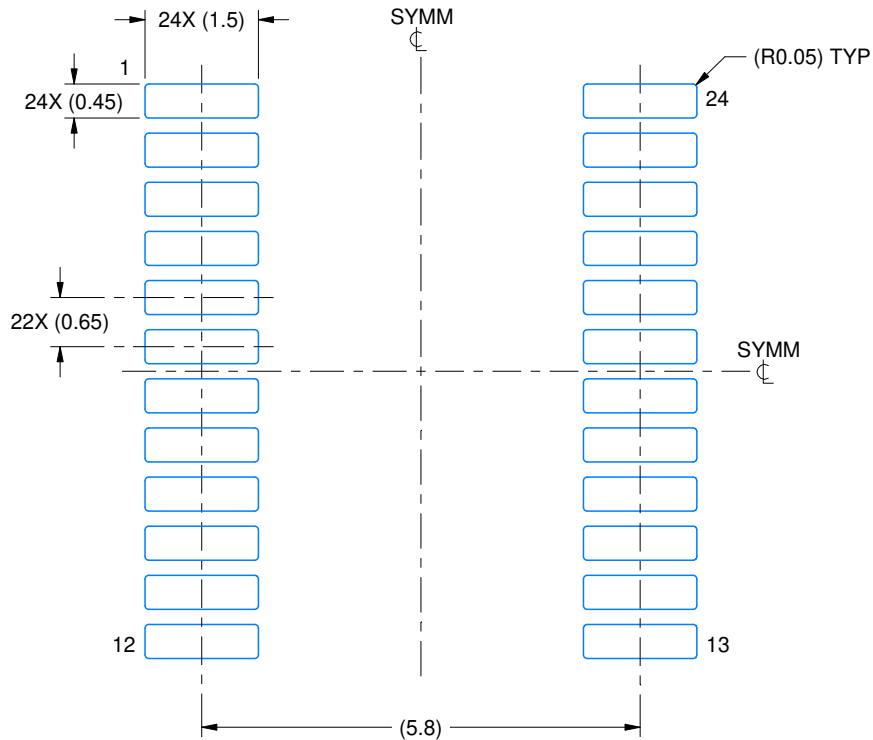
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

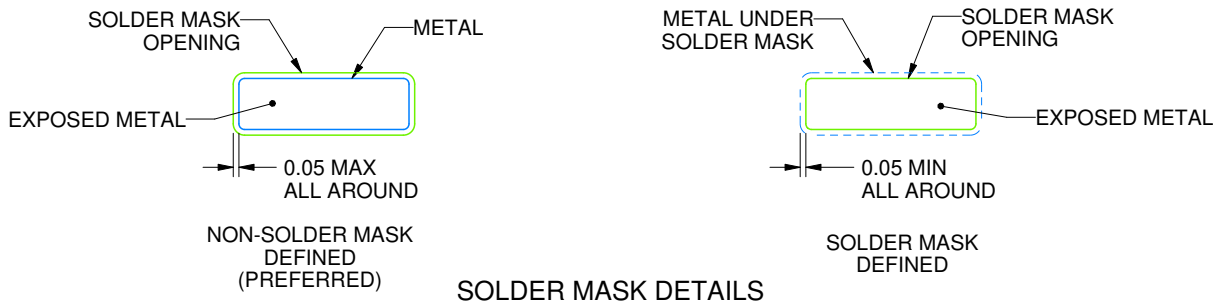
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

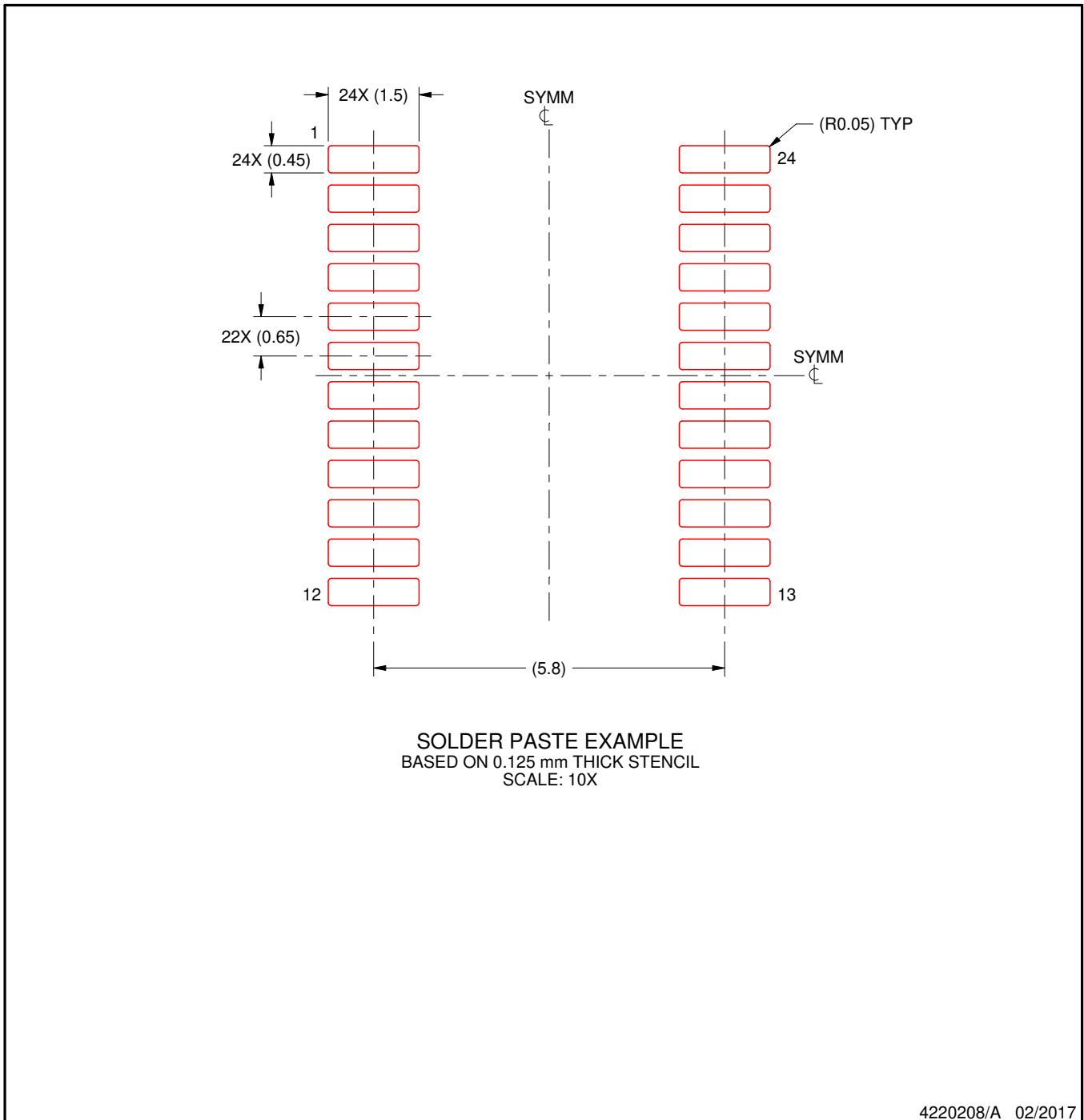
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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