BLF10H6600P; BLF10H6600PS

Power LDMOS transistor

AMPLEON

Rev. 3 — 1 September 2015

Product data sheet

1. Product profile

1.1 General description

A 600 W LDMOS RF power transistor for transmitter applications and industrial applications. The excellent ruggedness of this device makes it ideal for digital and analog transmitter applications.

Table 1. Application information

Test signal	f (MHz)	$P_{L(AV)}$ (W)	$P_{L(M)}$ (W)	G_p (dB)	η_D (%)	IMD3 (dBc)
RF performance in a common source 860 MHz narrowband test circuit						
2-tone, class-AB	f_1 = 860; f_2 = 860.1	250	-	20.8	46	−32
pulsed, class-AB	860	-	600	19.8	58	-

1.2 Features and benefits

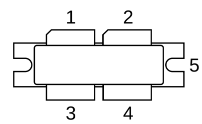
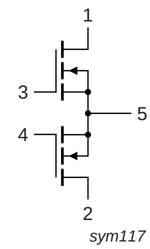
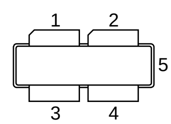
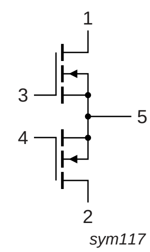
- Excellent ruggedness (VSWR ≥ 40 : 1 through all phases)
- Optimum thermal behavior and reliability, $R_{th(j-c)}$ = 0.15 K/W
- High power gain
- High efficiency
- Designed for broadband operation (400 MHz to 1000 MHz)
- Internal input matching for high gain and optimum broadband operation
- Excellent reliability
- Easy power control
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Communication transmitter applications
- Industrial applications

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLF10H6600P (SOT539A)				
1	drain1			
2	drain2			
3	gate1			
4	gate2			
5	source	[1]		
BLF10H6600PS (SOT539B)				
1	drain1			
2	drain2			
3	gate1			
4	gate2			
5	source	[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF10H6600P	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF10H6600PS	-	earless flanged balanced ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	110	V
V_{GS}	gate-source voltage		−0.5	+11	V
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; $P_{L(AV)}$ = 250 W	[1]	0.15	K/W

[1] $R_{th(j-c)}$ is measured under RF conditions.

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.4 mA	[1]	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 240 mA	[1]	1.4	1.9	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V		-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V		-	36	-	A
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V		-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 8.5 A	[1]	-	143	-	mΩ

[1] I_D is the drain current.

Table 7. AC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	[1]	-	220	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz		-	74	-	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz		-	1.2	-	pF

[1] Capacitance values without internal matching.

Table 8. RF characteristics

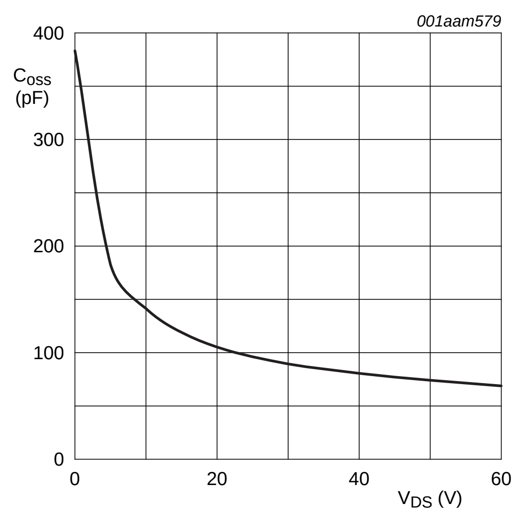
RF characteristics in Ampleon production narrowband test circuit; T_{case} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
2-Tone, class-AB							
V_{DS}	drain-source voltage			-	50	-	V
I_{Dq}	quiescent drain current		[1]	-	1.3	-	A
$P_{L(AV)}$	average output power	f_1 = 860 MHz; f_2 = 860.1 MHz		250	-	-	W
G_p	power gain	f_1 = 860 MHz; f_2 = 860.1 MHz		19.8	20.8	-	dB
η_D	drain efficiency	f_1 = 860 MHz; f_2 = 860.1 MHz		42	46	-	%
IMD3	third-order intermodulation distortion	f_1 = 860 MHz; f_2 = 860.1 MHz		-	−32	−28	dBc

Table 8. RF characteristics *...continued*
RF characteristics in Ampleon production narrowband test circuit; T_{case} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Pulsed, class-AB							
V_{DS}	drain-source voltage			-	50	-	V
I_{Dq}	quiescent drain current		[1]	-	1.3	-	A
$P_{L(M)}$	peak output power	f = 860 MHz		-	600	-	W
G_p	power gain	f = 860 MHz		17.2	19.8	-	dB
η_D	drain efficiency	f = 860 MHz		54	58	-	%
t_p	pulse duration			-	100	-	µs
δ	duty cycle			-	20	-	%

[1] I_{Dq} for total device



V_{GS} = 0 V; f = 1 MHz.

Fig 1. Output capacitance as a function of drain-source voltage; typical values per section

7. Test information

7.1 Ruggedness in class-AB operation

The BLF10H6600P and BLF10H6600PS are capable of withstanding a load mismatch corresponding to VSWR ≥ 40 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 1.3 A; P_L = 600 W (pulsed); f = 860 MHz.

7.2 Impedance information

Table 9. Typical push-pull impedance

Simulated Z_i and Z_L device impedance; impedance info at V_{DS} = 50 V and $P_{L(AV)}$ = 600 W (pulsed CW). See Figure 2 for definition of transistor impedance.

f MHz	Z_i Ω	Z_L Ω
300	0.607 + j0	5.495 + j1.936
325	0.622 – j1.441	5.324 + j2.008
350	0.639 – j1.121	5.151 + j2.065
375	0.658 – j0.826	4.977 + j2.107
400	0.679 – j0.551	4.805 + j2.136
425	0.703 – j0.291	4.634 + j2.153
450	0.73 – j0.044	4.466 + j2.157
475	0.76 + j0.194	4.301 + j2.151
500	0.793 + j0.424	4.14 + j2.134
525	0.83 + j0.648	3.984 + j2.109
550	0.872 + j0.869	3.833 + j2.075
575	0.919 + j1.088	3.687 + j2.033
600	0.972 + j1.305	3.546 + j1.985
625	1.032 + j1.523	3.411 + j1.931
650	1.101 + j1.741	3.281 + j1.871
675	1.179 + j1.963	3.156 + j1.807
700	1.268 + j2.187	3.036 + j1.738
725	1.371 + j2.416	2.922 + j1.666
750	1.49 + j2.651	2.813 + j1.591
775	1.629 + j2.891	2.708 + j1.512
800	1.792 + j3.138	2.609 + j1.432
825	1.984 + j3.39	2.514 + j1.349
850	2.212 + j3.649	2.423 + j1.264
875	2.484 + j3.91	2.336 + j1.178
900	2.812 + j4.17	2.254 + j1.091
925	3.209 + j4.421	2.175 + j1.003
950	3.689 + j4.648	2.1 + j0.913
975	4.27 + j4.829	2.029 + j0.823
1000	4.967 + j4.927	1.96 + j0.733

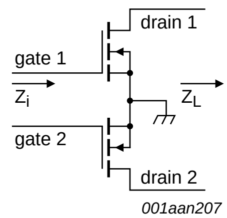


Fig 2. Definition of transistor impedance

7.3 Test circuit information

Table 10. List of components
For test circuit, see Figure 3, Figure 4 and Figure 5.

Component	Description	Value		Remarks
B1, B2	semi rigid coax	25 Ω; 49.5 mm		UT-090C-25 (EZ 90-25)
C1	multilayer ceramic chip capacitor	12 pF	[1]	
C2, C3, C4, C5, C6	multilayer ceramic chip capacitor	8.2 pF	[1]	
C7	multilayer ceramic chip capacitor	6.8 pF	[2]	
C8	multilayer ceramic chip capacitor	2.7 pF	[2]	
C9	multilayer ceramic chip capacitor	2.2 pF	[2]	
C10, C13, C14	multilayer ceramic chip capacitor	100 pF	[3]	
C11, C12	multilayer ceramic chip capacitor	10 pF	[2]	
C15, C16	multilayer ceramic chip capacitor	4.7 μF, 50 V		Kemet C1210X475K5RAC-TU or capacitor of same quality.
C17, C18, C23, C24	multilayer ceramic chip capacitor	100 pF	[2]	
C19, C20	multilayer ceramic chip capacitor	10 μF, 50 V		TDK C570X7R1H106KT000N or capacitor of same quality.
C21, C22	electrolytic capacitor	470 μF; 63 V		
C30	multilayer ceramic chip capacitor	10 pF	[4]	
C31	multilayer ceramic chip capacitor	9.1 pF	[4]	
C32	multilayer ceramic chip capacitor	3.9 pF	[4]	
C33, C34, C35	multilayer ceramic chip capacitor	100 pF	[4]	
C36, C37	multilayer ceramic chip capacitor	4.7 μF, 50 V		TDK C4532X7R1E475MT020U or capacitor of same quality.
L1	microstrip	-	[5]	(W × L) 15 mm × 13 mm
L2	microstrip	-	[5]	(W × L) 5 mm × 26 mm
L3, L32	microstrip	-	[5]	(W × L) 2 mm × 49.5 mm
L4	microstrip	-	[5]	(W × L) 1.7 mm 3.5 mm
L5	microstrip	-	[5]	(W × L) 2 mm × 9.5 mm
L30	microstrip	-	[5]	(W × L) 5 mm × 13 mm
L31	microstrip	-	[5]	(W × L) 2 mm × 11 mm
L33	microstrip	-	[5]	(W × L) 2 mm × 3 mm
R1, R2	wire resistor	10 Ω		

Table 10. List of components *…continued*

For test circuit, see Figure 3, Figure 4 and Figure 5.

Component	Description	Value	Remarks
R3, R4	SMD resistor	5.6 Ω	0805
R5, R6	wire resistor	100 Ω	
R7, R8	potentiometer	10 kΩ	

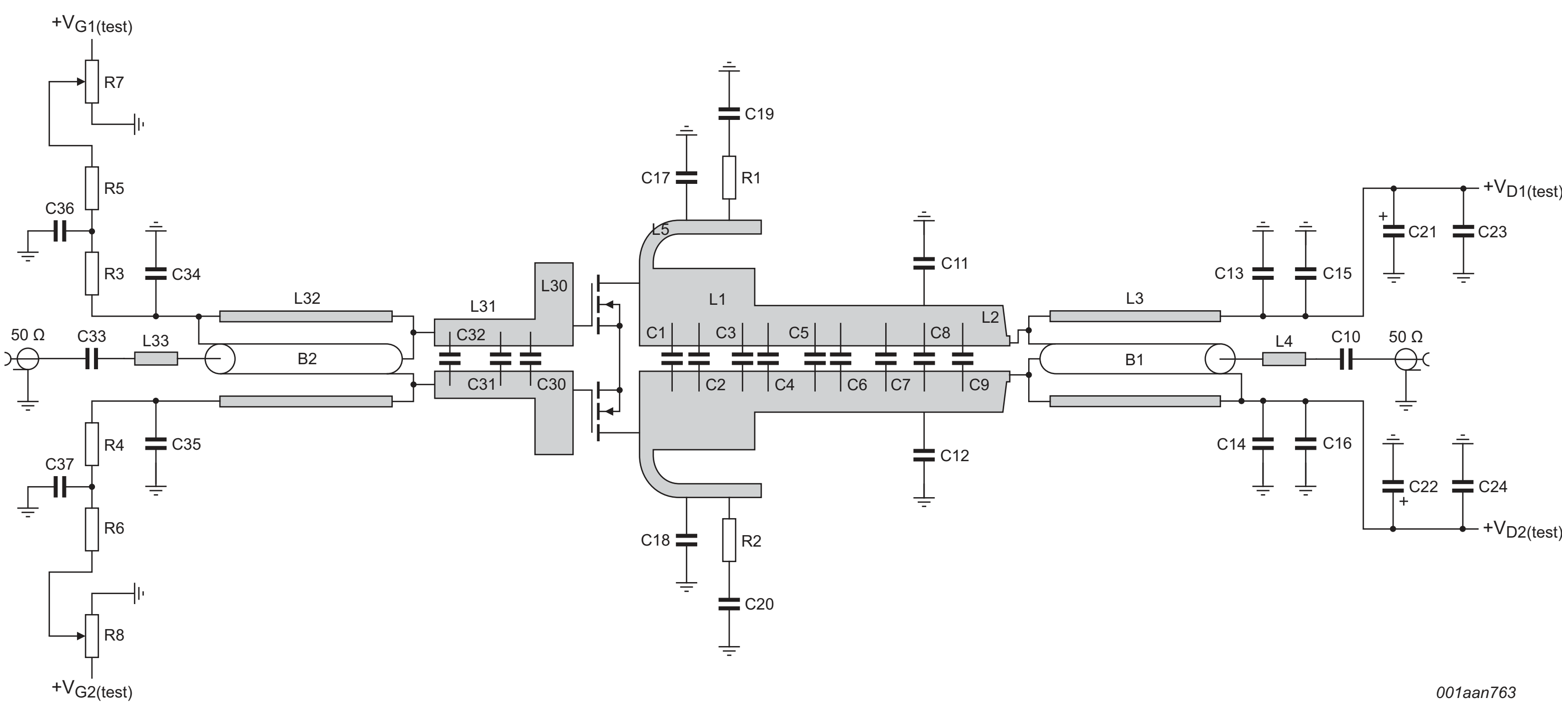
[1] American technical ceramics type 800R or capacitor of same quality.

[2] American technical ceramics type 800B or capacitor of same quality.

[3] American technical ceramics type 180R or capacitor of same quality.

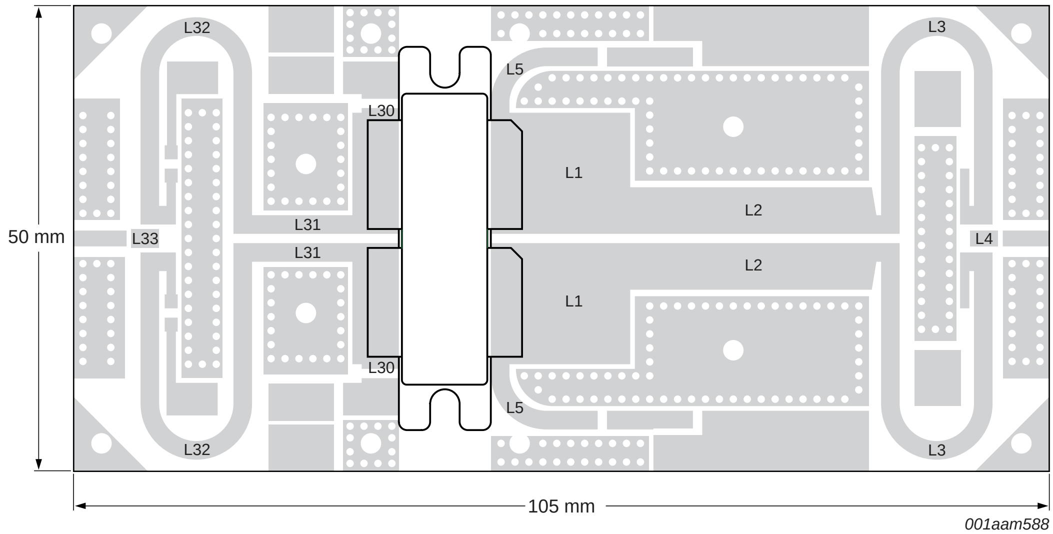
[4] American technical ceramics type 100A or capacitor of same quality.

[5] Printed-Circuit Board (PCB): Taconic RF35; ε_r = 3.5 F/m; height = 0.762 mm; Cu (top/bottom metallization); thickness copper plating = 35 μm.



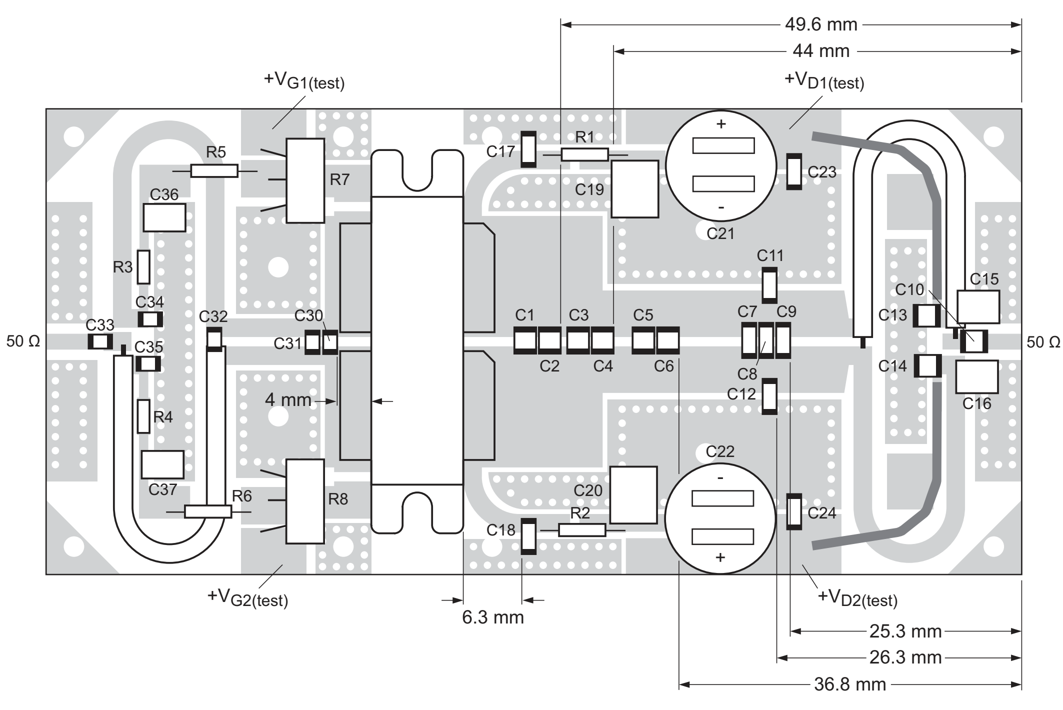
See Table 10 for a list of components.

Fig 3. Class-AB common source broadband amplifier; $V_{D1(test)}$, $V_{D2(test)}$, $V_{G1(test)}$ and $V_{G2(test)}$ are drain and gate test voltages



See Table 10 for a list of components.

Fig 4. Printed-Circuit Board (PCB) for class-AB common source amplifier

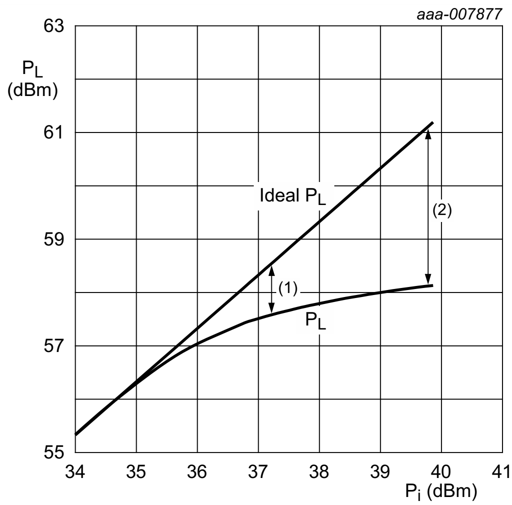


See Table 10 for a list of components.

Fig 5. Component layout for class-AB common source amplifier

7.4 Graphical data

7.4.1 Pulsed

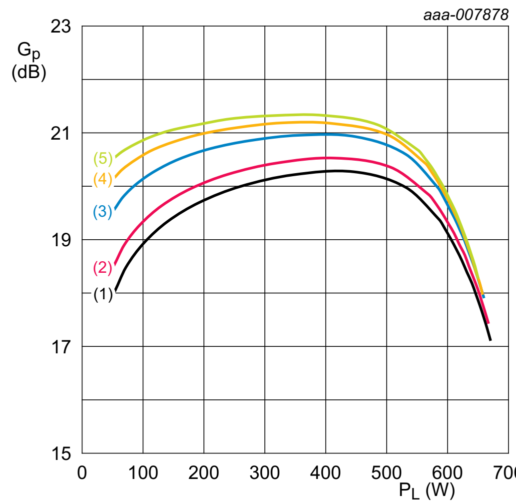


V_{DS} = 50 V; I_{Dq} = 1300 mA; f = 860 MHz; t_p = 100 μs; δ = 20 %.

(1) $P_{L(1dB)}$ = 57.6 dBm (575 W)

(2) $P_{L(3dB)}$ = 58.1 dBm (649 W)

Fig 6. Output power as a function of input power; typical values



V_{DS} = 50 V; f = 860 MHz; t_p = 100 μs; δ = 20 %.

(1) I_{Dq} = 100 mA

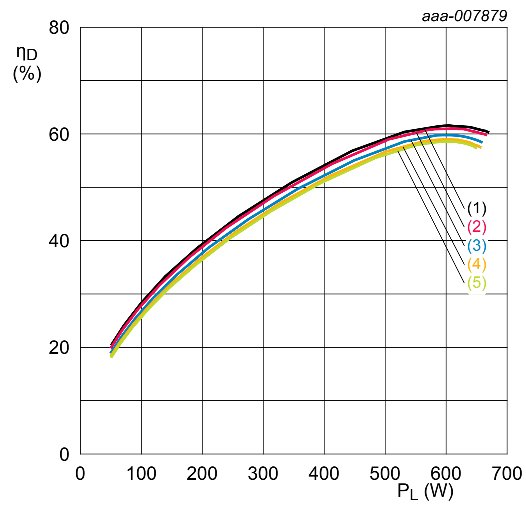
(2) I_{Dq} = 200 mA

(3) I_{Dq} = 600 mA

(4) I_{Dq} = 1000 mA

(5) I_{Dq} = 1300 mA

Fig 7. Power gain as a function of output power; typical values



V_{DS} = 50 V; f = 860 MHz; t_p = 100 μs; δ = 20 %.

(1) I_{Dq} = 100 mA

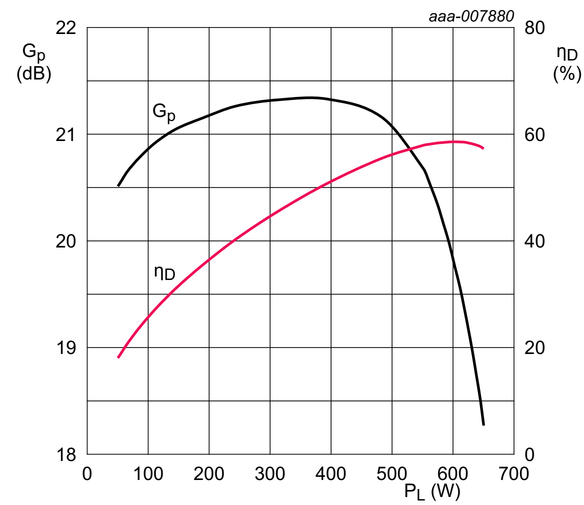
(2) I_{Dq} = 200 mA

(3) I_{Dq} = 600 mA

(4) I_{Dq} = 1000 mA

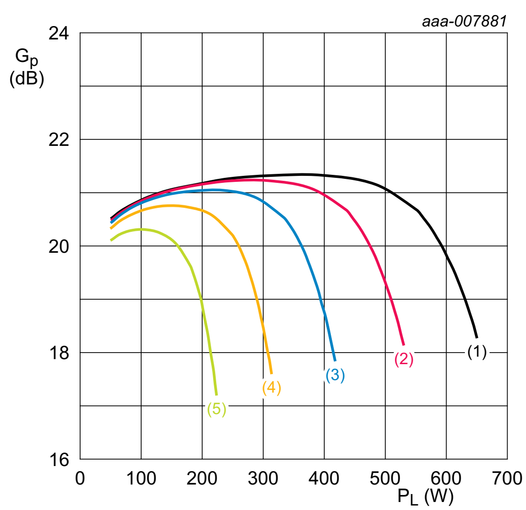
(5) I_{Dq} = 1300 mA

Fig 8. Drain efficiency as a function of output power; typical values



V_{DS} = 50 V; I_{Dq} = 1300 mA; f = 860 MHz; t_p = 100 μs; δ = 20 %.

Fig 9. Power gain and drain efficiency as function of output power; typical values



I_{Dq} = 1300 mA; f = 860 MHz; t_p = 100 μs; δ = 20 %.

(1) V_{DS} = 50 V

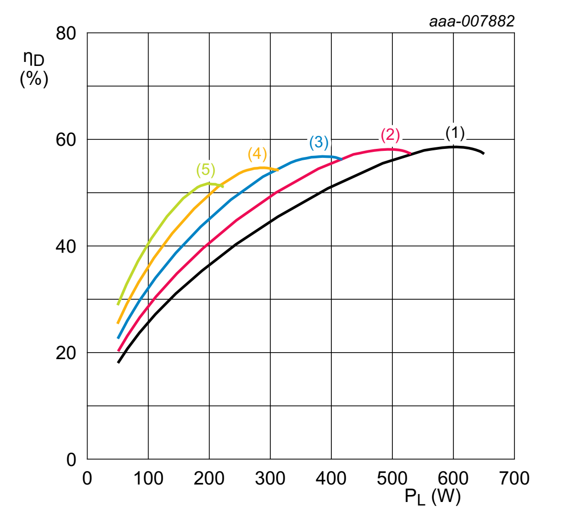
(2) V_{DS} = 45 V

(3) V_{DS} = 40 V

(4) V_{DS} = 35 V

(5) V_{DS} = 30 V

Fig 10. Power gain as a function of output power; typical values



I_{Dq} = 1300 mA; f = 860 MHz; t_p = 100 μs; δ = 20 %.

(1) V_{DS} = 50 V

(2) V_{DS} = 45 V

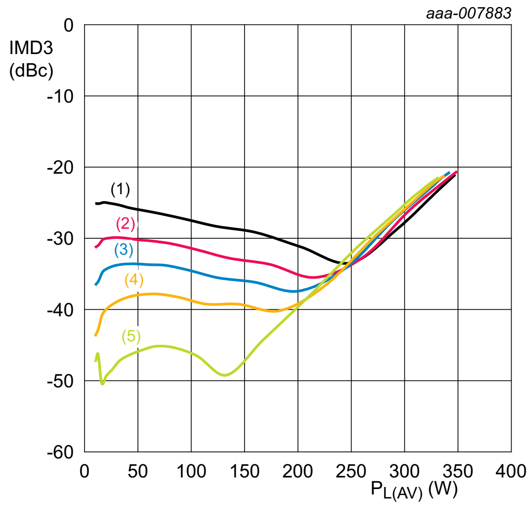
(3) V_{DS} = 40 V

(4) V_{DS} = 35 V

(5) V_{DS} = 30 V

Fig 11. Drain efficiency as a function of output power; typical values

7.4.2 2-Tone CW



V_{DS} = 50 V; f_1 = 860.0 MHz; f_2 = 860.1 MHz.

(1) I_{Dq} = 600 mA

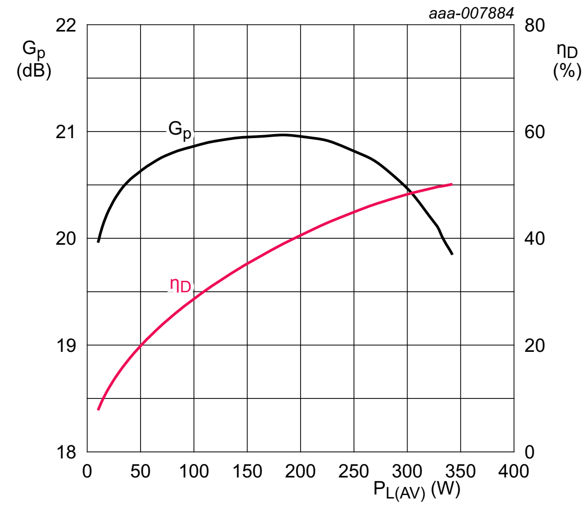
(2) I_{Dq} = 1000 mA

(3) I_{Dq} = 1300 mA

(4) I_{Dq} = 1600 mA

(5) I_{Dq} = 2000 mA

Fig 12. Third-order intermodulation distortion as a function of average output power; typical values

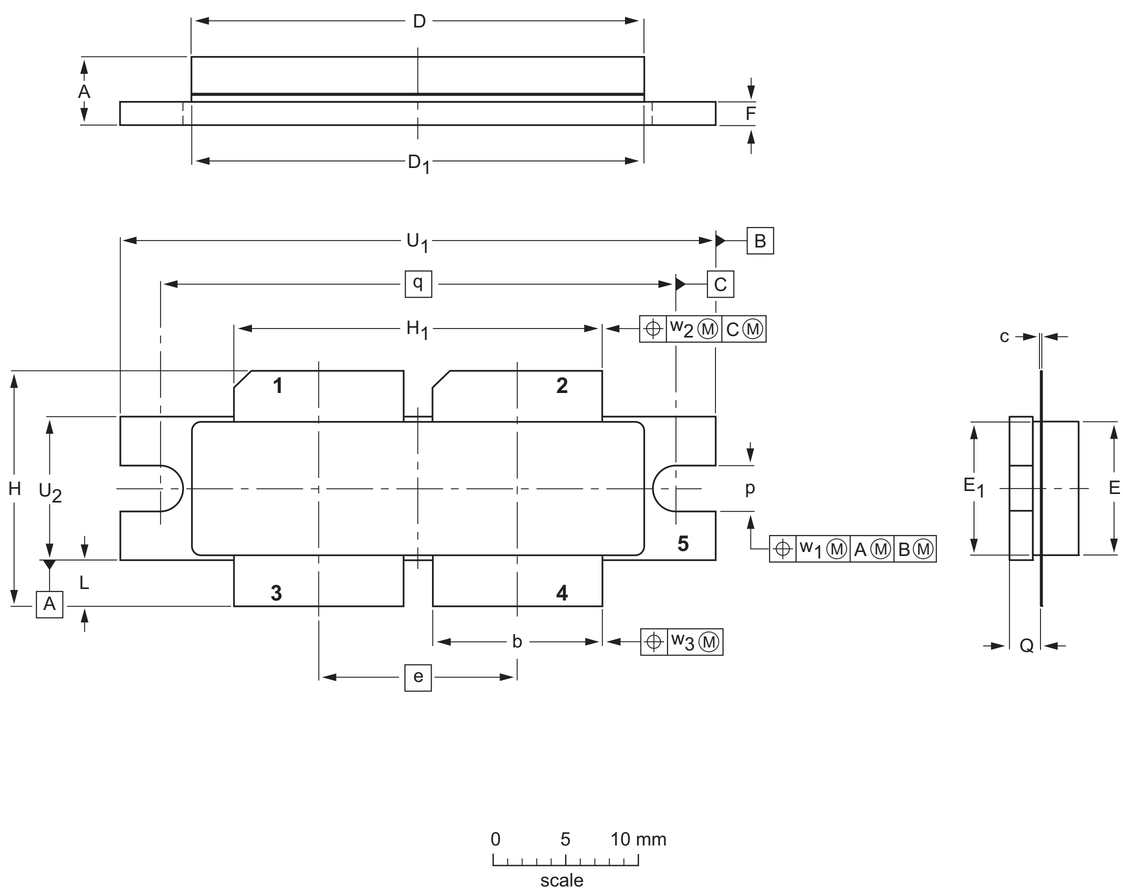


V_{DS} = 50 V; I_{Dq} = 1300 mA; f_1 = 860.0 MHz; f_2 = 860.1 MHz.

Fig 13. Power gain and drain efficiency as function of average output power; typical values

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

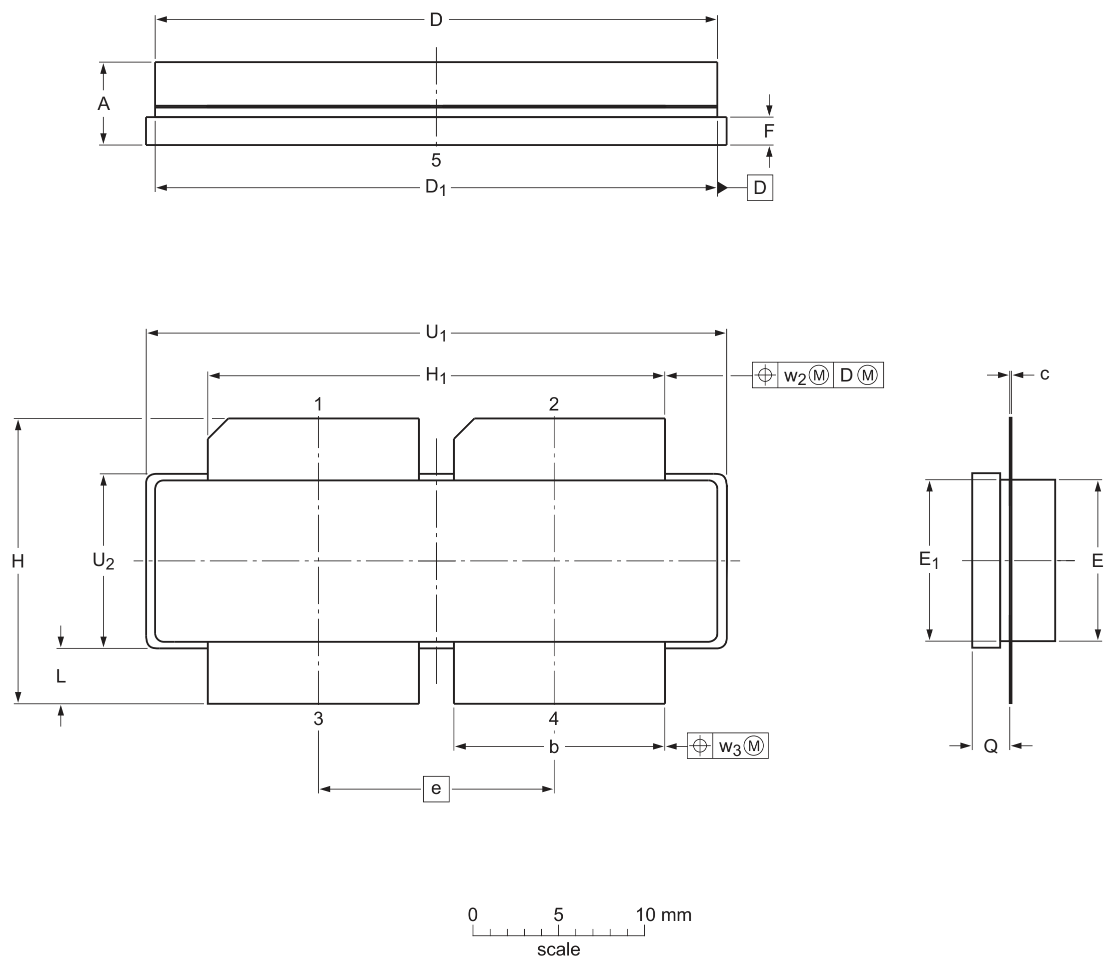
UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~10-02-02~~ 12-05-02

Fig 14. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads **SOT539B**



Dimensions

Unit(1)		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53		1.75	17.12	25.53	3.48	2.26	32.39	10.29		
	nom								13.72								0.25	0.25
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375		0.069	0.674	1.005	0.137	0.089	1.275	0.405		
	nom								0.54								0.01	0.01
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

Note

1. millimeter dimensions are derived from the original inch dimensions.

sot539b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539B						~~12-05-02~~ 13-05-24

Fig 15. Package outline SOT539B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF10H6600P_BLF10H6600PS#3	20150901	Product data sheet	-	BLF10H6600P_BLF10H6600PS v.2
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. • Legal texts have been adapted to the new company name where appropriate.			
BLF10H6600P_BLF10H6600PS v.2	20130620	Product data sheet	-	BLF0510H6600P v.1
BLF0510H6600P v.1	20121009	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

12.2 Definitions

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13. Contact information

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