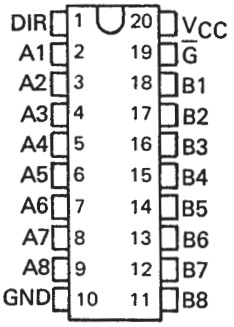
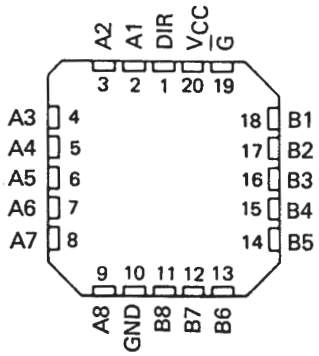
- **SN74LS64X-1 Versions Rated at $I_{OL}$ of 48 mA**
- **Bi-directional Bus Transceivers in High-Density 20-Pin Packages**
- **Hysteresis at Bus Inputs Improves Noise Margins**
- **Choice of True or Inverting Logic**
- **Choice of 3-State or Open-Collector Outputs**

| DEVICE | OUTPUT | LOGIC |
|---|---|---|
| 'LS640 | 3-State | Inverting |
| 'LS641 | Open-Collector | True |
| 'LS642 | Open-Collector | Inverting |
| 'LS644 | Open-Collector | True and inverting |
| 'LS645 | 3-State | True |

**SN54LS' . . . J PACKAGE**
**SN74LS' . . . DW OR N PACKAGE**
**(TOP VIEW)**




**SN54LS' . . . FK PACKAGE**
**(TOP VIEW)**




## description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are effectively isolated.

The -1 versions of the SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are identical to the standard versions except that the recommended maximum $I_{OL}$ is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645.

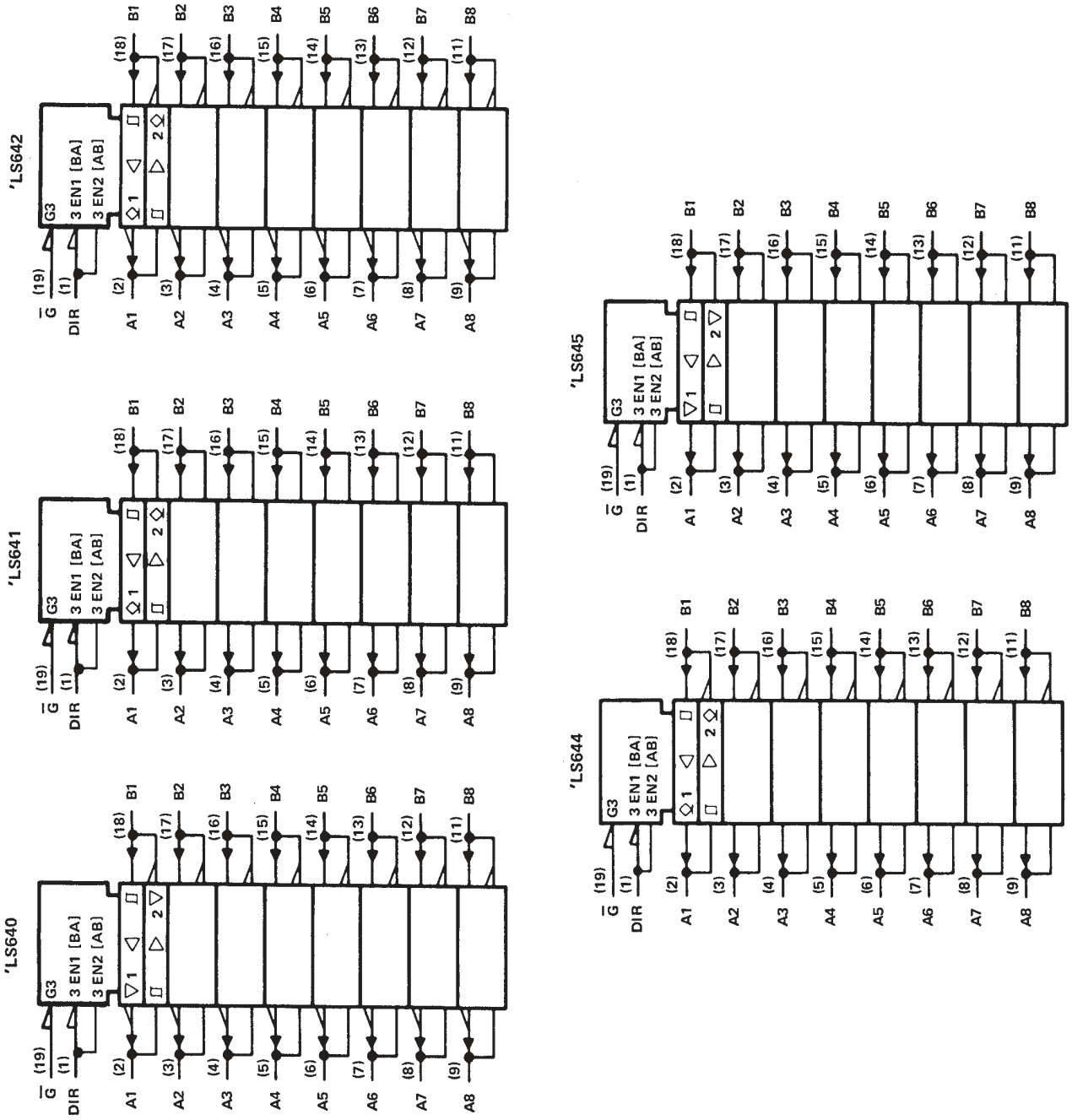
The SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

| CONTROL INPUTS | | OPERATION | | |
|---|---|---|---|---|
| $\overline{G}$ | DIR | 'LS640 'LS642 | 'LS641 'LS645 | 'LS644 |
| L | L | $\overline{B}$ data to A bus | B data to A bus | B data to A bus |
| L | H | $\overline{A}$ data to B bus | A data to B bus | $\overline{A}$ data to B bus |
| H | X | Isolation | Isolation | Isolation |

H = high level, L = low level, X = irrelevant

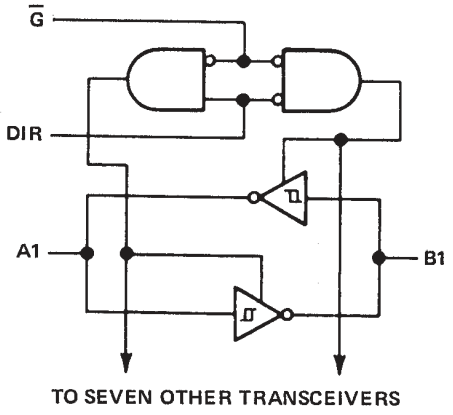
**logic symbols†**



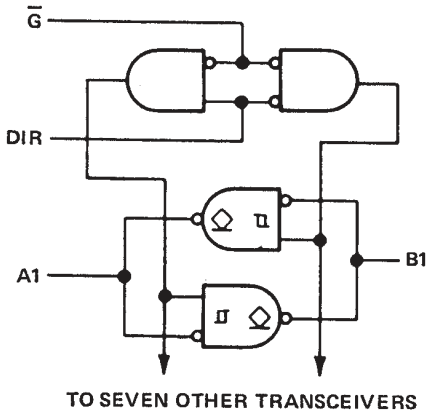

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

**logic diagrams (positive logic)**

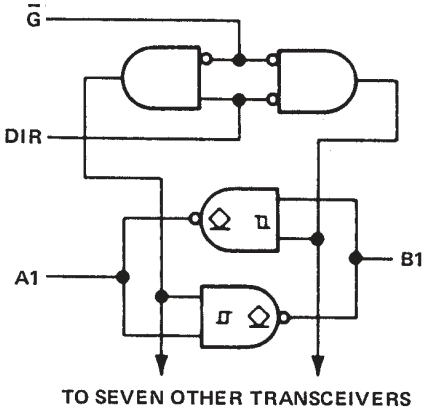
'LS640



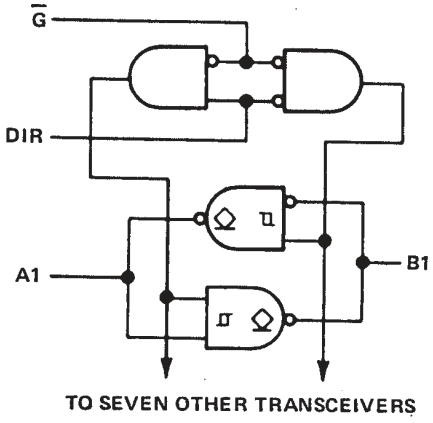

'LS641



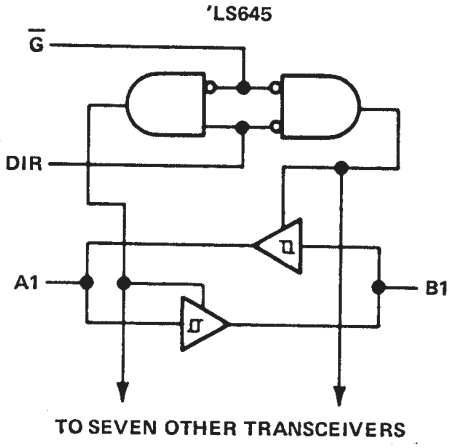

'LS642




'LS644




'LS645



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54LS640, SN54LS645 . . . . . −55°C to 125°C
SN74LS640, SN74LS645 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

### recommended operating conditions

| PARAMETER | | SN54LS640 SN54LS645 | | | SN74LS640 SN74LS645 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-lvel input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.5 | | | 0.6 | V |
| $I_{OH}$ | High-level output current | | | −12 | | | −15 | mA |
| $I_{OL}$ | Low-level output current | | | 12 | | | 24 | mA |
| | | | | | | | 48† | |
| $T_A$ | Operating free-air temperature | −55 | | 125 | 0 | | 70 | °C |

†The 48-mA limit applies for the SN74LS640-1 and SN74LS645-1 only.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS‡ | | | SN54LS640 SN54LS645 | | | SN74LS640 SN74LS645 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP§ | MAX | MIN | TYP§ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = MIN, $I_I$ = −18 mA | | | | | −1.5 | | | −1.5 | V |
| Hysteresis ($V_{T+} - V_{T-}$) | | $V_{CC}$ = MIN, | | A or B input | 0.1 | 0.4 | | 0.2 | 0.4 | | V |
| $V_{OH}$ | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = MAX | | $I_{OH}$ = −3 mA | 2.4 | 3.4 | | 2.4 | 3.4 | | |
| | | | | $I_{OH}$ = MAX | 2 | | | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = MAX | | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| | | | | $I_{OL}$ = 48 mA# | | | | | 0.4 | 0.5 | |
| $I_{OZH}$ | | $V_{CC}$ = MAX, $\overline{G}$ at 2 V, | | $V_O$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{OZL}$ | | $V_{CC}$ = MAX, $\overline{G}$ at 2 V, | | $V_O$ = 0.4 V | | | −0.4 | | | −0.4 | mA |
| $I_I$ | A or B | $V_{CC}$ = MAX | | $V_I$ = 5.5 V | | | 0.1 | | | 0.1 | mA |
| | DIR or $\overline{G}$ | | | $V_I$ = 7 V | | | 0.1 | | | 0.1 | |
| $I_{IH}$ | | $V_{CC}$ = MAX, $V_{IH}$ = 2.7 V | | | | | 20 | | | 20 | μA |
| $I_{IL}$ | | $V_{CC}$ = MAX, $V_{IL}$ = 0.4 V | | | | | −0.4 | | | −0.4 | mA |
| $I_{OS}$¶ | | $V_{CC}$ = MAX | | | −40 | | −225 | −40 | | −225 | mA |
| $I_{CC}$ | Outputs high | $V_{CC}$ = MAX, Outputs open | | | | 48 | 70 | | 48 | 70 | mA |
| | Outputs low | | | | | 62 | 90 | | 62 | 90 | |
| | Outputs at Hi-Z | | | | | 64 | 95 | | 64 | 95 | |

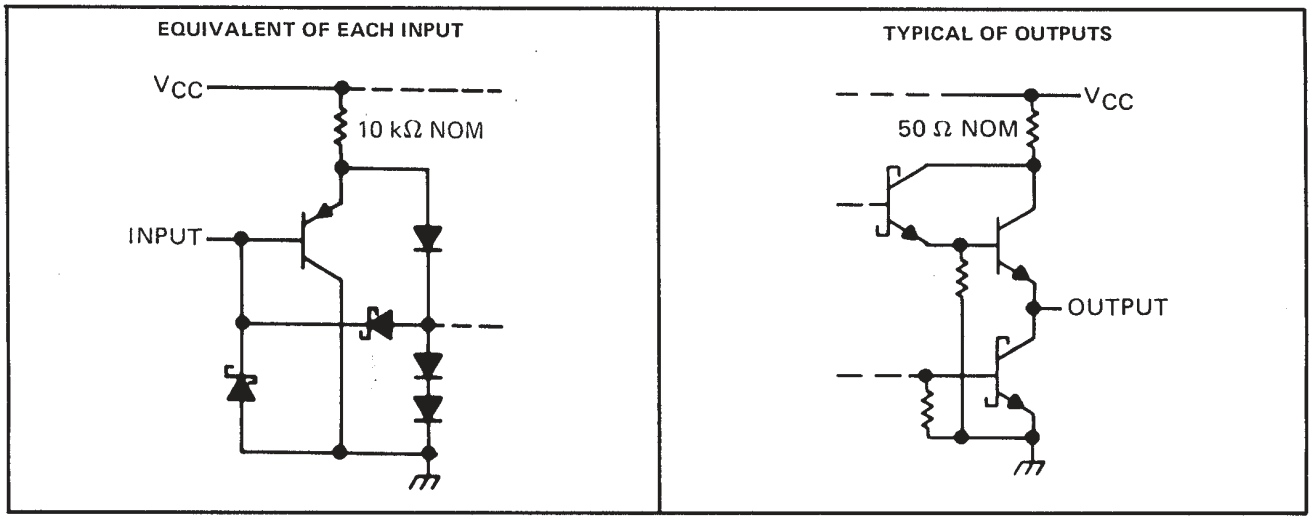
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
#The 48-mA condition applies for the SN74LS640-1 and SN74LS645-1 only.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | 'LS640, 'LS640-1 | | | 'LS645, 'LS645-1 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | A | B | $C_L$ = 45 pF, $R_L$ = 667 Ω, See Note 2 | | 6 | 10 | | 8 | 15 | ns |
| | | B | A | | | 6 | 10 | | 8 | 15 | |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | A | B | | | 8 | 15 | | 11 | 15 | ns |
| | | B | A | | | 8 | 15 | | 11 | 15 | |
| $t_{PZL}$ | Output enable time to low level | $\overline{G}$ | A | | | 31 | 40 | | 31 | 40 | ns |
| | | $\overline{G}$ | B | | | 31 | 40 | | 31 | 40 | |
| $t_{PZH}$ | Output enable time to high level | $\overline{G}$ | A | | | 23 | 40 | | 26 | 40 | ns |
| | | $\overline{G}$ | B | | | 23 | 40 | | 26 | 40 | |
| $t_{PLZ}$ | Output disable time from low level | $\overline{G}$ | A | $C_L$ = 5 pF, $R_L$ = 667 Ω, See Note 2 | | 15 | 25 | | 15 | 25 | ns |
| | | $\overline{G}$ | B | | | 15 | 25 | | 15 | 25 | |
| $t_{PHZ}$ | Output disable time from high level | $\overline{G}$ | A | | | 15 | 25 | | 15 | 25 | ns |
| | | $\overline{G}$ | B | | | 15 | 25 | | 15 | 25 | |

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

## schematics of inputs and outputs



## TYPICAL CHARACTERISTICS

SN54LS'
INVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

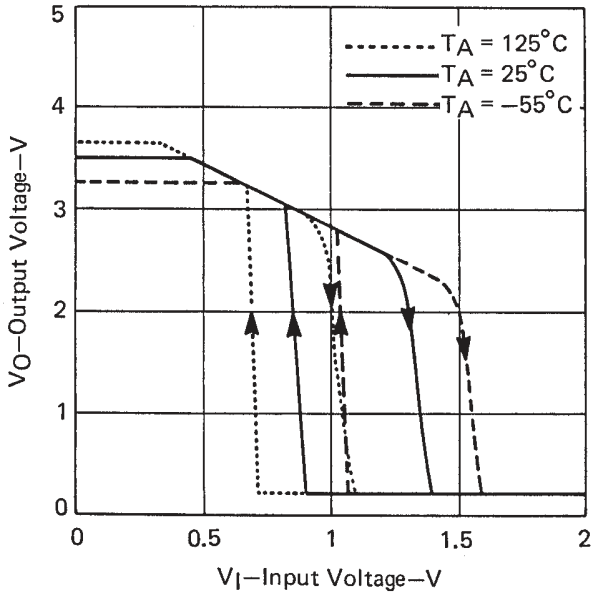



FIGURE 1

SN74LS'
INVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

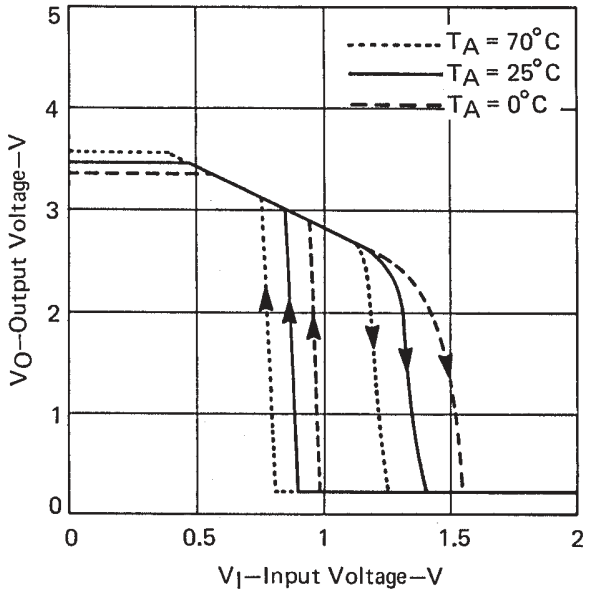



FIGURE 2

SN54LS'
NONINVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

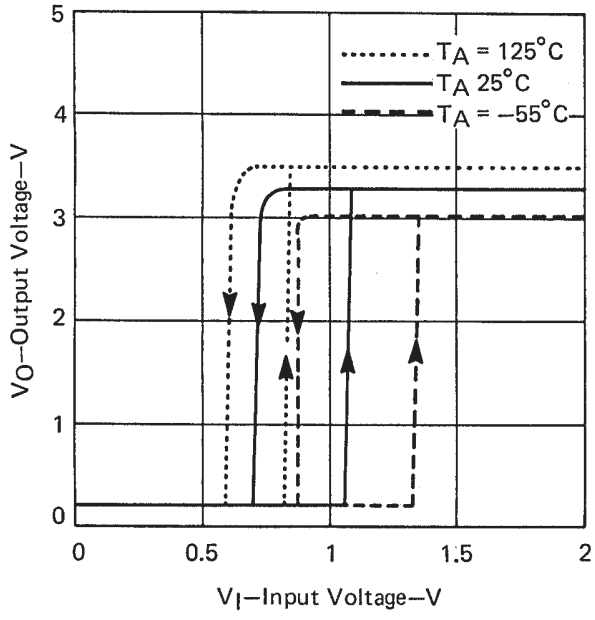



FIGURE 3

SN74LS'
NONINVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

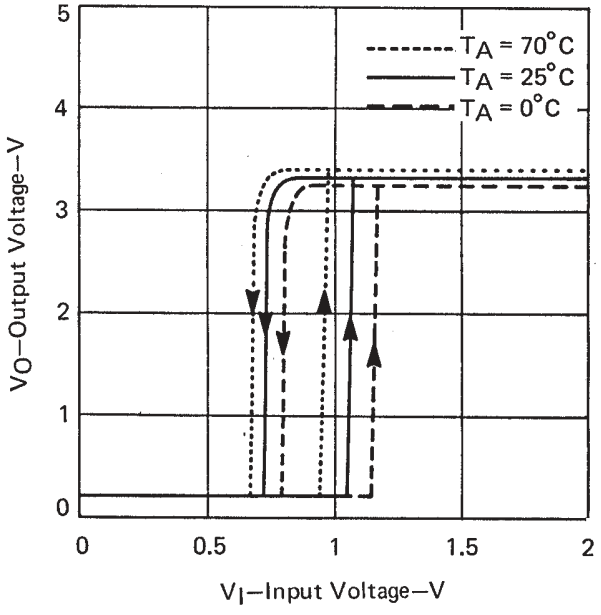



FIGURE 4

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54LS641, SN54LS642, SN54LS644 . . . . . – 55°C to 125°C
SN74LS641, SN74LS642, SN74LS644 . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

### recommended operating conditions

| PARAMETER | | SN54LS641 SN54LS642 SN54LS644 | | | SN74LS641 SN74LS642 SN74LS644 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.5 | | | 0.6 | V |
| $V_{OH}$ | High-level output voltage | | | 5.5 | | | 5.5 | V |
| $I_{OL}$ | Low-level output current | | | 12 | | | 24 | mA |
| | | | | | | | 48§ | |
| $T_A$ | Operating free-air temperature | – 55 | | 125 | 0 | | 70 | °C |

§The 48 mA limit applies for the SN74LS641-1, SN74LS642-1, and SN74LS644-1 only.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54LS641 SN54LS642 SN54LS644 | | | SN74LS641 SN74LS642 SN74LS644 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = MIN, | $I_I$ = – 18 mA | | | – 1.5 | | | – 1.5 | V |
| Hysteresis ($V_{T+} - V_{T-}$) | | $V_{CC}$ = MIN, | A or B input | 0.1 | 0.4 | | 0.2 | 0.4 | | V |
| $I_{OH}$ | | $V_{CC}$ = MIN, $V_{IL}$ = MAX, | $V_{IH}$ = 2 V, $V_{OH}$ = 5.5 V | | | 0.1 | | | 0.1 | mA |
| $V_{OL}$ | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = MAX | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| | | | $I_{OL}$ = 48 mA§ | | | | | 0.4 | 0.5 | |
| $I_I$ | A or B | $V_{CC}$ = MAX | $V_I$ = 5.5 V | | | 0.1 | | | 0.1 | mA |
| | DIR or $\overline{G}$ | | $V_I$ = 7 V | | | 0.1 | | | 0.1 | |
| $I_{IH}$ | | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| $I_{IL}$ | | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | – 0.4 | | | – 0.4 | mA |
| $I_{CC}$ | Outputs high | $V_{CC}$ = MAX, | Outputs open | | 48 | 70 | | 48 | 70 | mA |
| | Outputs low | | | | 62 | 90 | | 62 | 90 | |
| | Outputs at Hi-Z | | | | 64 | 95 | | 64 | 95 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§The 48 mA condition applies for the SN74LS641-1, SN74LS642-1, and SN74LS644-1 only.

## switching characteristics at $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | 'LS641, 'LS641–1 | | | 'LS642, 'LS642–1 | | | 'LS644, 'LS644–1 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | A | B | $C_L$ = 45 pF, $R_L$ = 667 Ω, See Note 2 | | 17 | 25 | | 19 | 25 | | 17 | 25 | ns |
| | | B | A | | | 17 | 25 | | 19 | 25 | | 19 | 25 | |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | A | B | | | 16 | 25 | | 14 | 25 | | 14 | 25 | ns |
| | | B | A | | | 16 | 25 | | 14 | 25 | | 16 | 25 | |
| $t_{PLH}$ | Output disable time from low level | $\overline{G}$, DIR | A | | | 23 | 40 | | 26 | 40 | | 26 | 40 | ns |
| | | $\overline{G}$, DIR | B | | | 25 | 40 | | 28 | 40 | | 25 | 40 | |
| $t_{PHL}$ | Output enable time from high level | $\overline{G}$, DIR | A | | | 34 | 50 | | 43 | 60 | | 43 | 60 | ns |
| | | $\overline{G}$, DIR | B | | | 37 | 50 | | 39 | 60 | | 37 | 50 | |

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

## schematics of inputs and outputs

EQUIVALENT OF EACH INPUT




TYPICAL OF OUTPUTS

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# SN74LS641, Octal bus transceivers with open collector outputs

DEVICE STATUS: ACTIVE

| PARAMETER NAME | SN74LS641 | SN74LS641-1 |
|---|---|---|
| Voltage Nodes (V) | 5 | 5 |
| Vcc range (V) | 4.75 to 5.25 | 4.75 to 5.25 |
| Input Level | TTL | TTL |
| Output Level | TTL | TTL |
| Output Drive (mA) | - /24 | - /48 |
| No. of Outputs | 8 | 8 |
| Logic | True | True |
| Static Current | 80 | 80 |
| tpd max (ns) | 25 | 25 |

## FEATURES

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- SN74LS64X-1 Versions Rated at $I_{OL}$ of 48 mA
- Bi-directional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

## DESCRIPTION

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These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G\) can be used to disable the device so the buses are effectively isolated.

The -1 versions of the SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are identical to the standard versions except that the recommended maximum $I_{OL}$ is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645.

The SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are characterized for operation from 0°C to 70°C.

## TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

## DATASHEET

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Full datasheet in Acrobat PDF: sn74ls641.pdf (336 KB) (Updated: 03/01/1988)

## APPLICATION NOTES

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View Application Notes for Digital Logic

- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Designing with the SN54/74LS123 (Rev. A) (SDLA006A - Updated: 03/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- LVT-to-LVTH Conversion (SCEA010 - Updated: 12/08/1998)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- Logic Solutions For IEEE Std 1284 (SCEA013 - Updated: 06/01/1999)

## RELATED DOCUMENTS

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View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

## PRICING/ AVAILABILITY/ PKG

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| DEVICE INFORMATION | | | | | | | TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002 | | | REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ORDERABLE DEVICE | STATUS | PACKAGE TYPE\| PINS | TEMP (°C) | PRODUCT CONTENT | BUDGETARY PRICING QTY \| $US | STD PACK QTY | IN STOCK | IN PROGRESS QTY\| DATE | LEAD TIME | DISTRIBUTOR COMPANY\| REGION | IN STOCK | PURCHASE |
| SN74LS641-1DW | ACTIVE | SOP (DW) \| 20 | 0 TO 70 | View Contents | 1KU \| 2.10 | 25 | N/A* | | 12 WKS | | | |
| SN74LS641-1DWR | ACTIVE | SOP (DW) \| 20 | 0 TO 70 | View Contents | 1KU \| 2.13 | 2000 | N/A* | | 12 WKS | | | |
| SN74LS641-1N | ACTIVE | PDIP (N) \| 20 | 0 TO 70 | View Contents | 1KU \| 2.10 | 20 | N/A* | | 12 WKS | Avnet \| AMERICA | > 1k | BUY NOW |
| SN74LS641-1N3 | OBSOLETE | PDIP (N) \| 20 | 0 TO 70 | View Contents | 1KU \| | | N/A* | | Not Available | | | |
| SN74LS641DW | ACTIVE | SOP (DW) \| 20 | 0 TO 70 | View Contents | 1KU \| 1.04 | 25 | N/A* | 250 \| 03 Oct | 4 WKS | | | |
| SN74LS641DWR | ACTIVE | SOP (DW) \| 20 | 0 TO 70 | View Contents | 1KU \| 1.06 | 2000 | N/A* | | 12 WKS | | | |
| SN74LS641N | ACTIVE | PDIP (N) \| 20 | 0 TO 70 | View Contents | 1KU \| 0.95 | 20 | N/A* | | 12 WKS | | | |
| SN74LS641N3 | OBSOLETE | PDIP (N) \| 20 | 0 TO 70 | View Contents | 1KU \| | | N/A* | | Not Available | | | |
| SN74LS641NSR | ACTIVE | SOP (NS) \| 20 | | View Contents | 1KU \| 0.95 | 2000 | N/A* | | 12 WKS | | | |

Table Data Updated on: 9/26/2002

# SN74LS640-1, OCTAL BUS TRANSCEIVER/ IOL=48mA 3-STATE

DEVICE STATUS: ACTIVE

| PARAMETER NAME | SN74LS640-1 |
|---|---|
| Voltage Nodes (V) | 5 |
| Vcc range (V) | 4.75 to 5.25 |
| Input Level | TTL |
| Output Level | TTL |
| Output Drive (mA) | -15/48 |
| No. of Outputs | 8 |
| Logic | Inv |
| Static Current | 80 |
| tpd max (ns) | 15 |

## FEATURES

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- SN74LS64X-1 Versions Rated at $I_{OL}$ of 48 mA
- Bi-directional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

## DESCRIPTION

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These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G\) can be used to disable the device so the buses are effectively isolated.

The -1 versions of the SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are identical to the standard versions except that the recommended maximum $I_{OL}$ is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645.

The SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are characterized for operation from 0°C to 70°C.

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Full datasheet in Acrobat PDF: sn74ls640-1.pdf (336 KB) (Updated: 03/01/1988)

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- Designing with the SN54/74LS123 (Rev. A) (SDLA006A - Updated: 03/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- LVT-to-LVTH Conversion (SCEA010 - Updated: 12/08/1998)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- Logic Solutions For IEEE Std 1284 (SCEA013 - Updated: 06/01/1999)

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View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

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| SN74LS640-1DW | ACTIVE | SOP (DW) \| 20 | 0 TO 70 | View Contents | 1KU \| 2.10 | 25 | N/A* | 125 \| 03 Oct | 4 WKS | | | |
| SN74LS640-1DWR | OBSOLETE | SOP (DW) \| 20 | 0 TO 70 | View Contents | 1KU \| | | N/A* | | Not Available | | | |
| SN74LS640-1N | ACTIVE | PDIP (N) \| 20 | 0 TO 70 | View Contents | 1KU \| 2.10 | 20 | N/A* | 2780 \| 03 Oct | 4 WKS | Avnet \| AMERICA | 711 | BUY NOW |
| SN74LS640-1NSR | ACTIVE | SOP (NS) \| 20 | | View Contents | 1KU \| 2.10 | 2000 | N/A* | | 12 WKS | | | |

Table Data Updated on: 9/26/2002

# SN74LS642, Octal bus transceivers with open collector outputs

DEVICE STATUS: ACTIVE

| PARAMETER NAME | SN74LS642 | SN74LS642-1 |
|---|---|---|
| Voltage Nodes (V) | 5 | 5 |
| Vcc range (V) | 4.75 to 5.25 | 4.75 to 5.25 |
| Input Level | TTL | TTL |
| Output Level | TTL | TTL |
| Output Drive (mA) | - /24 | - /48 |
| No. of Outputs | 8 | 8 |
| Logic | Inv | Inv |
| Static Current | 80 | 80 |
| tpd max (ns) | 25 | 25 |

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- SN74LS64X-1 Versions Rated at $I_{OL}$ of 48 mA
- Bi-directional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

## DESCRIPTION

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These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G\) can be used to disable the device so the buses are effectively isolated.

The -1 versions of the SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are identical to the standard versions except that the recommended maximum $I_{OL}$ is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645.

The SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are characterized for operation from 0°C to 70°C.

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Full datasheet in Acrobat PDF: sn74ls642.pdf (336 KB) (Updated: 03/01/1988)

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- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Designing with the SN54/74LS123 (Rev. A) (SDLA006A - Updated: 03/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- LVT-to-LVTH Conversion (SCEA010 - Updated: 12/08/1998)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- Logic Solutions For IEEE Std 1284 (SCEA013 - Updated: 06/01/1999)

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- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

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| SN74LS642-1DW | ACTIVE | SOP (DW) \| 20 | 0 TO 70 | View Contents | 1KU \| 3.15 | 25 | N/A* | | 12 WKS | | | |
| SN74LS642-1N | ACTIVE | PDIP (N) \| 20 | 0 TO 70 | View Contents | 1KU \| 3.15 | 20 | N/A* | | 12 WKS | | | |
| SN74LS642DW | ACTIVE | SOP (DW) \| 20 | 0 TO 70 | View Contents | 1KU \| 1.86 | 25 | N/A* | | 12 WKS | Avnet \| AMERICA | 357 | BUY NOW |
| SN74LS642N | ACTIVE | PDIP (N) \| 20 | 0 TO 70 | View Contents | 1KU \| 1.86 | 20 | N/A* | | 12 WKS | | | |
| SN74LS642NSR | ACTIVE | SOP (NS) \| 20 | | View Contents | 1KU \| 1.86 | 2000 | N/A* | | 12 WKS | | | |

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PRODUCT SUPPORT: TRAINING

# SN74LS645, Octal bus transceivers

DEVICE STATUS: ACTIVE

| PARAMETER NAME | SN54LS645 | SN74LS645 |
|---|---|---|
| Voltage Nodes (V) | 5 | 5 |
| Vcc range (V) | 4.5 to 5.5 | 4.75 to 5.25 |
| Input Level | TTL | TTL |
| Output Level | TTL | TTL |
| Output Drive (mA) | | -15/24 |
| No. of Outputs | 8 | 8 |
| Logic | True | True |
| Static Current | | 80 |
| tpd max (ns) | | 15 |

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- SN74LS64X-1 Versions Rated at $I_{OL}$ of 48 mA
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- Choice of 3-State or Open-Collector Outputs

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These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G\) can be used to disable the device so the buses are effectively isolated.

The -1 versions of the SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are identical to the standard versions except that the recommended maximum $I_{OL}$ is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645.

The SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are characterized for operation from 0°C to 70°C.

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Full datasheet in Acrobat PDF: sn74ls645.pdf (336 KB) (Updated: 03/01/1988)

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- Designing with the SN54/74LS123 (Rev. A) (SDLA006A - Updated: 03/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- LVT-to-LVTH Conversion (SCEA010 - Updated: 12/08/1998)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- Logic Solutions For IEEE Std 1284 (SCEA013 - Updated: 06/01/1999)

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View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

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| ORDERABLE DEVICE | STATUS | PACKAGE TYPE\| PINS | TEMP (°C) | PRODUCT CONTENT | BUDGETARY PRICING QTY \| $US | STD PACK QTY | IN STOCK | IN PROGRESS QTY\| DATE | LEAD TIME | DISTRIBUTOR COMPANY\| REGION | IN STOCK | PURCHASE |
| SN74LS645DW | ACTIVE | SOP (DW) \| 20 | 0 TO 70 | View Contents | 1KU \| 0.73 | 25 | N/A* | 250 \| 24 Sep | 4 WKS | Avnet \| AMERICA | > 1k | BUY NOW |
| | | | | | | | | 4170 \| 07 Oct | | | | |
| | | | | | | | | > 10k \| 14 Oct | | | | |
| | | | | | | | | 871 \| 21 Oct | | | | |
| SN74LS645DWR | OBSOLETE | SOP (DW) \| 20 | 0 TO 70 | View Contents | 1KU \| | | N/A* | | Not Available | | | |
| SN74LS645N | ACTIVE | PDIP (N) \| 20 | 0 TO 70 | View Contents | 1KU \| 0.64 | 20 | N/A* | 4406 \| 07 Oct | 4 WKS | | | |
| | | | | | | | | > 10k \| 14 Oct | | | | |
| | | | | | | | | > 10k \| 21 Oct | | | | |
| | | | | | | | | 720 \| 02 Dec | | | | |
| | | | | | | | | 200 \| 04 Dec | | | | |
| SN74LS645N3 | OBSOLETE | PDIP (N) \| 20 | 0 TO 70 | View Contents | 1KU \| | | N/A* | | Not Available | | | |

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS645NSR | ACTIVE | SOP (NS) \| 20 | | View Contents | 1KU \| 0.64 | 2000 | N/A* | > 10k \| 14 Oct | 4 WKS | | | |

Table Data Updated on: 9/26/2002

# SN74LS645-1, OCTAL BUS TRANSCEIVER/ IOL=48mA 3-STATE

DEVICE STATUS: ACTIVE

| PARAMETER NAME | SN74LS645-1 |
|---|---|
| Voltage Nodes (V) | 5 |
| Vcc range (V) | 4.75 to 5.25 |
| Input Level | TTL |
| Output Level | TTL |
| Output Drive (mA) | -15/48 |
| No. of Outputs | 8 |
| Logic | True |
| Static Current | 80 |
| tpd max (ns) | 15 |

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- Choice of 3-State or Open-Collector Outputs

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These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G\) can be used to disable the device so the buses are effectively isolated.

The -1 versions of the SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are identical to the standard versions except that the recommended maximum $I_{OL}$ is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645.

The SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are characterized for operation from 0°C to 70°C.

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- Designing with the SN54/74LS123 (Rev. A) (SDLA006A - Updated: 03/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- LVT-to-LVTH Conversion (SCEA010 - Updated: 12/08/1998)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- Logic Solutions For IEEE Std 1284 (SCEA013 - Updated: 06/01/1999)

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- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

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| ORDERABLE DEVICE | STATUS | PACKAGE TYPE\| PINS | TEMP (°C) | PRODUCT CONTENT | BUDGETARY PRICING QTY \| $US | STD PACK QTY | IN STOCK | IN PROGRESS QTY\| DATE | LEAD TIME | DISTRIBUTOR COMPANY\| REGION | IN STOCK | PURCHASE |
| SN74LS645-1DW | ACTIVE | SOP (DW) \| 20 | 0 TO 70 | View Contents | 1KU \| 2.10 | 25 | N/A* | 800 \| 03 Oct | 4 WKS | | | |
| | | | | | | | | 4420 \| 07 Oct | | | | |
| | | | | | | | | > 10k \| 14 Oct | | | | |
| | | | | | | | | 871 \| 21 Oct | | | | |
| SN74LS645-1DWR | ACTIVE | SOP (DW) \| 20 | 0 TO 70 | View Contents | 1KU \| 2.13 | 2000 | N/A* | 4405 \| 07 Oct | 4 WKS | | | |
| | | | | | | | | > 10k \| 14 Oct | | | | |
| SN74LS645-1N | ACTIVE | PDIP (N) \| 20 | 0 TO 70 | View Contents | 1KU \| 2.10 | 20 | N/A* | 622 \| 24 Sep | 4 WKS | Avnet \| AMERICA | > 1k | BUY NOW |
| | | | | | | | | 3606 \| 07 Oct | | | | |
| | | | | | | | | > 10k \| 14 Oct | | | | |
| | | | | | | | | 178 \| 15 Oct | | | | |
| | | | | | | | | > 10k \| 21 Oct | | | | |
| SN74LS645-1N3 | OBSOLETE | PDIP (N) \| 20 | 0 TO 70 | View Contents | 1KU \| | | N/A* | | Not Available | | | |

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS645-1NSR | ACTIVE | SOP (NS) \| 20 | | View Contents | 1KU \| 2.10 | 2000 | N/A* | 1416 \| 23 Sep | 4 WKS | | | |
| | | | | | | | | > 10k \| 14 Oct | | | | |

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PRODUCT SUPPORT: TRAINING

# SN74LS640, Octal bus transceivers

DEVICE STATUS: ACTIVE

| PARAMETER NAME | SN54LS640 | SN74LS640 |
|---|---|---|
| Voltage Nodes (V) | 5 | 5 |
| Vcc range (V) | 4.5 to 5.5 | 4.75 to 5.25 |
| Input Level | TTL | TTL |
| Output Level | TTL | TTL |
| Output Drive (mA) | | -15/24 |
| No. of Outputs | 8 | 8 |
| Logic | Inv | Inv |
| Static Current | | 80 |
| tpd max (ns) | | 15 |

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- SN74LS64X-1 Versions Rated at $I_{OL}$ of 48 mA
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- Choice of 3-State or Open-Collector Outputs

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These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G\) can be used to disable the device so the buses are effectively isolated.

The -1 versions of the SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are identical to the standard versions except that the recommended maximum $I_{OL}$ is increased to 48 milliamperes. There are no -1 versions of the SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645.

The SN54LS640 thru SN54LS642, SN54LS644, and SN54LS645 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS640 thru SN74LS642, SN74LS644, and SN74LS645 are characterized for operation from 0°C to 70°C.

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- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
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- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

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| ORDERABLE DEVICE | STATUS | PACKAGE TYPE\| PINS | TEMP (°C) | PRODUCT CONTENT | BUDGETARY PRICING QTY \| $US | STD PACK QTY | IN STOCK | IN PROGRESS QTY\| DATE | LEAD TIME | DISTRIBUTOR COMPANY\| REGION | IN STOCK | PURCHASE |
| SN74LS640DW | ACTIVE | SOP (DW) \| 20 | 0 TO 70 | View Contents | 1KU \| 0.99 | 25 | N/A* | 1813 \| 24 Sep | 4 WKS | Avnet \| AMERICA | 130 | BUY NOW |
| | | | | | | | | 1209 \| 03 Oct | | | | |
| SN74LS640DWR | ACTIVE | SOP (DW) \| 20 | 0 TO 70 | View Contents | 1KU \| 1.02 | 2000 | N/A* | | 12 WKS | | | |
| SN74LS640N | ACTIVE | PDIP (N) \| 20 | 0 TO 70 | View Contents | 1KU \| 0.91 | 20 | N/A* | 220 \| 03 Oct | 12 WKS | Avnet \| AMERICA | > 1k | BUY NOW |
| SN74LS640N3 | OBSOLETE | PDIP (N) \| 20 | 0 TO 70 | View Contents | 1KU \| | | N/A* | | Not Available | | | |
| SN74LS640NSR | ACTIVE | SOP (NS) \| 20 | | View Contents | 1KU \| 0.91 | 2000 | N/A* | | 12 WKS | | | |

Table Data Updated on: 9/26/2002