PI6LC4831A

Crystal to Differential HCSL/LVCMOS Frequency Synthesizer

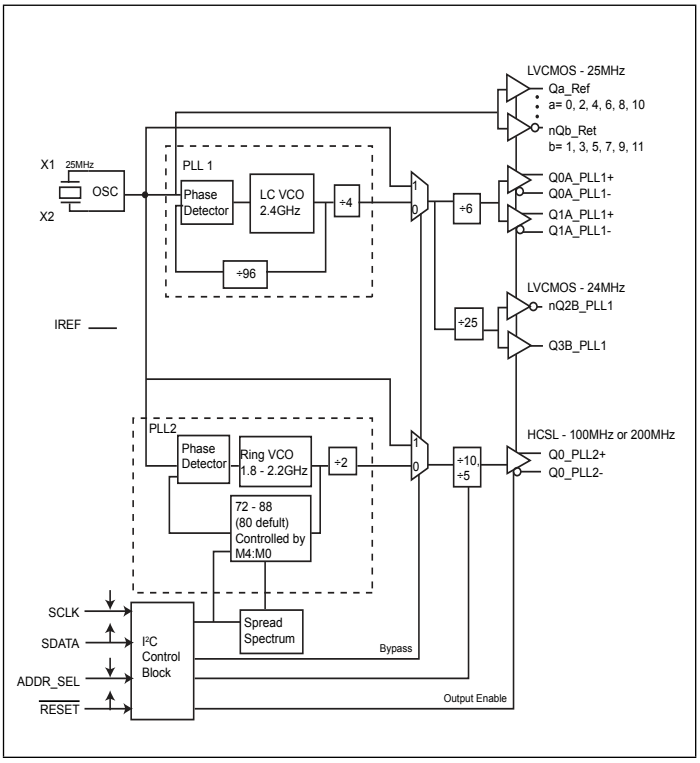
Features

- 3.3V ± 5% Supply Voltage
- Industrial temperature -40°C to 85°C
- Uses 25MHz xtal
- Two low jitter PCIe 100MHz outputs
- One 100/200MHz selectable HCSL output with spread spectrum support
- 12 LVCMOS 25MHz reference clock outputs
- Two LVCMOS 24MHz outputs
- I²C Interface
- Packaging (Pb-free & Green available):
  - 8mm × 8mm 56-pinTQFN

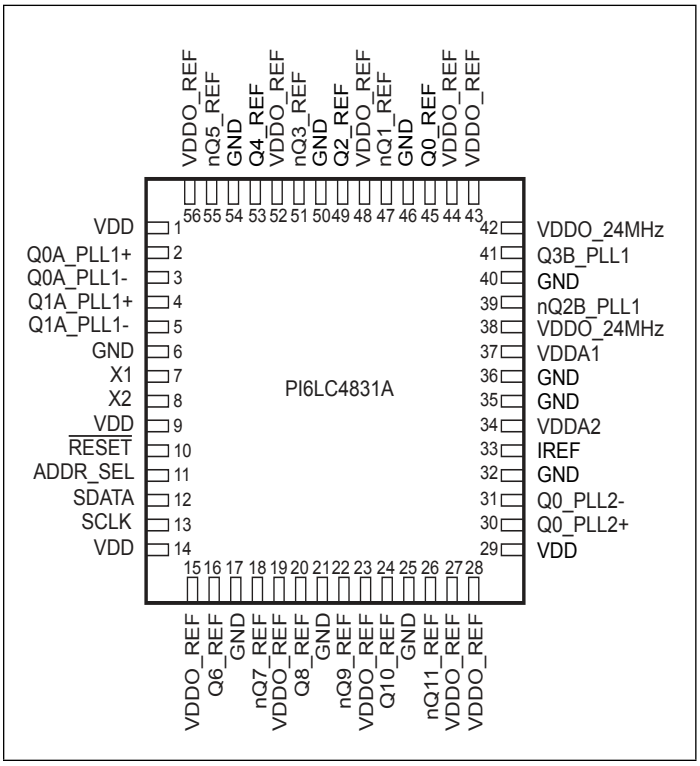
Description

The PI6LC4831A clock generator supports networking systems requiring 25MHz for ethernet and 100MHz for PCIe applications. This novel part includes both a low phase noise VCO and a traditional VCO which supports spread spectrum applications. Twelve copies of the 25MHz reference clock are provided, evenly divided between true and complimentary outputs to minimize EMI and di/dt. The low phase noise LC VCO drives 2 HCSL outputs and the 24MHz LVCMOS outputs. The Spread spectrum ring oscillator drives a 100MHz or 200MHz selectable HCSL output. I²C control is included for on-board frequency and spread spectrum functionality changes.

Block Diagram



Pin Configuration (56-Pin TQFN)



Pin Description

Pin Number	Pin Name	Type	Description
1	V_{DD}	Power	3.3V Supply Pin
2	Q0A_PLL1+	Output	LC Oscillator HCSL Output 100MHz nominal
3	Q0A_PLL1-	Output	LC Oscillator HCSL Output 100MHz nominal
4	Q1A_PLL1+	Output	LC Oscillator HCSL Output 100MHz nominal
5	Q1A_PLL1-	Output	LC Oscillator HCSL Output 100MHz nominal
6	GND	Power	Ground
7	X1	Input	Crystal input
8	X2	Output	Crystal output
9	V_{DD}	Power	3.3V Supply Pin
10	$\overline{\text{RESET}}$	Input	Resets PLL1 and I^2C registers to default settings. Q0:nQ11 output set to high Z mode for power sequencing. Internal 51K pull-up.
11	ADDR_SEL	Input	Selects between two different I^2C addresses. Internal 51K pull-down.
12	SDATA	I/O	I^2Ccompatible data line. Internal 51K pull-up.
13	SCLK	Input	I^2C compatible input clock. Internal 51K pull-down.
14	V_{DD}	Power	3.3V Supply Pin
15	V_{DDO_REF}	Power	V_{DD} for Q0:nQ11 output drivers
16	Q6_REF	Output	LVCMOS level reference oscillator output
17	GND	Power	GND
18	nQ7_REF	Output	LVCMOS level reference oscillator output
19	V_{DDO_REF}	Power	V_{DD} for Q0:nQ11 output drivers
20	Q8_REF	Output	LVCMOS level reference oscillator output
21	GND	Power	GND
22	nQ9_REF	Output	LVCMOS level reference oscillator output
23	V_{DDO_REF}	Power	V_{DD} for Q0:nQ11 output drivers
24	Q10_REF	Output	LVCMOS level reference oscillator output
25	GND	Power	GND
26	nQ11_REF	Output	LVCMOS level reference oscillator output
27	V_{DDO_REF}	Power	V_{DD} for Q0:nQ11 output drivers
28	V_{DDO_REF}	Power	V_{DD} for Q0:nQ11 output drivers
29	V_{DD}	Power	3.3V Supply Pin
30	Q0_PLL2+	Output	HCSL output from PLL2, nominal 100 or 200MHz
31	Q0_PLL2-	Output	HCSL output from PLL2, nominal 100 or 200MHz
32	GND	Power	GND
33	IREF	Output	External resistor connection for internal current reference. Connect 475 Ohm resistor to ground.
34	V_{DDA2}	Power	Analog Power for PLL2
35	GND	Power	GND

(Continued)

Pin Description (continued)

Pin Number	Pin Name	Type	Description
36	GND	Power	GND
37	V_{DDA1}	Power	Analog Power for PLL1
38	V_{DDO}_24MHz	Power	V_{DD} for 24MHz outputs. nQ2B_PLL1, Q3B_PLL1
39	nQ2B_PLL1	Output	LVCMOS output for PLL1, nominal 24MHz Output
40	GND	Power	GND
41	Q3B_PLL1	Output	LVCMOS output for PLL1, nominal 24MHz Output
42	V_{DDO}_24MHz	Power	V_{DD} for 24MHz outputs. nQ2B_PLL1, Q3B_PLL1
43	V_{DDO}_REF	Power	V_{DD} for Q0:nQ11 output drivers
44	V_{DDO}_REF	Power	V_{DD} for Q0:nQ11 output drivers
45	Q0_REF	Output	LVCMOS level reference oscillator output
46	GND	Power	GND
47	nQ1_REF	Output	LVCMOS level reference oscillator output
48	V_{DDO}_REF	Power	V_{DD} for Q0:nQ11 output drivers
49	Q2_REF	Output	LVCMOS level reference oscillator output
50	GND	Power	GND
51	nQ3_REF	Output	LVCMOS level reference oscillator output
52	V_{DDO}_REF	Power	V_{DD} for Q0:nQ11 output drivers
53	Q4_REF	Output	LVCMOS level reference oscillator output
54	GND	Power	GND
55	nQ5_REF	Output	LVCMOS level reference oscillator output
56	V_{DDO}_REF	Power	V_{DD} for Q0:nQ11 output drivers

Pin Characteristics

Symbol	Parameter	Typical	Units
C_{IN}	Input Capacitance	2	pF
R_{PULLUP}	Input Pullup Resistor	51	kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor	51	
R_{OUT}	Output Impedance (single-ended Output)	21	Ω
C_{INx}	Input Capacitance for pins X1, X2 (1)	11, 15	pF

Note:

1. Presents an effective C_L of 6.3pF to crystal.

Serial Data Interface I²C

The PI6LC4831A is a slave only I2C device that uses standard I2C protocol. Within any Byte, transmit direction is always from MSB to LSB.

Read/Write Example:

A read or write to the PI6LC4831A always consists of a Start bit, Address Byte, four Data Bytes, and a stop bit. All values are latched upon the IC receiving the Stop bit.

How to Write (M: abbreviation for Master or Controller; S: abbreviation for slave/clock)

1 bit	**8 bits**	**1 bit**	**8 bits**	**1 bit**		**8 bits**	**1 bit**	**1 bit**
(M) Start bit	(M) Address	(S)Ack	(M) Data Byte 0	(S)Ack	…	(M) Data Byte3	(S)Ack	(M) Stop bit

How to Read (M: abbreviation for Master or Controller; S: abbreviation for slave/clock)

1 bit	**8 bits**	**1 bit**	**8 bits**	**1 bit**	**…**	**8 bits**	**1 bit**	**1 bit**
(M) Start bit	(M) Send read address	(S) Ack	(S) Send Data Byte 0	(M) Ack	…	(S) Data Byte3	(M) Not Acknowledge	(M) Stop bit

Note that after the last Data Byte is sent by the slave, there is no Ack pulse. SData remains high.

- ➔ START: A Start bit is defined as a HIGH to LOW transition on SDATA while SCLK is high.
- ➔ DATA: Data may change only when SCLK is LOW and must be stable when SCLK is HIGH. See Data Byte descriptions for detail on the functionality of the bit settings.
- ➔ ACKNOWLEDGE: SDATA is driven LOW by the PI6LC4831A before the SCLK rising edge and held LOW until the SCLK falling edge.
- ➔ STOP: A Stop bit is defined as a LOW to HIGH transition on SDATA while SCLK is High.

I²C Address

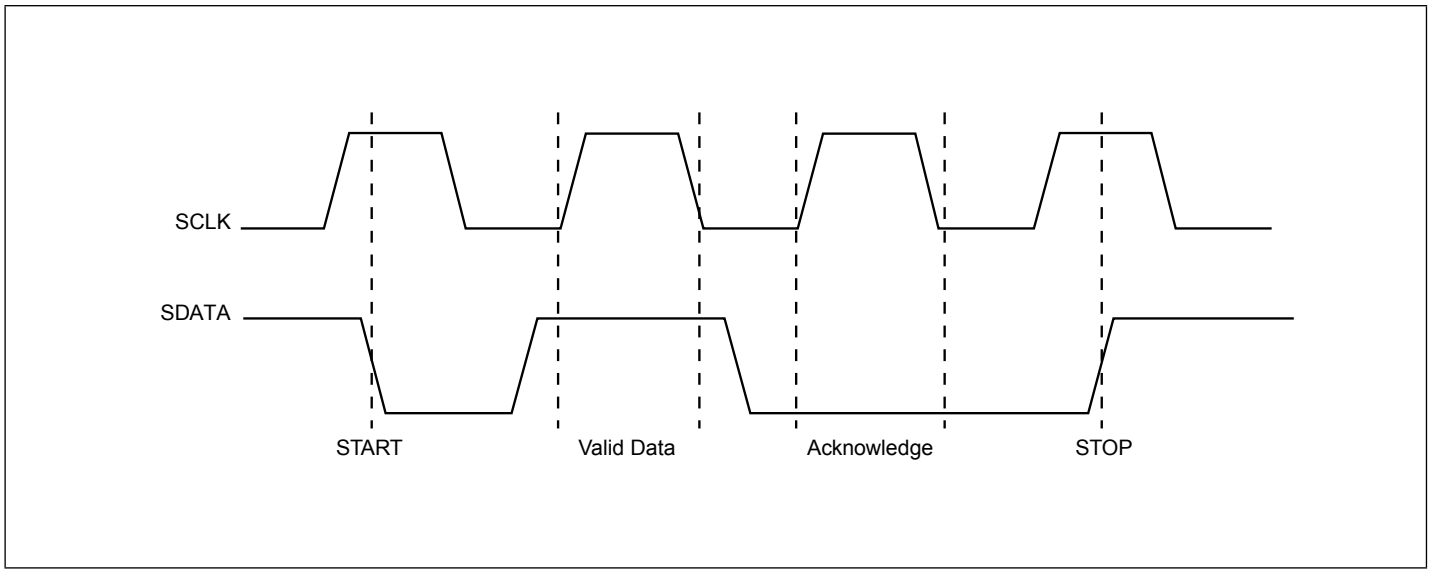
PI6LC4831A I²C Address: The PI6LC4831A can be set to accept one of two different addresses, see table below. Selecting between the two addresses is accomplished by setting the external ADDR_SEL (pin 11) to the desired logic level.

ADDR_SEL = 0 (default)

Write = 98 (h) Read = 99 (h)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	0	1	1	0	0	R/W

ADDR_SEL = 1

Write = 9c (h) Read = 9d (h)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	0	1	1	1	0	R/W



I2C Interface Waveforms

Byte 0: Control Register

Bit	Description	Type	Power Up Condition	Notes
7	OE for Q0A_PLL1	RW	1	0: Hi-Z;1:enabled
6	OE for Q1A_PLL1	RW	1	0: Hi-Z;1:enabled
5	OE for Q3B_PLL1	RW	1	0: Hi-Z;1:enabled
4	OE for nQ2B_PLL1	RW	1	0: Hi-Z;1:enabled
3	OE for Q0_PLL2	RW	0	0: Hi-Z;1:enabled
2	OE for nQ11_REF	RW	1	0: Hi-Z;1:enabled
1	OE for Q10_REF	RW	1	0: Hi-Z;1:enabled
0	OE for nQ9_REF	RW	1	0: Hi-Z;1:enabled

Byte 1: Control Register

Bit	Description	Type	Power Up Condition	Notes
7	OE for Q8_REF	RW	1	0: Hi-Z;1:enabled
6	OE for nQ7_REF	RW	1	0: Hi-Z;1:enabled
5	OE for Q6_REF	RW	1	0: Hi-Z;1:enabled
4	OE for nQ5_REF	RW	1	0: Hi-Z;1:enabled
3	OE for Q4_REF	RW	1	0: Hi-Z;1:enabled
2	OE for nQ3_REF	RW	1	0: Hi-Z;1:enabled
1	OE for Q2_REF	RW	1	0: Hi-Z;1:enabled
0	OE for nQ1_REF	RW	1	0: Hi-Z;1:enabled

Byte 2: Control Register

Bit	Description	Type	Power Up Condition	Notes
7	OE for Q0_REF	RW	1	0: Hi-Z;1:enabled
6	PLL2 feedback divider M4	RW	0	see feedback divider frequency table
5	PLL2 feedback divider M3	RW	1	see feedback divider frequency table
4	PLL2 feedback divider M2	RW	0	see feedback divider frequency table
3	PLL2 feedback divider M1	RW	0	see feedback divider frequency table
2	PLL2 feedback divider M0	RW	0	see feedback divider frequency table
1	Spread Spectrum Enable/Disable	RW	0	0: SS Off;1:-0.5% down-spread
0	PLL 1 and 2 Bypass	RW	0	0: PLL output;1:Output from crystal oscillator circuit

Byte 3: Control Register

Bit	Description	Type	Power Up Condition	Notes
7	100/200MHz selector for Q0_PLL2	RW	0	0: 200MHz;1:100MHz
6	IC silicon revision	RW	1	
5	Rev ID	RW	0	
4	Rev ID	RW	1	
3	Vendor ID	RW	0	
2	Vendor ID	RW	0	
1	Vendor ID	RW	1	
0	Vendor ID	RW	1	

PLL2 Feedback Divider Frequency Table Q0_PLL2

VCO Frequency (MHz)	Q0_PLL2 Frequency (MHz)	Feedback Divide	M4	M3	M2	M1	M0
1800	90	72	0	0	0	0	0
1825	91.25	73	0	0	0	0	1
1850	92.5	74	0	0	0	1	0
1875	93.75	75	0	0	0	1	1
1900	95	76	0	0	1	0	0
1925	96.25	77	0	0	1	0	1
1950	97.5	78	0	0	1	1	0
1975	98.75	79	0	0	1	1	1
2000	100	80 (default)	0	1	0	0	0
2025	101.25	81	0	1	0	0	1
2050	102.5	82	0	1	0	1	0
2075	103.75	83	0	1	0	1	1
2100	105	84	0	1	1	0	0
2125	106.25	85	0	1	1	0	1
2150	107.5	86	0	1	1	1	0
2175	108.75	87	0	1	1	1	1
2200	110	88	1	0	0	0	0
Not used	Not used	Not used	1	0	0	0	1
			• • •				
			1	1	1	1	1

Maximum Ratings (1)

Supply Voltage (V_{DD}) ..... +4.6V
Inputs, V_I ……..-0.5V to V_{DD}+0.5V
Outputs, V_O (LVCMOS & HCSL).....-0.5V to V_{DDO} +0.5V
Package Thermal Impedance (θ_{JA}) ..... 31.4°C/W (0 Mps)
Storage Temperature (T_{STG})..... -65°C to +150°C
ESD Protection (HBM) ……2000V

Notes:
Stresses greater then those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Power Supply Characteristics (V_{DD} = V_{DDO}_REF = V_{DDO}_24MHz = 3.3V±5%, TA = -40°C to 85°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA1}, V_{DDA2}	Analog Supply Voltage		V_{DD} – 0.31	3.3	V_{DD}	
V_{DDO_REF}	Output Supply Voltage		3.135	3.3	3.465	
I_{DD}	Power Supply Current	No Load			170	mA
I_{DDA1}	PLL1 Analog Supply Current				42	
I_{DDA2}	PLL2 Analog Supply Current				22	
I_{DDO_REF}	Output Supply Current, 25MHz	No Load. Q0_REF, nQ11_REF at 25MHz			16	
I_{DDO_24MHz}	Output Supply Current, 24MHz	No Load. nQ2B_PLL1, Q3B_PLL1				

LVCMOS/LVTTL DC Characteristics (V_{DD} = V_{DDO}_REF = V_{DDO}_24MHz = 3.3V±5%, TA = -40°C to 85°C)

Symbol	Parameter		Test Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			– 0.3		0.8	
I_{IH}	Input High Current	ADDR_SEL, SCLK	V_{DD} = V_{IN} = 3.465V			150	µA
		SDATA, $\overline{\text{RESET}}$	V_{DD} = V_{IN} = 3.465V			10	
I_{IL}	Input Low Current	ADDR_SEL, SCLK	V_{DD} = 3.465V, V_{IN} = 0V	– 10			
		SDATA, $\overline{\text{RESET}}$	V_{DD} = 3.465V, V_{IN} = 0V	– 150			
V_{OH}	Output High Voltage		I_{OH} = –12mA	2.6			V
V_{OL}	Output Low Voltage		I_{OL} = 12mA			0.5	

AC Characteristics (V_{DD}=V_{DDO}_REF=V_{DDO}_24MHz=3.3V±5%, T_A=–40°C to 80°C)

Symbol	Parameter		Test Conditions	Min	Typ	Max	Units
f_{OUT}	Output Frequency	Q0_Ref: nQ11_Ref			25		MHz
		Q0_PLL2±			100		
		Q3B_PLL1, nQ2B_PLL1			24		
		Q(0,1)A_PLL1±			100		
$t_{jit(per)}$	Period Jitter, Peak-to-Peak	Q0_PLL2±	BER = 10E-12, 100MHz			70	ps
		Q3B_PLL1, nQ2B_PLL1	BER = 10E-12, 24MHz			95	
		Q(0,1)A_PLL1±	BER = 10E-12, 100MHz			70	
$t_{jit(cc)}$	Cycle-to-Cycle Jitter; (1, 2)	Q0_Ref: nQ11_Ref	25MHz			30	
		Q0_PLL2±	100MHz			80	
		Q3B_PLL1, nQ2B_PLL1	24MHz			90	
		Q(0,1)A_PLL1±	100MHz			70	
t_{RESET}	Minimum Reset Time for $\overline{RESET}$			1.6			ns
t_{OEPD}	Maximum Propagation Delay from OE Register to Clock					100	
t_L	PLL Lock Time					50	ms
F_{xtal}	Crystal Input Range (1)				25		MHz
F_M	SSC Modulation Frequency (3)			29		33.33	kHz
F_{MF}	SSC Modulation Factor (3)				–0.4	–0.5	%
SSC_{red}	Spectral Reduction (3)			4	6		dB
t_{STABLE}	Power-up to Stable Clock Output (4,5)			500			ps
V_{MAX}	Absolute Maximum Output Volltage; (6,7)		HCSL Levels			1150	mV
V_{MIN}	Absolute Minimum Output Volltage; (6,8)		HCSL Levels	–300			
V_{rb}	Ringback Voltage; (4,5)		HCSL Levels	–100		100	
V_{CROSS}	Absolute Crossing Voltage; (6, 9, 10)		HCSL Levels	250		550	
ΔV_{CROSS}	Total Variation of VCROSS; (6, 9, 11)		HCSL Levels			140	
t_R / t_F	Output Rise/ Fall Time	Q0_Ref : nQ11_Ref, Q3B_ PLL1, nQ2B_PLL1	20% to 80%	150		350	ps
	Rise/Fall Edge Rate	Q(0,1)A_PLL1±, Q0_ PLL2± (4)		0.6		5	V/ns
odc	Output Duty Cycle;	Q0_Ref: nQ11_Ref		42		58	%
		Q3B_PLL1, nQ2B_PLL1		49		51	
		Q(0,1)A_PLL1±, Q0_ PLL2± (4)		49		51	

(see notes on following page)

AC Characteristics (table notes continued from previous page)

NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 2: Only valid within the VCO operating range.

NOTE 3: Spread Spectrum clocking enabled.

NOTE 4: Measurement taken from differential waveform.

NOTE 5: TSTABLE is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to droop back into the VRB ±100mV differential range.

NOTE 6: Measurement taken from single-ended waveform.

NOTE 7: Defined as the maximum instantaneous voltage including overshoot.

NOTE 8: Defined as the minimum instantaneous voltage including undershoot.

NOTE 9: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx+ equals the falling edge of Qx–.

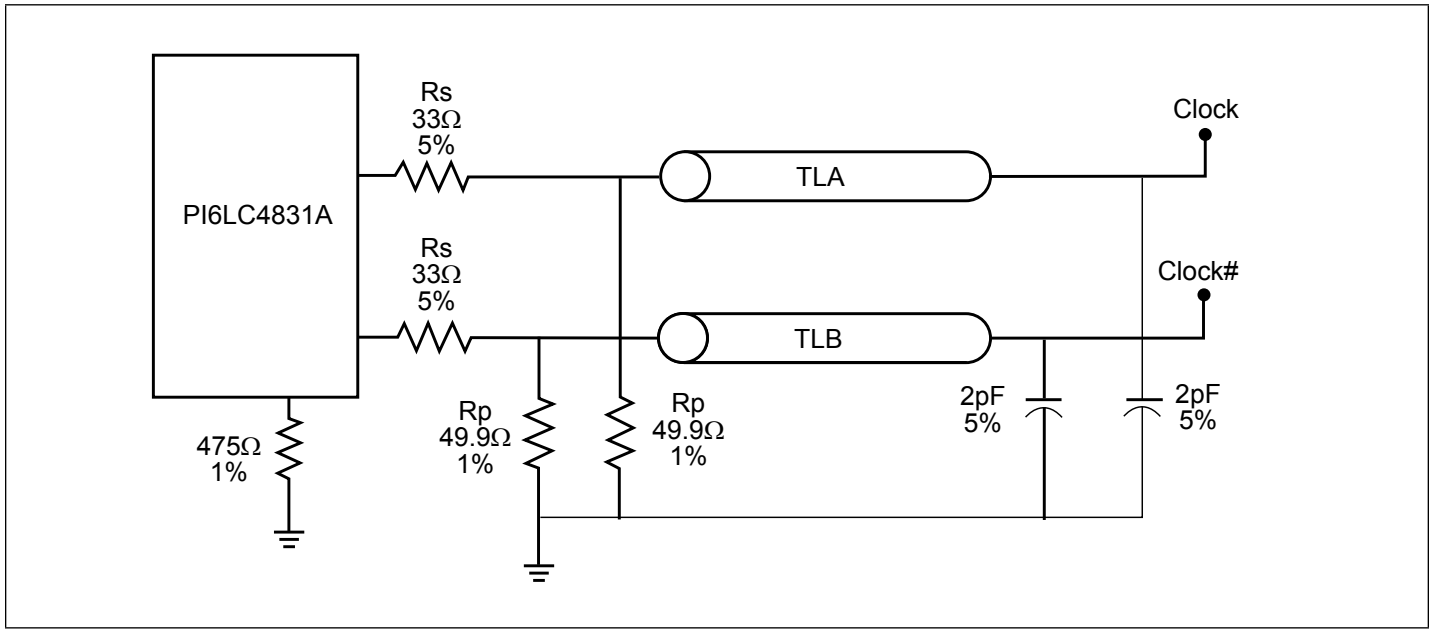
NOTE 10: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing.

Refers to all crossing points for this measurement.

NOTE 11: Defined as the total variation of all crossing voltage of Rising Qx+ and Falling Qx–. This is the maximum allowed variance in the VCROSS for any particular system.

NOTE 12: Measured from -150mV to +150mV on the differential waveform (derived from Qx+ minus Qx–). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

Configuration



Configuration test load board termination for HCSL Outputs

Crystal Characteristics

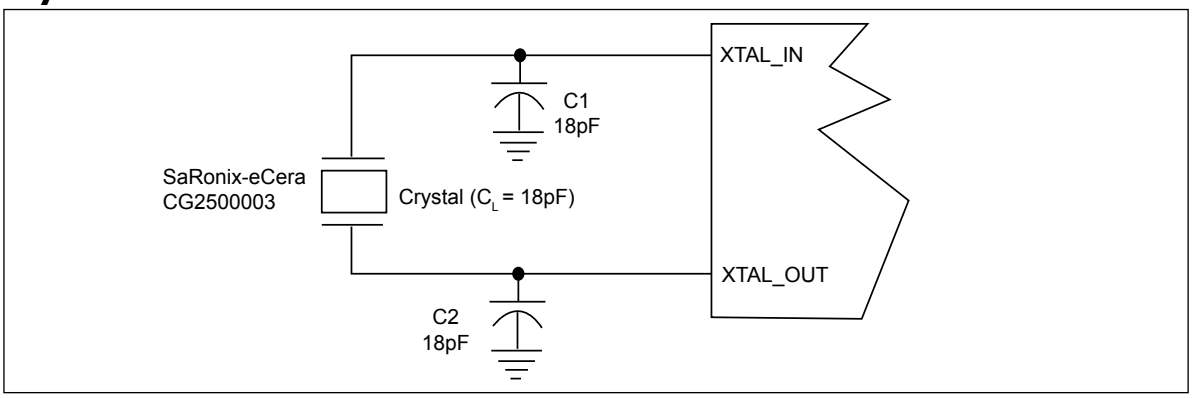
Parameter	Test Conditions	Min	Typ	Max	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ohm
Shunt Capacitance				7	pF
Drive Level				100	µW

Application Notes

Crystal circuit connection

The following diagram shows PI6LC4831A crystal circuit connection with a parallel crystal. For the CL=18pF crystal, it is suggested to use C1= 18pF, C2= 18pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

Crystal Oscillator Circuit



Recommended Crystal Specification

Pericom recommends:

a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf

b) FY2500081, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm, http://www.pericom.com/pdf/datasheets/se/FL.pdf

Application Information

Decoupling Capacitors

Decoupling capacitors of 0.01µF should be connected between each V_{DD} pin and the ground plane and placed as close to the V_{DD} pin as possible.

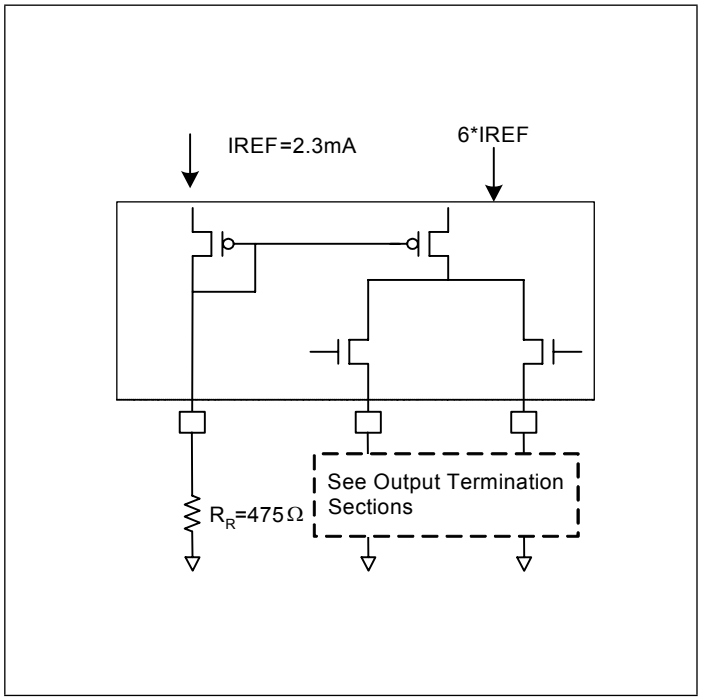
Current Source (IREF) Reference Resistor - R_R

If board target trace impedance is 50Ω,
then R_R = 475Ω providing an IREF of 2.32 mA. The output current (I_{OH}) is 6*IREF.

Output Termination

The PCI Express differential clock outputs of the PI6LC4831A are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the PCI Express Layout Guidelines section.

Output Structures



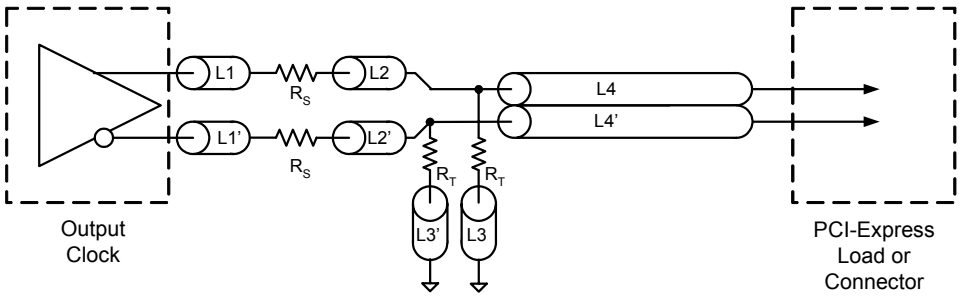
PCI Express Layout Guidelines

Common Recommendations for Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50Ω trace.	0.5 max	inch
L2 length, route as non-coupled 50Ω trace.	0.2 max	inch
L3 length, route as non-coupled 50Ω trace.	0.2 max	inch
R_S	33	Ω
R_T	49.9	Ω

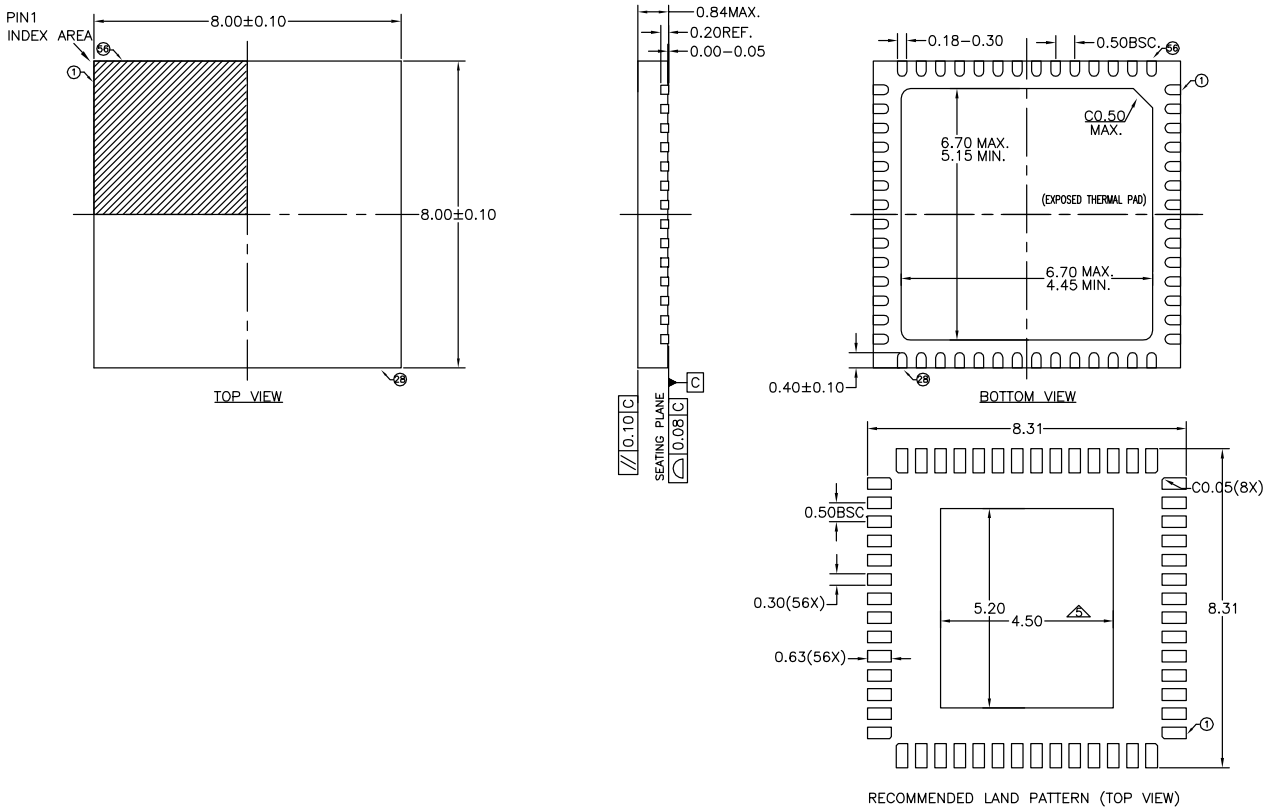
Differential Routing on a Single PCB	Dimension or Value	Unit
L4 length, route as coupled microstrip 100Ω differential trace.	2 min to 16 max	inch
L4 length, route as coupled stripline 100Ω differential trace.	1.8 min to 14.4 max	inch

Differential Routing to a PCI Express connector	Dimension or Value	Unit
L4 length, route as coupled microstrip 100Ω differential trace.	0.25 min to 14 max	inch
L4 length, route as coupled stripline 100Ω differential trace.	0.225 min to 12.6 max	inch

PCI Express Device Routing



Packaging Mechanical: 56-contact, TQFN (ZB)



Notes:
1. All dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed thermal pad as well as the terminals.
3. Refer JEDEC MO-137 AE
4. Recommended land pattern is for reference only.
5. Thermal pad soldering area (mesh stencile design is recommended).

PERICOM Enabling Serial Connectivity

DATE: 10/05/10

DESCRIPTION: 56-Pin, Thin Fine Pitch Quad Flat No-lead, TQFN

PACKAGE CODE: ZB (ZB56)

DOCUMENT CONTROL #: PD-2008 **REVISION: G**

Ordering Information(1-3)

Ordering Code	Package Code	Package Description
PI6LC4831AZBIE	ZB	56-pin, Pb-free and Green (TQFN)

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

2. E = Pb-free and Green

3. Adding an X suffix = Tape/Reel