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Evaluating the ADE7854A/ADE7858A/ADE7868A/ADE7878A Energy Metering ICs

FEATURES

- Evaluation board designed to be used with accompanying software to implement a fully functional 3-phase energy meter
- Easy connection of external transducers via screw terminals
- Easy modification of signal conditioning components using PCB sockets
- LED indicators on the CF1, CF2, CF3, IRQ0, and IRQ1 logic outputs
- Digitally isolated metering components and USB-based communication with a PC
- External voltage reference option available for on-chip reference evaluation
- PC COM port-based firmware updates

EVALUATION KIT CONTENTS

- EVAL-ADE7878AEBZ evaluation board
- USB cable

ONLINE RESOURCES

- ADE7854A/ADE7858A/ADE7868A/ADE7878A data sheet
- EVAL-ADE7878AEBZ user guide

GENERAL DESCRIPTION

The ADE7854A/ADE7858A/ADE7868A/ADE7878A are high accuracy, 3-phase electrical energy measurement ICs with serial interfaces and three flexible pulse outputs. These ICs incorporate second-order sigma-delta (Σ-Δ) analog-to-digital converters (ADCs), a digital integrator, reference circuitry, and all of the signal processing required to perform the total (fundamental and harmonic) active and apparent energy measurements, rms calculations, and fundamental-only active and reactive energy measurements.

This user guide describes the evaluation kit hardware, firmware, and software functionality. The evaluation board contains an IC and an LPC2368 microcontroller from NXP Semiconductors. The energy metering IC and its associated metering components are digitally isolated from the microcontroller. The microcontroller communicates with the PC using a USB interface.

The EVAL-ADE7878AEBZ and this user guide, together with the ADE7854A/ADE7858A/ADE7868A/ADE7878A data sheet, provide a complete evaluation platform for the ADE7854A/ADE7858A/ADE7868A/ADE7878A.

The evaluation board has been designed so that the ADE7854A/ADE7858A/ADE7868A/ADE7878A can be evaluated as an energy meter. Using appropriate current transducers, the evaluation board can be connected to a test bench or high voltage (240 V rms) test circuit. On-board resistor divider networks provide the attenuation for the line voltages.

This user guide describes how to connect the current transducers for the best performance. The evaluation board requires one external power supply of 3.3 V applied to the P9 connector. Appropriate current transducers are also required.

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REVISION HISTORY

7/14—Revision 0: Initial Version

EVALUATION BOARD CONNECTION DIAGRAM

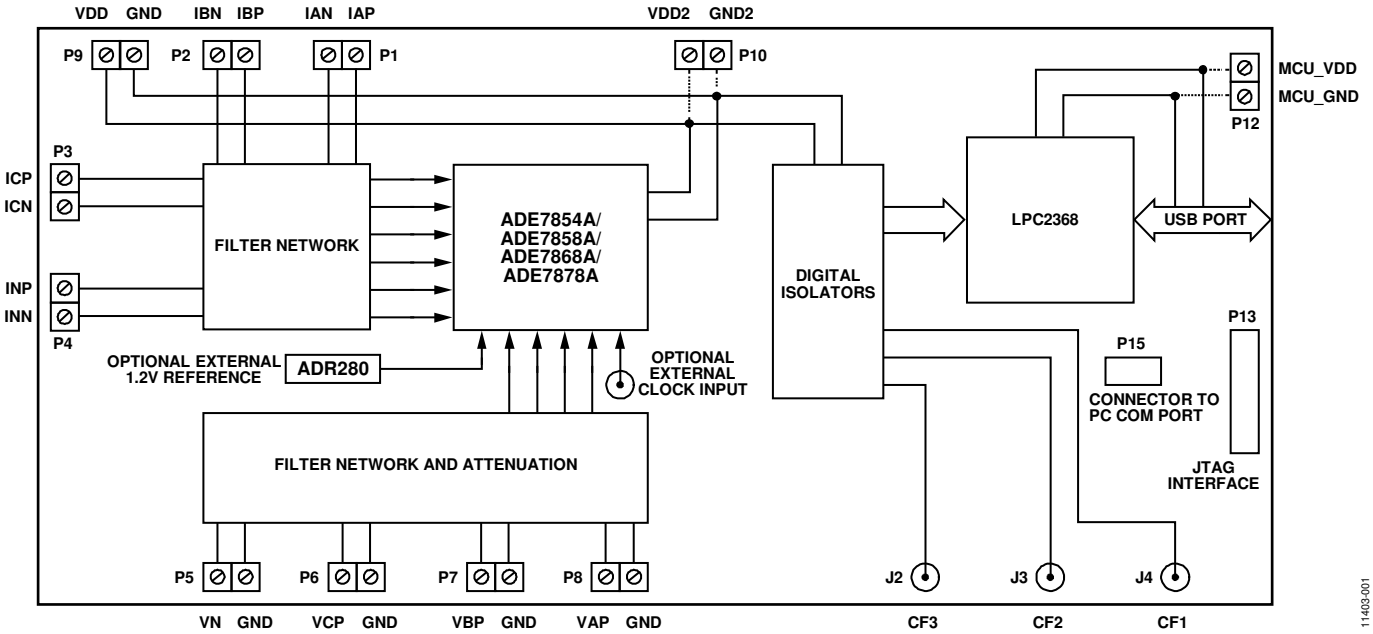


Figure 1.

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The evaluation board has two power domains: one domain supplies the microcontroller and one side of the *i*Coupler®, and one domain supplies the other side of the *i*Coupler and the ADE7854A/ADE7858A/ADE7868A/ADE7878A. The ground of the microcontroller's power domain is connected to the ground of the PC through the USB cable. The ground of the ADE7854A/ADE7858A/ADE7868A/ADE7878A power domain is determined by the ground of the phase voltages, VAP, VBP, VCP, and VN, and must be different from the ground of the microcontroller's power domain.

The microcontroller 3.3 V supply is provided by the PC through the USB cable. Alternatively, if Jumper JP24 is connected between Pin 1 and Pin 2, the 3.3 V supply can be provided at the P12 connector. The ADE7854A/ADE7858A/ADE7868A/ADE7878A 3.3 V supply is provided at the P9 connector. Ensure that Jumper JP11 is connected between Pin 1 and Pin 2 to ensure the same 3.3 V supply from the ADE7854A/ADE7858A/ADE7868A/ADE7878A is also provided at the *i*Couplers.

ANALOG INPUTS (P1 TO P4 AND P5 TO P8)

Current and voltage signals are connected at the screw terminals, P1 to P4 and P5 to P8, respectively. All analog input signals are filtered using the on-board antialiasing filters before the signals are connected to the ADE7854A/ADE7858A/ADE7868A/ADE7878A. The components used on the board are the recommended values to be used with the ADE7854A/ADE7858A/ADE7868A/ADE7878A.

Current Sense Inputs (P1, P2, P3, and P4)

The ADE7854A/ADE7858A/ADE7868A/ADE7878A measures 3-phase currents and the neutral current. Current trans-formers or Rogowski coils can be used to sense the currents. These sensors cannot be mixed together for the phase currents sensing, but the neutral current may be sensed using a different sensor. The IC contains different internal PGA gains on phase currents and on the neutral current; therefore, sensors with different ratios can be used. The only requirement is to have the same scale signals at the PGA outputs; otherwise, the mismatch functionality of the IC is compromised (see the ADE7854A/ADE7858A/ADE7868A/ADE7878A data sheet for more details about neutral current mismatch). Figure 2 shows the structure used for the Phase A current; the sensor outputs are connected to the P1 connector.

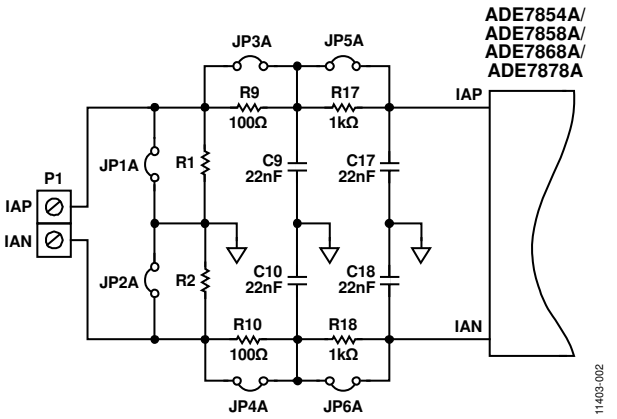


Figure 2. Phase A Current Input Structure on the Evaluation Board

The R1 and R2 resistors are the burden resistors and, by default, they are not populated. They can also be disabled using the JP1A and JP2A jumpers. The R9/C9 and R10/C10 RC networks are used in conjunction with Rogowski coils. They can be disabled using the JP3A and JP4A jumpers. The R17/C17 and R18/C18 RC networks are the antialiasing filters. The default corner frequency of these low-pass filters is 7.2 kHz (1 kΩ/22 nF). These filters can easily be adjusted by replacing the components on the evaluation board.

All the other current channels (that is, Phase B, Phase C, and the neutral current) have an identical input structure.

Using a Current Transformer as the Current Sensor

Figure 3 shows how a current transformer can be used as a current sensor in one phase of a 3-phase, 4-wire distribution system (Phase A). The other two phases and the neutral current require similar connections.

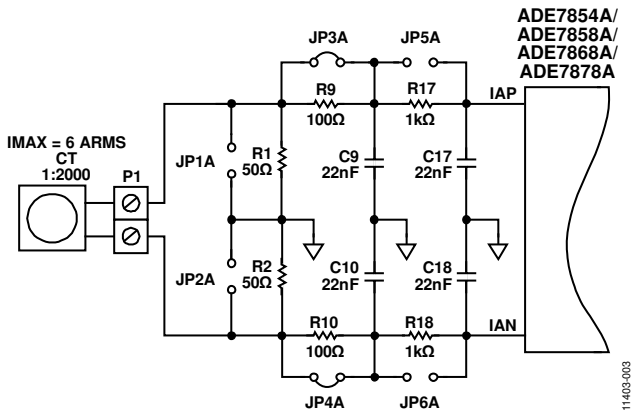


Figure 3. Example of a Current Transformer Connection

The R1 and R2 burden resistors must be defined as functions of the current transformer ratio and the maximum current of the system, using the following formula:

$$R1 = R2 = 1/2 \times 0.5/\sqrt{2} \times N/I_{FS}$$

where:
$0.5/\sqrt{2}$ is the rms value of the full-scale voltage accepted at the ADC input.
N is the input-to-output ratio of the current transformer. Figure 3 shows an example for $N = 2000$.
I_{FS} is the maximum rms current to be measured.

The JP1A and JP2A jumpers should be opened if R1 and R2 are used. The antialiasing filters should be enabled by opening the J5A and J6A jumpers (see Figure 3).

The secondary current of the transformer is converted to a voltage by using a burden resistor across the secondary winding outputs. Care should be taken when using a current transformer as the current sensor. If the secondary is left open (that is, no burden is connected), a large voltage may be present at the secondary outputs. This can cause an electric shock hazard and potentially damage electronic components.

For this particular example, burden resistors of 50 Ω signify an input current of 7.05 A rms at the ADE7854A/ADE7858A/ADE7868A/ADE7878A ADC full-scale input (0.5 V). In addition, the PGA gains for the current channel must be set to 1. For more information about setting PGA gains, see the ADE7854A/ADE7858A/ADE7868A/ADE7878A data sheet. The evaluation software allows the user to configure the current channel gain.

Using a Rogowski Coil as the Current Sensor

Figure 4 shows how a Rogowski coil can be used as a current sensor in one phase of a 3-phase, 4-wire distribution system (Phase A). The other two phases and the neutral current require identical connections. The Rogowski coil does not require any burden resistors; therefore, R1 and R2 should not be populated. The antialiasing filters should be enabled by opening the JP5A and JP6A jumpers. To account for the high frequency noise introduced by the coil, an additional antialiasing filter must be introduced by opening the JP3A and JP4A jumpers. Then, to compensate for the 20 dB/dec gain introduced by the di/dt sensor, the integrator of the IC must be enabled by setting Bit 0 (INTEN) of the CONFIG register. The integrator has a −20 dB/dec attenuation and a phase shift of approximately −90° and, when combined with the di/dt sensor, results in a magnitude and phase response with a flat gain over the frequency band of interest.

Voltage Sense Inputs (P5, P6, P7, and P8 Connectors)

The voltage input connections on the EVAL-ADE7878AEBZ can be directly connected to the line voltage sources. The line voltages are attenuated using a simple resistor divider network before they are supplied to the IC. The attenuation network on the voltage channels is designed so that the 3 dB corner frequency of the network matches that of the antialiasing filters in the current channel inputs. This prevents the occurrence of large energy errors at low power factors.

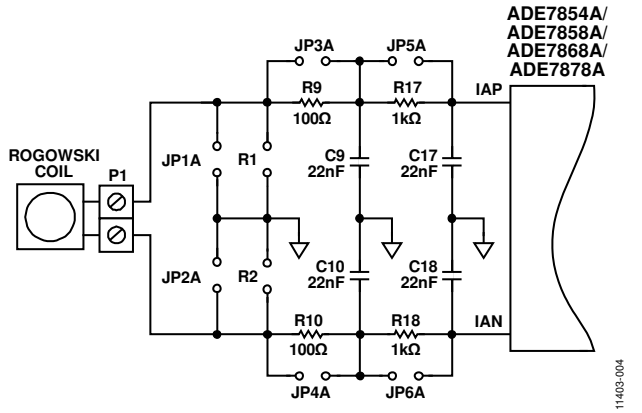


Figure 4. Example of a Rogowski Coil Connection

Figure 5 shows a typical connection of the Phase A voltage input; the resistor divider is enabled by opening the JP7A jumper, closing JP9A and connecting JP8A to AGND (Pin 1). The antialiasing filter on the VN datapath is enabled by opening the JP7N jumper. The VN analog input is connected to AGND via the R25/C25 antialiasing filter using the P5 connector. The neutral can be tied to ground by inserting the neutral into the P5 connector and connecting the two terminals together.

The attenuation networks can be easily modified by the user to accommodate any input level. However, the value of R32 (1 kΩ), should be modified only together with the corresponding resistors in the current channel (R17 and R18 on the Phase A current datapath).

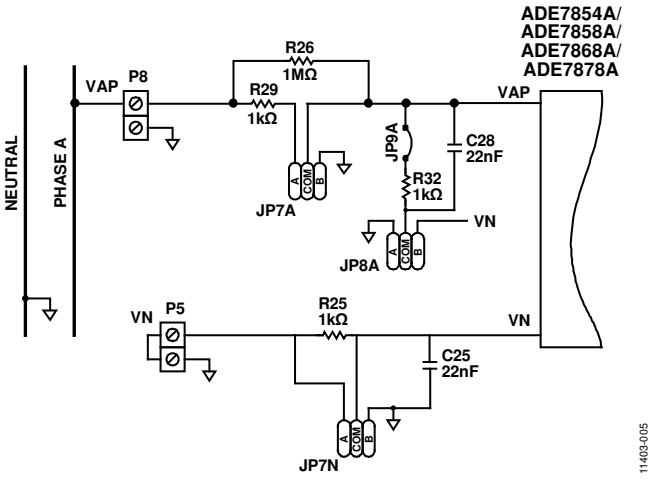


Figure 5. Phase A Voltage Input Structure on the Evaluation Board

The maximum signal level permissible at the VAP, VBP, and VCP pins of the ADE7854A/ADE7858A/ADE7868A/ADE7878A is 0.5 V peak. Although the IC analog inputs can withstand ±2 V without risk of permanent damage, the signal range should not exceed ±0.5 V with respect to AGND for a specified operation.

Table 1. Recommended Settings for Evaluation Board Connectors

Jumper	Option	Description
JP1A	Closed	Connects Pin 1 of the Channel IA pin connector, P1, to AGND. Use this configuration in conjunction with JP3A and JP5A to short the IAP pin of the ADE7854A/ADE7858A/ADE7868A/ADE7878A to AGND.
	Open (default)	Pin 1 of the Channel IA pin connector, P1, is left floating. Use this configuration in normal operation to drive IAP with analog signal.
JP1B	Closed	Connects Pin 1 of the Channel IB pin connector, P2, to AGND. Use this configuration in conjunction with JP3B and JP5B to short the IBP pin of the ADE7854A/ADE7858A/ADE7868A/ADE7878A to AGND.
	Open (default)	Pin 1 of the Channel IB pin connector, P2, is left floating. Use this configuration in normal operation to drive IBP with analog signal.
JP1C	Closed	Connects Pin 1 of the Channel IC pin connector, P3, to AGND. Use this configuration in conjunction with JP3C and JP5C to short the ICP pin of the ADE7854A/ADE7858A/ADE7868A/ADE7878A to AGND.
	Open (default)	Pin 1 of the Channel IC pin connector, P3, is left floating. Use this configuration in normal operation to drive ICP with analog signal.
JP1N	Closed	Connects Pin 1 of the Channel IN pin connector, P4, to AGND. Use this configuration in conjunction with JP3N and JP5N to short the INP pin of the ADE7854A/ADE7858A/ADE7868A/ADE7878A to AGND.
	Open (default)	Pin 1 of the Channel IN pin connector, P4, is left floating. Use this configuration in normal operation to drive INP with analog signal.
JP2A	Closed	Connects Pin 2 of the Channel IA pin connector, P1, to AGND. Use this configuration in conjunction with JP4A and JP6A to short the IAN pin of the ADE7854A/ADE7858A/ADE7868A/ADE7878A to AGND.
	Open (default)	Pin 2 of the Channel IA pin connector, P1, is left floating. Use this configuration in normal operation when driving a differential input to IAN.
JP2B	Closed	Connects Pin 2 of the Channel IB pin connector, P2, to AGND. Use this configuration in conjunction with JP4B and JP6B to short the IBN pin of the ADE7854A/ADE7858A/ADE7868A/ADE7878A to AGND.
	Open (default)	Pin 2 of the Channel IB pin connector, P2, is left floating. Use this configuration in normal operation when driving a differential input to IBN.
JP2C	Closed	Connects Pin 2 of the Channel IC pin connector, P3, to AGND. Use this configuration in conjunction with JP4C and JP6C to short the ICN pin of the ADE7854A/ADE7858A/ADE7868A/ADE7878A to AGND.
	Open (default)	Pin 2 of the Channel IC pin connector, P3, is left floating. Use this configuration in normal operation when driving a differential input to ICN.
JP2N	Closed	Connects Pin 2 of the Channel IN pin connector, P4, to AGND. Use this configuration in conjunction with JP4N and JP6N to short the INN pin of the ADE7854A/ADE7858A/ADE7868A/ADE7878A to AGND.
	Open (default)	Pin 2 of the Channel IBN pin connector, P2, is left floating. Use this configuration in normal operation when driving a differential input to IBN.
JP3A	Closed (default)	Disables the phase compensation network (composed by R9 and C9) in the IAP datapath.
	Open	Enables the phase compensation network (composed by R9 and C9) in the IAP datapath.
JP3B	Closed (default)	Disables the phase compensation network (composed by R11 and C11) in the IBP datapath.
	Open	Enables the phase compensation network (composed by R11 and C11) in the IBP datapath.
JP3C	Closed (default)	Disables the phase compensation network (composed by R13 and C13) in the ICP datapath.
	Open	Enables the phase compensation network (composed by R13 and C13) in the ICP datapath.
JP3N	Closed (default)	Disables the phase compensation network (composed by R15 and C15) in the INP datapath.
	Open	Enables the phase compensation network (composed by R15 and C15) in the INP datapath.
JP4A	Closed (default)	Disables the phase compensation network (composed by R10 and C10) in the IAN datapath.
	Open	Enables the phase compensation network (composed by R10 and C10) in the IAN datapath.
JP4B	Closed (default)	Disables the phase compensation network (composed by R12 and C12) in the IBN datapath.
	Open	Enables the phase compensation network (composed by R12 and C12) in the IBN datapath.
JP4C	Closed (default)	Disables the phase compensation network (composed by R14 and C14) in the ICN datapath.
	Open	Enables the phase compensation network (composed by R14 and C14) in the ICN datapath.
JP4N	Closed (default)	Disables the phase compensation network (composed by R16 and C16) in the INN datapath.
	Open	Enables the phase compensation network (composed by R16 and C16) in the INN datapath.
JP5A	Closed	Disables the phase antialiasing filter (composed by R17 and C17) in the IAP datapath.
	Open (default)	Enables the phase antialiasing filter (composed by R17 and C17) in the IAP datapath.
JP5B	Closed	Disables the phase antialiasing filter (composed by R19 and C19) in the IBP datapath.
	Open (default)	Enables the phase antialiasing filter (composed by R19 and C19) in the IBP datapath.

Jumper	Option	Description
JP5C	Closed	Disables the phase antialiasing filter (composed by R21 and C21) in the ICP datapath.
	Open (default)	Enables the phase antialiasing filter (composed by R21 and C21) in the ICP datapath.
JP5N	Closed	Disables the phase antialiasing filter (composed by R23 and C23) in the INP datapath.
	Open (default)	Enables the phase antialiasing filter (composed by R23 and C23) in the INP datapath.
JP6A	Closed	Disables the phase antialiasing filter (composed by R18 and C18) in the IAN datapath.
	Open (default)	Enables the phase antialiasing filter (composed by R18 and C18) in the IAN datapath.
JP6B	Closed	Disables the phase antialiasing filter (composed by R20 and C20) in the IBN datapath.
	Open (default)	Enables the phase antialiasing filter (composed by R20 and C20) in the IBN datapath.
JP6C	Closed	Disables the phase antialiasing filter (composed by R22 and C22) in the ICN datapath.
	Open (default)	Enables the phase antialiasing filter (composed by R22 and C22) in the ICN datapath.
JP6N	Closed	Disables the phase antialiasing filter (composed by R24 and C24) in the INN datapath.
	Open (default)	Enables the phase antialiasing filter (composed by R24 and C24) in the INN datapath.
JP7A	Closed between Pin 2 and Pin 1	Disables the resistor divider (composed by R26, R29, and R32) when JP9A is open. Use this configuration when using a low voltage signal source in the VAP datapath.
	Closed between Pin 2 and Pin 3	Connects the VAP pin of the ADE7854A/ADE7858A/ADE7868A/ADE7878A to AGND. Use this configuration when no signal source is desired in the VAP datapath.
	Unconnected (default)	Enables the resistor divider (composed by R26, R29, and R32) when JP9A is closed. Use this configuration when using a high voltage signal source in the VAP datapath in 3-phase, 4-wire and 3-phase, 3-wire configurations.
JP7B	Closed between Pin 2 and Pin 1	Disables the resistor divider (composed by R27, R30, and R33) when JP9B is open. Use this configuration when using a low voltage signal source in the VBP datapath.
	Closed between Pin 2 and Pin 3	Connects the VBP pin of the ADE7854A/ADE7858A/ADE7868A/ADE7878A to AGND. Use this configuration when no signal source is desired in the VBP datapath, such as 3-phase, 3-wire configuration.
	Unconnected (default)	Enables the resistor divider (composed by R27, R30, and R33) when JP9B is closed. Use this configuration when using a high voltage signal source in the VBP datapath in 3-phase, 4-wire configuration.
JP7C	Closed between Pin 2 and Pin 1	Disables the resistor divider (composed by R28, R31, and R34) when JP9C is open. Use this configuration when using a low voltage signal source in the VCP datapath.
	Closed between Pin 2 and Pin 3	Connects the VCP pin of the ADE7854A/ADE7858A/ADE7868A/ADE7878A to AGND. Use this configuration when no signal source is desired in the VCP datapath.
	Unconnected (default)	Enables the resistor divider (composed by R28, R31, and R34) when JP9C is closed. Use this configuration when using a high voltage signal source in the VCP datapath in 3-phase, 4-wire and 3-phase, 3-wire configurations.
JP7N	Closed between Pin 2 and Pin 1	Disables the antialiasing filter (composed by R25 and C25) in the VN datapath. Use this configuration when normal single ended signals are connected to the ADE7854A/ADE7858A/ADE7868A/ADE7878A voltage channels.
	Closed between Pin 2 and Pin 3	Connects the VN pin of the ADE7854A/ADE7858A/ADE7868A/ADE7878A to AGND. Use this configuration when the ADE7854A/ADE7858A/ADE7868A/ADE7878A voltage channels are connected to AGND.
	Unconnected (default)	Enables the antialiasing filter in the VN datapath. Use this configuration when the ADE7854A/ADE7858A/ADE7868A/ADE7878A voltage channels are differential, in 3-phase, 4-wire and 3-phase, 3-wire configurations.
JP8A	Soldered between Pin 2 and Pin 1 (default)	Connects C28 to AGND. Use this configuration when the ADE7854A/ADE7858A/ADE7868A/ADE7878A voltage channels are differential, in 3-phase, 4-wire and 3-phase, 3-wire configurations.
	Soldered between Pin 2 and Pin 3	Connects C28 to VN. Use this configuration, with JP7N connected between Pin 2 and Pin 3, when the ADE7854A/ADE7858A/ADE7868A/ADE7878A voltage channels are single-ended.
JP8B	Soldered between Pin 2 and Pin 1 (default)	Connects C27 to AGND. Use this configuration when the ADE7854A/ADE7858A/ADE7868A/ADE7878A voltage channels are differential, in 3-phase, 4-wire and 3-phase, 3-wire configurations.
	Soldered between Pin 2 and Pin 3	Connects C27 to VN. Use this configuration, with JP7N connected between Pin 2 and Pin 3, when the ADE7854A/ADE7858A/ADE7868A/ADE7878A voltage channels are single-ended.

Jumper	Option	Description
JP8C	Soldered between Pin 2 and Pin 1 (default)	Connects C25 to AGND. Use this configuration when ADE7854A/ADE7858A/ADE7868A/ADE7878A voltage channels are differential, in 3-phase, 4-wire and 3-phase, 3-wire configurations.
	Soldered between Pin 2 and Pin 3	Connects C25 to VN. Use this configuration, with JP7N connected between Pin 2 and Pin 3, when the ADE7854A/ADE7858A/ADE7868A/ADE7878A voltage channels are single-ended.
JP9A	Closed (default)	Enables the resistor divider (composed by R26, R29, and R32) when JP7A is unconnected. Use this configuration when using a high voltage signal source in the VAP datapath, in 3-phase, 4-wire and 3-phase, 3-wire configurations.
	Open	Disables the resistor divider (composed by R26, R29, and R32) when JP7A is closed between Pin 1 and Pin 2. Use this configuration when using a low voltage signal source in the VAP datapath.
JP9B	Closed (default)	Enables the resistor divider (composed by R27, R30, and R33) when JP7B is unconnected. Use this configuration when using a high voltage signal source in the VBP datapath in 3-phase, 4-wire and 3-phase, 3-wire configurations.
	Open	Disables the resistor divider (composed by R27, R30, and R33) when JP7B is closed between Pin 1 and Pin 2. Use this configuration when using a low voltage signal source in the VBP datapath.
JP9C	Closed (default)	Enables the resistor divider (composed by R28, R31, and R34) when JP7C is unconnected. Use this configuration when using a high voltage signal source in the VCP datapath in 3 phase, 4 wire and 3-phase, 3-wire configurations.
	Open	Disables the resistor divider (composed by R28, R31, and R34) when JP7C is closed between Pin 1 and Pin 2. Use this configuration when using a low voltage signal source in the VCP datapath.
JP10	Soldered between Pin 2 and Pin 1 (default)	Connects the on-board 16.384 MHz crystal, Y1, to the CLKIN pin of the ADE7854A/ADE7858A/ ADE7868A/ADE7878A. Use this configuration when Crystal Y1 is used as the clock source for the ADE7854A/ADE7858A/ADE7868A/ADE7878A.
	Soldered between Pin 2 and Pin 3	Disconnects the on-board 16.384 MHz crystal, Y1, from the CLKIN pin of the ADE7854A/ADE7858A/ ADE7868A/ADE7878A. Use this configuration when an external clock is used. This clock can be connected to the EXT_CLKIN connector.
JP11	Closed between Pin 2 and Pin 1 (default)	Connects the supply of the secondary side of the *i*Couplers (VDD2) to VDD, the supply of the ADE7854A/ADE7858A/ADE7868A/ADE7878A.
	Closed between Pin 2 and Pin 3	Connects the supply of the secondary side of the *i*Couplers (VDD2) to a 3.3 V supply provided at the P10 connector.
JP12	Closed	Connects the ADR280 voltage reference to the $REF_{IN/OUT}$ pin of the ADE7854A/ADE7858A/ ADE7868A/ADE7878A. Use this configuration when the ADE7854A/ADE7858A/ADE7868A/ ADE7878A are configured to use an external reference.
	Open (default)	Disconnects the ADR280 voltage reference from the $REF_{IN/OUT}$ pin of the ADE7854A/ADE7858A/ ADE7868A/ADE7878A. Use this configuration in normal operation when the ADE7854A/ADE7858A/ADE7868A/ADE7878A are configured to use the internal reference.
JP21	Closed	Signals the NXP LPC2368 microcontroller to declare all I/O pins as outputs. Use this configuration when another microcontroller manages the ADE7854A/ADE7858A/ADE7868A/ADE7878A through the P17 socket.
	Open (default)	Disables the option to use another microcontroller to manage the ADE7854A/ADE7858A/ ADE7868A/ADE7878A through the P17 socket. Use this configuration in normal operation to allow the NXP LPC2368 microcontroller to manage the ADE7854A/ADE7858A/ADE7868A/ADE7878A.
JP24	Closed between Pin 2 and Pin 1	Selects an external 3.3 V power supply provided at P12 connector to power the domain that includes the NXP LPC2368 and one side of the *i*Couplers. Use this configuration if USB provided power supply is not desired.
	Closed between Pin 2 and Pin 3 (default)	Selects the USB provided power supply to power the domain that includes the NXP LPC2368 and one side of the *i*Couplers. Use this configuration in normal operation to provide power to the NXP LPC2368 and one side of the *i*Couplers from the PC.
JP31, JP32, JP33, JP34	Closed between Pin 2 and Pin 1	When I^2C communication between the NXP LPC2368 and the ADE7854A/ADE7858A/ ADE7868A/ADE7878A is used, the HSDC port of the IC is also enabled and the SPI ports of the IC are disabled. Use this configuration when I^2C communication is selected.
	Closed between Pin 2 and Pin 3 (default)	When SPI communication between the NXP LPC2368 and the ADE7854A/ADE7858A/ADE7868A/ ADE7878A is used, the I^2C and HSDC ports of the IC are disabled. Use this configuration when SPI communication is selected.

SETTING UP THE EVALUATION BOARD AS AN ENERGY METER

Figure 6 shows a typical setup for the EVAL-ADE7878AEBZ board. In this example, an energy meter for a 3-phase, 4-wire, wye distribution system is shown. Current transformers are used to sense the phase and neutral currents and are connected as shown in Figure 6. The line voltages are connected directly to the evaluation board as shown. Note that the state of all jumpers must match the states shown in Figure 6, equal to the default states in Table 1.

The board is supplied from two different power supplies. One is supplied by the PC through the USB cable and is used for the NXP LPC2368 and for one side of the *i*Couplers. The other is an external 3.3 V supply used for theADE7854A/ADE7858A/ADE7868A/ADE7878A domain and the other side of the *i*Couplers. Because the two domains are isolated to ensure that there is no electrical connection between the high voltage test circuit and the control circuit, the external power supply should have floating voltage outputs.

Figure 7 shows a setup for the evaluation board as an energy meter for a 3-phase, 3-wire, delta distribution system. The Phase B voltage is used as a ground reference, and the VN pin of the ADE7854A/ADE7858A/ADE7868A/ADE7878A IC is connected to it.

The evaluation board is connected to the PC using a USB cable supplied with the board. When the evaluation board is connected to the PC, the enumeration process begins. The PC recognizes new hardware and asks to install the appropriate driver. The driver can be found in the VirCOM_Driver_XP folder in the evaluation software, downloadable from the product website, for a Windows® XP PC or in VirCom_Driver_W7_64bit for a Windows 7 64-bit PC. After the driver is installed, the supplied evaluation software can be started. The Evaluation Board Software section describes the evaluation software in detail and how it can be installed and uninstalled.

Activating Serial Communication Between the IC and the NXP LPC2368

The EVAL-ADE7878AEBZ provides communication between the ADE7854A/ADE7858A/ADE7868A/ADE7878A and the NXP LPC2368 that is set through the SPI ports. The JP31, JP32, JP33, and JP34 jumpers are closed between Pin 2 and Pin 3. The SPI port should be chosen as the active port in the ADE7854A/ADE7858A/ADE7868A/ADE7878A Control Panel.

Communication between the ADE7854A/ADE7858A/ADE7868A/ADE7878Aand the NXP LPC2368 is also possible using the I²C ports. To accomplish this, the JP31, JP32, JP33, and JP34 jumpers should be closed between Pin 2 and Pin 1. In this case, the I²C port should be chosen as the active port in the Control Panel (see Table 2). Note that the HSDC port of the ADE7854A/ADE7858A/ADE7868A/ADE7878A also becomes available to communicate with the NXP LPC2368 in this case.

Table 2. Jumper State to Activate SPI or I²C Communication

Active Communication	JP31, JP32, JP33, JP34 Jumpers
SPI (Default)	Closed between Pin 2 and Pin 3
I²C	Closed between Pin 2 and Pin 1

Using the Evaluation Board with Another Microcontroller

It is possible to manage the ADE7854A/ADE7858A/ADE7868A/ADE7878A mounted on the evaluation board with a different microcontroller mounted on another board. The IC can be connected to this second board through one of two connectors: P11 or P17. P11 is placed on the same power domain as the ADE7854A/ADE7858A/ADE7868A/ADE7878A. P17 is placed on the power domain of the NXP LPC2368 and communicates with the ADE7854A/ADE7858A/ADE7868A/ADE7878A through the *i*Couplers.

If P11 is used, the USB cable should not be connected to the P14 connector to avoid supplying the power domain of the NXP LPC2368. In addition, it is recommended to remove the *i*Couplers from the board in these instances. If P17 is used, a conflict may arise with the NXP LPC2368 I/O ports. To avoid this conflict, close the JP21 jumper. This tells the NXP LPC2368 to set all of its I/O ports to a high impedance state to allow the other microcontroller to communicate with the ADE7854A/ADE7858A/ADE7868A/ADE7878A.

After JP21 is closed, press the S2 reset button low to reset the NXP LPC2368. This is necessary because the state of JP21 is checked inside the NXP LPC2368 program only once after reset. Based on the communication port used, solder jumpers JP71, JP72, JP73, and JP74 appropriately. In the case of SPI, solder jumpers between Pin 2 (middle) and Pin 3 (top); in the case of I²C, solder jumpers between Pin 1(bottom) and Pin 2 (middle).

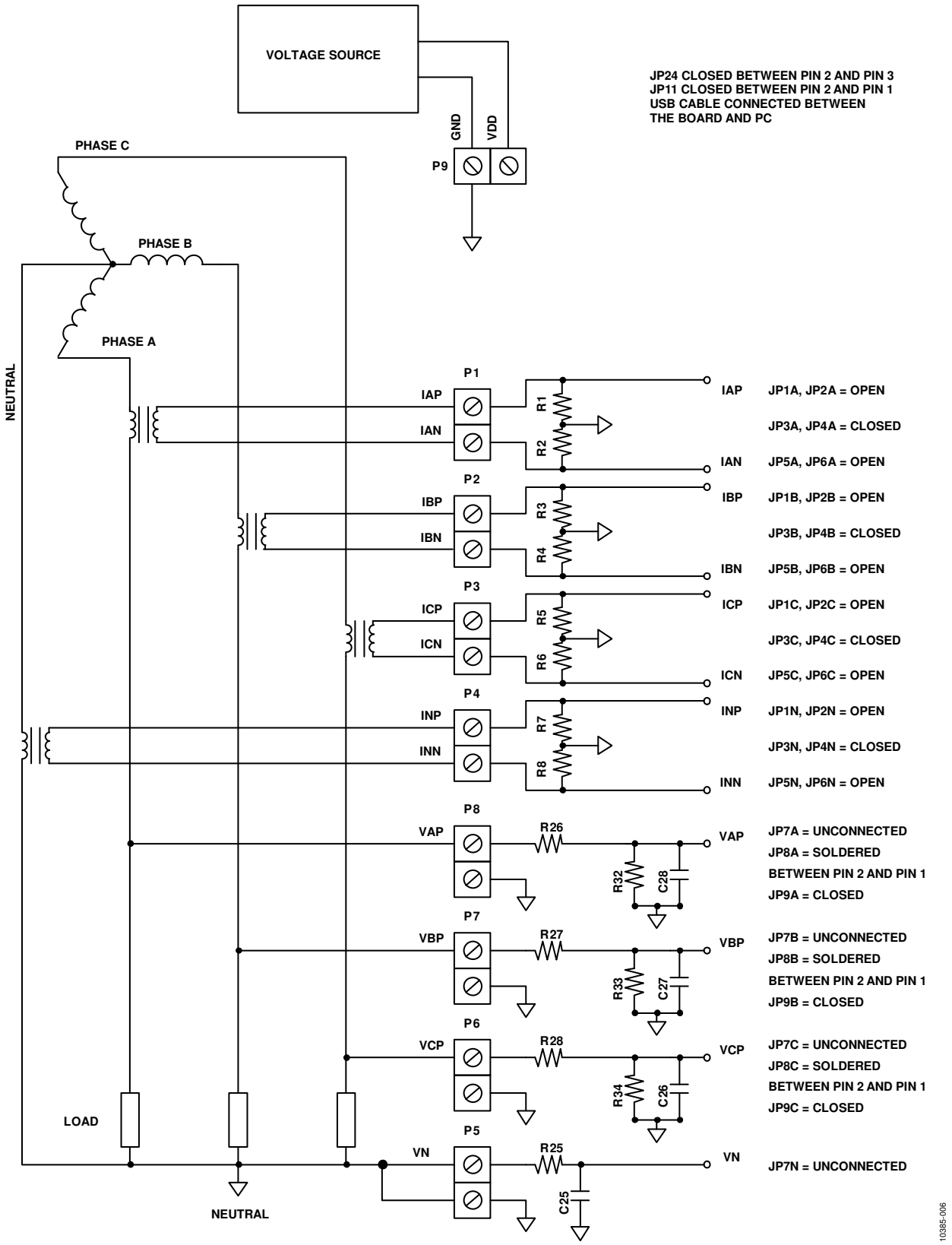
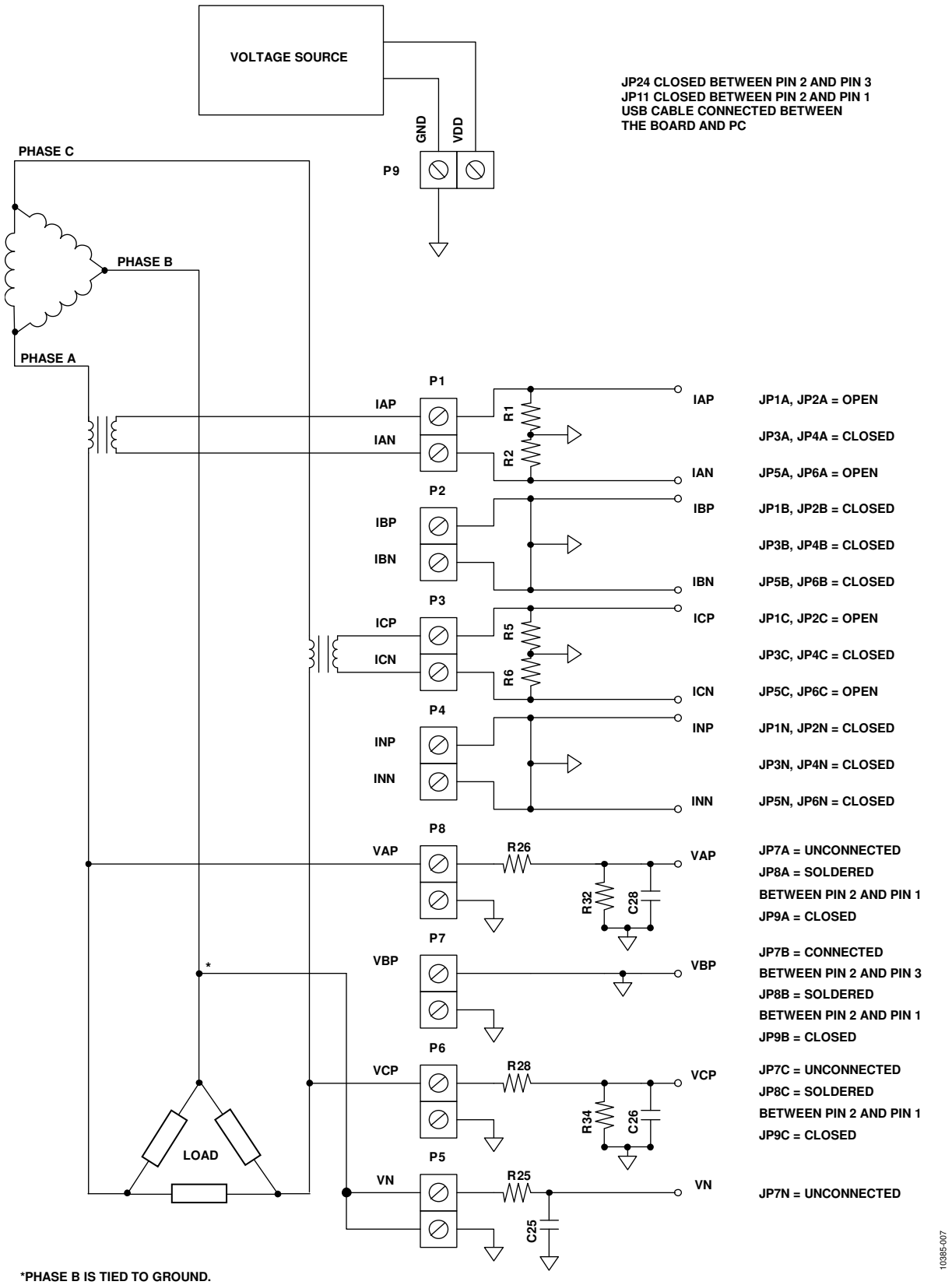


Figure 6. Typical Setup for the ADE7854A/ADE7858A/ADE7868A/ADE7878A Evaluation Board for 3-Phase, 4-Wire, Wye Distribution Systems



*PHASE B IS TIED TO GROUND.

Figure 7. Typical Setup for the ADE7854A/ADE7858A/ADE7868A/ADE7878A Evaluation Board for 3-Phase, 3-Wire, Delta Distribution Systems

EVALUATION BOARD SOFTWARE

The EVAL-ADE7878AEBZ is supported by Windows based software that allows the user to access all the functionality of the IC. The software communicates with the NXP LPC2368 microcontroller using the USB as a virtual COM port. The NXP LPC2368 communicates with the ADE7854A/ADE7858A/ADE7868A/ADE7878A to process the requests that are sent from the PC.

INSTALLING AND UNINSTALLING THE ADE7854A/ADE7858A/ADE7868A/ADE7878A SOFTWARE

The ADE7854A/ADE7858A/ADE7868A/ADE7878A software, downloadable from the product website, includes two projects: one that represents the NXP LPC2368 project and a LabVIEW™ based program that runs on the PC. The NXP LPC2368 project is already loaded into the processor, but the LabVIEW based program must be installed.

1. To install the software, open **LabView_project\installation_files\setup.exe**. This launches the setup program that automatically installs all the software components, including the uninstall program, and creates the required directories.
2. To launch the software, go to the **Start/Programs/ ADE7854A/ADE7858A/ADE7868A/ADE7878A Eval Software** menu and click **ADE7854A/ADE7858A/ADE7868A/ADE7878A Eval Software**.

Both the evaluation software program and the NI run-time engine are easily uninstalled by using the **Add/Remove Programs** option in the Control Panel.

1. Before installing a new version of the evaluation software, first uninstall the previous version.
2. Select the **Add/Remove Programs** option in the Windows Control Panel.
3. Select the program to uninstall and click the **Add/Remove** button.

FRONT PANEL

When the software is launched, the Front Panel is opened. This panel contains two panes. The left pane shows the communication selector and the main menu options. The right pane shows all the submenu options along with the indicators that show the COM port, the firmware version downloaded to the microcontroller, and the IC on the board (see Figure 8).

When you run the software, the COM port and the firmware version indicators are populated first. The COM port box displays the port that matches the echo function communication protocol (see the Managing the Communication Protocol section)and then sets it to 115,200 baud, eight data bits, no parity, no flow control, one stop bit.

Serial communication between the microcontroller and the ADE7854A/ADE7858A/ADE7868A/ADE7878A is then introduced using a switch. By default, the SPI port is used. Note that the active serial port must first be set in the hardware. See the Activating Serial Communication Between the IC and the NXP LPC2368 section for details on how to set it up. Once this is set up, the indicator box showing the IC on board is populated.

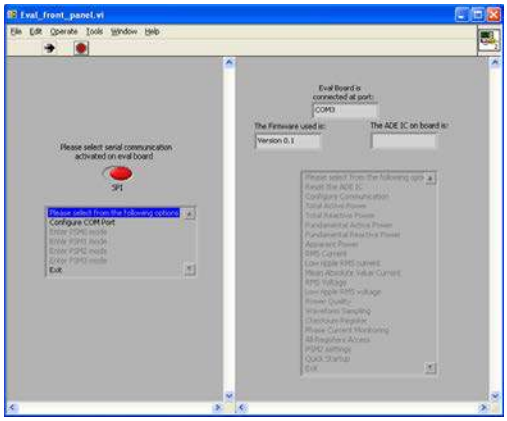


Figure 8. Front Panel of Software

When the chip is detected, the next main menu options are enabled. These options allow you to command the ADE7854A/ADE7858A/ADE7868A/ADE7878A in either PSM0 or PSM3 power mode. The other power modes, PSM1 and PSM2, are not available because initializations have to be made in PSM0 before the device can be used in one of these other modes.

Once the power mode main menu option is selected, the corresponding selectable options are enabled in the submenu category on the right pane.

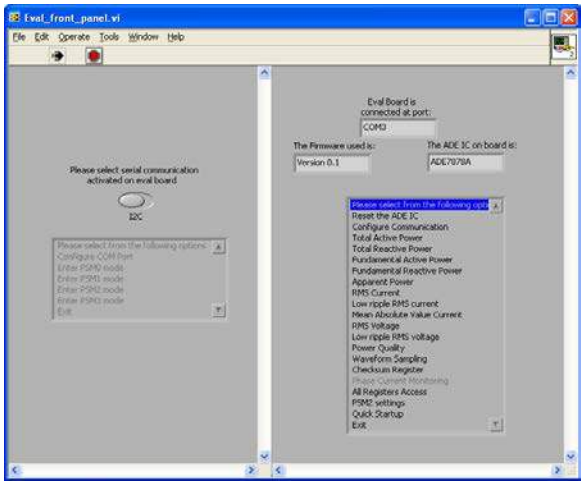


Figure 9. Front Panel After PSMO Mode is Selected

PSM0 MODE—NORMAL POWER MODE

Enter PSM0 Mode

When the evaluation board is powered up, the device is in PSM3 sleep mode. When **Enter PSM0 mode** is selected, the microcontroller manipulates the PM0 and PM1 pins of the ADE7854A/ADE7858A/ADE7868A/ADE7878A to switch it into PSM0 mode and the Front Panel windows appears (see Figure 9). It waits 50 ms for the circuit to power up, and, if SPI communication is activated on the board, it executes three SPI write operations to Address 0xEBFF of the ADE7854A/ADE7858A/ADE7868A/ADE7878A to activate the SPI port.

If the operation has been correctly executed or I²C communication is used, the message **Configuring LPC2368—ADE7854A/ADE7858A/ADE7868A/ADE7878A communication was successful** is displayed, and you must click **OK** to continue. The only error that may occur during this operation is communication related; if this happens, the following message is displayed: **Configuring LPC2368—ADE7854A/ADE7858A/ADE7868A/ADE7878A communication was not successful. Please check the communication between the PC and ADE7854A/ADE7858A/ADE7868A/ADE7878A evaluation board and between LPC2368 and ADE78xxA**.

Bit 1 (I2C_LOCK) of the CONFIG2[7:0] register is now set to 1 to lock in the serial port choice. Then, the DICOEFF register is initialized with 0xFF8000, and the DSP of the ADE7854A/ADE7858A/ADE7868A/ADE7878A is started when the software program writes **RUN = 0x1**. At the end of this process, the entire main menu is grayed out, and the submenu is enabled. You can now manage all functionality of the IC in PSM0 mode.

To switch the ADE7854A/ADE7858A/ADE7868A/ADE7878A to another power mode, click **Exit** on the submenu. The state of the Front Panel is shown in Figure 10.

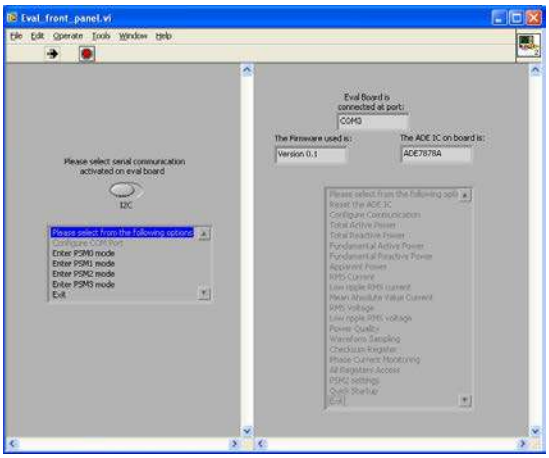


Figure 10. Front Panel Showing All Mode Selection Options

Reset the ADE7854A/ADE7858A/ADE7868A/ADE7878A

When **Reset ADE78xxA** is selected on the Front Panel, the $\overline{\text{RESET}}$ pin of the ADE7854A/ADE7858A/ADE7868A/ADE7878A is kept low for 20 ms and then is set high. If the operation is correctly executed, the message **ADE7854A/ADE7858A/ADE7868A/ADE7878A was reset successfully** is displayed, and you must click **OK** to continue. The only error that may occur during this operation is communication related; if this happens, the following message is displayed: **The communication between PC and ADE7854A/ADE7858A/ADE7868A/ADE7878A evaluation board or between LPC2368 and ADE78xxA did not function correctly. There is no guarantee the reset of ADE7854A/ADE7858A/ADE7868A/ADE7878A has been performed.**

Configure Communication

When **Configure Communication** is selected on the Front Panel, the panel shown in Figure 11 opens. This panel is useful if an ADE7854A/ADE7858A/ADE7868A/ADE7878A reset has been performed and the SPI is no longer the active serial port. Select the SPI port by clicking the **I2C/SPI Selector** and then click **OK** to update the selection and lock the port. This submenu is also useful to switch the active communication port from SPI to I²C.

If the port selection is successful, the message **Configuring LPC2368—ADE7854A/ADE7858A/ADE7868A/ADE7878A communication was successful** is displayed, and you must click **OK** to continue.

If a communication error occurs, the message, **Configuring LPC2368—ADE7854A/ADE7858A/ADE7868A/ADE7878A communication was not successful. Please check the communication between the PC and ADE7854A/ADE7858A/ADE7868A/ADE7878A evaluation board** is displayed.

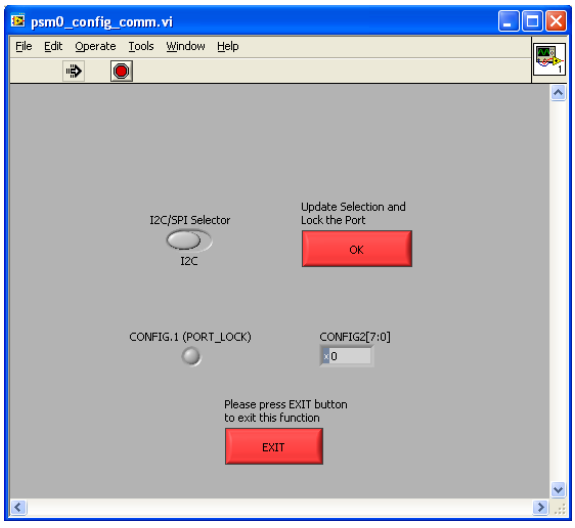


Figure 11. Configure Communication Panel

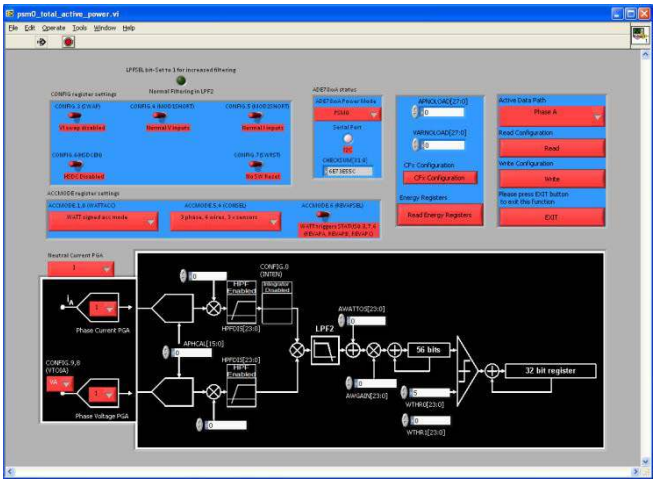
The CONFIG2[7:0] register is written with Bit 1 (I2C_LOCK) set to 1 so that you do not need to remember to set it once the

communication is set. The contents of CONFIG2[7:0] are then read back and displayed with Bit 1 (I2C_LOCK).

To close the panel, click **Exit**; the cursor is now at **Please select from the following options** in the submenu of the Front Panel.

Total Active Power

When **Total Active Power** is selected on the Front Panel, the panel shown in Figure 12 is opened. The screen has an upper half and a lower half: the lower half shows the total active power datapath of one phase, and the upper half shows bits, registers, and commands necessary to power management.

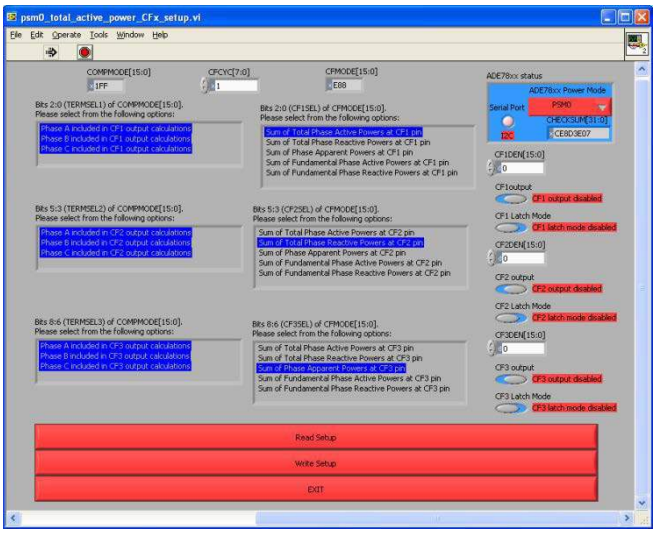


11403-012

Figure 12. Total Active Power Panel

Active Data Path manages which datapath is shown in the bottom half. Some registers or bits, like the WTHR0[23:0] register or Bit 0 (INTEN) of the CONFIG[15:0] register, are common to all datapaths, independent of the phase shown. When these registers are updated, all the values in all datapaths are updated. The HPFDIS[23:0] register is included twice in the datapath, but only the register value from the current datapath is written into the device. All the other instances take this value directly.

1. Click **Read Configuration** to read and display all registers that manage the total active power. Registers from the inactive datapaths are also read and updated.
2. Click **Write Configuration** to write all registers that manage the total active power into the ADE7854A/ADE7858A/ADE7868A/ADE7878A. Registers from the inactive datapaths are also written. The **ADE78xxA status** box shows which power mode the IC is in (it should always be PSM0 in this window), the active serial port (it should always be SPI), and the CHECKSUM[31:0] register. After every read and write operation, the CHECKSUM[31:0] register is read and its contents displayed.
3. Click **CFx Configuration** to open a new panel (see Figure 13). This panel gives access to all bits and registers that configure the CF1, CF2, and CF3 outputs of the ADE7854A/ADE7858A/ADE7868A/ADE7878A. **Read Setup** and **Write Setup** update and display the CF1, CF2, and CF3 output values.



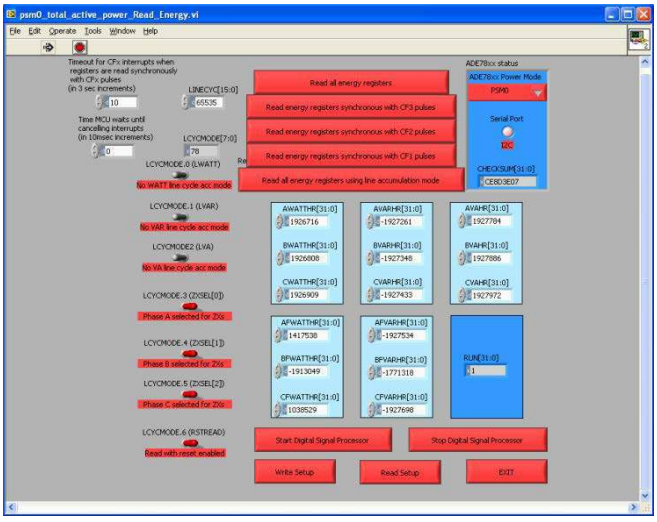
11403-013

Figure 13. CFx Configuration Panel

Like the **Total Active Power** panel, the CHECKSUM[31:0] register is read back whenever a read or write operation is executed in the **CFx Configuration** panel. To select more than one option for a TERMSELx bit in the COMPMODE [15:0] register, press the **CTRL** key while clicking the options you want. Note that a special select bit, the LPFSEL bit of the CONFIG_A register, is made available for ICs datapath; when set, this bit enables a stronger filter for power calculations.

Clicking **EXIT** closes the panel and redisplays the **Total Active Power** panel. When the **Read Energy Registers** button in the **Total Active Power** panel is clicked, a new panel is opened (see Figure 14). This panel gives access to bits and registers that configure the energy accumulation. The **Read Setup** and **Write Setup** buttons update and display the bit and register values.

The CHECKSUM[31:0] register is read back whenever a read or write operation is executed in the **Read Energy Registers** panel. Clicking **Read all energy registers** causes all energy registers to be read immediately, without regard to the modes in which they function.



11403-014

Figure 14. Read Energy Registers Panel

The panel also gives the choice of reading the energy registers synchronous to CFx interrupts (pulses) or using line cycle accumulation mode. When **Read energy registers synchronous with CF1 pulses** is clicked, the following sequence occurs:

1. The STATUS0[31:0] register is read and then written back so that all nonzero interrupt flag bits are cancelled.
2. Bit 14 (CF1) in the MASK0[31:0] register is set to 1, and the interrupt protocol is started (see the Managing the Communication Protocol section for protocol details).
3. The microcontroller then waits until the $\overline{\text{IRQ0}}$ pin goes low. If the wait is longer than the timeout indicated in 3 sec increments, the following error message is displayed: **No CF1 pulse was generated. Verify all the settings before attempting to read energy registers in this mode!**
4. When the $\overline{\text{IRQ0}}$ pin goes low, the STATUS0[31:0] register is read and written back to cancel Bit 14 (CF1); then the energy registers involved in the CF1 signal are read and their contents are displayed. A timer in 10 ms increments can be used to measure the reaction time after the $\overline{\text{IRQ0}}$ pin goes low.
5. The operation is repeated until the button is clicked again.

The process is similar when the other CF2, CF3, and line accumulation (**Read Energy Registers** panel) buttons are clicked.

It is recommended to always use a timeout when dealing with interrupts. By default, the timeout is set to 10 (indicating a 30 sec timeout), and the timer is set to 0 (indicating that the STATUSx[31:0] and energy registers are read immediately after the $\overline{\text{IRQ0}}$ pin goes low).

When clicking on the Front Panel, the **Total Reactive Power**, **Fundamental Active Power**, and **Fundamental Reactive Power** buttons open panels that are very similar to the **Total Active Power** panel. These panels are shown in Figure 15, Figure 16, and Figure 17.

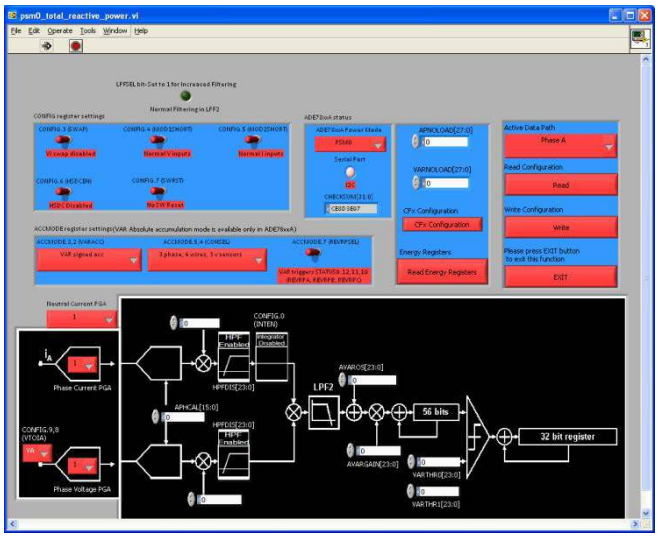


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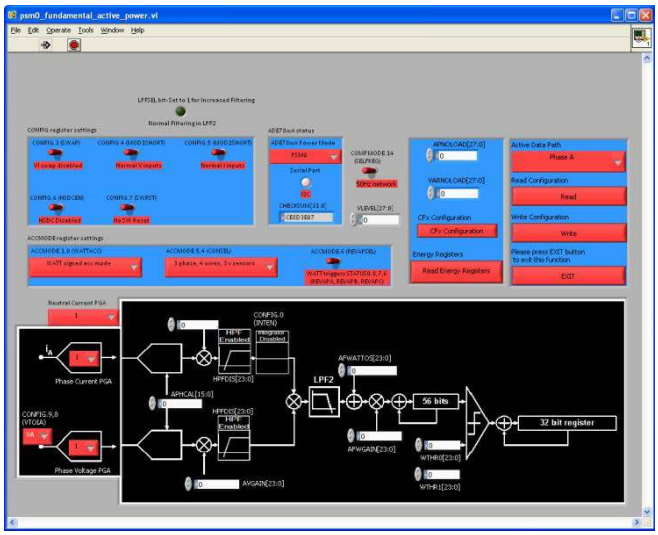
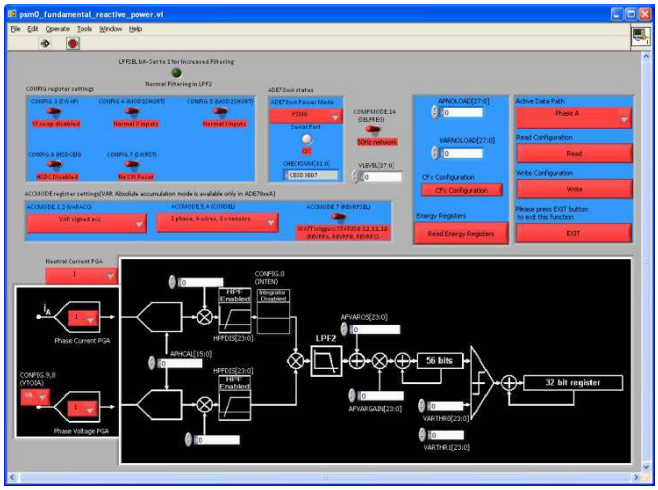
Figure 15. Total Reactive Power Panel



11403-016

Figure 16. Fundamental Active Power Panel

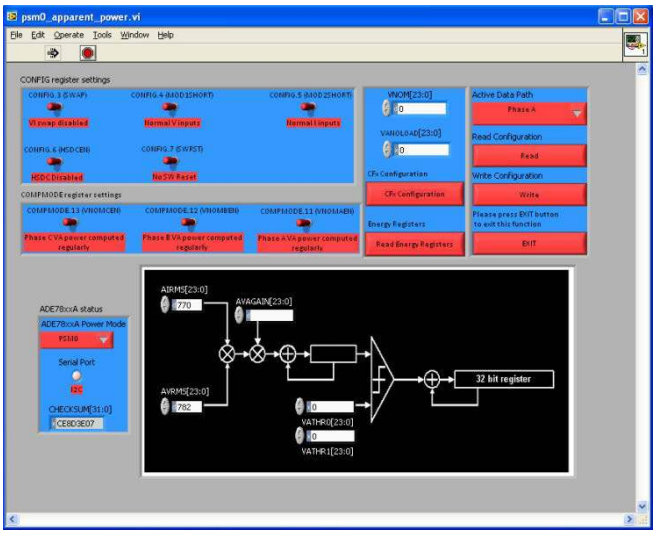


11403-017

Figure 17. Fundamental Reactive Power Panel

Apparent Power

When **Apparent Power** is selected on the Front Panel, a new panel opens (see Figure 18). Similar to the other panels that deal with power measurement, this panel is divided into two parts: the lower half shows the apparent power datapath of one phase and the ADE7854A/ADE7858A/ADE7868A/ADE7878A status; the upper half shows the bits, registers, and commands necessary to power management.



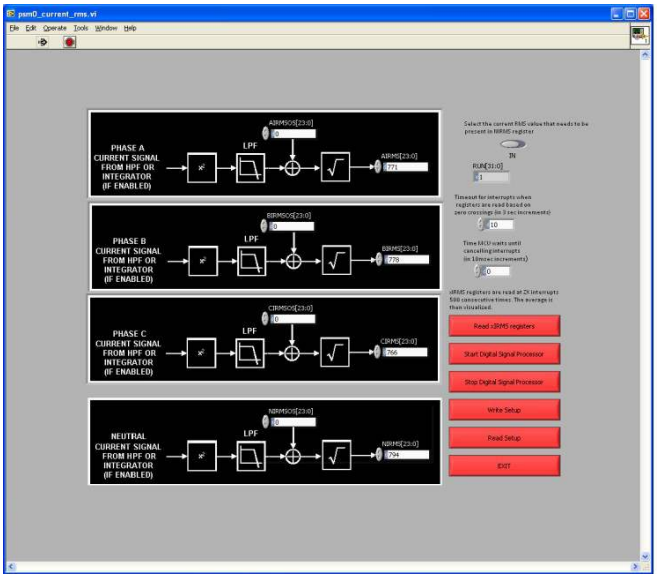
11403-018

Figure 18. Apparent Power Panel

Current RMS

When **RMS Current** is selected on the Front Panel, a new panel is opened (see Figure 19). All datapaths of all phases are available.

There is a special select bit that is made available for ADE7868A/ADE7878A parts called the INSEL bit of the CONFIG_A register. Setting this bit calculates and routes the sum value of all phase currents to the NIRMS register, which would otherwise be displaying the neutral channel current.



11403-019

Figure 19. Current RMS Panel

Clicking the **Read Setup** button causes a read of all registers shown in the panel. Clicking the **Write Setup** button causes writes to the xIRMSOS[23:0] registers.

You can use the **Start Digital Signal Processor** and **Stop Digital Signal Processor** buttons to manage the Run[15:0] register. You can use and the **Read xIRMS registers** button, which uses the ZXIA, ZXIB, and ZXIC interrupts at the $\overline{\text{IRQ1}}$ pin, to read the xIRMS[23:0] registers 500 consecutive times and then computes and displays their average. If no interrupt occurs for the time indicated by the timeout (in 3 sec increments), the following message is displayed: **No ZXIA, ZXIB or ZXIC interrupt was generated. Verify at least one sinusoidal signal is provided between IAP-IAN, IBP-IBN or ICP-ICN pins**. A delay can be introduced (in 10 ms increments) between the time the $\overline{\text{IRQ1}}$ pin goes low and the moment the xIRMS registers are read. The operation is repeated until the button is clicked again.

The **Low ripple RMS current** submenu is also quite similar to the regular RMS current, in terms of window display. These low ripple registers update every 1.024 second and contain an averaged version of the regular current RMS data. Internally, 8192 averages are performed to get a single low ripple RMS measurement.

Mean Absolute Value Current

When **Mean Absolute Value Current** is selected on the Front Panel, a new panel is opened (see Figure 20). When the **Read xIMAV registers** button is clicked, the xIMAV[19:0] registers are read 10 consecutive times, and their average is computed and displayed. After this operation, the button is returned to high automatically. The ADE7854A/ADE7858A/ADE7868A/ADE7878A status is also displayed.

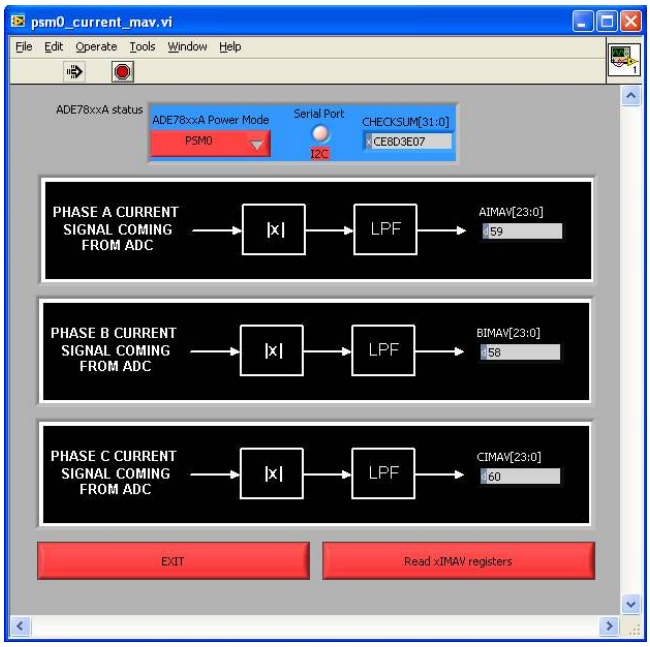


Figure 20. Mean Absolute Value Current Panel

Voltage RMS

When **RMS Voltage** is selected on the Front Panel, the **Voltage RMS** panel is opened (see Figure 21). This panel is very similar to the **Current RMS** panel. Clicking the **Read Setup** button executes a read of the xVRMSOS[23:0] and xVRMS[23:0] registers.

Clicking **Write Setup** writes the xVRMSOS[23:0] registers into the ADE7854A/ADE7858A/ADE7868A/ADE7878A. The **Start Digital Signal Processor** and **Stop Digital Signal Processor** buttons manage the Run[15:0] register.

When the **Read xVRMS registers** button is clicked, the xVRMS[23:0] registers are read 500 consecutive times and the average is displayed. The operation is repeated until the button is clicked again. Note that the ZXVA, ZXVB, and ZXVC zero-crossing interrupts are not used in this case because they are disabled when the voltages go below 10% of full scale. This allows rms voltage registers to be read even when the phase voltages are very low.

The **Low ripple RMS voltage** submenu is also quite similar to the regular rms voltage, in terms of window display. These low ripple registers update every 1.024 second and contain an averaged version of the regular voltage rms data. Internally, 8192 averages are performed to get a single low ripple rms measurement.

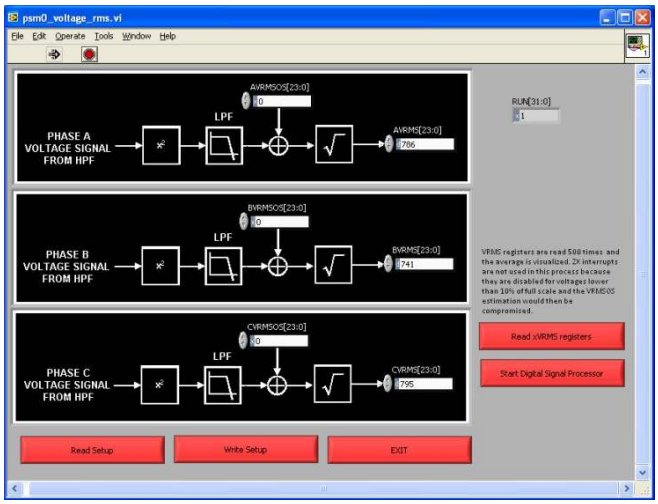


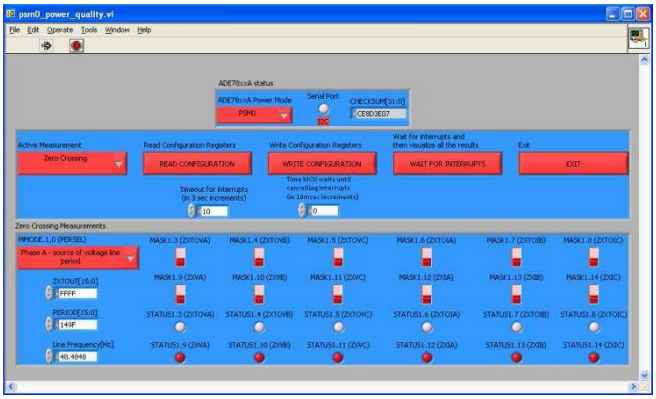
Figure 21. Voltage RMS Panel

Power Quality

The **Power Quality** panel is accessible from the Front Panel and is divided into two parts (see Figure 22). The lower part displays registers that manage the power quality measurement functions for the **Active Measurement** button in the upper part of the panel. The upper part also displays the ADE7854A/ADE7858A/ADE7868A/ADE7878A status and the buttons that manage the measurements.

When the **READ CONFIGURATION** button is clicked, all power quality registers (MASK1[31:0], STATUS1[31:0], PERIOD[15:0], MMODE[7:0], ISUM[27:0], OVLVL[23:0], OILVL[23:0], PHSTATUS[15:0], IPEAK[31:0], VPEAK[31:0], SAGLVL[23:0], SAGCYC[7:0], ANGLE0[15:0], ANGLE1[15:0], ANGLE2[15:0], COMPMODE[15:0], CHECKSUM[31:0], and PEAKCYC[7:0]) are read, and the ones belonging to the active panel are displayed. Based on the PERIOD[15:0] register, the line frequency is computed and displayed in the lower part of the panel, in **Zero Crossing Measurements**. Based on the ANGLEx[15:0] registers, cos(ANGLEx) is computed and displayed in the **Time Intervals Between Phases** panel that is accessible from the **Active Measurement Zero Crossing** drop-down box (see Figure 22).

When the **WRITE CONFIGURATION** button is clicked, MMODE[7:0], OVLVL[23:0], OILVL[23:0], SAGLVL[23:0], SAGCYC[7:0], COMPMODE[15:0], and PEAKCYC[7:0] are written into the ADE7854A/ADE7858A/ADE7868A/ADE7878A, and CHECKSUM[31:0] is read back and displayed in the CHECKSUM[31:0] box at the top of the upper part of the panel.



11403-022

Figure 22. Power Quality Zero-Crossing Measurements Panel

When the **WAIT FOR INTERRUPTS** button is clicked, the interrupts that you have enabled in the MASK1[31:0] register are monitored. When the $\overline{\text{IRQ1}}$ pin goes low, the STATUS1[31:0] register is read and its bits are displayed. The ISUM[27:0], PHSTATUS[15:0], IPEAK[31:0], VPEAK[31:0], ANGLE0[15:0], ANGLE1[15:0], and ANGLE2[15:0] registers are also read and displayed. A timeout should be introduced in 3 sec increments to ensure that the program does not wait indefinitely for interrupts. A timer (in 10 ms increments) is provided to allow reading of the registers with a delay from the moment the interrupt is triggered.

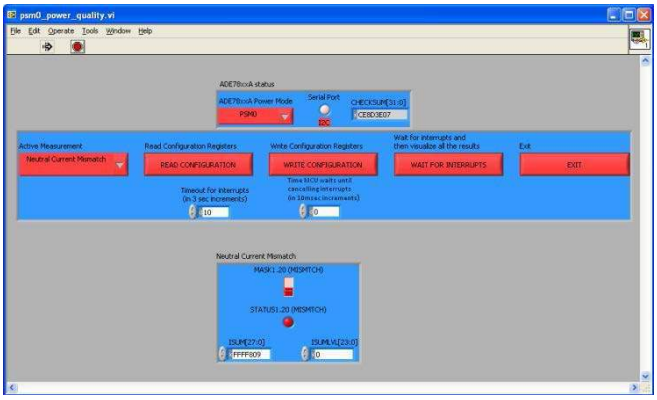
The **Active Measurement Zero Crossing** button gives access to the **Zero Crossing**, **Neutral Current Mismatch**, **Overvoltage and Overcurrent Measurement**, **Peak Detection**, and **Time Intervals Between Phases** panels (see Figure 22 through Figure 26).

The line frequency is computed using the PERIOD[15:0] register, based on the following formula:

$$f = \frac{256{,}000}{Period}[Hz]$$

The cosine of the ANGLE0[15:0], ANGLE1[15:0], and ANGLE2[15:0] measurements is computed using the following formula:

$$cos(ANGLEx) = cos\left(\frac{ANGLEx \times 360 \times f}{256{,}000}\right)$$



11403-023

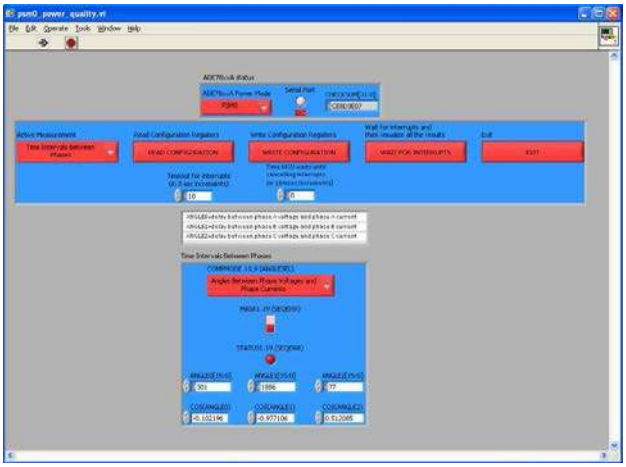
Figure 23. Neutral Current Mismatch Panel

11403-024

Figure 24. Overvoltage and Overcurrent Measurements Panel

11403-025

Figure 25. Peak Detection Panel



11403-026

Figure 26. Time Intervals Between Phases Panel

Waveform Sampling

The **Waveform Sampling** panel (see Figure 27) is accessible from the Front Panel and uses the HSDC port to acquire data from the ADE7854A/ADE7858A/ADE7868A/ADE7878A and display it.

The HSDC port can be accessed only if the communication between the ADE7854A/ADE7858A/ADE7868A/ADE7878A and the NXP LPC2368 is through the I^2C. See the Activating Serial Communication Between the IC and the NXP LPC2368 section for details on how to set I^2C communication on the evaluation board.

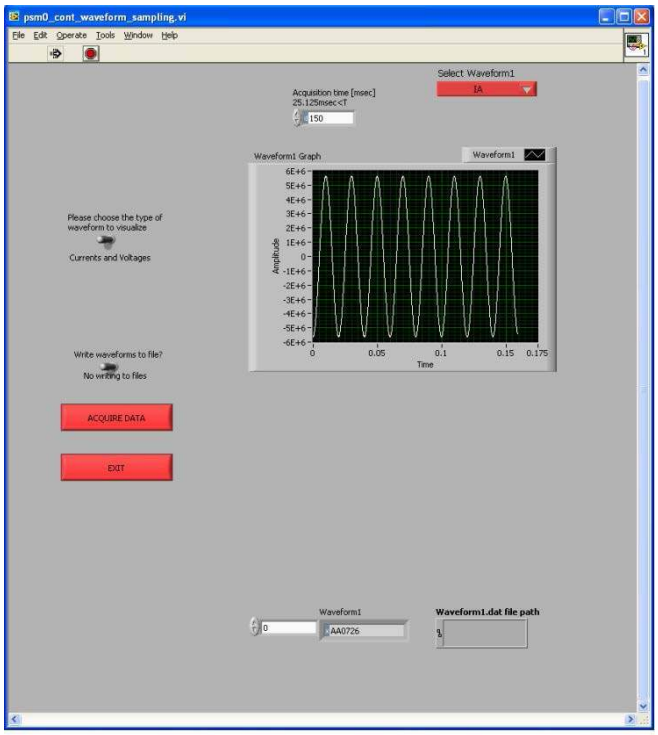


Figure 27. Waveform Sampling Panel

The HSDC transmits data to the NXP LPC2368 at 4 MHz because this is the maximum speed at which the slave SPI of the NXP LPC2368 can receive data. The panel contains some switches that must be set before acquiring data.

- One switch chooses the quantities that are displayed: phase currents and voltages or phase powers. For every set of quantities, only one can be acquired at a time. This choice is made using the **Select Waveform** button.
- A second switch allows acquired data to be stored in files for further use. This switch is set with the **ACQUIRE DATA** button.
- The acquisition time should also be set before an acquisition is ordered. By default, this time is 150 ms. It is unlimited for phase currents and voltages and for phase powers. The NXP LPC2368 executes in real time three tasks using the ping-pong buffer method: continuously receiving data from HSDC, storing the data into its USB memory, and sending the data to the PC. Transmitting seven phase currents and voltages at 4 MHz takes 103.25 µs (which is less than 125 µs); therefore, the HSDC update rate is 8 kHz (HSDC_CFG = 0x0F). Transmitting nine phase powers takes 72 µs (again, less than 125 µs); therefore, the HSDC update rate is also 8 kHz (HSDC_CGF = 0x11).

To start the acquisition, click the **ACQUIRE DATA** button. The data is displayed on one plot. If you click the **Write waveforms to file?/No writing to files** switch to enable the writing of waveforms to a file, the program asks for the name and location of the files before storing the waveform.

Checksum Register

The **Checksum Register** panel is accessible from the Front Panel and gives access to all ADE7854A/ADE7858A/ADE7868A/ADE7878A registers used to compute the CHECKSUM[31:0] register (see Figure 28). You can read/write the values of these registers by clicking the **Read** and **Write** buttons. The LabView program estimates the value of the CHECKSUM[31:0] register and displays it whenever one of the registers is changed. When the **Read** button is pressed, the registers are read and the CHECKSUM[31:0] register is read and its values displayed. This allows you to compare the value of the CHECKSUM[31:0] register estimated by LabView with the value read from the parts. The values should always be identical, after the setup is read.

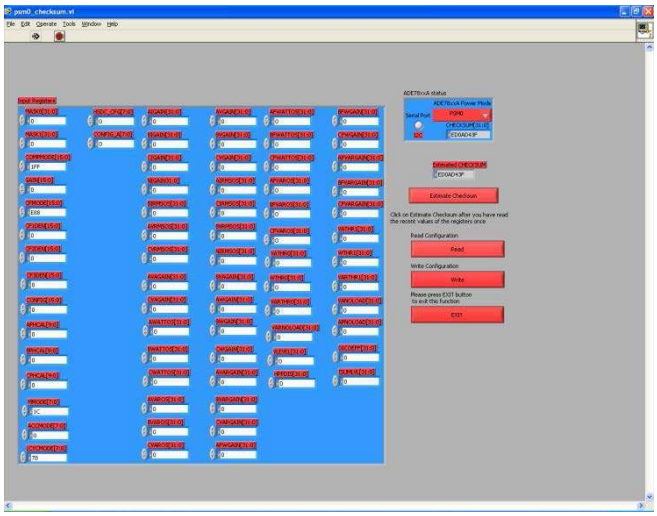


Figure 28. Checksum Register Panel

All Registers Access

The **All Registers Access** panel provides access to the ADE7854A/ADE7858A/ADE7868A/ADE7878A registers. Because there are many, the panel can be scrolled up and down and has multiple read, write, and exit buttons (see Figure 29 and Figure 30).

The registers are listed in columns in alphabetical order, starting at the upper left, except for the new registers, which are displayed at the end.

The panel also allows you to save all control registers into a data file by clicking the **Save All Regs into a file** button. By clicking the **Load All Regs from a file** button, you can load all control registers from a data file. Then, by clicking the **Write All Regs** button, you can load these values into the IC. The order in which the registers are stored into a file is shown in the Control Registers Data File section.

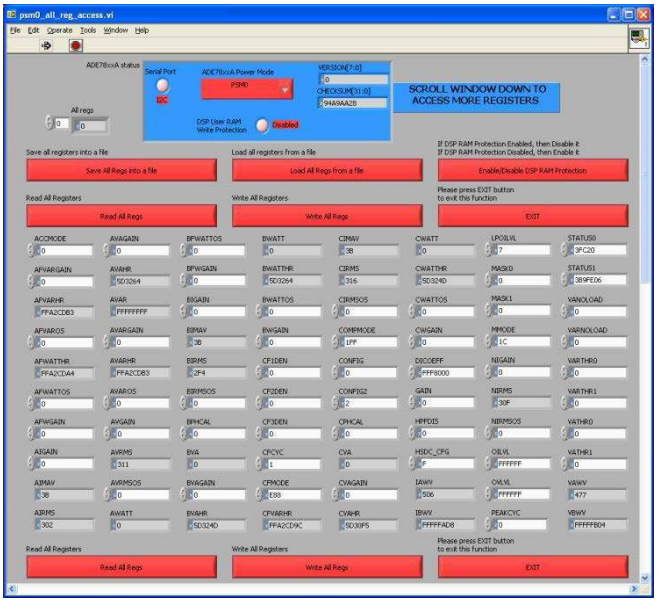


Figure 29. Panel Giving Access to All Registers (1)

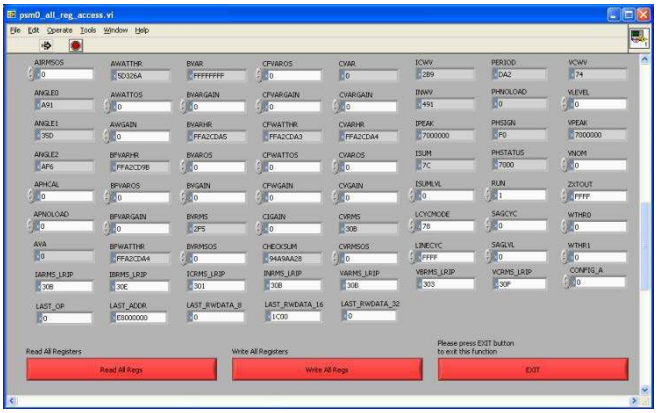


Figure 30. Panel Giving Access to All Registers (2)

Quick Startup

The **Quick Startup** panel, accessible from the Front Panel, can be used to rapidly initialize a 3-phase meter (see Figure 31).

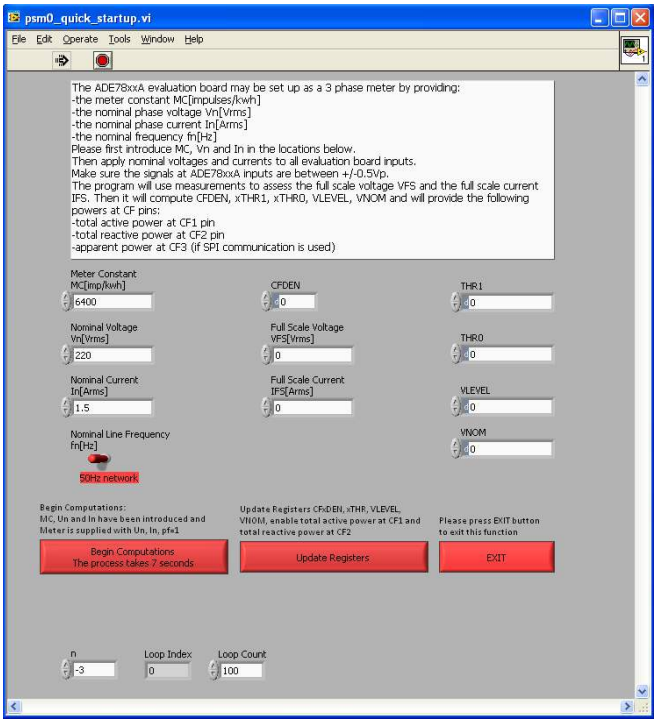


Figure 31. Panel Used to Quickly Set Up the 3-Phase Meter

The meter constant (MC, in impulses/kWh), the nominal voltage (Un, in V rms units), the nominal current (In, in A rms units), and the nominal line frequency (fn, in either 50 Hz or 60 Hz) must be introduced in the panel controls. Then phase voltages and phase currents must be provided through the relative sensors.

Clicking the **Begin Computations** button starts the program that reads rms voltages and currents and calculates the full-scale voltage and currents used to further initialize the meter. This process takes 7 seconds as the program reads the rms voltages 100 times and the rms currents 100 times, and then averages them (this is because the PC reads the rms values directly and cannot synchronize the readings with the zero crossings).

The program then computes the full-scale voltages and currents and the constants that are important for setting up the ADE7854A/ADE7858A/ADE7868A/ADE7878A: nominal values (n), CFDEN, WTHR1, VARTHR1, VATHR1, WTHR0, VARTHR0, and VATHR0.

At this point, you can overwrite these values. You can also click the **Update Registers** button to cause the program to do the following:

- Initialize the CFxDEN and xTHR registers
- Enable the CF1 pin to provide a signal proportional to the total active power, enable the CF2 pin to provide a signal proportional to the total reactive power, and enable the CF3 pin to provide a signal proportional to the apparent power.

Throughout the program, it is assumed that PGA gains are 1 (for simplicity) and that the Rogowski coil integrators are disabled. You can enter and modify the PGAs and enable the integrators before executing this quick startup, if necessary.

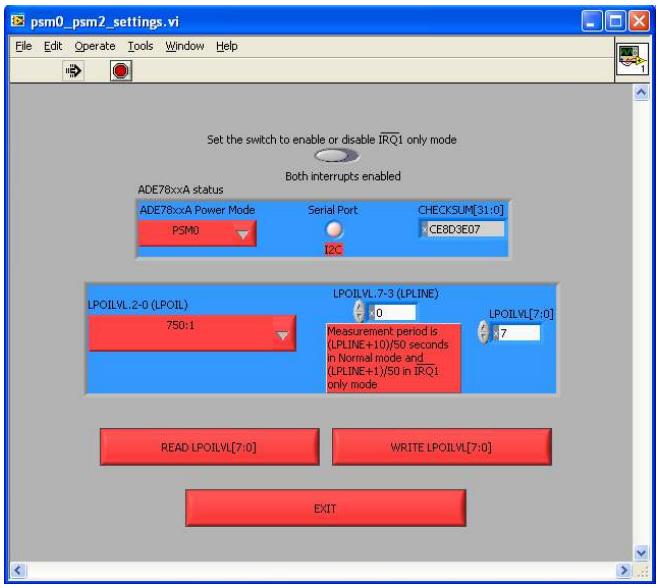
At this point, the evaluation board is set up as a 3-phase meter, and calibration can be executed. To store the register initializations, click the **Save All Regs into a file** button in the **All Registers Access** panel.

After the board is powered down and then powered up again, the registers can be loaded into the ADE7854A/ADE7858A/ADE7868A/ADE7878A by simply loading back the content of the data file. To do this, click the **Load All Regs from a file** button in the **All Registers Access** panel.

PSM2 Settings

The **PSM2 Settings** panel, which is accessible from the Front Panel, gives access to the LPOILVL[7:0] register that is used to access PSM2 low power mode (see Figure 32). You can manipulate its LPOIL[2:0] and LPLINE[4:0] bits. The value shown in the LPOILVL[7:0] register is composed from these bits and then displayed. Note that you cannot write a value into the register by writing a value in the LPOILVL[7:0] register box.

You can select the PSM2 $\overline{\text{IRQ1}}$ only mode by selecting the appropriate control available. Doing so pulls $\overline{\text{IRQ0}}$ to high always and $\overline{\text{IRQ1}}$ alone would determine if a tamper condition occurs.



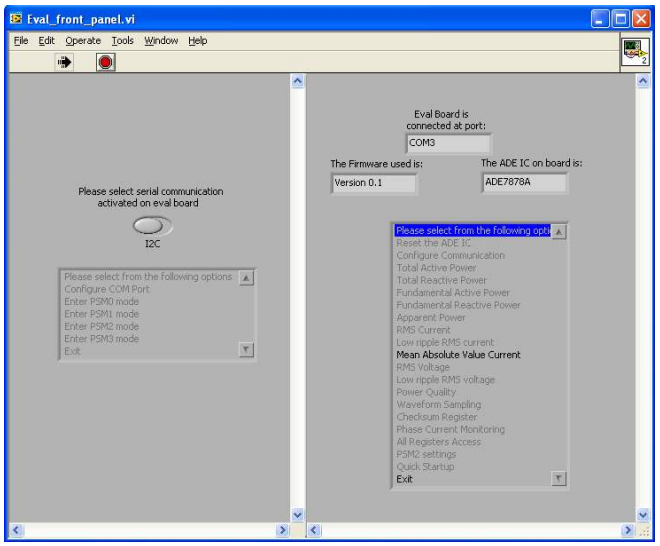
11403-032

Figure 32. PSM2 Settings Panel

PSM1 MODE

Enter PSM1 Mode

When **Enter PSM1 mode** is selected on the Front Panel, the microcontroller manipulates the PM0 and PM1 pins of the ADE7868A/ADE7878A to switch the ADE7868A/ADE7878A into PSM1 reduced power mode. Then, the submenu allows access only to the **Mean Absolute Value Current** function because this is the only ADE7868A/ADE7878A functionality available in this reduced power mode (see Figure 33).



11403-033

Figure 33. Front Panel After the IC Enters PSM1 Mode

Mean Absolute Value Current in PSM1 Mode

The **Mean Absolute Value Current** panel, which is accessible from the Front Panel when **Enter PSM1 mode** is selected, is very similar to the panel accessible in PSM0 mode (see the Mean Absolute Value Current section for details). The only difference is that **ADE7868A/ADE7878A status** does not show the CHECKSUM[31:0] register because it is not available in PSM1 mode (see Figure 34).

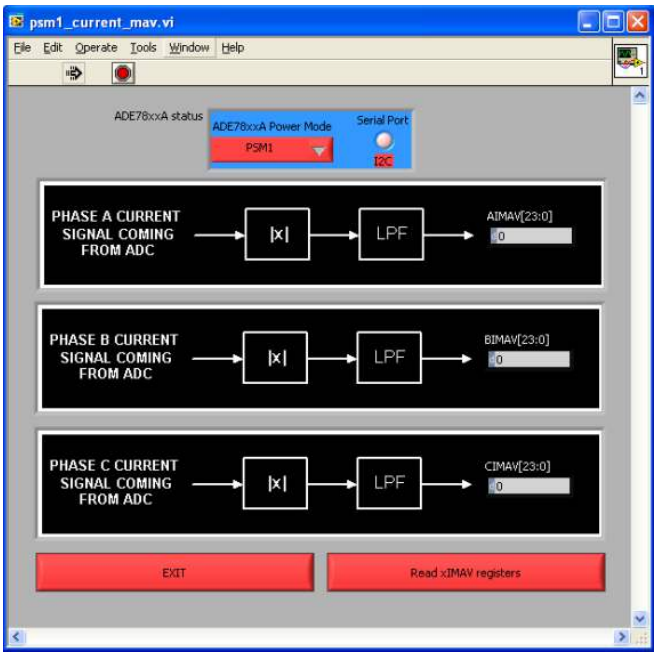


Figure 34. Mean Absolute Value Currents Panel in PSM1 Mode

PSM2 MODE

Enter PSM2 Mode

When **Enter PSM2 mode** is selected on the Front Panel, the microcontroller manipulates the PM0 and PM1 pins of the ADE7868A/ADE7878A to switch the ADE7868A/ADE7878A into PSM2 low power mode. Then, the submenu allows access only to the **Phase Current Monitoring** function because this is the only ADE7868A/ADE7878A functionality available in this low power mode (see Figure 35).

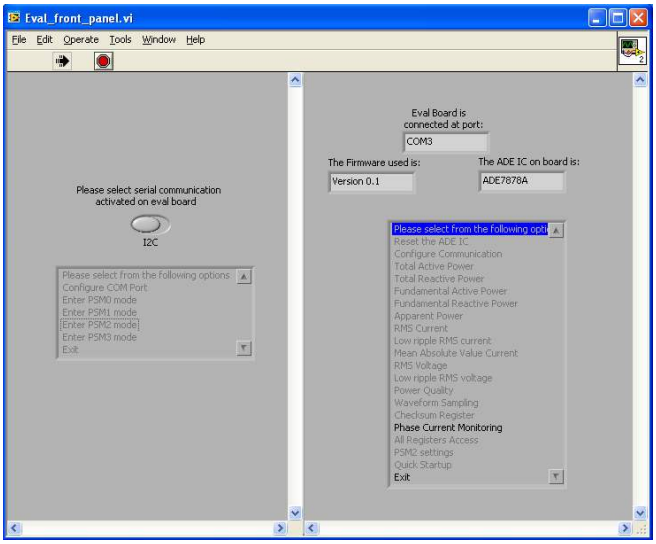


Figure 35. Front Panel After the IC Enters PSM2 Mode

Phase Current Monitoring

The **Phase Current Monitoring** panel is accessible from the Front Panel when **Enter PSM2 mode** is selected; it allows you to display the state of the $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ pins because, in PSM2 low power mode, the ADE7868A/ADE7878A compares the phase currents against a threshold determined by the LPOILVL[7:0] register (see Figure 36). Clicking the **READ STATUS OF $\overline{\text{IRQ0}}$ AND $\overline{\text{IRQ1}}$ PINS** button reads the status of these pins and displays and interprets the status.

You can select the PSM2 $\overline{\text{IRQ1}}$ only mode by selecting the appropriate control from the window. Doing so keeps $\overline{\text{IRQ0}}$ at high always; $\overline{\text{IRQ1}}$ alone determines if a tamper condition occurs.

This Phase Current Monitoring operation is managed by the LPOILVL[7:0] register and can be modified only in PSM0 mode. The panel offers this option by switching the ADE7868A/ADE7878A into PSM0 mode and then back to PSM2 mode when one of the **READ LPOILVL/WRITE LPOILVL** buttons is clicked. To avoid toggling both the PM0 and PM1 pins at the same time during this switch, the ADE7868A/ADE7878A is set to PSM3 when changing modes.

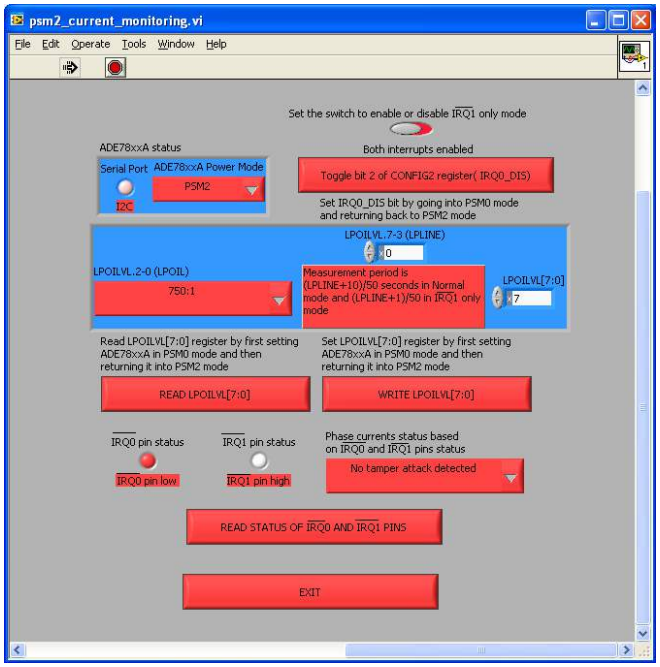


Figure 36. Panel Managing Current Monitoring in PSM2 Mode

PSM3 MODE

Enter PSM3 Mode

In PSM3 sleep mode, most of the internal circuits of the ADE7854A/ADE7858A/ADE7868A/ADE7878A are turned off. Therefore, no submenu is activated while in this mode. You can select the **Enter PSM0 mode**, **Enter PSM1 mode**, or **Enter PSM2 mode** menu options to set the IC to one of these power modes.

MANAGING THE COMMUNICATION PROTOCOL

This sections lists the protocol commands implemented to manage the ADE7854A/ADE7858A/ADE7868A/ADE7878A from the PC using the microcontroller.

The microcontroller is a pure slave during the communication process. It receives a command from the PC, executes the command, and sends an answer to the PC. The PC waits for the answer before sending a new command to the microcontroller.

There are two versions of microcontroller codes for ADE7854A/ADE7858A/ADE7868A/ADE7878A parts: Version 0.0 and Version 0.1. Version 0.0 is the microcontroller code originally written for ADE7854A/ADE7858A/ADE7868A/ADE7878A parts. It can be used with ADE7854A/ADE7858A/ADE7868A/ADE7878A parts as well. Version 0.1, the latest version, reads rms values at zero-crossings thus improving the accuracy of the readings. The evaluation software detects the version of the microcontroller code programmed in the board and makes internal changes accordingly.

Table 3. Echo Command—Message from the PC to the Microcontroller

Byte	Description
0	A = 0x41
1	N = number of bytes transmitted after this byte
2	Data Byte N – 1 (MSB)
3	Data Byte N – 2
4	Data Byte N – 3
…	…
N	Data Byte 1
N + 1	Data Byte 0 (LSB)

Table 4. Echo Command—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52
1	A = 0x41
2	N = number of bytes transmitted after this byte
3	Data byte N – 1 (MSB)
4	Data byte N – 2
…	…
N + 1	Data Byte 1
N + 2	Data Byte 0 (LB)

Table 5. Power Mode Select—Message from the PC to the Microcontroller

Byte	Description
0	B = 0x42, change PSM mode
1	N = 1
2	Data Byte 0: 0x00 = PSM0 0x01 = PSM1 0x02 = PSM2 0x03 = PSM3

Table 6. Power Mode Select—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52
1	~ = 0x7E, to acknowledge that the operation was successful

Table 7. Reset—Message from the PC to the Microcontroller

Byte	Description
0	C = 0x43, toggle the $\overline{\text{RESET}}$ pin and keep it low for at least 10 ms
1	N = 1
2	Data Byte 0: this byte can have any value

Table 8. Reset—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52
1	~ = 0x7E, to acknowledge that the operation was successful

Table 9. I²C/SPI Select (Configure Communication)—Message from the PC to the Microcontroller

Byte	Description
0	D = 0x44, select I²C and SPI and initialize them; then set CONFIG2[7:0] = 0x2 to lock in the port choice. When I²C is selected, also enable SSP0 of the LPC2368 (used for HSDC).
1	N = 1.
2	Data Byte 0: 0x00 = I²C, 0x01 = SPI.

Table 10. I²C/SPI Select (Configure Communication)—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52
1	~ = 0x7E, to acknowledge that the operation was successful

Table 11. Data Write—Message from the PC to the Microcontroller

Byte	Description
0	E = 0x45
1	N = number of bytes transmitted after this byte. N can be 1 + 2, 2 + 2, 4 + 2, or 6 + 2
2	MSB of the address
3	LSB of the address
4	Data Byte N − 3 (MSN)
5	Data Byte N − 4
6	Data Byte N − 5
…	…
N + 2	Data Byte 1
N + 3	Data Byte 0 (LSB)

Table 12. Data Write—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52
1	~ = 0x7E, to acknowledge that the operation was successful

Table 13. Data Read—Message from the PC to the Microcontroller

Byte	Description
0	F = 0x46.
1	N = number of bytes transmitted after this byte; N = 3.
2	MSB of the address.
3	LSB of the address.
4	M = number of bytes to be read from the address above. M can be 1, 2, 4, or 6.

Table 14. Data Read—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52.
1	MSB of the address.
2	LSB of the address.
3	Byte 5, Byte 3, Byte 1, or Byte 0 (MSB) read at the location indicated by the address. The location may contain 6, 4, 2, or 1 byte. The content is transmitted MSB first.
4	Byte 4, Byte 2, or Byte 0.
5	Byte 3, Byte 1.
6	Byte 2, Byte 0.
7	Byte 1.
8	Byte 0.

Table 15. Interrupt Setup—Message from the PC to the Microcontroller

Byte	Description
0	J = 0x4A.
1	N = 8, number of bytes transmitted after this byte.
2	MSB of the MASK1[31:0] or MASK0[31:0] register.
3	LSB of the MASK1[31:0] or MASK0[31:0] register.
4	Byte 3 of the desired value of the MASK0[31:0] or MASK1[31:0] register.
5	Byte 2.
6	Byte 1.
7	Byte 0.
8	Time out byte: time the MCU must wait for the interrupt to be triggered. It is measured in 3 sec increments. Time out byte (TOB) = 0 means that timeout is disabled.
9	IRQ timer: time the MCU leaves the $\overline{\text{IRQx}}$ pin low before writing back to clear the interrupt flag. It is measured in 10 ms increments. Timer = 0 means that timeout is disabled.

Table 16. Interrupt Setup—Message from the Microcontroller to the PC

Byte	Description
0	R = 0x52.
1	Byte 3 of the STATUS0[31:0] or STATUS1[31:0] register. If the program waited for TOB × 3 sec and the interrupt was not triggered, then Byte 3 = Byte 2 = Byte 1 = Byte 0 = 0xFF.
2	Byte 2 of the STATUS0[31:0] or STATUS1[31:0] register.
3	Byte 1 of the STATUS0[31:0] or STATUS1[31:0] register.
4	Byte 0 of the STATUS0[31:0] or STATUS1[31:0] register.

The microcontroller executes the following operations once the interrupt setup command is received:

1. Reads the STATUS0[31:0] or STATUS1[31:0] register (depending on the address received from the PC) and, if it shows an interrupt already triggered (one of its bits is equal to 1), it erases the interrupt by writing it back.
2. Writes to the MASK0[31:0] or MASK1[31:0] register with the value received from the PC.
3. Waits for the interrupt to be triggered. If the wait is more than the timeout specified in the command, 0xFFFFFFFF is sent back.
4. If the interrupt is triggered, the STATUS0[31:0] or STATUS1[31:0] register is read and then written back to clear it. The value read at this point is the value sent back to the PC so that you can see the source of the interrupts.
5. Sends back the answer.

Table 17. Interrupt Pins Status—Message from the PC to the Microcontroller

Byte	Description
0	H = 0x48.
1	N = 1, number of bytes transmitted after this byte.
2	Any byte. This value is not used by the program, but it is used in the communication because N must not be equal to 0.

Table 18. Interrupt Pins Status—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52.
1	A number representing the status of the $\overline{IRQ0}$ and $\overline{IRQ1}$ pins. 0: $\overline{IRQ0}$ = low, $\overline{IRQ1}$ = low. 1: $\overline{IRQ0}$ = low, $\overline{IRQ1}$ = high. 2: $\overline{IRQ0}$ = high, $\overline{IRQ1}$ = low. 3: $\overline{IRQ0}$ = high, $\overline{IRQ1}$ = high. The reason for the $\overline{IRQ0}$ and $\overline{IRQ1}$ order is that on the microcontroller IO port, $\overline{IRQ0}$ = P0.1 and $\overline{IRQ1}$ = P0.0.

ACQUIRING HSDC DATA CONTINUOUSLY

This function acquires data from the HSDC continuously for a defined time period and for up to two variables. The microcontroller sends data in packages of 4 kB.

Table 19 describes the protocol when two instantaneous phase currents or voltages are acquired.

Table 19. Acquire HSDC Data Continuously—Message from the PC to the Microcontroller if Phase Currents and Voltages are Acquired

Byte	Description
0	G = 0x47.
1	N = number of bytes transmitted after this byte. N = 32.
2	0: corresponds to Byte 3 of IA. Because this byte is only a sign extension of Byte 2, it is not sent back by the microcontroller.
3	Increment_IA_Byte2. If IA is to be acquired, Byte 3, Byte 4, and Byte 5 are 1. Otherwise, they are 0.
4	Increment_IA_Byte1.
5	Increment_IA_Byte2.
6	0.
7	Increment_VA_Byte2. If VA is to be acquired, Byte 7, Byte 8, and Byte 9 are 1. Otherwise, they are 0.
8	Increment_VA_Byte1.
9	Increment_VA_Byte0.
10	0.
11	Increment_IB_Byte2. If IB is to be acquired, Byte 11, Byte 12, and Byte 13 are 1. Otherwise, they are 0.
12	Increment_IB_Byte1.
13	Increment_IB_Byte0.
14	0.
15	Increment_VB_Byte2. If VB is to be acquired, Byte 15, Byte 16, and Byte 17 are 1. Otherwise, they are 0.
16	Increment_VB_Byte1.
17	Increment_VB_Byte0.
18	0.
19	Increment_IC_Byte2. If IC is to be acquired, Byte 19, Byte 20, and Byte 21 are 1. Otherwise, they are 0.
20	Increment_IC_Byte1.
21	Increment_IC_Byte0.
22	0.
23	Increment_VC_Byte2. If VC is to be acquired, Byte 23, Byte 24, and Byte 25 are 1. Otherwise, they are 0.
24	Increment_VC_Byte1.
25	Increment_VC_Byte0.
26	0.
27	Increment_IN_Byte2. If IN is to be acquired, Byte 27, Byte 28, and Byte 29 are 1. Otherwise, they are 0.
28	Increment_IN_Byte1.
29	Increment_IN_Byte0.

Byte	Description
30	Byte 1 of M. M is a 16-bit number. The number of 32-bit samples acquired by the microcontroller is (2 × M + 1) × 67 per channel.
31	Byte 0 of M.

If two of the phase powers are to be acquired, the protocol changes (see Table 20).

Table 20. Acquire HSDC Data Continuously—Message from the PC to the Microcontroller if Phase Powers are Acquired

Byte	Description
0	G = 0x47.
1	N = number of bytes transmitted after this byte. N = 38.
2	0: corresponds to Byte 3 of AVA. Because this byte is only a sign extension of Byte 2, it is not sent back by the microcontroller.
3	Increment_AVA_Byte2. If AVA is to be acquired, Byte 3, Byte 4, and Byte 5 are 1. Otherwise, they are 0.
4	Increment_AVA_Byte1.
5	Increment_AVA_Byte2.
6	0.
7	Increment_BVA_Byte2. If BVA is to be acquired, Byte 7, Byte 8, and Byte 9 are 1. Otherwise, they are 0.
8	Increment_BVA_Byte1.
9	Increment_BVA_Byte0.
10	0.
11	Increment_CVA_Byte2. If CVA is to be acquired, Byte 11, Byte 12, and Byte 13 are 1. Otherwise, they are 0.
12	Increment_CVA_Byte1.
13	Increment_CVA_Byte0.
14	0.
15	Increment_AWATT_Byte2. If AWATT is to be acquired, Byte 15, Byte 16, and Byte 17 are 1. Otherwise, they are 0.
16	Increment_AWATT_Byte1.
17	Increment_AWATT_Byte0.
18	0.
19	Increment_BWATT_Byte2. If BWATT is to be acquired, then Byte 19, Byte 20, and Byte 21 are 1. Otherwise, they are 0.
20	Increment_BWATT_Byte1.
21	Increment_BWATT_Byte0.
22	0.
23	Increment_CWATT_Byte2. If CWATT is to be acquired, Byte 23, Byte 24, and Byte 25 are 1. Otherwise, they are 0.
24	Increment_CWATT_Byte1.
25	Increment_CWATT_Byte0.
26	0.
27	Increment_AVAR_Byte2. If AVAR is to be acquired, Byte 27, Byte 28, and Byte 29 are 1. Otherwise, they are 0.
28	Increment_AVAR_Byte1.
29	Increment_AVAR_Byte0.
30	0.
31	Increment_BVAR_Byte2. If BVAR is to be acquired, then Byte 31, Byte 32, and Byte 33 are 1. Otherwise, they are 0.
32	Increment_BVAR_Byte1.
33	Increment_BVAR_Byte0.
34	0.
35	Increment_CVAR_Byte2. If CVAR is to be acquired, Byte 35, Byte 36, and Byte 37 are 1. Otherwise, they are 0.
36	Increment_CVAR_Byte1.
37	Increment_CVAR_Byte0.
38	Byte 1 of M. M is a 16-bit number. The number of 32-bit samples acquired by the microcontroller is (2 × M + 1) × 67 per channel.
39	Byte 0 of M.

After receiving the command, the microcontroller enables the HSDC port and acquires 67 × 7 × 4 = 1876 bytes into BUFFER0. As soon as BUFFER0 is filled, data is acquired in BUFFER1 (equal in size to BUFFER0), while 2 × 3 × 67 = 402 bytes (134 24-bit words) from BUFFER0 are transmitted to the PC. As soon as BUFFER1 is filled, data is acquired into BUFFER0 while 402 bytes from BUFFER1 are transmitted to the PC. Only the less significant 24 bits of every 32-bit instantaneous value are sent to the PC to decrease the size of the buffer sent to the PC. The most significant eight bits are only an extension of a 24-bit signed word; therefore, no information is lost. The protocol used by the microcontroller to send data to the PC is shown in Table 21.

Table 21. Acquire HSDC Data Continuously—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52
1	Byte 2 (MSB) of Word 1
2	Byte 1 of Word 1
3	Byte 0 (LSB) of Word 1
4	Byte 2 (MSB) of Word 2
5	Byte 1 (MSB) of Word 2
…	…
402	Byte 0 (LSB) of Word 134

STARTING THE ADE7854A/ADE7858A/ADE7868A/ADE7878A DSP

This function orders the microcontroller to start the DSP. The microcontroller writes to the run register with 0x1.

Table 22. Start ADE7854A/ADE7858A/ADE7868A/ADE7878A DSP—Message from the PC to the Microcontroller

Byte	Description
0	N = 0x4E
1	N = number of bytes transmitted after this byte; N = 1
2	Any byte

Table 23. Start ADE7854A/ADE7858A/ADE7868A/ADE7878A DSP—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52
1	~ = 0x7E, to acknowledge that the operation was successful

STOPPING THE ADE7854A/ADE7858A/ADE7868A/ADE7878A DSP

This function orders the microcontroller to stop the DSP. The microcontroller writes to the run register with 0x0.

Table 24. Stop ADE7854A/ADE7858A/ADE7868A/ADE7878A DSP—Message from the PC to the Microcontroller

Byte	Description
0	O = 0x4F
1	N = number of bytes transmitted after this byte; N = 1
2	Any byte

Table 25. Stop ADE7854A/ADE7858A/ADE7868A/ADE7878A DSP—Answer from the Microcontroller to the PC

Byte	Description
0	R = 0x52
1	~ = 0x7E to acknowledge that the operation was successful

UPGRADING MICROCONTROLLER FIRMWARE

Although the evaluation board is supplied with the microcontroller firmware already installed, the ADE7854A/ADE7858A/ADE7868A/ADE7878A evaluation software, downloadable from the product website, provides the NXP LPC2368 microcontroller project developed under the IAR embedded workbench environment for ARM. Users in possession of this tool can modify the project at will and can download it using an IAR J-link debugger. As an alternative, the executable can be downloaded using the Flash Magic program available on the Flash Magic website.

Flash Magic uses the PC COM port to download the microcontroller firmware. The procedure for using Flash Magic is as follows:

1. Plug a serial cable into the P15 connector of the evaluation board and into a PC COM port. As an alternative, use a USB-to-UART board together with a USB cable. If doing so, plug the USB-to-UART board into the P15 connector of the evaluation board with the VDD pin of the USB-to-UART board aligned at Pin 1 of P15.
2. Launch the **Device Manager** under Windows XP by writing **devmgmt.msc** into the **Start/Run** box. This helps to identify which COM port is used by the serial cable.
3. Connect Jumper JP8. The P2.10/EINT0 pin of the microcontroller is now connected to ground.
4. Supply the board with two 3.3 V supplies at the P10 and P12 connectors.
5. Press and release the reset button, S2, on the evaluation board.
6. Launch Flash Magic and complete the following:
   a. Select a COM port (COMx as seen in the **Device Manager**).
   b. Set the baud rate to 115,200.
   c. Select the NXP LPC2368 device.
   d. Set the interface to none (ISP).
   e. Set the oscillator frequency (MHz) to 12.0.
   f. Select **Erase all Flash + Code Rd Block**.
   g. Choose **ADE7854A/ADE7858A/ADE7868A/ADE7878A_Eval_Board.hex** from the **\Debug\Exe** project folder.
   h. Select **Verify after programming**.

The Flash Magic settings are shown in Figure 37.

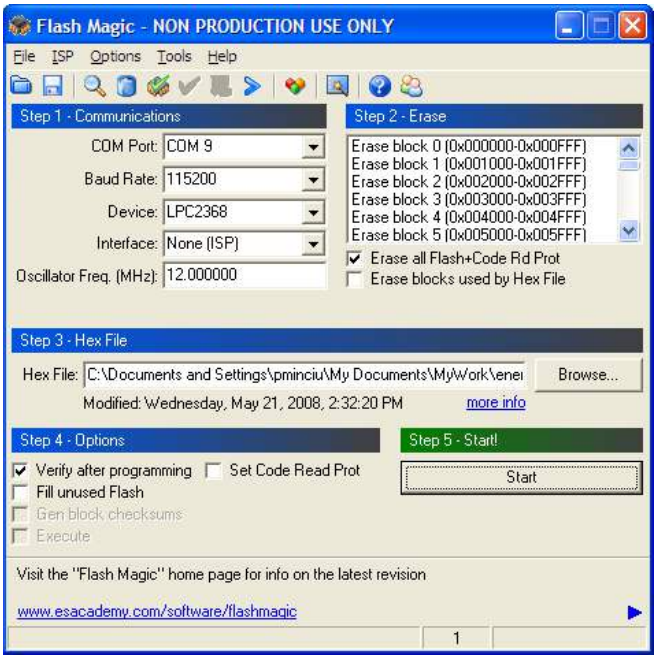


Figure 37. Flash Magic Settings

7. Click **Start** to begin the download process.
8. After the process finishes, extract the JP8 jumper.
9. Reset the evaluation board by pressing and releasing the S2 reset button.

At this point, the program should be functional, and a USB cable can be connected to the board. When the PC recognizes the evaluation board and asks for a driver, indicate the **\VirCOM_Driver_XP** folder for a Windows XP PC or to the **\VirCOM_Driver_W7_64bit** folder for a Windows 7 PC.

CONTROL REGISTERS DATA FILE

Table 26 shows the order in which the control registers of the IC are stored into a data file when you click the **Save All Regs into a file** button in the **All Registers Access** panel.

Table 26. Control Register Data File Content

Line Number	Register
1	AIGAIN
2	AVGAIN
3	BIGAIN
4	BVGAIN
5	CIGAIN
6	CVGAIN
7	NIGAIN
8	AIRMSOS
9	AVRMSOS
10	BIRMSOS
11	BVRMSOS
12	CIRMSOS
13	CVRMSOS
14	NIRMSOS
15	AVAGAIN
16	BVAGAIN
17	CVAGAIN
18	AWGAIN
19	AWATTOS
20	BWGAIN
21	BWATTOS
22	CWGAIN
23	CWATTOS
24	AVARGAIN
25	AVAROS
26	BVARGAIN
27	BVAROS
28	CVARGAIN
29	CVAROS
30	AFWGAIN
31	AFWATTOS
32	BFWGAIN
33	BFWATTOS
34	CFWGAIN
35	CFWATTOS
36	AFVARGAIN
37	AFVAROS
38	BFVARGAIN
39	BFVAROS
40	CFVARGAIN
41	CFVAROS
42	VATHR1
43	VATHR0
44	WTHR1
45	WTHR0
46	VARTHR1
47	VARTHR0
48	VANOLOAD
49	APNOLOAD
50	VARNOLOAD
51	VLEVEL
52	DICOEFF

Line Number	Register
53	HPFDIS
54	ISUMLVL
55	RUN
56	OILVL
57	OVLVL
58	SAGLVL
59	MASK0
60	MASK1
61	VNOM
62	LINECYC
63	ZXTOUT
64	COMPMODE
65	GAIN
66	CFMODE
67	CF1DEN
68	CF2DEN
69	CF3DEN
70	APHCAL
71	BPHCAL
72	CPHCAL
73	CONFIG
74	MMODE
75	ACCMODE
76	LCYCMODE
77	PEAKCYC
78	SAGCYC
79	CFCYC
80	HSDC_CFG
81	CONFIG_A
82	LPOILVL
83	CONFIG2

TROUBLESHOOTING

This section provides troubleshooting tips for resolving the most commonly encountered difficulties.

While executing the evaluation software, if the power supply to the board is not connected, the name of the IC displayed on the main screen of the front panel will be faulty. In addition, you will not be able to communicate with the IC correctly. If this occurs, provide power to the evaluation board and restart the execution of the evaluation software.

If the registers read all FFs or 00s, then

- Check the power supply to the board. If there is no power, power up the board and restart the software.
- Check if the jumper connections made on the evaluation board match the communication protocol selected. If not, reconfigure the jumpers properly and restart the software.
- Check if the DSP is running: Write 0x01 to the Run register and verify if the registers can be accessed properly. Note that if a reset has been performed, set the Run register to 0x01 before accessing other registers.

If the USB connection to the evaluation board was terminated while the software execution was taking place, then an error will be reported while re-executing the software. When encountering this problem, remove the USB cable from the evaluation board and press the S2 ($\overline{\text{MRESET}}$) button once. Now, connect the USB cable to the board and restart the evaluation software.

EVALUATION BOARD SCHEMATICS AND LAYOUT

SCHEMATICS

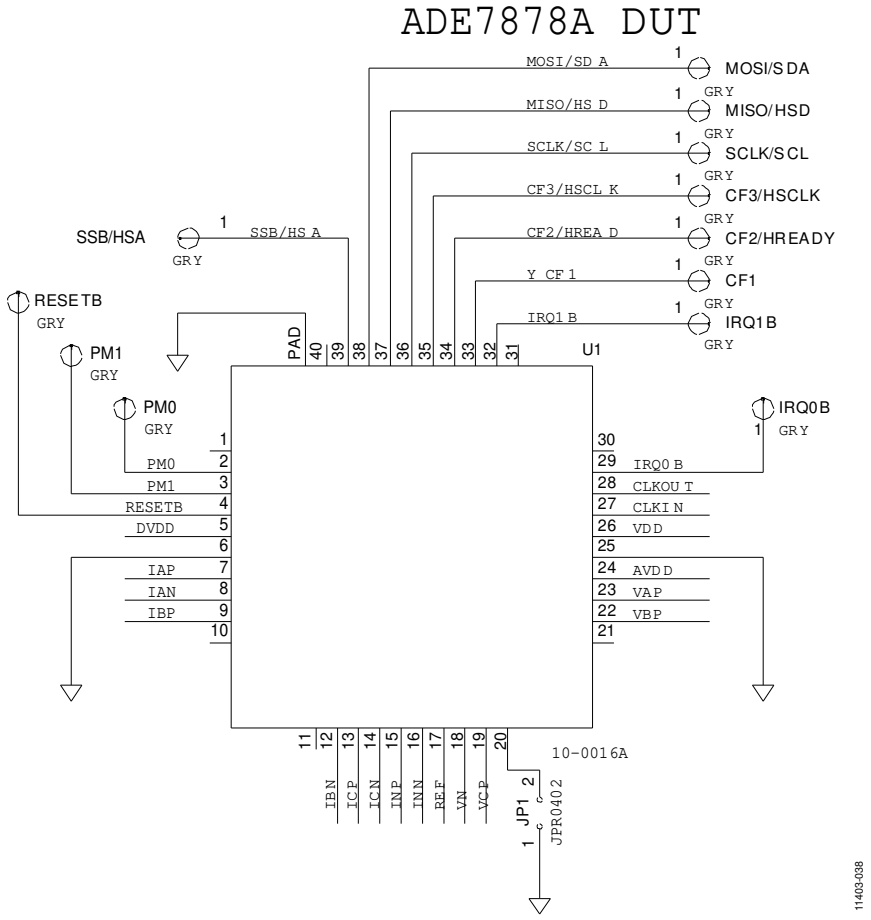


Figure 38. ADE7854A/ADE7858A/ADE7868A/ADE7878A Schematic

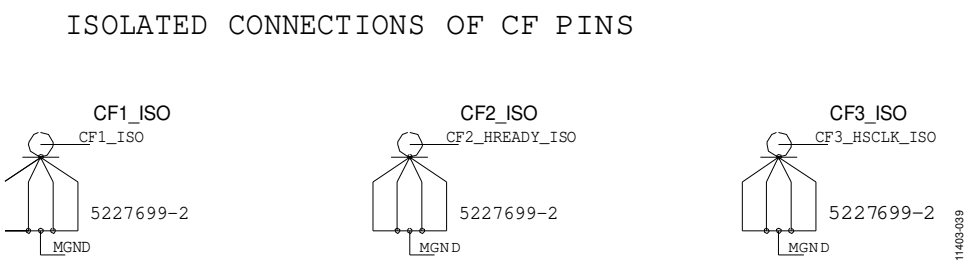


Figure 39. Isolated Connections of CF Pins

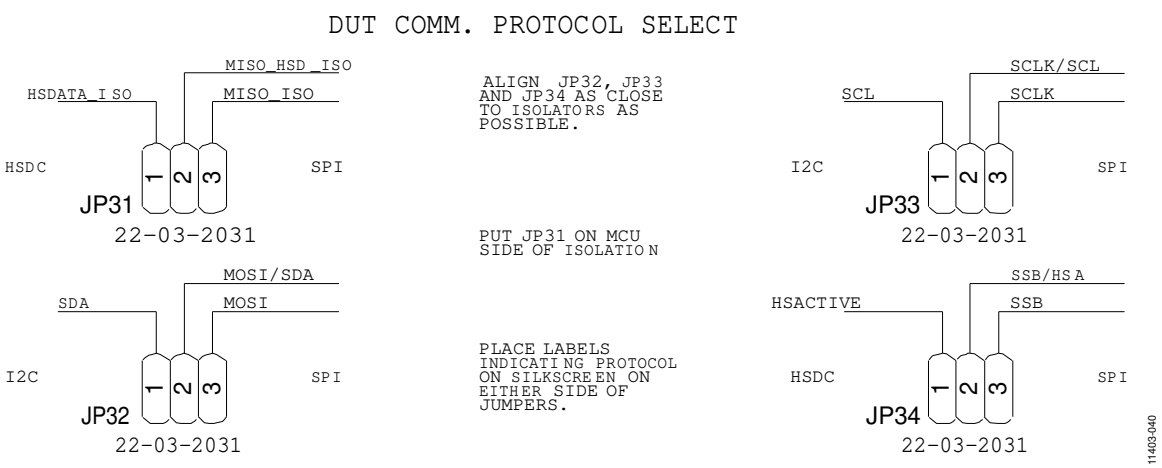


Figure 40. Communication Protocol Selection

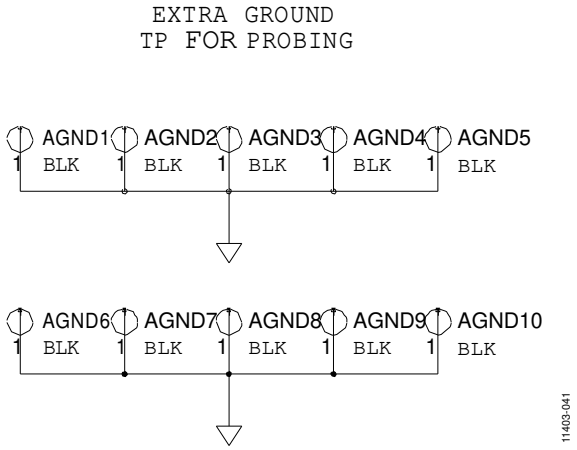


Figure 41. Ground Connections

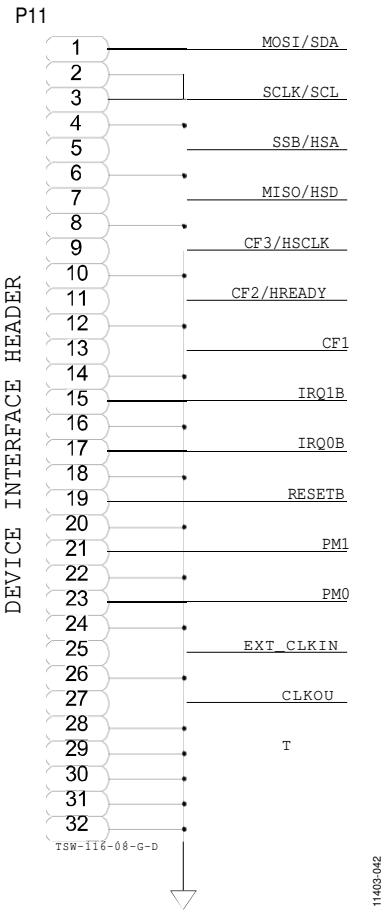


Figure 42. Device Interface Header

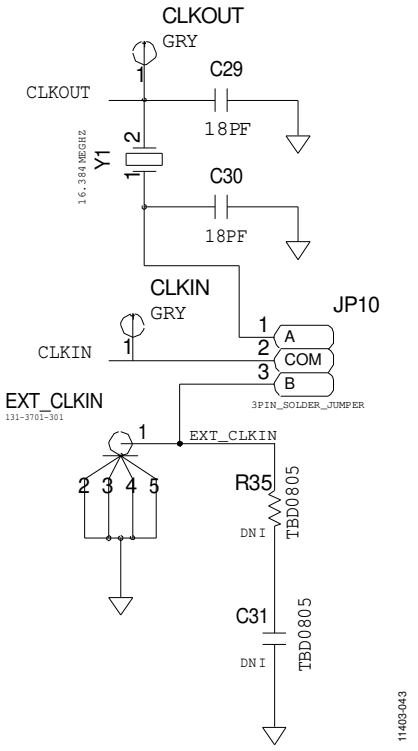


Figure 43. ADE7854A/ADE7858A/ADE7868A/ADE7878A Clock Circuitry

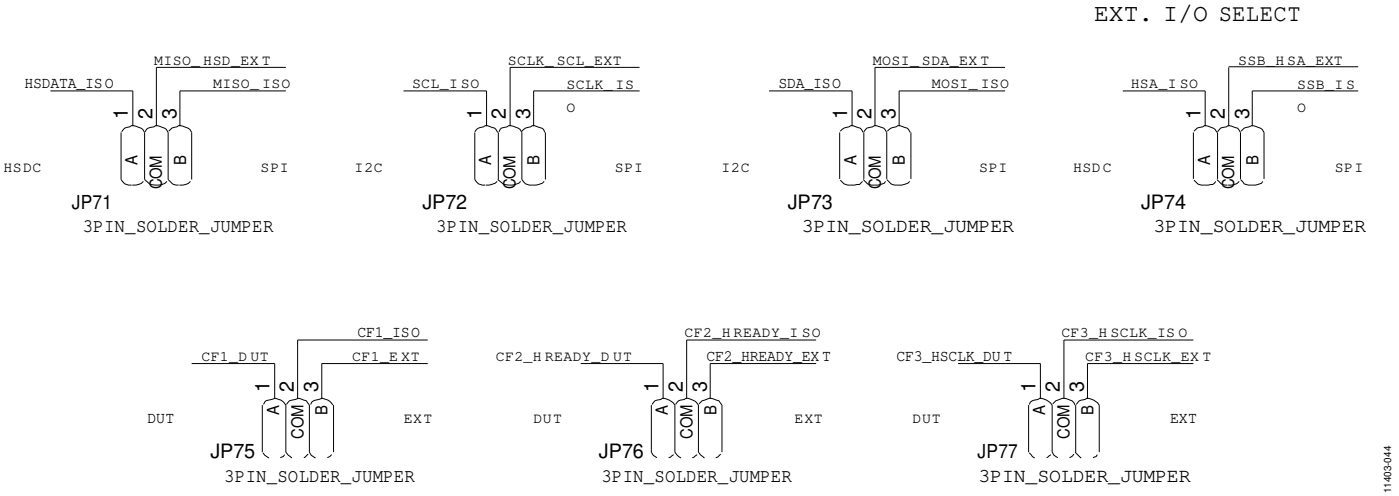


Figure 44. I/O Selection

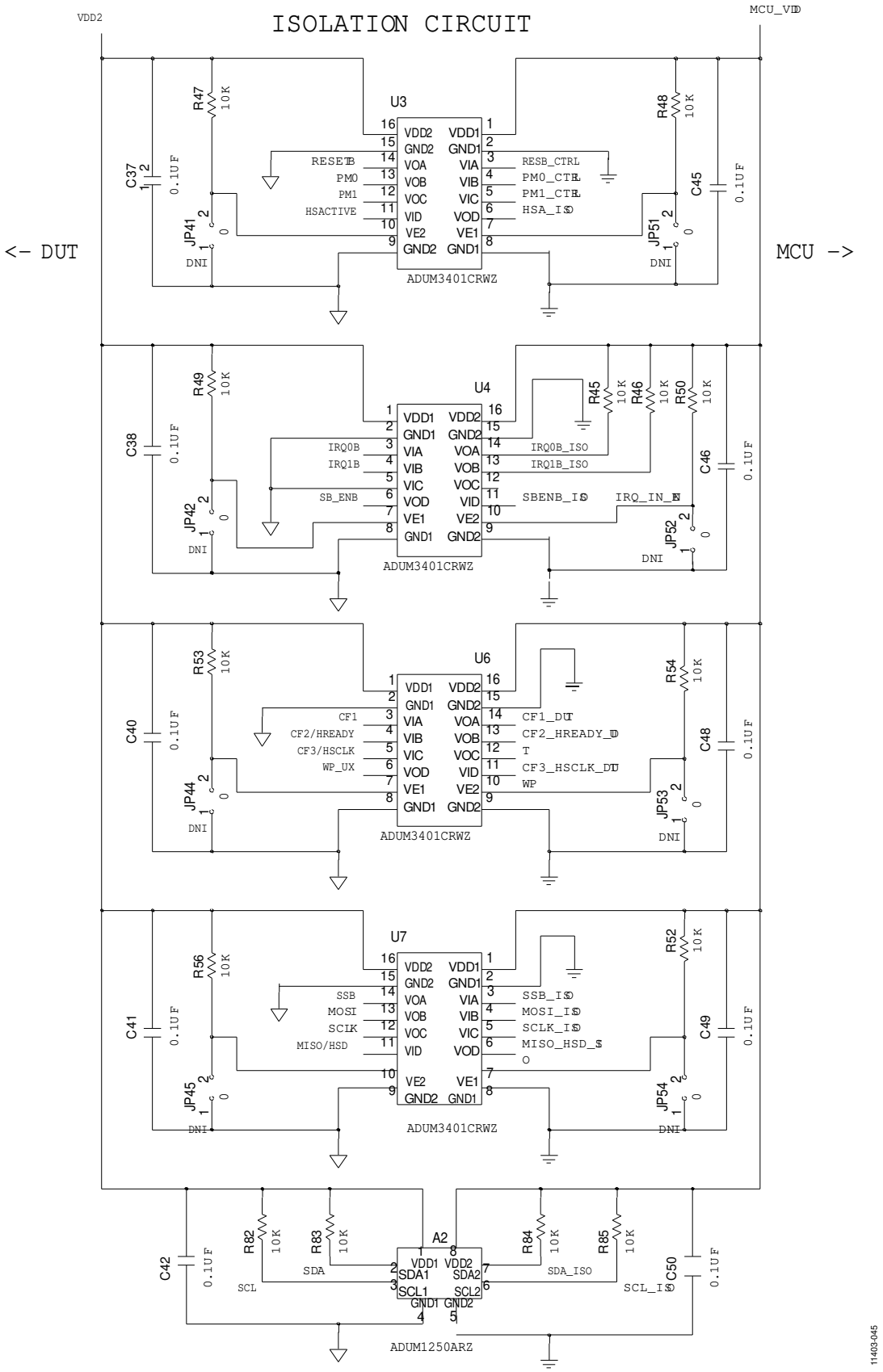


Figure 45. Isolation Circuitry

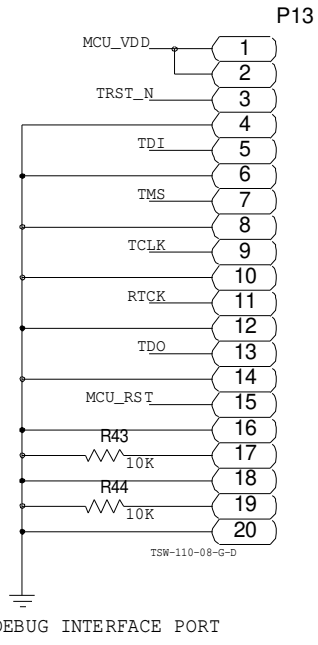


Figure 46. JTAG Interface Port

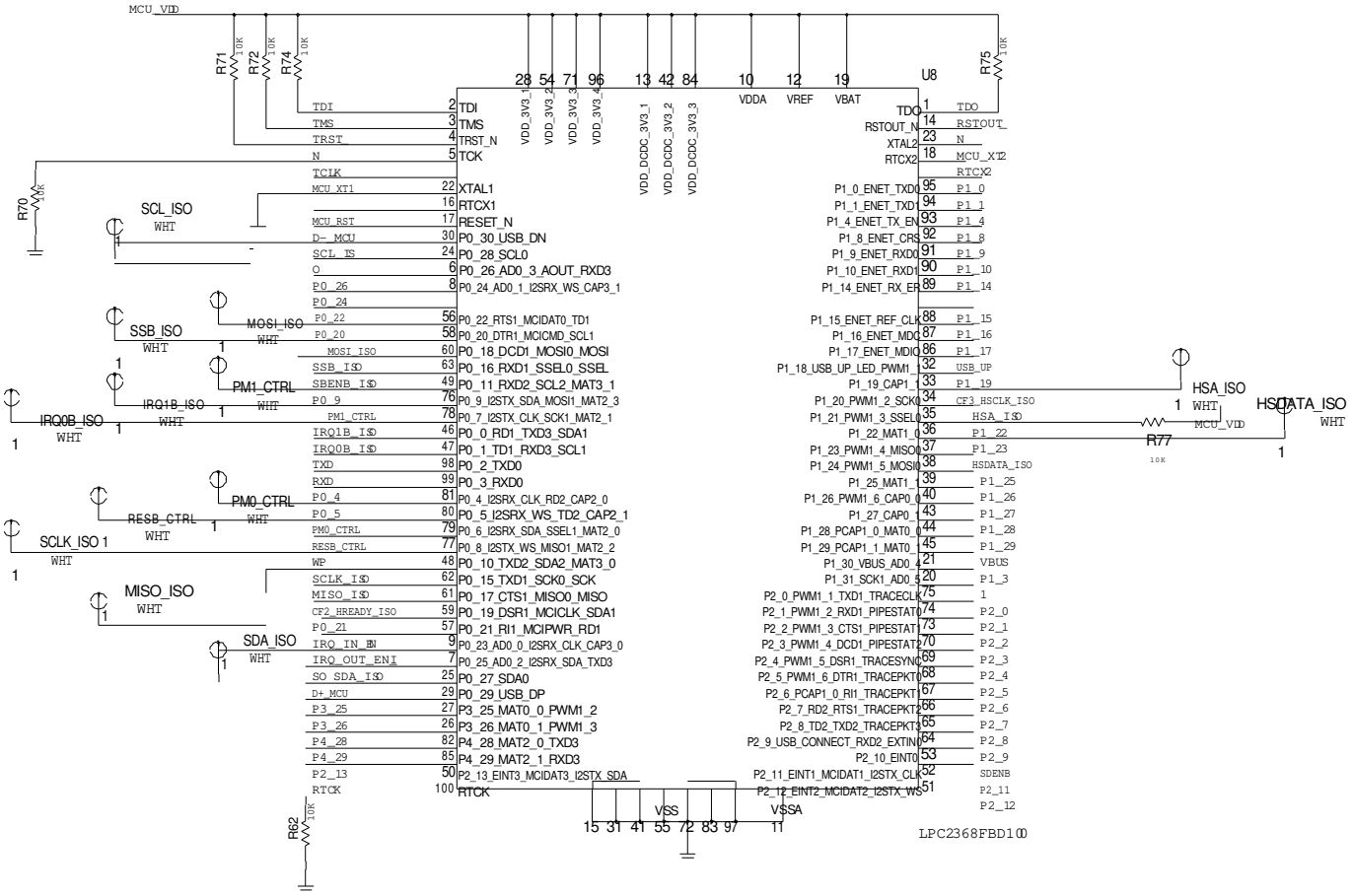


Figure 47. LPC2368 Schematic

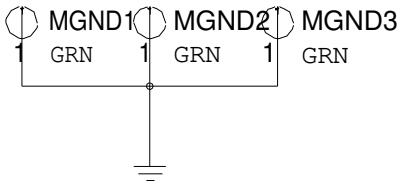


Figure 48. Ground Test Points

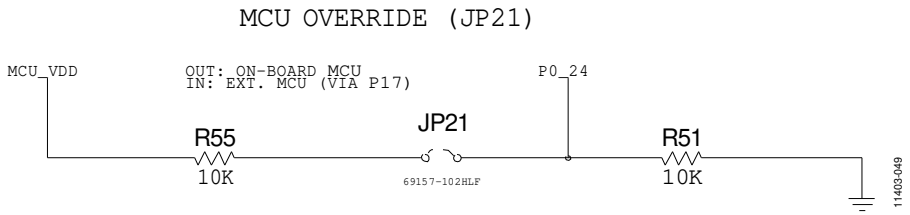


Figure 49. MCU Override

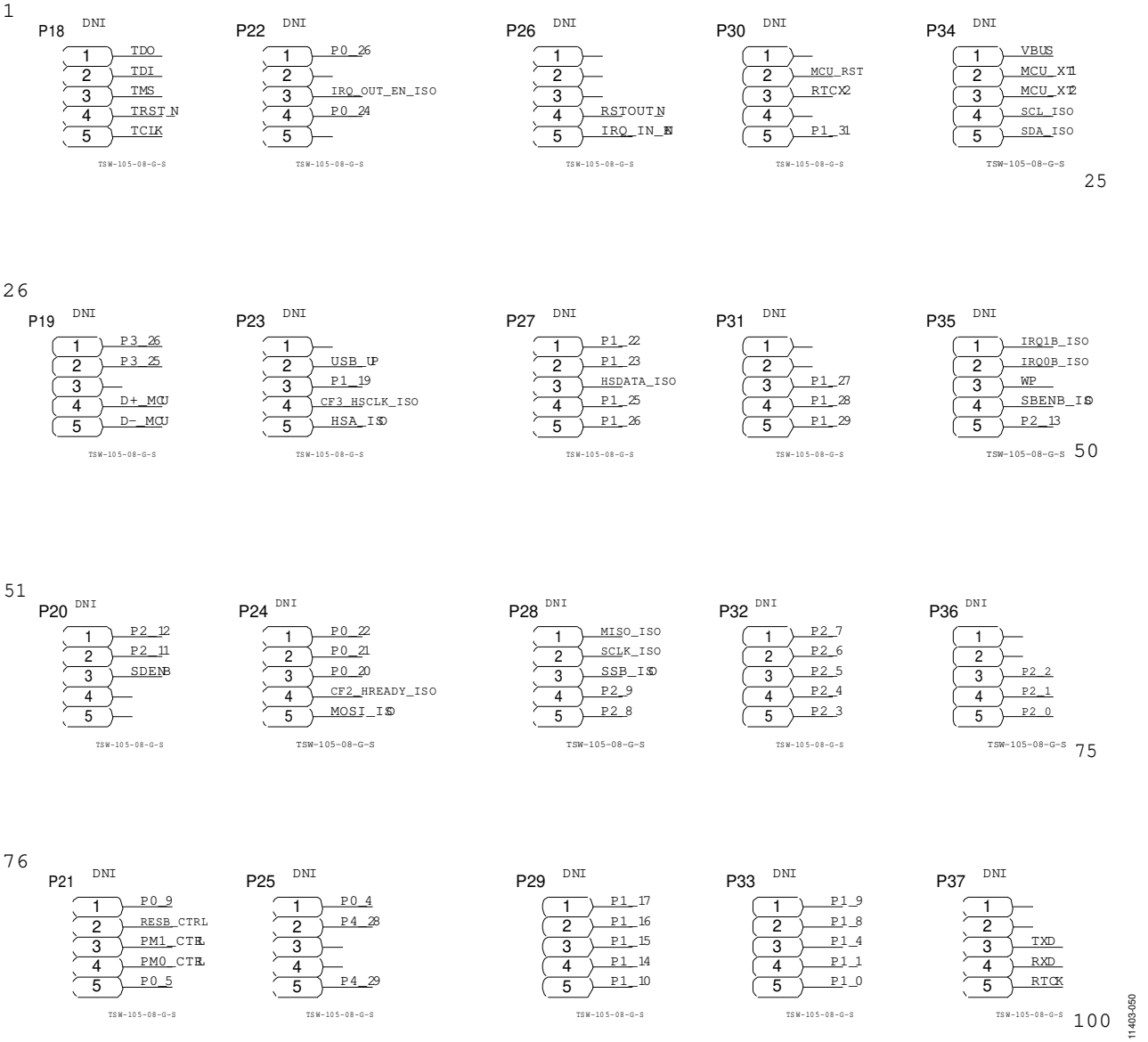


Figure 50. MCU Pin Connections

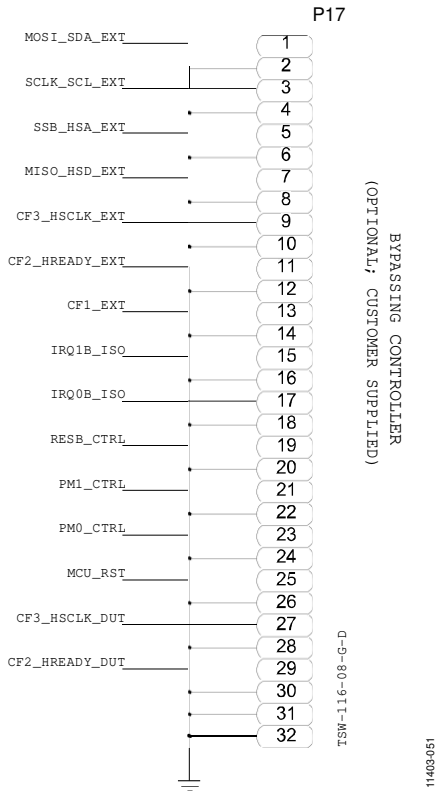


Figure 51. Interface Header When MCU is Bypassed

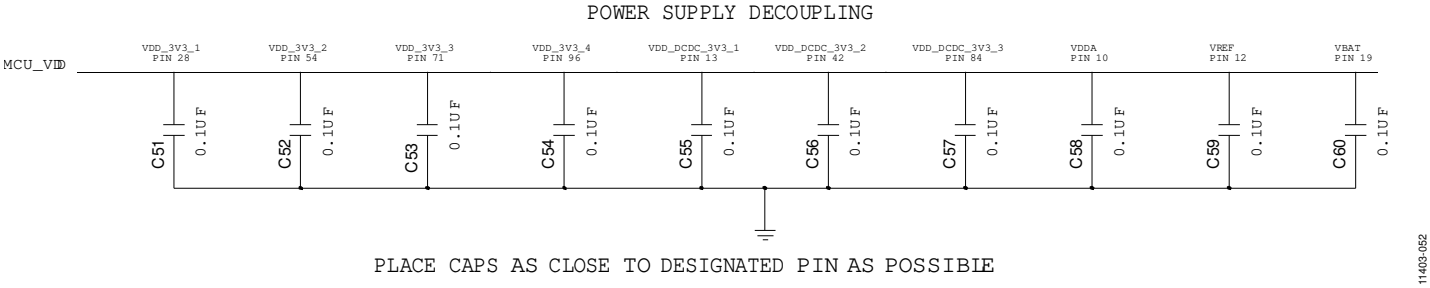


Figure 52. Power Supply Decoupling

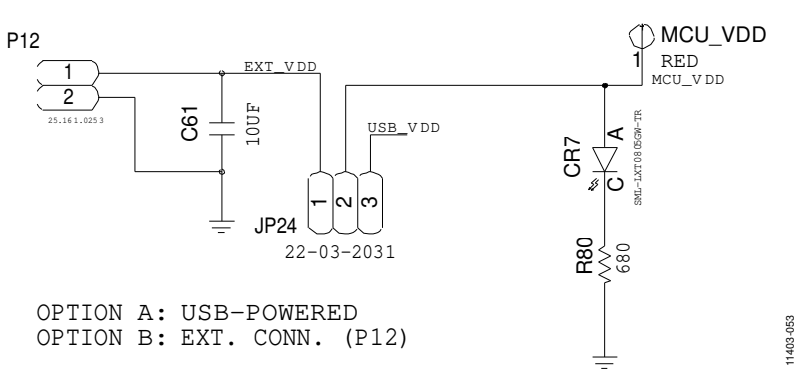


Figure 53. MCU Power Supply Selection

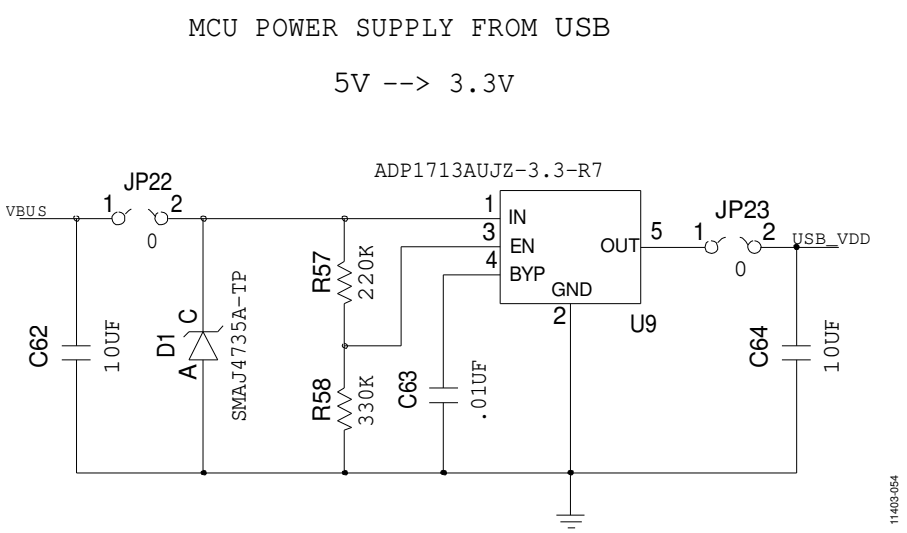


Figure 54. MCU Power Supply Regulator

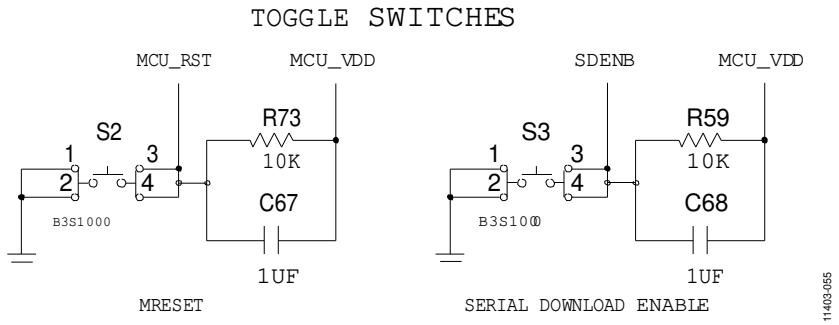


Figure 55. MCU Reset and Boot Switches

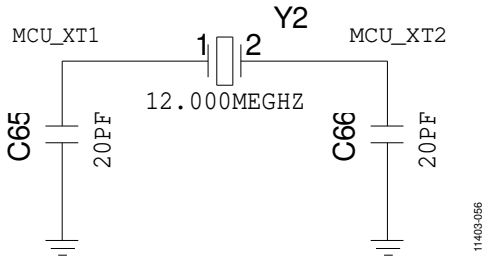


Figure 56. MCU Clock Circuit

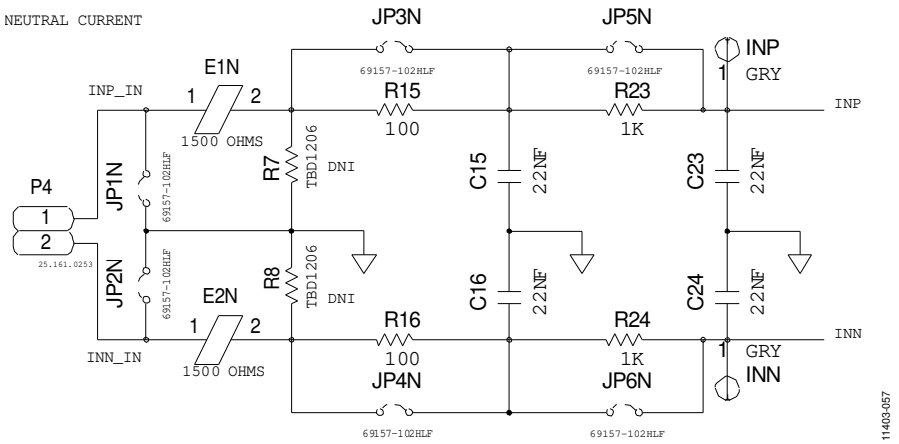


Figure 57. Neutral Current Circuit

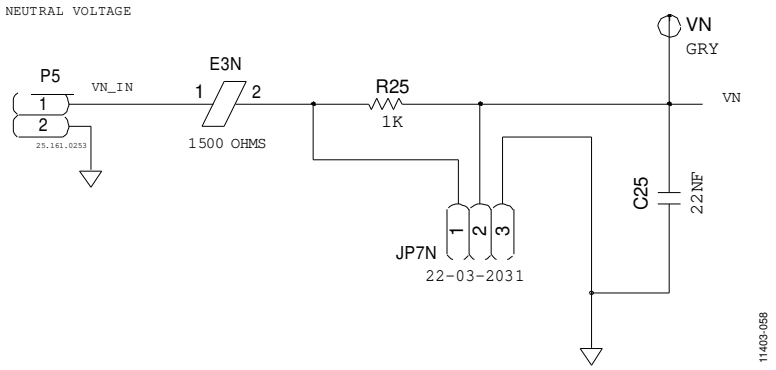


Figure 58. VN Circuit

OUTPUT LED CIRCUIT

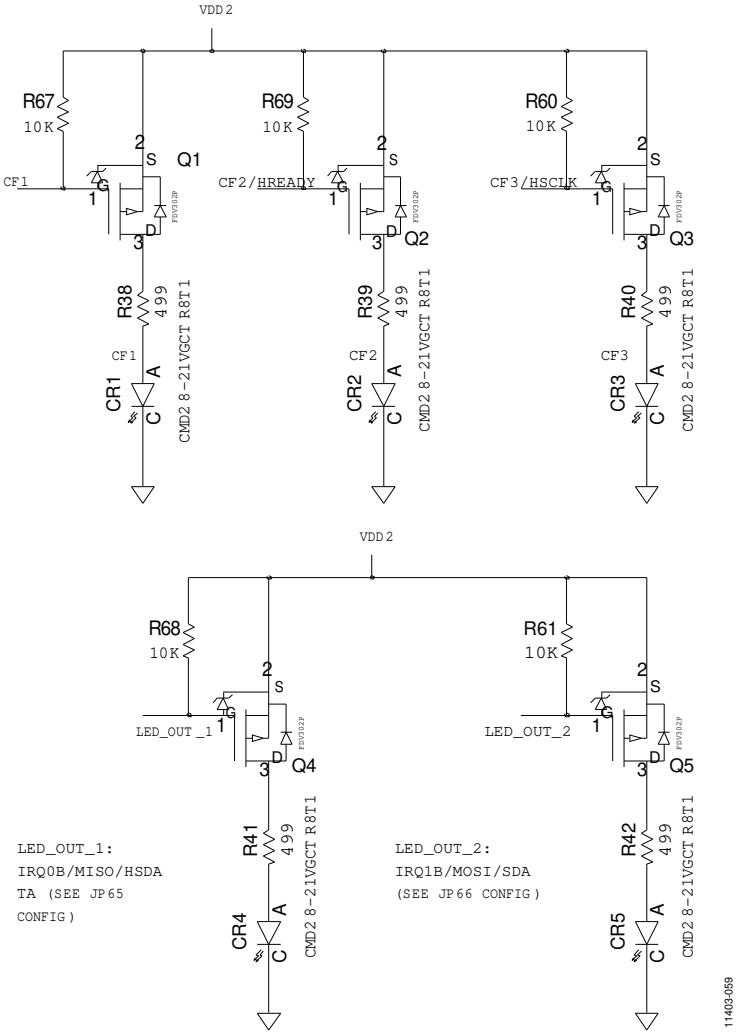


Figure 59. Output LED Circuit

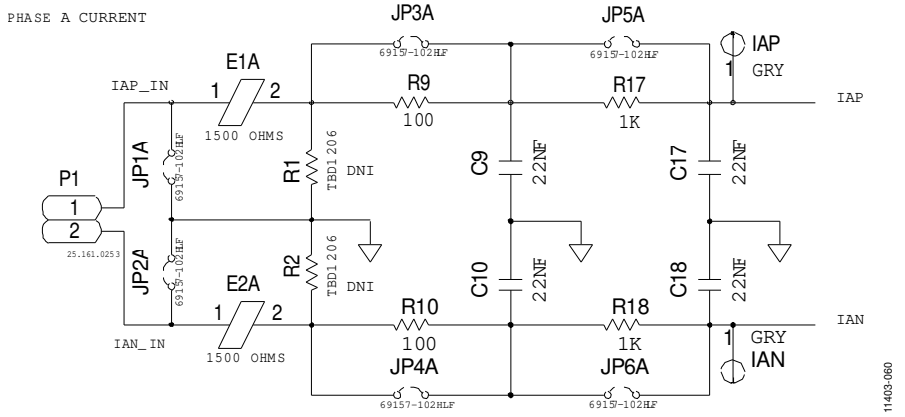


Figure 60. Phase A Current

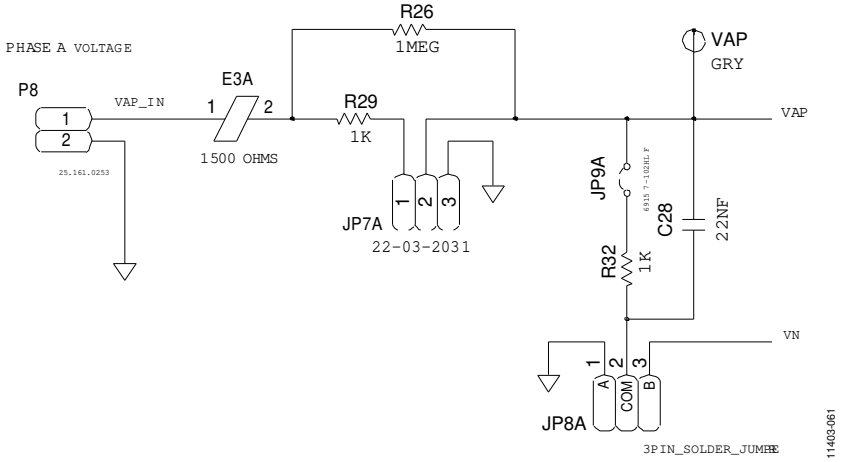


Figure 61. Phase A Voltage

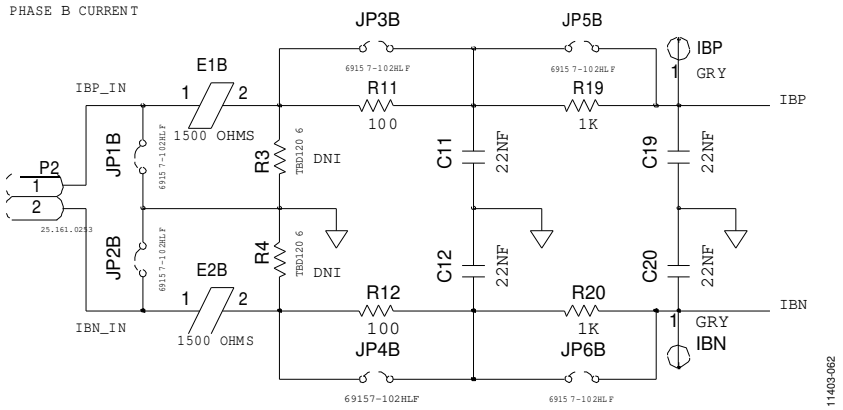


Figure 62. Phase B Current

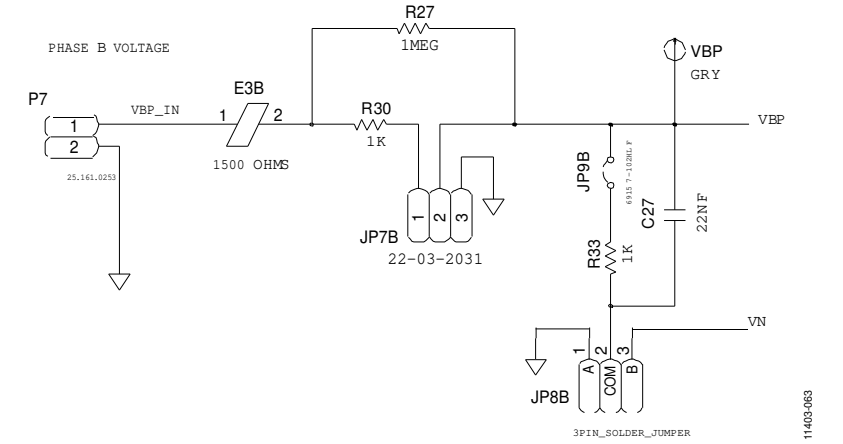


Figure 63. Phase B Voltage

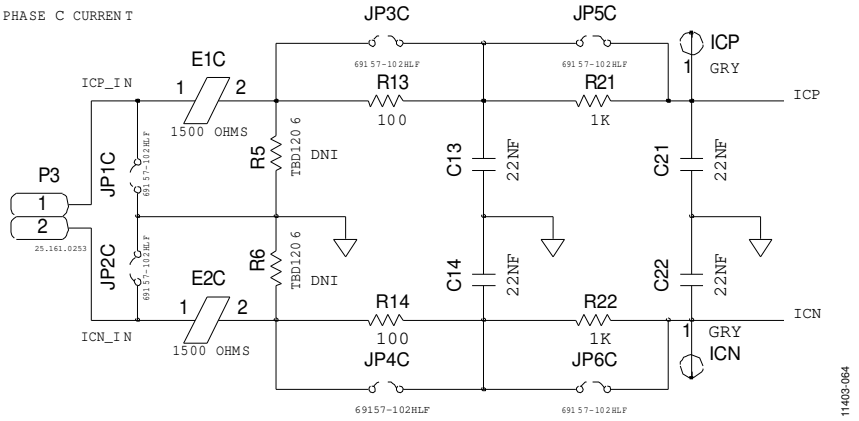


Figure 64. Phase C Current

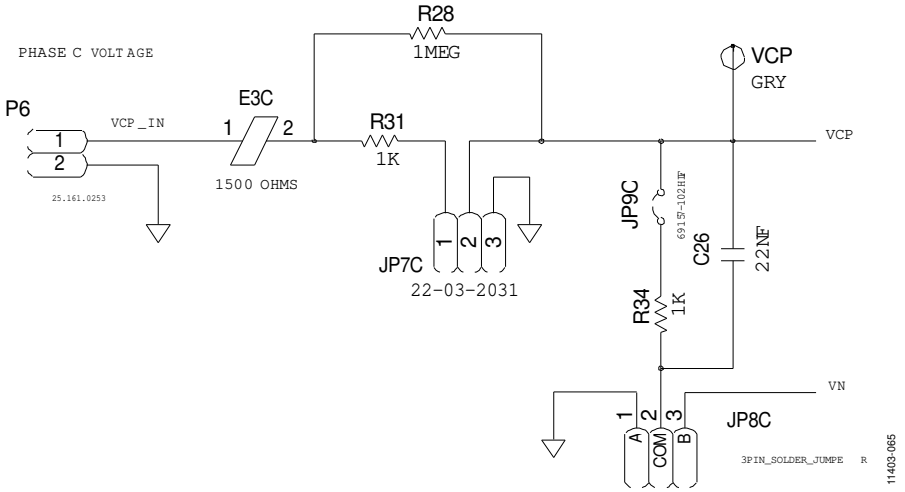


Figure 65. Phase C Voltage

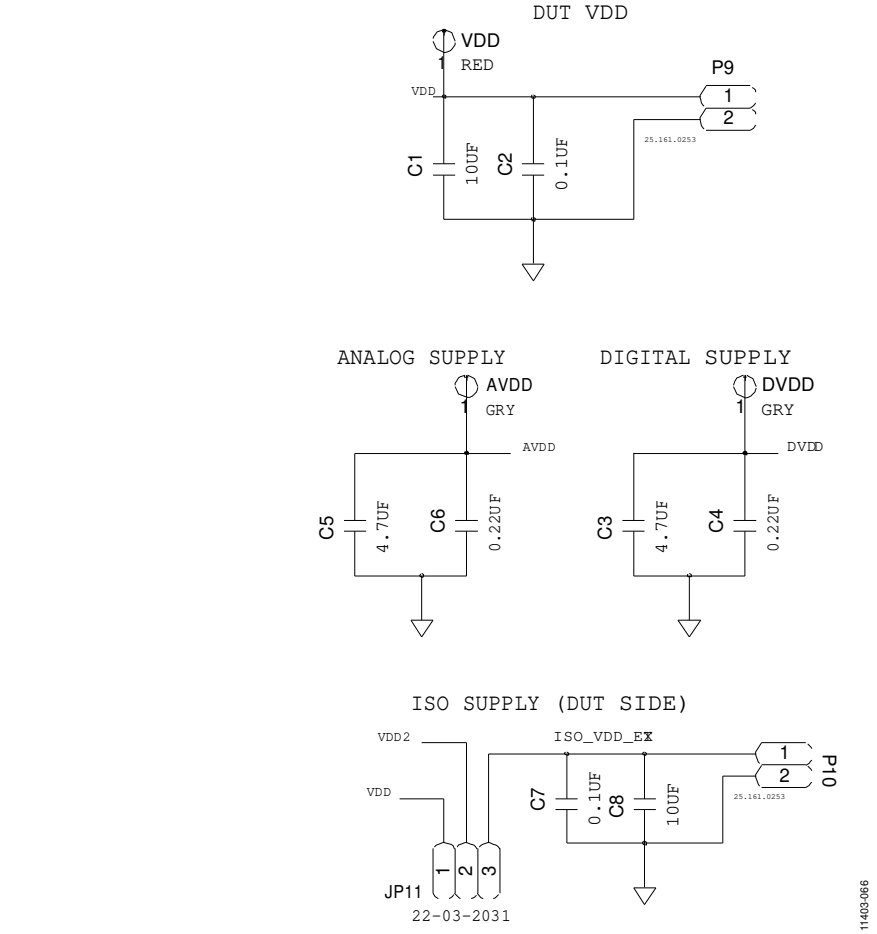


Figure 66. Power Supply Connections

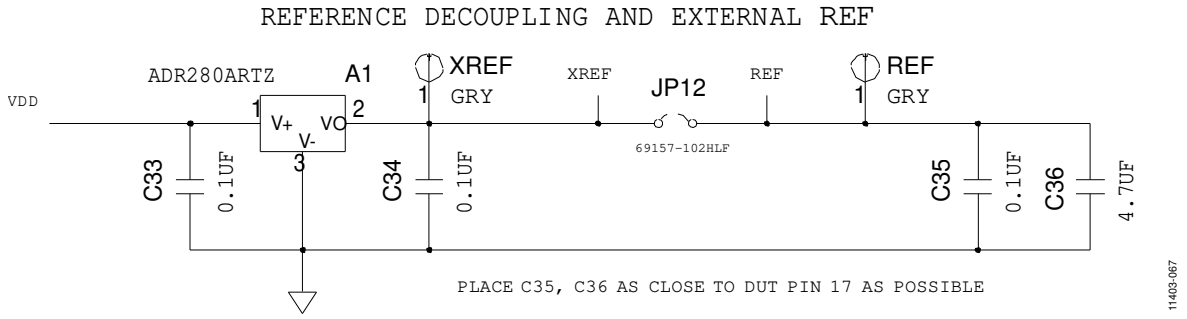


Figure 67. Reference Voltage Circuit

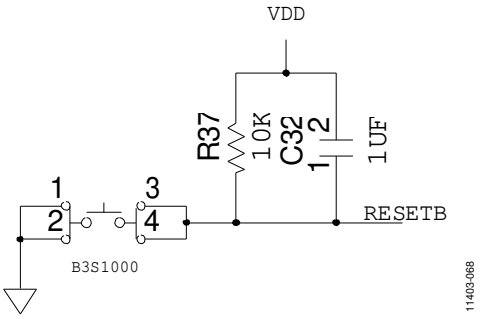


Figure 68. ADE7854A/ADE7858A/ADE7868A/ADE7878A Reset Circuit

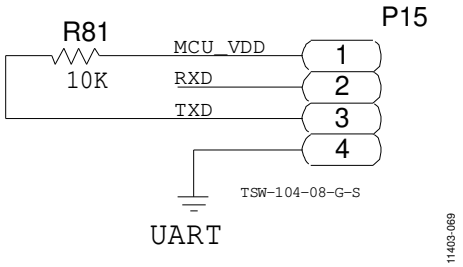


Figure 69. UART Circuit

USB INTERFACE

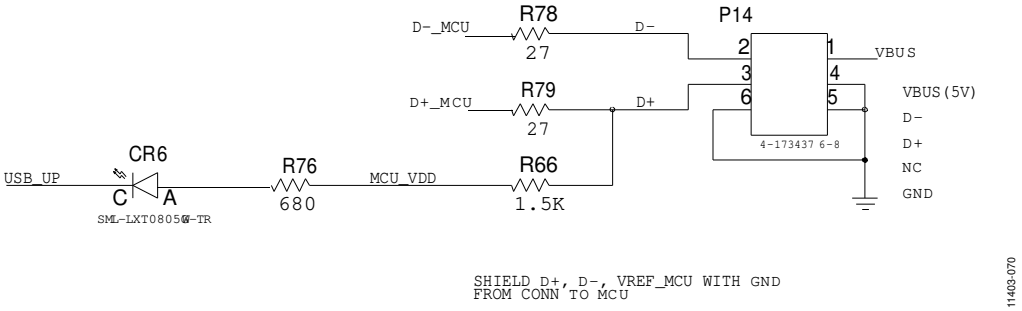


Figure 70. USB Interface

LAYOUT

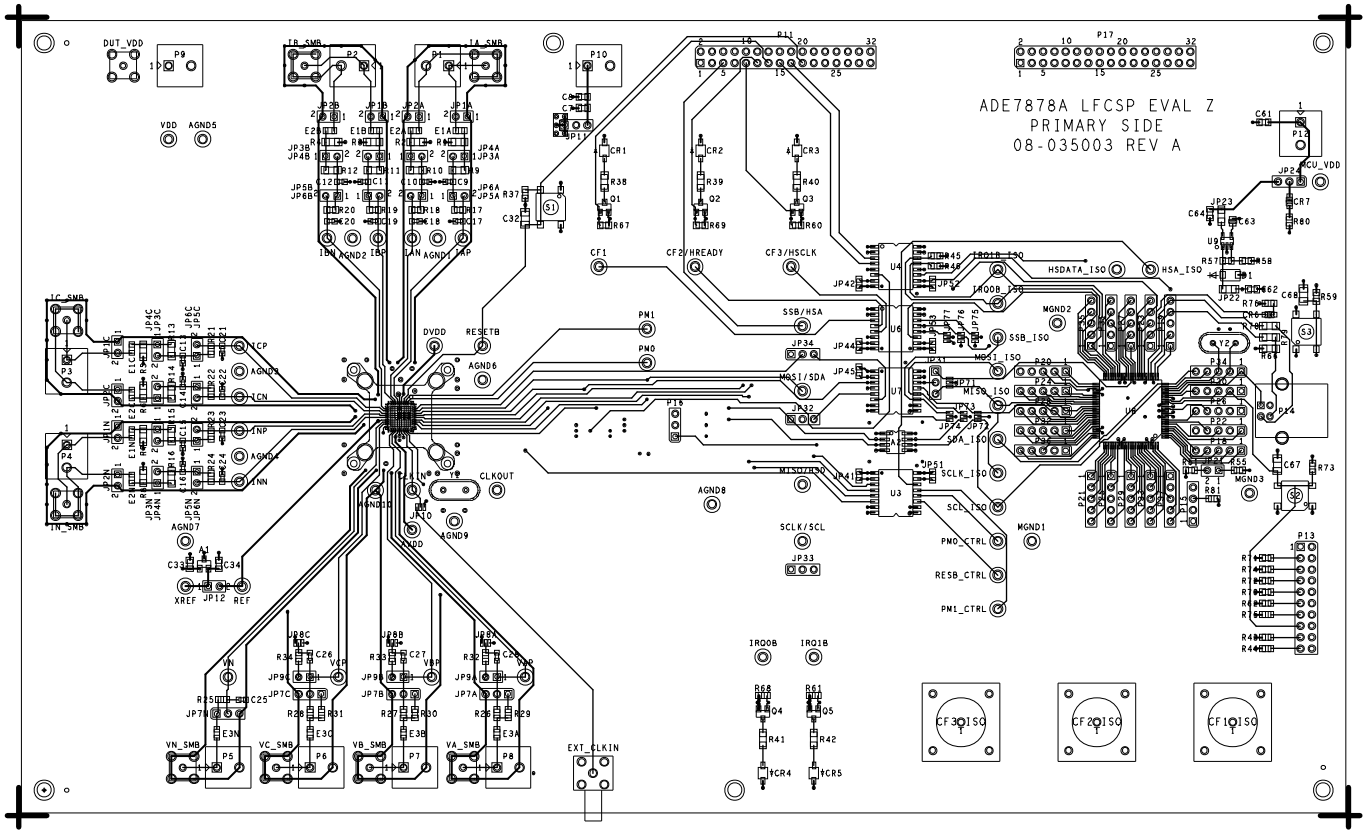


Figure 71. Layer Top Layer

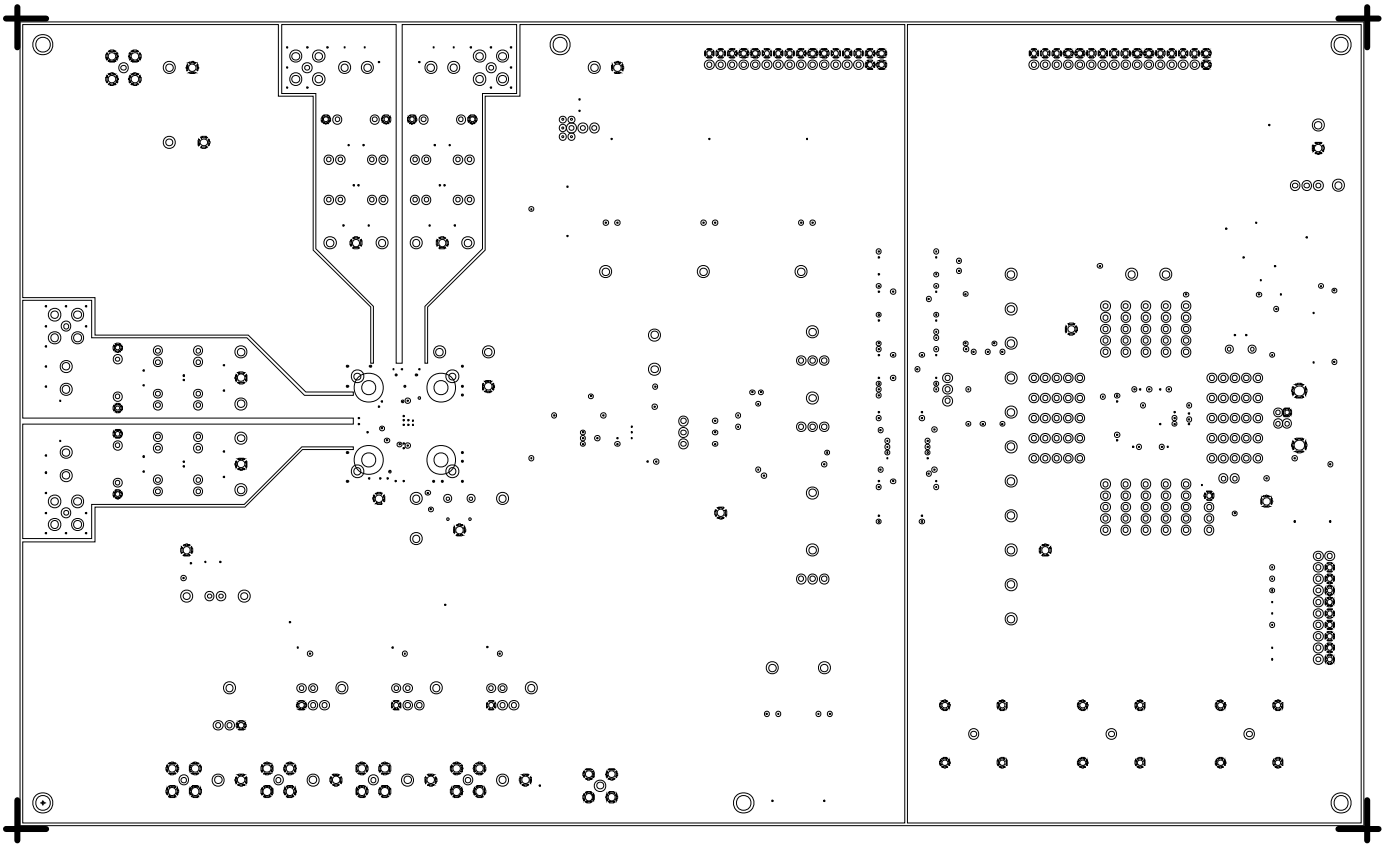


Figure 72. Layer 2

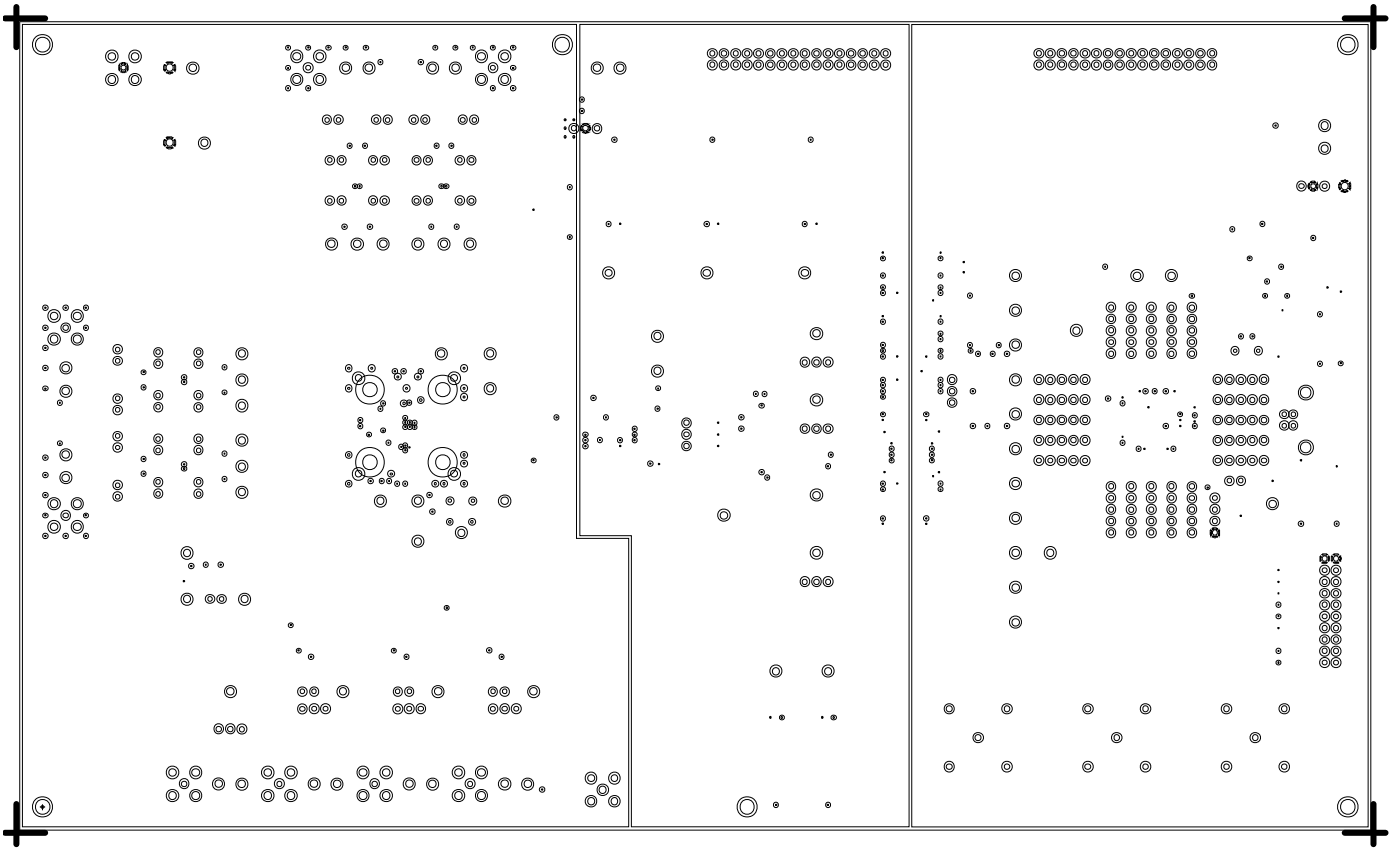


Figure 73. Layer 3

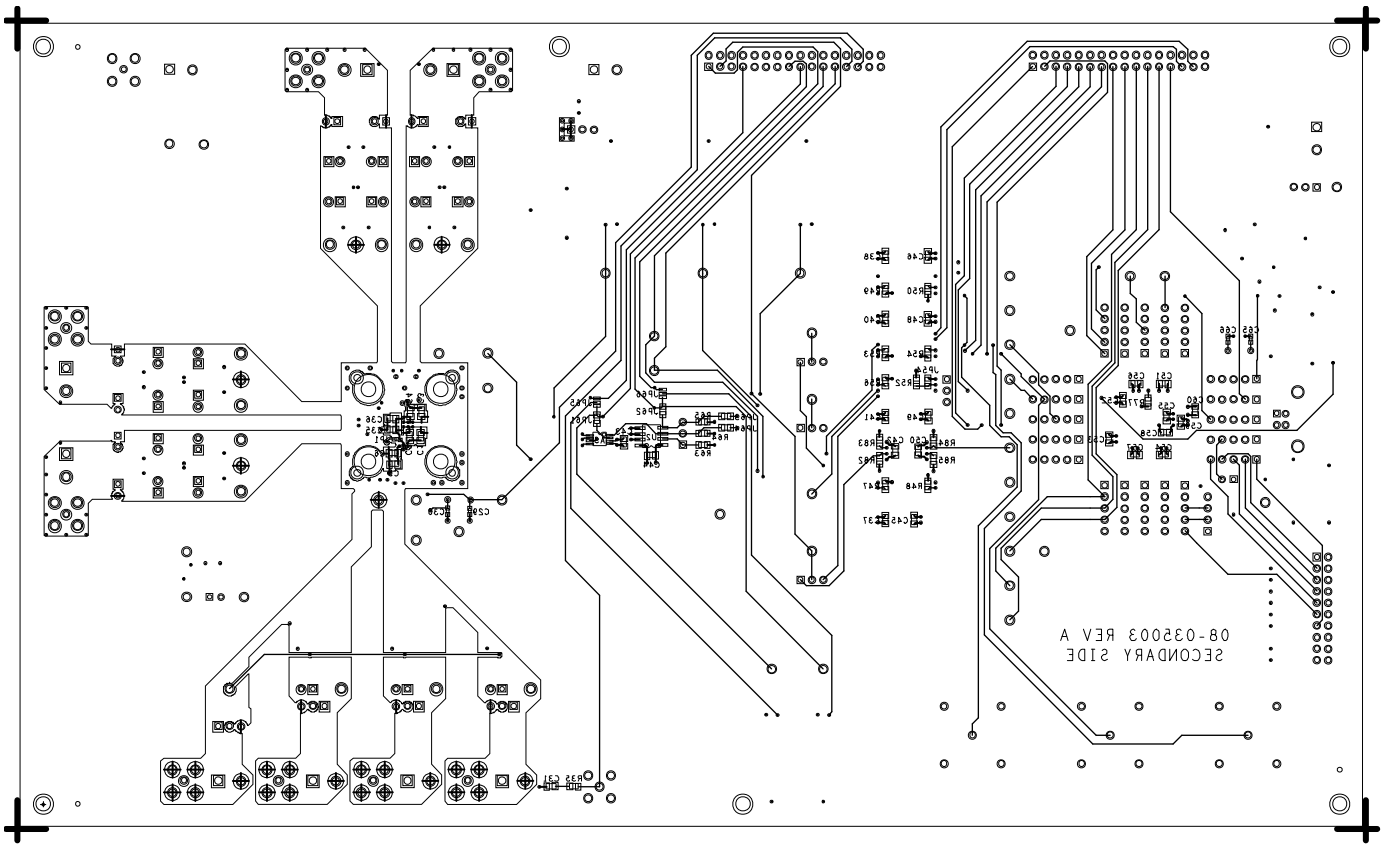


Figure 74. Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 27.

Qty	Designator	Description	Manufacturer/Part Number
1	A1	IC, 1.2 V ultralow power high PSRR voltage reference	Analog Devices/ADR280ARTZ
1	A2	IC, swappable dual isolator	Analog Devices/ADuM1250ARZ
10	AGND1 to AGND10	Connector, PCB, test point, black	Components Corporation/TP-104-01-00
30	VN, CF1, IAN, IAP, IBN, IBP, ICN, ICP, INN, INP, PM0, PM1, REF, VAP, VBP, VCP, AVDD, DVDD, XREF, CLKIN, IRQ0, IRQ1, CLKOUT, RESET, SS/HSA, MISO/HSD, MOSI/SDA, SCLK/SCL, CF3/HSCLK, CF2/HREADY	Connector, PCB, test point, grey	Components Corporation/TP-104-01-08
5	C1, C8, C61, C62, C64	Capacitor, monolithic, ceramic, 10 µF	Murata/GRM21BR61C106KE15L
20	C9 to C28	Capacitor, ceramic chip, C0G, 0603, 22 nF	Digi-Key/0603YC223KAT2A
27	C2, C7, C33 to C35, C37, C38, C40 to C46, C48 to C60	Capacitor, X7R, 0805, 100 nF	Murata/GRM21BR71H104KA01L
4	C29, C30, C65, C66	Capacitor, monolithic, ceramic, C0G, 0402, 20 pF	Murata/GRM1555C1H200JZ01D
3	C3, C5, C36	Capacitor, ceramic, 0805, X5R, 4.7 µF	Taiyo Yuden/EMK212BJ475KG-T
3	C32, C67, C68	Capacitor, ceramic, 1206, X7R, 1 µF	Taiyo Yuden/GMK316B7105KL-T
2	C4, C6	Capacitor, ceramic, X7R, 0.22 µF	Phycomp (Yageo)/2222 780 15654
1	C63	Capacitor, ceramic, X7R, 0.01 µF	AVX/0306ZC103KAT2A
3	CF1_ISO to CF3_ISO	Connector, PCB coax, vertical, BNC, 50 Ω	Tyco Electronics/5227699-2
5	CR1 to CR5	Diode, LED, green, SMD	Chicago Mini Lamp/CMD28-21VGCTR8T1
2	CR6, CR7	LED, green, surface mount	Lumex/SML-LXT0805GW-TR
1	D1	Diode, 6.2 V, Zener, SMA	Micro Commercial Co./SMAJ4735A-TP
12	E1A to E3A, E1B to E3B, E1C to E3C, E1N to E3N	Inductor, chip, ferrite bead, 0805, 1500 Ω	Murata/BLM21BD152SN1D
1	EXT_CLKIN	Connector, PCB coax, SMB, RA	Johnson/131-3701-301
13	HSA_ISO, SCL_ISO, SDA_ISO, SSB_ISO, MISO_ISO, MOSI_ISO, PM0_CTRL, PM1_CTRL, SCLK_ISO, IRQ0B_ISO, IRQ1B_ISO, RESB_CTRL, HSDATA_ISO	Connector, PCB, test point, white	Components Corporation/TP-104-01-09
10	JP11, JP24, JP31 to JP34, JP7A, JP7B, JP7C, JP7N	3-pin jumper	N/A
29	JP12, JP1A to JP6A, JP1B to JP6B, JP1C to JP6C, JP1N to JP6N, JP21, JP9A, JP9B, JP9C	Connector, PCB Berg jumper, ST, male 2-pin	BERG/69157-102
2	JP22, JP23	Resistor jumper, SMD 1206 (short)	Panasonic/ERJ-8GEYJ0.0
2	JP61, JP62	Resistor jumper, SMD 0805 (open)	Panasonic/ERJ-6GEYJ0.0
2	VDD, MCU_VDD	Connector, PCB, test point, red	Components Corporation/TP-104-01-02
3	MGND1 to MGND3	Connector, PCB, test point, green	Components Corporation/TP-104-01-05
11	P1 to P10, P12	Connector, PCB term, black, 2-pin, ST	Weiland/25.161.0253

Qty	Designator	Description	Manufacturer/Part Number
2	P11, P17	Connector, PCB, header, SHRD, ST, male 32-pin	Samtec/TSW-1-30-08-G-D
1	P13	Connector, PCB, header, ST, male 20-pin	Samtec/TSW-110-08-G-D
1	P14	Connector, PCB, USB, Type B, R/A, through hole	AMP/4-1734376-8
1	P15	Connector, PCB, header, ST, male 4-pin	Samtec/TSW-104-08-G-S
1	P16	Connector, PCB, straight header 3-pin	Molex/22-03-2031
5	Q1 to Q5	Trans digital FET P channel	Fairchild/FDV302P
8	R9 to R16	Resistor, precision thick film, chip R1206, 100 Ω	Panasonic/ERJ-8ENF1000V
15	R17 to R25, R29 to R34	Resistor, precision thick film, chip R0805, 1 kΩ	Panasonic/ERJ-6ENF1001V
3	R26 to R28	Resistor, precision thick film, chip R0805, 1 MΩ	Panasonic/ERJ-6ENF1004V
37	R37, R43 to R56, R59 to R65, R67 to R75, R77, R81 to R85	Resistor, precision thick film, chip R0805, 10 kΩ	Panasonic/ERJ-6ENF1002V
5	R38 to R42	Resistor, precision thick film, chip R1206, 499 Ω	Panasonic/ERJ-8ENF4990V
1	R57	Resistor, film, SMD 0805, 220 kΩ	Multicomp/MC 0.1W 0805 1% 220K
1	R58	Resistor, film, SMD 0805, 330 kΩ	Panasonic/ERJ-6GEYJ334V
1	R66	Resistor, PREC, thick film chip, R1206, 1.5 kΩ	Panasonic/ERJ-8ENF1501V
2	R76, R80	Resistor, film, SMD 0805, 680 Ω	Multicomp/MC 0.1W 0805 1% 680R
2	R78, R79	Resistor, film, SMD 1206, 27 Ω	Phycomp (Yageo)/9C12063A27R0FKHFT
3	S1 to S3	SW SM mechanical key switch	Omron/B3S1000
4	U3, U4, U6, U7	IC quad channel digital isolator	Analog Devices/ADuM3401CRWZ
1	U8	IC ARM7, MCU, flash, 512K 100 LQFP	NXP/LPC2368FBD100
1	U9	IC 300mA low dropout CMOS linear regulator	Analog Devices/ADP1713AUJZ-3.3-R7
1	Y1	IC crystal, 16.384 MHz maximum drive level: 500 µW maximum ESR: 40 Ω	ECS/ECS-163.8-18-4XEN
1	Y2	IC crystal quartz, 12.0 MHz	ECS/ECS-120-20-4X

NOTES

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NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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