# BQ25628 / BQ25629 I²C Controlled, 2-A, Maximum 18-V Input, Charger with NVDC Power Path Management and OTG Output

## 1 Features

- High-efficiency, 1.5-MHz, synchronous switching mode buck charger for single cell battery
  - >90% efficiency down to 25-mA output current from 5-V input
  - Charge termination from
  - Flexible JEITA profile for safe charging over temperature
- BATFET control to support shutdown, ship mode and full system reset
  - 1.5-μA quiescent current in battery only mode
  - 0.15-μA battery leakage current in ship mode
  - 0.1-μA battery leakage current in shutdown
- Supports Boost Mode operation to power accesory
  - Boost Mode operation supporting 3.84-V to 5.2-V output
  - >90% boost efficiency down to 100-mA boost current for 5-V PMID
- Supports a wide range of input sources
  - 3.9-V to 18-V wide input operating voltage range with 26-V absolute maximum input voltage
  - Maximizes source power with input voltage regulation (VINDPM) and input current regulation (IINDPM)
  - VINDPM threshold automatically tracks battery voltage
- Efficient battery operation with 15-mΩ BATFET
- Narrow VDC (NVDC) power path management
  - System instant-on with depleted or no battery
  - Battery supplement when adapter is fully loaded
- Flexible autonomous or I²C-controlled modes
- Integrated 12-bit ADC for voltage, current, temperature monitoring
- High Accuracy
  - ±0.4% charge voltage regulation
  - ±5% charge current regulation
  - ±5% input current regulation
- Safety
  - Thermal regulation and thermal shutdown
  - Input, system, and battery overvoltage protection
  - Battery, and converter overcurrent protection
  - Charging safety timer

## 2 Applications

- Consumer Wearables, Smartwatch
- Portable Speakers, TWS Earphone
- Hearing Aid or TWS Charging Case

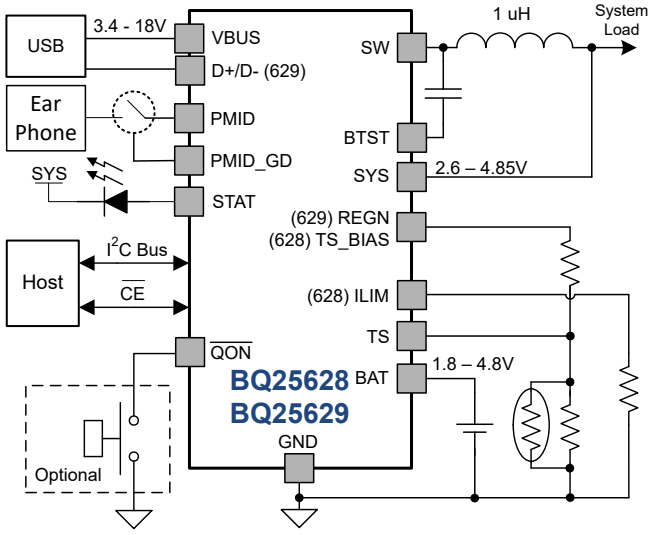
## 3 Description

The BQ25628 and BQ25629 are highly-integrated 2-A switch-mode battery charge management and system power path management devices for single cell Li-ion and Li-polymer batteries. The solution is highly integrated with built-in current sensing, loop compensation, input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4) between system and battery. The device uses narrow VDC power path management, regulating the system slightly above the battery voltage without dropping below a configurable minimum system voltage. The low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time, extends battery life during discharging phase, and the ultra-low 0.15-μA ship mode current extends battery shelf life. The I²C serial interface with charging and system settings makes BQ25628 and BQ25629 truly flexible solutions.

**Device Information**

| PART NUMBER | PACKAGE(1) | BODY SIZE (NOM) |
|---|---|---|
| BQ25628 | WQFN (18) | 2.50 mm × 3.00 mm |
| BQ25629 | WQFN (18) | 2.50 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**BQ25628/629 Simplified Application**

# Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| December 2022 | * | Initial Release |

## 5 Description (continued)

The BQ25628 supports a wide range of input sources, including standard USB host port, USB charging port, and USB compliant high voltage adapter. The BQ25629 has the ILIM pin to set the default input current limit and TS_BIAS pin for controlled thermistor bias. The device is compliant with USB 2.0 and USB 3.0 power specifications for input current and voltage regulation and meets the USB On-the-Go (OTG) operation power rating specification up to 2.0 A.

The power path management regulates the system slightly above battery voltage but does not drop below the programmable minimum system voltage. With this feature, the system maintains operation even when the battery is completely depleted or removed. When the input current limit or input voltage limit is reached, the power path management automatically reduces the charge current. As the system load continues to increase, the battery starts to discharge until the system power requirement is met. This supplement mode prevents overloading the input source.

The BQ25628 and BQ25629 power an accessory attached to PMID either directly from the adapter or from the battery in either boost or bypass OTG modes. Boost OTG provides a regulated voltage at PMID from the battery via boost operation in the converter. Bypass OTG provides a direct path from the battery to PMID for highest efficiency. The BQ25628 and BQ25629 may be configured to automatically transition into boost OTG mode when the adapter is removed, and back into forward charging when the adapter is attached in order to power PMID in either configuration without host intervention. In forward charging, boost OTG and bypass OTG, the PMID_GD signal indicates PMID voltage and current are within accepted ranges. PMID_GD may be used to drive an external PMOS FET to protect attached accessories by disconnecting them from PMID if an out-of-range voltage or current is detected.

The BQ25628 and BQ25629 initiate and complete a charging cycle without host control. By sensing the battery voltage, it charges the battery in four different phases: trickle charge, pre-charge, constant current (CC) charge and constant voltage (CV) charge. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset threshold and the battery voltage is higher than the recharge threshold. Termination is supported for all TS pin temperature zones.

The BQ25628 and BQ25629 provide various safety features for battery charging and system operations, including battery negative temperature coefficient thermistor monitoring, charging safety timer and overvoltage and overcurrent protections. The thermal regulation reduces charge current when the junction temperature exceeds the programmable threshold. The STAT output reports the charging status and any fault conditions. Other safety features include battery temperature sensing for charge mode and OTG boost mode, thermal shutdown and input UVLO and overvoltage protection. The $\overline{\text{INT}}$ output notifies the host when a fault occurs or status changes.

The BQ25628 and BQ25629 are available in a 18-pin, 2.5 mm × 3.0 mm WQFN package.

# 6 Device Comparison

**Table 6-1. Device Comparison**

| FUNCTION | BQ25618 | BQ25628 | BQ25629 |
|---|---|---|---|
| Input Voltage Range | 4V - 13.5V | 3.9V - 18V | 3.9V - 18V |
| Part Configuration | I2C | I2C | I2C |
| Programmable Charge Voltage | 3.5 - 4.3V (100mV per step); 4.3 - 4.52V (10mV per step) | 3.5 - 4.8V (10mV per step) | 3.5 - 4.8V (10mV per step) |
| D+/D- USB Detection | Yes | No | Yes |
| ILIM Pin | No | Yes | No |
| TS Profile | JEITA | JEITA | JEITA |
| Quiescent Battery Current | 9.5µA | 1.5µA | 1.5µA |
| OTG | Yes | Yes | Yes |
| OTG Voltage Range | 4.6V/4.75V/5V/5.15V | 3.84V - 5.2V (80mV per step) | 3.84V - 5.2V (80mV per step) |
| Package | 2x2.4mm$^2$ WCSP (30) | 2.5x3mm$^2$ QFN (18) | 2.5x3mm$^2$ QFN (18) |

# 7 Pin Configuration and Functions

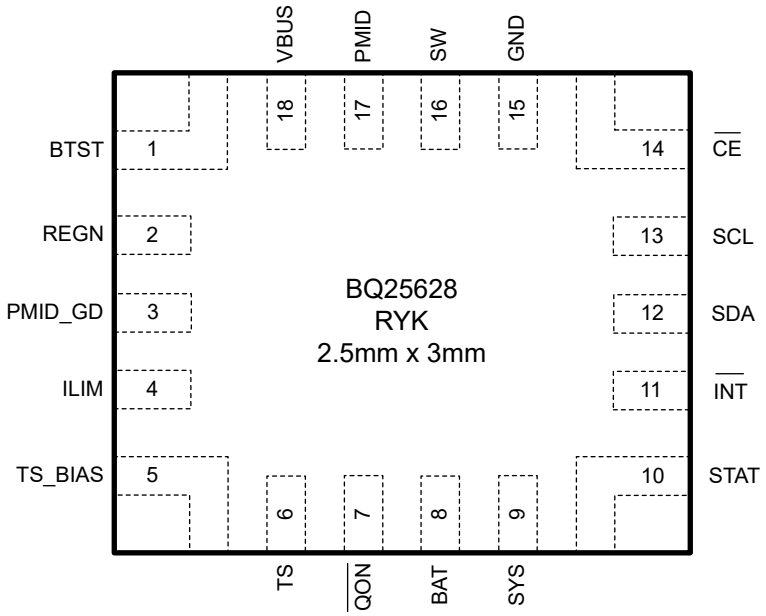



**Figure 7-1. BQ25628 Pinout, 18-Pin WQFN Top View**

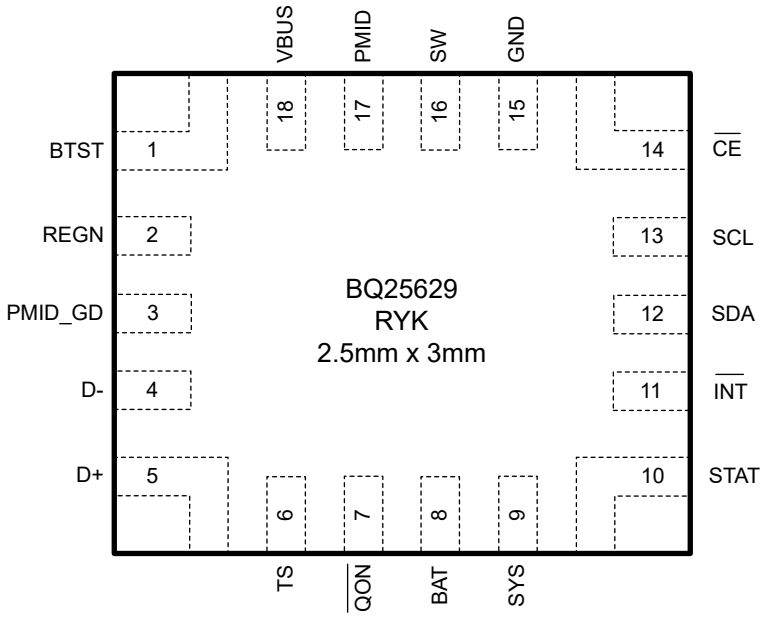



**Figure 7-2. BQ25629 Pinout, 18-Pin WQFN Top View**

**Table 7-1. Pin Functions**

| NAME | | NO. | TYPE[1] | DESCRIPTION |
|---|---|---|---|---|
| BQ25628 | BQ25629 | | | |
| BTST | | 1 | P | **High Side Switching MOSFET Gate Driver Power Supply –** Connect a 10V or higher rating, 47nF ceramic capacitor between SW and BTST as the bootstrap capacitor for driving high side switching MOSFET (Q2). |
| REGN | | 2 | P | **The Charger Internal Linear Regulator Output –** Internally, REGN is connected to the anode of the boost-strap diode. Connect a 10V or higher rating, 4.7µF ceramic capacitor from REGN to power ground, The capacitor should be placed close to the IC. The REGN LDO output is used for the internal MOSFETs gate driving voltage and for biasing the external TS pin thermistor in BQ25629. |

**Table 7-1. Pin Functions (continued)**

| NAME | | NO. | TYPE(1) | DESCRIPTION |
|---|---|---|---|---|
| BQ25628 | BQ25629 | | | |
| PMID_GD | | 3 | DO | **Open Drain Active High PMID Good Indicator –** Connect to the pull up rail REGN through 10 kΩ resistor. HIGH indicates PMID output voltage is good. This signal can be used to drive external PMOS FET to disconnect the PMID under charging load when boost mode output voltage is too high or output current is too high. |
| ILIM | D- | 4 | AIO | **Input Current Limit Setting Input Pin –** ILIM pin sets the input current limit as $I_{INREG}$ = $K_{ILIM}$ / $R_{ILIM}$, where $R_{ILIM}$ is connected from ILIM pin to GND. The input current is limited to the lower of the two values set by ILIM pin and IINDPM register bits. The ILIM pin can also be used to monitor input current. The input current is proportional to the voltage on ILIM pin and can be calculated by $I_{IN}$ = ($K_{ILIM}$ x $V_{ILIM}$) / ($R_{ILIM}$ x 0.8). The ILIM pin function is disabled when EN_EXTILIM bit is set to 0. |
| | | | | **Negative Line of the USB Data Line Pair –** D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2. |
| TS_BIAS | D+ | 5 | P | **Bias for the TS Resistor Voltage Divider –** Provides the bias voltage for the TS resistor voltage divider. |
| | | | AIO | **Positive Line of the USB Data Line Pair –** D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2. |
| TS | | 6 | AI | **Temperature Qualification Voltage Input –** Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from TS pin bias reference (REGN in BQ25629, TS_BIAS in BQ25628) to TS, then to GND. Charge suspends when TS pin voltage is out of range. Recommend a 103AT-2 10kΩ thermistor. |
| $\overline{QON}$ | | 7 | DI | **BATFET Enable or System Power Reset Control Input –** If the charger is in ship mode, a logic low on this pin with $t_{SM\_EXIT}$ duration forces the device to exit ship mode. If the charger is not in ship mode, a logic low on this pin with $t_{RST}$ initiates a full system power reset if either $V_{VBUS}$ < $V_{VBUS\_UVLO}$ or BATFET_CTRL_WVBUS = 1. $\overline{QON}$ has no effect during shutdown mode. The pin contains an internal pull-up to maintain default high logic. |
| BAT | | 8 | P | **The Battery Charging Power Connection –** Connect to the positive terminal of the battery pack. The internal BATFET is connected between SYS and BAT. |
| SYS | | 9 | P | **The Charger Output Voltage to System –**The Buck converter output connection point to the system. The internal BATFET is connected between SYS and BAT. |
| STAT | | 10 | DO | **Open Drain Charge Status Output –** It indicates various charger operations. Connect to the pull up rail via 10kΩ resistor. LOW indicates charging in progress. HIGH indicates charging completed or charging disabled. When any fault condition occurs, STAT pin blinks at 1Hz. Setting DIS_STAT = 1 disables the STAT pin function, causing the pin to be pulled HIGH. Leave floating if unused. |
| $\overline{INT}$ | | 11 | DO | **Open Drain Interrupt Output. –** Connect to the pull up rail via 10kΩ resistor. The $\overline{INT}$ pin sends an active low, 256μs pulse to the host to report the charger device status and faults. |
| SDA | | 12 | DIO | **I²C Interface Data –** Connect SDA to the logic rail through a 10 kΩ resistor. |
| SCL | | 13 | DI | **I²C Interface Clock –** Connect SCL to the logic rail through a 10 kΩ resistor. |
| $\overline{CE}$ | | 14 | DI | **Active Low Charge Enable Pin –** Battery charging is enabled when EN_CHG bit is 1 and $\overline{CE}$ pin is LOW. $\overline{CE}$ pin must be pulled HIGH or LOW, do not leave floating. |
| GND | | 15 | P | **Ground Return** |
| SW | | 16 | P | **Switching Node Connecting to Output Inductor –** Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 47 nF bootstrap capacitor from SW to BTST. |
| PMID | | 17 | P | **HSFET Drain Connection –** Internally PMID is connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. |
| VBUS | | 18 | P | **Charger Input Voltage –** The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. |

(1) AI = Analog input, AO = Analog Output, AIO = Analog input Output, DI = Digital input, DO = Digital Output, DIO = Digital input Output, P = Power

# 8 Specifications

## 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage range (with respect to GND) | VBUS (converter not switching) | –2 | 26 | V |
| | PMID (converter not switching) | –0.3 | 26 | V |
| | BAT, SYS (converter not switching) | –0.3 | 6 | V |
| | SW | –2 (50ns) | 21 | V |
| | BTST (when converter switching) | –0.3 | 27 | V |
| | $\overline{CE}$, STAT, SCL, SDA, $\overline{INT}$, REGN, $\overline{QON}$ | –0.3 | 6 | V |
| | D+, D-, ILIM, TS, TS_BIAS , PMID_GD | –0.3 | 6 | V |
| Output Sink Current | $\overline{INT}$, STAT, PMID_GD | | 6 | mA |
| Differential Voltage | BTST-SW | –0.3 | 6 | V |
| | PMID-VBUS | –0.3 | 6 | V |
| | SYS-BAT | –0.3 | 6 | V |
| $T_J$ | Junction temperature | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 8.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{VBUS}$ | Input voltage | 3.9 | | 18 | V |
| $V_{BAT}$ | Battery voltage | | | 4.8 | V |
| $I_{VBUS}$ | Input current | | | 3.2 | A |
| $I_{SW}$ | Output current (SW) | | | 3.5 | A |
| $I_{BAT}$ | Fast charging current | | | 3.5 | A |
| | RMS discharge current (continuously) | | | 6 | A |
| | Peak discharge current (up to 50ms) | | | 10 | A |
| $I_{REGN}$ | Maximum REGN Current | | | 20 | mA |
| $T_A$ | Ambient temperature | –40 | | 85 | °C |
| $T_J$ | Junction temperature | –40 | | 125 | °C |
| $L_{SW}$ | Inductor for the switching regulator | 0.68 | | 2.2 | µH |
| $C_{VBUS}$ | VBUS capacitor (without de-rating) | 1 | | | µF |
| $C_{PMID}$ | PMID capacitor (without de-rating) | 10 | | | µF |
| $C_{SYS}$ | SYS capacitor (without de-rating) | 20 | | 500 | µF |

## 8.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $C_{BAT}$ | BAT capacitor (without de-rating) | 10 | | | µF |

## 8.4 Thermal Information

| THERMAL METRIC(1) | | BQ25620, BQ25622 RYK (QFN) 18 pins | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 60.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 42.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 13.0 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 1.3 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 12.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 8.5 Electrical Characteristics

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$, $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **QUIESCENT CURRENTS** | | | | | | |
| $I_{Q\_BAT}$ | Quiescent battery current (BAT, SYS, SW) when the charger is in the battery only mode, BATFET is enabled, ADC is disabled | VBAT = 4V, No VBUS, BATFET is enabled, I2C enabled, ADC disabled, system is powered by battery. -40 °C < $T_J$ < 60 °C | | 1.5 | 3 | µA |
| $I_{Q\_BAT\_ADC}$ | Quiescent battery current (BAT, SYS, SW) when the charger is in the battery only mode, BATFET is enabled, ADC is enabled | VBAT = 4V, No VBUS, BATFET is enabled, I2C enabled, ADC enabled, system is powered by battery. -40 °C < $T_J$ < 60 °C | | 260 | | µA |
| $I_{Q\_BAT\_SD}$ | Quiescent battery current (BAT) when the charger is in shutdown mode, BATFET is disabled, ADC is disabled | VBAT = 4V, No VBUS, BATFET is disabled, I2C disabled, in shutdown mode, ADC disabled, $T_J$ < 60 °C | | 0.1 | 0.2 | µA |
| $I_{Q\_BAT\_SHIP}$ | Quiescent battery current (BAT) when the charger is in ship mode, BATFET is disabled, ADC is disabled | VBAT = 4V, No VBUS, BATFET is disabled, I2C disabled, in ship mode, ADC disabled, $T_J$ < 60 °C | | 0.15 | 0.5 | µA |
| $I_{Q\_VBUS}$ | Quiescent input current (VBUS) | VBUS = 5V, VBAT = 4V, charge disabled, converter switching, ISYS = 0A, PFM enabled | | 450 | | µA |
| $I_{Q\_VBUS\_HIZ}$ | Quiescent input current (VBUS) in HIZ | VBUS = 5V, VBAT = 4V, HIZ mode, ADC disabled | | 5 | 20 | µA |
| | | VBUS = 15V, VBAT = 4V, HIZ mode, ADC disabled | | 20 | 35 | µA |
| $I_{Q\_BOOST}$ | Quiescent battery current (BAT, SYS, SW) in boost mode | VBAT = 4.2V, VPMID = 5V, Boost mode enabled, converter switching, PFM enabled, $I_{VPMID}$ = 0A | | 220 | | µA |
| $I_{Q\_BYP\_OTG}$ | Quiescent battery current (BAT, SYS) in bypass OTG mode | VBAT = 4V, bypass OTG mode enabled, IPMID = 0A | | 500 | 850 | µA |
| **VBUS / VBAT SUPPLY** | | | | | | |
| $V_{VBUS\_OP}$ | VBUS operating range | | 3.9 | | 18 | V |
| $V_{VBUS\_UVLO}$ | VBUS falling to turn off I2C, no battery | VBUS falling | 3.0 | 3.15 | 3.3 | V |

## 8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ}$ < $V_{VBUS}$ < $V_{VBUS\_OVP}$, $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{VBUS\_UVLOZ}$ | VBUS rising for active I2C, no battery | VBUS rising | 3.2 | 3.35 | 3.5 | V |
| $V_{VBUS\_OVP}$ | VBUS overvoltage rising threshold | VBUS rising, VBUS_OVP = 0 | 6.1 | 6.4 | 6.7 | V |
| $V_{VBUS\_OVPZ}$ | VBUS overvoltage falling hreshold | VBUS rising, VBUS_OVP = 0 | 5.8 | 6.0 | 6.2 | V |
| $V_{VBUS\_OVP}$ | VBUS overvoltage rising threshold | VBUS rising, VBUS_OVP = 1 | 18.2 | 18.5 | 18.8 | V |
| $V_{VBUS\_OVPZ}$ | VBUS overvoltage falling threshold | VBUS falling, VBUS_OVP = 1 | 17.4 | 17.7 | 18.0 | V |
| $V_{PMID\_OVP}$ | Forward mode PMID OVP to drive PMID_GD low | $V_{PMID}$ rising | 5.5 | 5.75 | 6.0 | V |
| $V_{PMID\_OVPZ}$ | Forward mode PMID voltage threshold to exit OVP and drive PMID_GD high | $V_{PMID}$ falling | 5.25 | 5.5 | 5.75 | V |
| $V_{SLEEP}$ | Enter Sleep mode threshold | (VBUS - VBAT), VBUS falling | 9 | 45 | 85 | mV |
| $V_{SLEEPZ}$ | Exit Sleep mode threshold | (VBUS - VBAT), VBUS rising | 115 | 220 | 340 | mV |
| $V_{BAT\_UVLOZ}$ | BAT voltage for active I2C, turn on BATFET, no VBUS | VBAT rising | 2.3 | 2.4 | 2.5 | V |
| $V_{BAT\_UVLO}$ | BAT voltage to turnoff I2C, turn off BATFET, no VBUS | VBAT falling, VBAT_UVLO = 0 | 2.1 | 2.2 | 2.3 | V |
| | | VBAT falling, VBAT_UVLO = 1 | 1.7 | 1.8 | 1.9 | V |
| $V_{BAT\_OTG}$ | BAT voltage rising threshold to enable OTG mode | VBAT rising, VBAT_OTG_MIN = 0 | 2.9 | 3.0 | 3.1 | V |
| | | VBAT rising, VBAT_OTG_MIN = 1 | 2.5 | 2.6 | 2.7 | V |
| $V_{BAT\_OTGZ}$ | BAT voltage falling threshold to disable OTG mode | VBAT falling, VBAT_OTG_MIN = 0 | 2.7 | 2.8 | 2.9 | V |
| | | VBAT falling, VBAT_OTG_MIN = 1 | 2.3 | 2.4 | 2.5 | V |
| $V_{POORSRC}$ | Bad adapter detection threshold | VBUS falling | 3.6 | 3.7 | | V |
| $I_{POORSRC}$ | Bad adapter detection current source | | | 10 | | mA |
| **POWER-PATH MANAGEMENT** | | | | | | |
| $V_{SYS\_REG\_ACC}$ | Typical system voltage regulation | ISYS = 0A, VBAT > VSYSMIN, Charge Disabled. Offset above VBAT | | 50 | | mV |
| | | ISYS = 0A, $V_{BAT}$ < VSYSMIN, Charge Disabled. Offset above VSYSMIN | | 230 | | mV |
| $V_{SYSMIN\_RNG}$ | VSYSMIN register range | | 2.56 | | 3.84 | V |
| $V_{SYSMIN\_REG\_STEP}$ | VSYSMIN register step size | | | 80 | | mV |
| $V_{SYSMIN\_REG\_ACC}$ | Minimum DC system voltage output | ISYS = 0A, $V_{BAT}$ < VSYSMIN = B00h (3.52V), Charge Disabled | 3.52 | 3.75 | | V |
| $V_{SYS\_SHORT}$ | VSYS short voltage falling threshold to enter forced PFM | | | 0.9 | | V |
| $V_{SYS\_SHORTZ}$ | VSYS short voltage rising threshold to exit forced PFM | | | 1.1 | | V |
| **BATTERY CHARGER** | | | | | | |
| $V_{REG\_RANGE}$ | Typical charge voltage regulation range | | 3.50 | | 4.80 | V |
| $V_{REG\_STEP}$ | Typical charge voltage step | | | 10 | | mV |
| $V_{REG\_ACC}$ | Charge voltage accuracy | $T_J$ = 25°C | –0.3 | | 0.3 | % |
| | | $T_J$ = –10°C - 85°C | –0.4 | | 0.4 | % |
| $I_{CHG\_RANGE}$ | Typical charge current regulation range | | 0.04 | | 2.00 | A |
| $I_{CHG\_STEP}$ | Typical charge current regulation step | | | 40 | | mA |

## 8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ}$ < $V_{VBUS}$ < $V_{VBUS\_OVP}$, $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{CHG\_ACC}$ | Charge current accuracy | VBAT = 3.1V or 3.8V, ICHG = 1040mA, $T_J$ = –10°C - 85°C | –5.5 | | 5.5 | % |
| | | VBAT = 3.1V or 3.8V, ICHG = 320mA, $T_J$ = –10°C - 85°C | –5.5 | | 5.5 | % |
| | | VBAT = 3.1V or 3.8V, ICHG = 240mA, $T_J$ = –10°C - 85°C | –10 | | 10 | % |
| | | VBAT = 3.1V or 3.8V, ICHG = 80mA, $T_J$ = –10°C - 85°C | 60 | 80 | 100 | mA |
| $I_{PRECHG\_RANGE}$ | Typical pre-charge current range | | 10 | | 310 | mA |
| $I_{PRECHG\_STEP}$ | Typical pre-charge current step | | | 10 | | mA |
| $I_{PRECHG\_ACC}$ | Pre-charge current accuracy when $V_{BAT}$ below $V_{SYSMIN}$ setting | VBAT = 2.5V, IPRECHG = 250mA, $T_J$ = –10°C - 85°C | –12 | | 12 | % |
| | | VBAT = 2.5V, IPRECHG = 100mA, $T_J$ = –10°C - 85°C | –15 | | 15 | % |
| | | VBAT = 2.5V, IPRECHG = 50mA, $T_J$ = –10°C - 85°C | –25 | | 25 | % |
| $I_{TERM\_RANGE}$ | Typical termination current range | | 5 | | 310 | mA |
| $I_{TERM\_STEP}$ | Typical termination current step | | | 5 | | mA |
| $I_{TERM\_ACC}$ | Termination current accuracy | ITERM = 10mA, $T_J$ = –10°C - 85°C | –80 | | 80 | % |
| | | ITERM = 50mA, $T_J$ = –10°C - 85°C | –17 | | 17 | % |
| | | ITERM = 100mA, $T_J$ = –10°C - 85°C | –10 | | 10 | % |
| $V_{BAT\_SHORTZ}$ | Battery short voltage rising threshold to start pre-charge | VBAT rising | | 2.25 | | V |
| $V_{BAT\_SHORT}$ | Battery short voltage falling threshold to stop pre-charge | VBAT falling, VBAT_UVLO=0 | | 2.05 | | V |
| $V_{BAT\_SHORT}$ | Battery short voltage falling threshold to stop pre-charge | VBAT falling, VBAT_UVLO=1 | | 1.85 | | V |
| $I_{BAT\_SHORT}$ | Battery short trickle charging current | VBAT < $V_{BAT\_SHORTZ}$, ITRICKLE = 0 | 5 | 10 | 17 | mA |
| | | VBAT < $V_{BAT\_SHORTZ}$, ITRICKLE = 1 | 28 | 40 | 52 | mA |
| $V_{BAT\_LOWVZ}$ | Battery voltage rising threshold | Transition from pre-charge to fast charge | 2.9 | 3.0 | 3.1 | V |
| $V_{BAT\_LOWV}$ | Battery voltage falling threshold | Transition from fast charge to pre-charge | 2.7 | 2.8 | 2.9 | V |
| $V_{RECHG}$ | Battery recharge threshold below $V_{REG}$ | VBAT falling, VRECHG = 0 | | 100 | | mV |
| | | VBAT falling, VRECHG = 1 | | 200 | | mV |
| $I_{PMID\_LOAD}$ | PMID discharge load current | | 20 | 30 | | mA |
| $I_{BAT\_LOAD}$ | Battery discharge load current | | 20 | 30 | | mA |
| $I_{SYS\_LOAD}$ | System discharge load current | | 20 | 30 | | mA |
| **BATFET** | | | | | | |
| $R_{BATFET}$ | MOSFET on resistance from SYS to BAT | | | 15 | 25 | mΩ |
| **BATTERY PROTECTIONS** | | | | | | |
| $V_{BAT\_OVP}$ | Battery overvoltage rising threshold | As percentage of VREG | 103 | 104 | 105 | % |
| $V_{BAT\_OVPZ}$ | Battery overvoltage falling threshold | As percentage of VREG | 101 | 102 | 103 | % |
| $I_{BATFET\_OCP}$ | BATFET over-current rising threshold | | 6 | | | A |

## 8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ}$ < $V_{VBUS}$ < $V_{VBUS\_OVP}$, $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{BAT\_PK}$ | Battery discharging peak current rising threshold | IBAT_PK = 00 | 1.5 | | | A |
| | | IBAT_PK = 01 | 3 | | | A |
| | | IBAT_PK = 10 | 6 | | | A |
| | | IBAT_PK = 11 | 12 | | | A |
| **INPUT VOLTAGE / CURRENT REGULATION** | | | | | | |
| $V_{INDPM\_RANGE}$ | Typical input voltage regulation range | | 3.8 | | 16.8 | V |
| $V_{INDPM\_STEP}$ | Typical input voltage regulation step | | | 40 | | mV |
| $V_{INDPM\_ACC}$ | Input voltage regulation accuracy | VINDPM=4.6V | –4 | | 4 | % |
| | | VINDPM=8V | –3 | | 3 | % |
| | | VINDPM=16V | –2 | | 2 | % |
| $V_{INDPM\_BAT\_TRACK}$ | Battery tracking VINDPM accuracy | VBAT = 3.9V, VINDPM_BAT_TRACK=1, VINDPM = 4V | 4.15 | 4.3 | 4.45 | V |
| $I_{INDPM\_RANGE}$ | Typical input current regulation range | | 0.1 | | 3.2 | A |
| $I_{INDPM\_STEP}$ | Typical input current regulation step | | | 20 | | mA |
| $I_{INDPM\_ACC}$ | Input current regulation accuracy | IINDPM = 500mA, VBUS=5V | 450 | 475 | 500 | mA |
| | | IINDPM = 900mA, VBUS=5V | 810 | 855 | 900 | mA |
| | | IINDPM = 1500mA, VBUS=5V | 1350 | 1425 | 1500 | mA |
| $I_{VBUS\_OCP}$ | Forwrad mode VBUS overcurrent to drive PMID_GD low as a percentage of IINDPM | As a percentage of IINDPM | | 108 | | % |
| $K_{ILIM}$ | ILIM Pin Scale Factor, IINREG = $K_{ILIM}$ / $R_{ILIM}$ | INREG = 1.6 A | 2250 | 2500 | 2750 | AΩ |
| **D+ / D- DETECTION** | | | | | | |
| $V_{D+D-\_0p6V\_SRC}$ | D+/D- voltage source (600 mV) | 1 mA load on D+/D- | 400 | 600 | 800 | mV |
| $I_{D+D-\_LKG}$ | Leakage current into D+/D- | HiZ mode | –1 | | 1 | µA |
| $V_{D+D-\_2p8}$ | D+/D- comparator threshold for non-standard adapter | | 2.55 | | 2.85 | V |
| $V_{D+D-\_2p0}$ | D+/D- comparator threshold for non-standard adapter | | 1.85 | | 2.15 | V |
| **THERMAL REGULATION AND THERMAL SHUTDOWN** | | | | | | |
| $T_{REG}$ | Junction temperature regulation accuracy | TREG = 1 | | 120 | | °C |
| | | TREG = 0 | | 60 | | °C |
| $T_{SHUT}$ | Thermal Shutdown Rising Threshold | Temperature Increasing | | 140 | | °C |
| $T_{SHUT\_HYS}$ | Thermal Shutdown Falling Hysteresis | Temperature Decreasing by $T_{SHUT\_HYS}$ | | 30 | | °C |
| **THERMISTOR COMPARATORS (CHARGE MODE)** | | | | | | |
| $V_{TS\_COLD}$ | TS pin rising voltage threshold for TH1 comparator to transition from TS_COOL to TS_COLD. Charge suspended above this voltage. | As Percentage to TS pin bias reference (-5°C w/ 103AT), TS_TH1_TH2_TH3 = 100, 101, 110 | 75.0 | 75.5 | 76.0 | % |
| | | As Percentage to TS pin bias reference (0°C w/ 103AT), Fixed JEITA threshold or TS_TH1_TH2_TH3 = 000, 001, 010, 011, 111 | 72.8 | 73.3 | 73.8 | % |

## 8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ}$ < $V_{VBUS}$ < $V_{VBUS\_OVP}$, $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{TS\_COLDZ}$ | TS pin falling voltage threshold for TH1 comparator to transition from TS_COLD to TS_COOL. TS_COOL charge settings resume below this voltage. | As Percentage to TS pin bias reference (-2.5°C w/ 103AT), TS_TH1_TH2_TH3 = 100, 101, 110 | 73.9 | 74.4 | 74.9 | % |
| | | As Percentage to TS pin bias reference (2.5°C w/ 103AT), Fixed JEITA threshold or TS_TH1_TH2_TH3 = 000, 001, 010, 011, 111 | 71.7 | 72.2 | 72.7 | % |
| $V_{TS\_COOL}$ | TS pin rising voltage threshold for TH2 comparator to transition from TS_PRECOOL to TS_COOL. TS_COOL charging settings used above this voltage. | As Percentage to TS pin bias reference (5°C w/ 103AT), TS_ISET_COOL = 00 or TS_TH1_TH2_TH3 = 000, 100 | 70.6 | 71.1 | 71.6 | % |
| | | As Percentage to TS pin bias reference (10°C w/ 103AT), TS_ISET_COOL = 01 or TS_TH1_TH2_TH3 = 001, 101, 110, 111 | 67.9 | 68.4 | 68.9 | % |
| | | As Percentage to TS pin bias reference (15°C w/ 103AT), TS_ISET_COOL = 10 or TS_TH1_TH2_TH3 = 010 | 65.0 | 65.5 | 66.0 | % |
| | | As Percentage to TS pin bias reference (20°C w/ 103AT), TS_ISET_COOL = 11 or TS_TH1_TH2_TH3 = 011 | 61.9 | 62.4 | 62.9 | % |
| $V_{TS\_COOLZ}$ | TS pin falling voltage threshold for TH2 comparator to transition from TS_COOL to TS_PRECOOL. TS_PRECOOL charging settings resume below this voltage. | As Percentage to TS pin bias reference (7.5°C w/ 103AT), TS_ISET_COOL = 00 or TS_TH1_TH2_TH3 = 000, 100 | 69.3 | 69.8 | 70.3 | % |
| | | As Percentage to TS pin bias reference (12.5°C w/ 103AT), TS_ISET_COOL = 01 or TS_TH1_TH2_TH3 = 001, 101, 110, 111 | 66.6 | 67.1 | 67.6 | % |
| | | As Percentage to TS pin bias reference (17.5°C w/ 103AT), TS_ISET_COOL = 10 or TS_TH1_TH2_TH3 = 010 | 63.7 | 64.2 | 64.7 | % |
| | | As Percentage to TS pin bias reference (22.5°C w/ 103AT), TS_ISET_COOL = 11 or TS_TH1_TH2_TH3 = 011 | 60.6 | 61.1 | 61.6 | % |
| $V_{TS\_PRECOOL}$ | TS pin rising voltage threshold for TH3 comparator to transition from TS_NORMAL to TS_PRECOOL. TS_PRECOOL charge settings used above this voltage. | As Percentage to TS pin bias reference (15°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 001, 100, 101 | 65.0 | 65.5 | 66.0 | % |
| | | As Percentage to TS pin bias reference (20°C w/ 103AT), TS_TH1_TH2_TH3 = 010, 011, 110, 111 | 61.9 | 62.4 | 62.9 | % |
| $V_{TS\_PRECOOLZ}$ | TS pin falling voltage threshold for TH3 comparator to transition from TS_PRECOOL to TS_NORMAL. Normal charging resumes below this voltage. | As Percentage to TS pin bias reference (17.5°C w/ 103AT), TS_TH1_TH2_TH3 = 000, 001, 100, 101 | 63.7 | 64.2 | 64.7 | % |
| | | As Percentage to TS pin bias reference (22.5°C w/ 103AT), TS_TH1_TH2_TH3 = 010, 011, 110, 111 | 60.6 | 61.1 | 61.6 | % |
| $V_{TS\_PREWARM}$ | TS pin falling voltage threshold for TH4 comparator to transition from TS_NORMAL to TS_PREWARM. TS_PREWARM charging settings used below this voltage. | As Percentage to TS pin bias reference (35°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 001, 010, 100, 101 | 51.5 | 52.0 | 52.5 | % |
| | | As Percentage to TS pin bias reference (40°C w/ 103AT), TS_TH4_TH5_TH6 = 011, 110, 111 | 47.9 | 48.4 | 48.9 | % |

## 8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ}$ < $V_{VBUS}$ < $V_{VBUS\_OVP}$, $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{TS\_PREWARMZ}$ | TS pin rising voltage threshold for TH4 comparator to transition from TS_PREWARM to TS_NORMAL. Normal charging resumes above this voltage. | As Percentage to TS pin bias reference (32.5°C w/ 103AT), TS_TH4_TH5_TH6 = 000, 001, 010, 100, 101 | 53.3 | 53.8 | 54.3 | % |
| | | As Percentage to TS pin bias reference (37.5°C w/ 103AT), TS_TH4_TH5_TH6 = 011, 110, 111 | 49.2 | 49.7 | 50.2 | % |
| $V_{TS\_WARM}$ | TS pin falling voltage threshold for TH5 comparator to transition from TS_PREWARM to TS_WARM. TS_WARM charging settings used below this voltage. | As Percentage to TS pin bias reference (40°C w/ 103AT), TS_ISET_WARM = 00 or TS_TH4_TH5_TH6 = 000, 100 | 47.9 | 48.4 | 48.9 | % |
| | | As Percentage to TS pin bias reference (45°C w/ 103AT), TS_ISET_WARM = 01 or TS_TH4_TH5_TH6 = 001, 101, 110 | 44.3 | 44.8 | 45.3 | % |
| | | As Percentage to TS pin bias reference (50°C w/ 103AT), TS_ISET_WARM = 10 or TS_TH4_TH5_TH6 = 010, 111 | 40.7 | 41.2 | 41.7 | % |
| | | As Percentage to TS pin bias reference (55°C w/ 103AT), TS_ISET_WARM = 11 or TS_TH4_TH5_TH6 = 011 | 37.2 | 37.7 | 38.2 | % |
| $V_{TS\_WARMZ}$ | TS pin rising voltage threshold for TH5 comparator to transition from TS_WARM to TS_PREWARM. TS_PREWARM charging settings resume above this voltage. | As Percentage to TS pin bias reference (37.5°C w/ 103AT), TS_ISET_WARM = 00 or TS_TH4_TH5_TH6 = 000, 100 | 49.2 | 49.7 | 50.2 | % |
| | | As Percentage to TS pin bias reference (42.5°C w/ 103AT), TS_ISET_WARM = 01 or TS_TH4_TH5_TH6 = 001, 101, 110 | 45.6 | 46.1 | 46.6 | % |
| | | As Percentage to TS pin bias reference (47.5°C w/ 103AT), TS_ISET_WARM = 10 or TS_TH4_TH5_TH6 = 010, 111 | 42.0 | 42.5 | 43.0 | % |
| | | As Percentage to TS pin bias reference (52.5°C w/ 103AT), TS_ISET_WARM = 11 or TS_TH4_TH5_TH6 = 011 | 38.5 | 39 | 39.5 | % |
| $V_{TS\_HOT}$ | TS pin falling voltage threshold for TH6 comparator to transition from TS_WARM to TS_HOT. Charging is suspended below this voltage. | As Percentage to TS pin bias reference (50°C w/ 103AT), TS_TH4_TH5_TH6 = 100 or 101 | 40.7 | 41.2 | 41.7 | % |
| | | As Percentage to TS pin bias reference (60°C w/ 103AT), Fixed JEITA threshold or TS_TH4_TH5_TH6 = 000, 001, 010, 011, 110 or 111 | 33.9 | 34.4 | 34.9 | % |
| $V_{TS\_HOTZ}$ | TS pin rising voltage threshold for TH6 comparator to transition from TS_HOT to TS_WARM. TS_WARM charging settings resume above this voltage. | As Percentage to TS pin bias reference (47.5°C w/ 103AT), TS_TH4_TH5_TH6 = 100 or 101 | 42.0 | 42.5 | 43.0 | % |
| | | As Percentage to TS pin bias reference (57.5°C w/ 103AT), Fixed JEITA threshold or TS_TH4_TH5_TH6 = 000, 001, 010, 011, 110 or 111 | 35.2 | 35.7 | 36.2 | % |
| **THERMISTOR COMPARATORS (OTG MODE)** | | | | | | |
| $V_{TS\_OTG\_COLD}$ | TS pin rising voltage threshold to transition from TS_OTG_NORMAL to TS_OTG_COLD. OTG suspended above this voltage. | As Percentage to TS pin bias reference (–20°C w/ 103AT), TS_TH_OTG_COLD = 0 | 79.5 | 80.0 | 80.5 | % |
| | | As Percentage to TS pin bias reference (–10°C w/ 103AT), TS_TH_OTG_COLD = 1 | 76.6 | 77.1 | 77.6 | % |

## 8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$, $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{TS\_OTG\_COLDZ}$ | TS pin falling voltage threshold to transition from TS_OTG_COLD to TS_OTG_NORMAL. OTG resumes below this voltage. | As Percentage to TS pin bias reference (–15°C w/ 103AT), TS_TH_OTG_COLD = 0 | 78.2 | 78.7 | 79.2 | % |
| | | As Percentage to TS pin bias reference (–5°C w/ 103AT), TS_TH_OTG_COLD = 1 | 75.0 | 75.5 | 76.5 | % |
| $V_{TS\_OTG\_HOT}$ | TS pin falling voltage threshold to transition from TS_OTG_NORMAL to TS_OTG_HOT. OTG suspended below this voltage. | As Percentage to TS pin bias reference (55°C w/ 103AT), TS_OTG_HOT = 00 | 37.2 | 37.7 | 38.2 | % |
| | | As Percentage to TS pin bias reference (60°C w/ 103AT), TS_OTG_HOT = 01 | 33.9 | 34.4 | 34.9 | % |
| | | As Percentage to TS pin bias reference (65°C w/ 103AT), TS_OTG_HOT = 10 | 30.8 | 31.3 | 31.8 | % |
| $V_{TS\_OTG\_HOTZ}$ | TS pin rising voltage threshold to transition from TS_OTG_HOT to TS_OTG_NORMAL. OTG resumes above this threshold. | As Percentage to TS pin bias reference (52.5°C w/ 103AT), TS_OTG_HOT = 00 | 38.5 | 39.0 | 39.5 | % |
| | | As Percentage to TS pin bias reference (57.5°C w/ 103AT), TS_OTG_HOT = 01 | 35.2 | 35.7 | 36.2 | % |
| | | As Percentage to TS pin bias reference (62.5°C w/ 103AT), TS_OTG_HOT = 10 | 32.0 | 32.5 | 33.0 | % |
| **SWITCHING CONVERTER** | | | | | | |
| $F_{SW}$ | PWM switching frequency | Oscillator frequency | 1.35 | 1.5 | 1.65 | MHz |
| **MOSFET TURN-ON RESISTANCE** | | | | | | |
| $R_{Q1\_ON}$ | VBUS to PMID on resistance | $T_j$ = –40°C-85°C | | 26 | 34 | mΩ |
| $R_{Q2\_ON}$ | Buck high-side switching MOSFET turn on resistance between PMID and SW | $T_j$ = –40°C-85°C | | 55 | 78 | mΩ |
| $R_{Q3\_ON}$ | Buck low-side switching MOSFET turn on resistance between SW and PGND | $T_j$ = –40°C-85°C | | 60 | 90 | mΩ |
| **OTG MODE CONVERTER** | | | | | | |
| $V_{BOOST\_RANGE}$ | Typical boost mode voltage regulation range | | 3.8 | | 5.2 | V |
| $V_{BOOST\_STEP}$ | Typical boost mode voltage regulation step | | | 80 | | mV |
| $V_{BOOST\_ACC}$ | Boost mode voltage regulation accuracy | IVBUS = 0A, VOTG = 5V | –3 | | 3 | % |
| $V_{OTG\_UVP}$ | OTG mode undervoltage falling threshold at PMID | | | 3.4 | | V |
| $V_{OTG\_VBUS\_OVP}$ | OTG mode overvoltage rising threshold at VBUS | | 5.5 | 5.75 | 6.0 | V |
| $V_{BYPASS\_PMID\_OVP}$ | Bypass OTG Mode overvoltage rising threshold at PMID | As a percentage of VSYS | 105 | 107 | 109 | % |
| $V_{BOOST\_PMID\_OVP}$ | Boost OTG mode overvoltage rising threshold at PMID | As percentage of VOTG regulation | 105 | 107 | 109 | % |
| $I_{BYPASS\_RCP}$ | Bypass OTG Mode reverse current (from PMID to BAT) threshold | | 415 | 500 | 550 | mA |
| **REGN LDO** | | | | | | |
| $V_{REGN}$ | REGN LDO output voltage | $V_{VBUS}$ = 5V, $I_{REGN}$ = 20mA | 4.4 | 4.6 | | V |
| | | $V_{VBUS}$ = 9V, $I_{REGN}$ = 20mA | 4.8 | 5.0 | 5.2 | V |

## 8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ}$ < $V_{VBUS}$ < $V_{VBUS\_OVP}$, $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{REGNZ\_OK}$ | REGN not good falling threshold | Converter switching | | 3.2 | | V |
| | | Converter not switching | | 2.3 | | V |
| $I_{REGN\_LIM}$ | REGN LDO current limit | $V_{VBUS}$ = 5V, VREGN = 4.3V | 20 | | | mA |
| $I_{TS\_BIAS\_FAULT}$ | Rising threshold to transition from TSBIAS good condition to fault condition | REGN=5V; ISINK applied on TS_BIAS pin | 2.5 | 4.5 | 8 | mA |
| $I_{TS\_BIAS\_FAULTZ}$ | Falling threshold to transition from TSBIAS fault condition to good condition | REGN=5V; ISINK applied on TS_BIAS pin | 2 | 3.85 | 7 | mA |
| **ADC MEASUREMENT ACCURACY AND PERFORMANCE** | | | | | | |
| $t_{ADC\_CONV}$ | Conversion-time, Each Measurement | ADC_SAMPLE = 00 | | 24 | | ms |
| | | ADC_SAMPLE = 01 | | 12 | | ms |
| | | ADC_SAMPLE = 10 | | 6 | | ms |
| | | ADC_SAMPLE = 11 | | 3 | | ms |
| $ADC_{RES}$ | Effective Resolution | ADC_SAMPLE = 00 | 11 | 12 | | bits |
| | | ADC_SAMPLE = 01 | 10 | 11 | | bits |
| | | ADC_SAMPLE = 10 | 9 | 10 | | bits |
| | | ADC_SAMPLE = 11 | 8 | 9 | | bits |
| **ADC MEASUREMENT RANGE AND LSB** | | | | | | |
| IBUS_ADC | ADC Bus Current Reading (both forward and OTG) | Range | –4 | | 4 | A |
| | | LSB | | 2 | | mA |
| VBUS_ADC | ADC VBUS Voltage Reading | Range | 0 | | 19.85 | V |
| | | LSB | | 3.97 | | mV |
| VPMID_ADC | ADC PMID Voltage Reading | Range | 0 | | 19.85 | V |
| | | LSB | | 3.97 | | mV |
| VBAT_ADC | ADC BAT Voltage Reading | Range | 0 | | 5.572 | V |
| | | LSB | | 1.99 | | mV |
| VSYS_ADC | ADC SYS Voltage Reading | Range | 0 | | 5.572 | V |
| | | LSB | | 1.99 | | mV |
| IBAT_ADC | ADC BAT Current Reading | Range | -7.5 | | 4.0 | A |
| | | LSB | | 2 | | mA |
| TS_ADC | ADC TS Voltage Reading | Range as a percent of REGN (–40 °C to 85 °C for 103AT) | 20.9 | | 83.2 | % |
| | ADC TS Voltage Reading | LSB | | 0.0961 | | % |
| TDIE_ADC | ADC Die Temperature Reading | Range | –40 | | 150 | °C |
| | | LSB | | 0.5 | | °C |
| **I2C INTERFACE (SCL, SDA)** | | | | | | |
| $V_{IH}$ | Input high threshold level, SDA and SCL | | 0.78 | | | V |
| $V_{IL}$ | Input low threshold level, SDA and SCL | | | | 0.42 | V |
| $V_{OL\_SDA}$ | Output low threshold level | Sink current = 5mA, 1.2V VDD | | | 0.3 | V |
| $I_{BIAS}$ | High-level leakage current | Pull up rail 1.8V | | | 1 | µA |
| $C_{BUS}$ | Capacitive load for each bus line | | | | 400 | pF |
| **LOGIC OUTPUT PIN ($\overline{INT}$, STAT, PMID_GD)** | | | | | | |
| $V_{OL}$ | Output low threshold level | Sink current = 5mA | | | 0.3 | V |

## 8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ}$ < $V_{VBUS}$ < $V_{VBUS\_OVP}$, $T_J$ = -40°C to +125°C, and $T_J$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{OUT\_BIAS}$ | High-level leakage current | Pull up rail 1.8V | | | 1 | µA |
| **LOGIC INPUT PIN (CE, QON)** | | | | | | |
| $V_{IH\_CE}$ | Input high threshold level, /CE | | 0.78 | | | V |
| $V_{IL\_CE}$ | Input low threshold level, /CE | | | | 0.4 | V |
| $I_{IN\_BIAS\_CE}$ | High-level leakage current, /CE | Pull up rail 1.8V | | | 1 | µA |
| $V_{IH\_QON}$ | Input high threshold level, /QON | | 1.3 | | | V |
| $V_{IL\_QON}$ | Input low threshold level, /QON | | | | 0.4 | V |
| $V_{QON}$ | Internal /QON pull up | /QON is pulled up internally | | 5 | | V |
| $R_{QON}$ | Internal /QON pull up resistance | | | 250 | | kΩ |

## 8.6 Timing Requirements

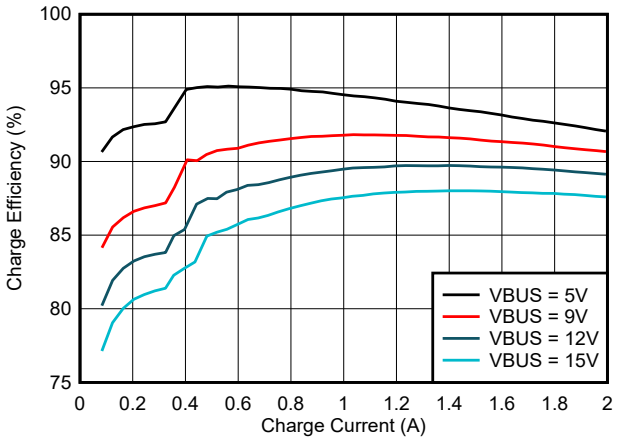
| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VBUS / VBAT POWER UP** | | | | | | |
| $t_{VBUS\_OVP\_PROP}$ | VBUS_OVP propagation delay to stop converter, VBUS rising (no deglitch) | | | 130 | | ns |
| $t_{VBUS\_OVP}$ | VBUS OVP deglitch time to set VBUS_OVP_STAT and VBUS_OVP_FLAG | | | 200 | | µs |
| $t_{POORSRC}$ | Bad adapter detection duration | | | 30 | | ms |
| $t_{POORSRC\_RETRY}$ | Bad adapter detection retry wait time | | | 2 | | s |
| $t_{POORSRC\_RESTART}$ | Restart the bad adapter detection after latchoff | | | 15 | | min |
| $t_{VBUS\_PD}$ | The duration of the pull down current source applied on VBUS | | | 30 | | ms |
| **BATTERY CHARGER** | | | | | | |
| $t_{TERM\_DGL}$ | Deglitch time for charge termination | | | 50 | | ms |
| $t_{RECHG\_DGL}$ | Deglitch time for recharge threshold at VBAT falling | | | 256 | | ms |
| $t_{PMID\_OVP\_PROP}$ | (SPEC ONLY) Propagation delay for PMID OVP in forward mode | | | 3 | | µs |
| $t_{PMID\_OVP\_FALL}$ | (SPEC ONLY) PMID OVP falling deglitch time in forward mode | | | 8 | | ms |
| $t_{TOP\_OFF}$ | Typical top-off timer accuracy | | 12 | 15 | 18 | min |
| | | | 24 | 30 | 36 | min |
| | | | 36 | 45 | 54 | min |
| $t_{SAFETY\_TRKCHG}$ | Charge safety timer accuracy in trickle charge | | 0.85 | 1 | 1.1 | hr |
| $t_{SAFETY\_PRECHG}$ | Charge safety timer accuracy in pre-charge | PRECHG_TMR = 0 | 1.75 | 2 | 2.2 | hr |
| | | PRECHG_TMR = 1 | 0.43 | 0.5 | 0.55 | hr |
| $t_{SAFETY}$ | Charge safety timer accuracy in fast charge | CHG_TMR = 0 | 10.5 | 11.5 | 12.5 | hr |
| | | CHG_TMR = 1 | 21.0 | 22.5 | 24.5 | hr |
| **BATFET CONTROL** | | | | | | |

## 8.6 Timing Requirements (continued)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{BATFET\_DLY}$ | Time after writing to BATFET_CTRL before BATFET turned off for ship mode or shutdown | BATFET_DLY = 1 | | 10 | | s |
| | | BATFET_DLY = 0 | | 20 | | ms |
| $t_{SM\_EXIT}$ | Deglitch time for $\overline{QON}$ to be pulled low in order to exit from Ship Mode | | 0.55 | 0.65 | 0.75 | s |
| $t_{QON\_RST}$ | Time $\overline{QON}$ is held low to initiate system power reset | | 9.0 | 10 | 11.5 | s |
| $t_{BATFET\_RST}$ | Duration that BATFET is disabled during system power reset | | | 350 | | ms |
| **I2C INTERFACE** | | | | | | |
| $f_{SCL}$ | SCL clock frequency | | | | 1.0 | MHz |
| **DIGITAL CLOCK AND WATCHDOG** | | | | | | |
| $t_{LP\_WDT}$ | Watchdog Reset time (EN_HIZ = 1, WATCHDOG = 160s) | | 100 | 160 | | s |
| $t_{WDT}$ | Watchdog Reset time (EN_HIZ = 0, WATCHDOG = 160s) | | 136 | 160 | | s |

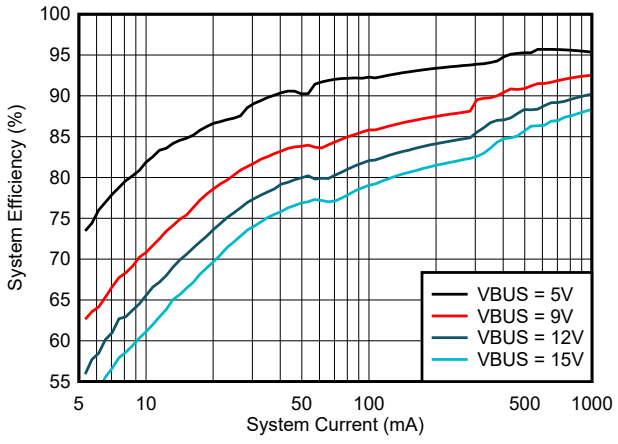
## 8.7 Typical Characteristics

$C_{VBUS}$ = 1µF, $C_{PMID}$= 10µF, $C_{SYS}$= 20µF, $C_{BAT}$= 1µF, L= 1µH (unless otherwise specified)



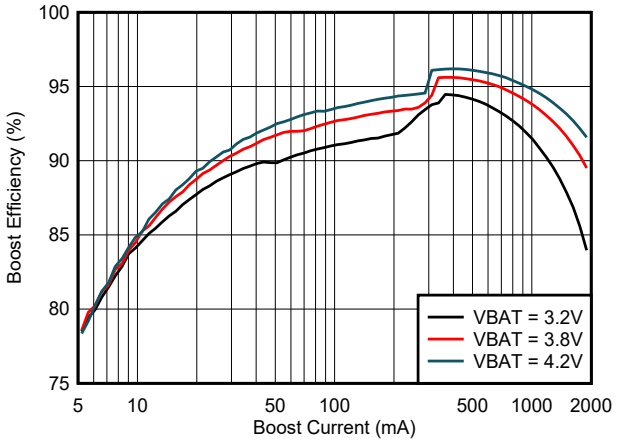

VBAT = 3.8 DCR = 15mΩ

**Figure 8-1. Charge Efficiency vs. Charge Current**



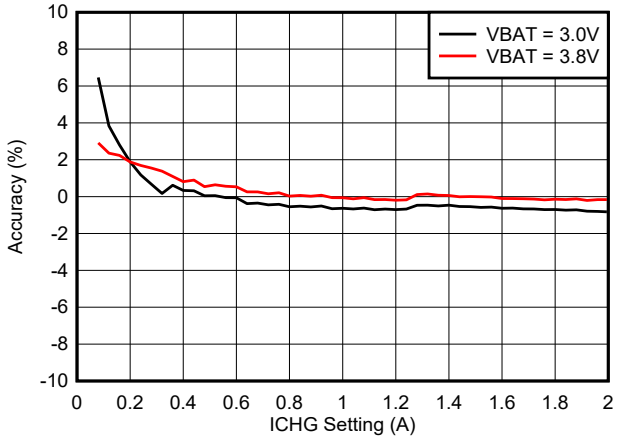

VSYSMIN = 3.52V DCR = 15mΩ

**Figure 8-2. System Light Load Efficiency vs. System Current**




VOTG = 5.04V DCR = 15mΩ

**Figure 8-3. Boost Mode Efficiency vs. Boost Output Current**




VBUS = 5V

**Figure 8-4. Charge Current Accuracy vs. ICHG Setting**

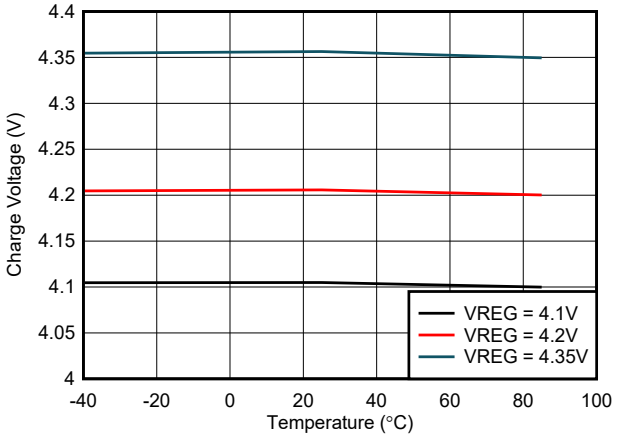
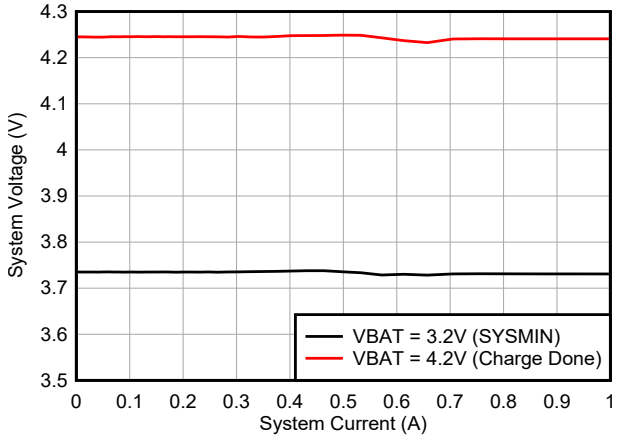



**Figure 8-5. Charge Voltage Accuracy vs. VREG Setting**

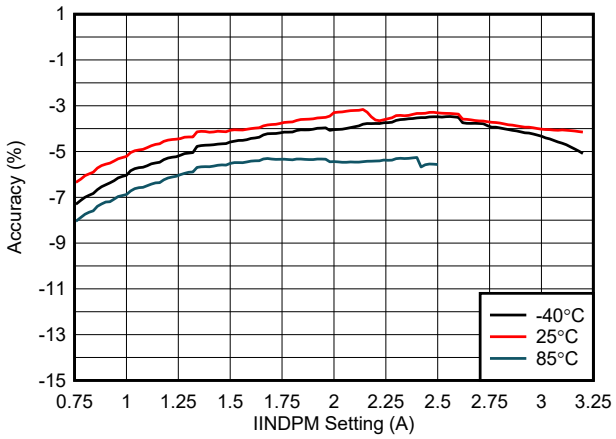



VBUS = 12V

**Figure 8-6. System Load Regulation for SYSMIN and After Charge Done**

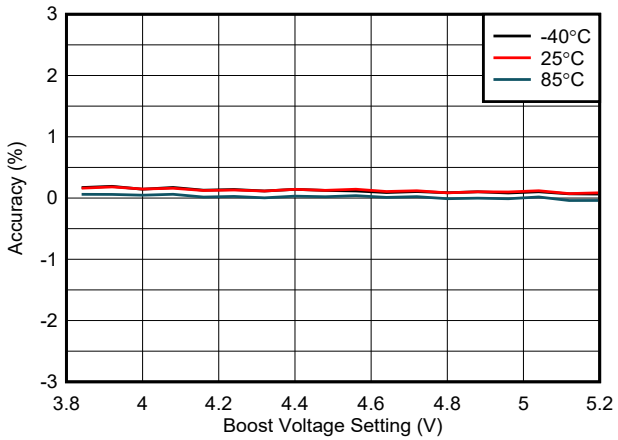
## 8.7 Typical Characteristics (continued)

$C_{VBUS}$ = 1µF, $C_{PMID}$= 10µF, $C_{SYS}$= 20µF, $C_{BAT}$= 1µF, L= 1µH (unless otherwise specified)




VBUS = 5V

**Figure 8-7. Input Current Regulation Accuracy vs. IINDPM Setting**




VBAT = 3.2V

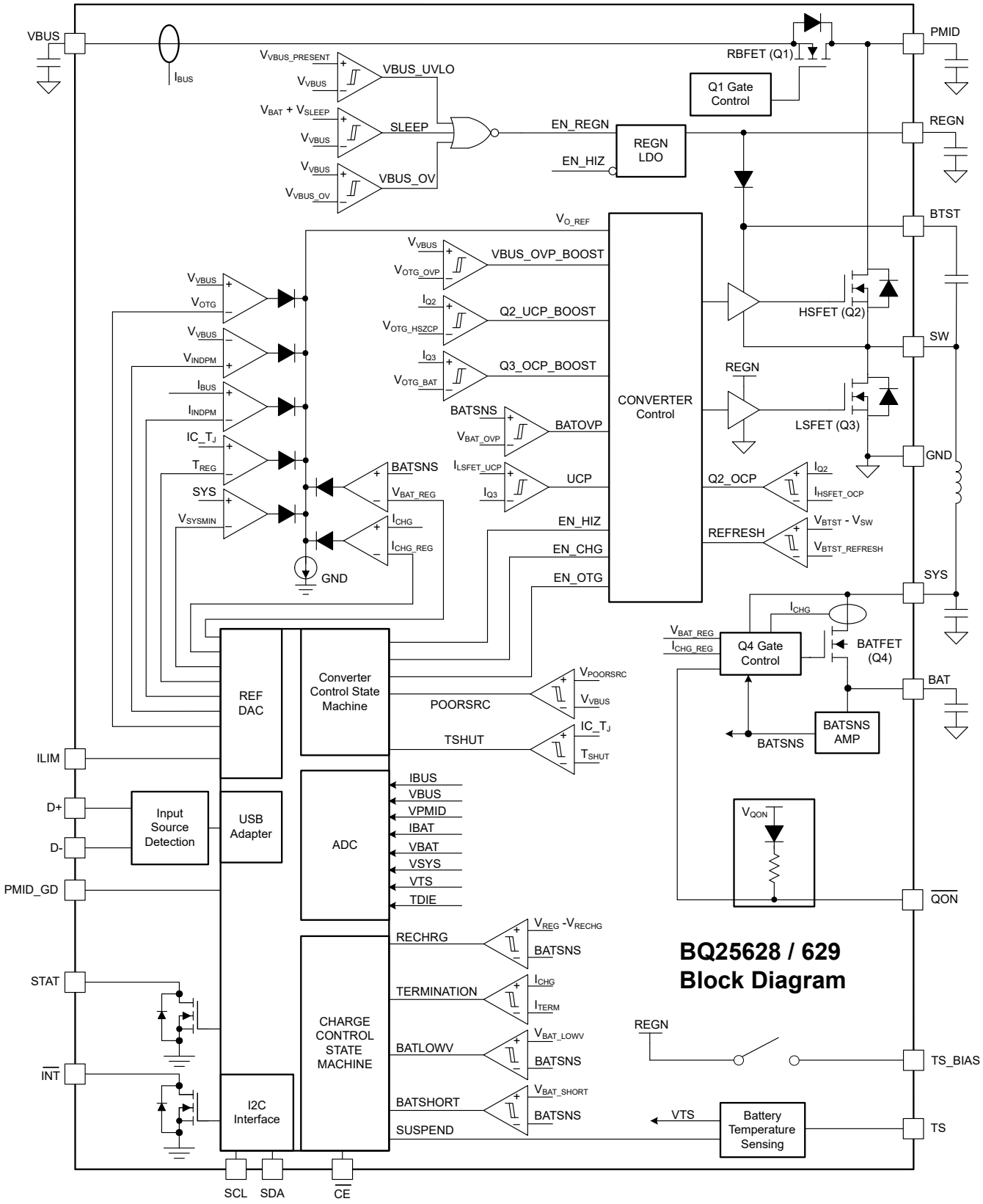
**Figure 8-8. Boost Voltage Regulation Accuracy vs Boost Voltage Setting**

# 9 Detailed Description

## 9.1 Overview

BQ25628 and BQ25629 are highly-integrated 2A switch-mode battery chargers for single-cell Li-ion and Li-polymer batteries. The device includes input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), battery FET (BATFET, Q4), and bootstrap diode for the high-side gate driver.

## 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Power-On-Reset (POR)

BQ25628 and BQ25629 power internal bias circuits from the higher voltage of VBUS and BAT. When either voltage rises above its undervoltage lockout (UVLO) threshold, all registers are reset to their POR values and the $I^2C$ interface is enabled for communication. A non-maskable $\overline{INT}$ pulse is generated, after which the host can access all of the registers.

### 9.3.2 Device Power Up from Battery

If only the battery is present and the VBAT is above depletion threshold ($V_{BAT\_UVLOZ}$), BQ25628 and BQ25629 perform a power-on reset then turns on the BATFET to connect the battery to system. The REGN LDO output remains off to minimize the quiescent current. The low RDSON of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

### 9.3.3 Device Power Up from Input Source

When a valid input source is plugged in with VBAT < $V_{BAT\_UVLOZ}$, BQ25628 and BQ25629 perform a power-on reset then checks the input source voltage to turn on the REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power up sequence from input source is as listed:

1. REGN LDO power up (Section 9.3.3.1)
2. Poor source qualification (Section 9.3.3.2)
3. Input voltage limit threshold setting (Section 9.3.3.5)
4. Converter power-up (Section 9.3.3.6)

#### *9.3.3.1 REGN LDO Power Up*

The REGN LDO regulator supplies internal bias circuits as well as the HSFET and LSFET gate drive. The REGN LDO also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN is enabled when all the below conditions are valid:

- VBUS above $V_{VBUS\_UVLOZ}$
- VBUS above $V_{BAT}$ + $V_{SLEEPZ}$
- EN_HIZ = 0
- After 220-ms delay is completed

If any one of the above conditions is not valid, the REGN LDO and the converter power stage remain off with the converter disabled. In this state, the battery supplies power to the system.

#### *9.3.3.2 Poor Source Qualification*

After the REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements in order to move forward to the next power on steps.

1. VBUS voltage below $V_{VBUS\_OVP}$
2. VBUS voltage above $V_{POORSRC}$ when pulling $I_{POORSRC}$

Once these conditions are met, BQ25628 and BQ25629 set VBUS_STAT to 0x4 and VBUS_FLAG transitions to 1.

#### *9.3.3.3 D+/D– Detection Sets Input Current Limit (BQ25629)*

After the REGN LDO is powered, the adapter has been qualified as a good source, and AUTO_INDET_EN bit = 1 (POR default), BQ25629 runs input source detection through D+/D– lines to detect USB Battery Charging Specification 1.2 (BC1.2) input sources (CDP / SDP / DCP) and non-standard adapters. The detection algorithm runs automatically each time that VBUS is plugged in, updating the IINDPM according to Table 9-2. If AUTO_INDET_EN = 0, the detection algorithm is not run and IINDPM remains unchanged. The host can force the detection algorithm to run and update IINDPM by setting FORCE_INDET to 1.

The USB BC1.2 is able to identify Standard Downstream Port (SDP), Charging Downstream Port (CDP), and Dedicated Charging Port (DCP). When the Data Contact Detection (DCD) timer of 500ms is expired, the non-standard adapter detection is applied to set the input current limit.

The secondary detection is used to distinguish two types of charging ports (CDP and DCP). Most of the time, a CDP requires the portable device (such as smart phone, tablet) to send back an enumeration within 2.5 seconds of CDP plug-in. Otherwise, the port reverts back to SDP even though the D+/D– detection indicates CDP.

Upon the completion of input source type detection, the following registers are changed:

1. Input Current Limit (IINDPM) register is changed to set current limit
2. VBUS_STAT bits are updated to indicate the detected input source type

After detection completes, the host can over-write the IINDPM register to change the input current limit if needed.

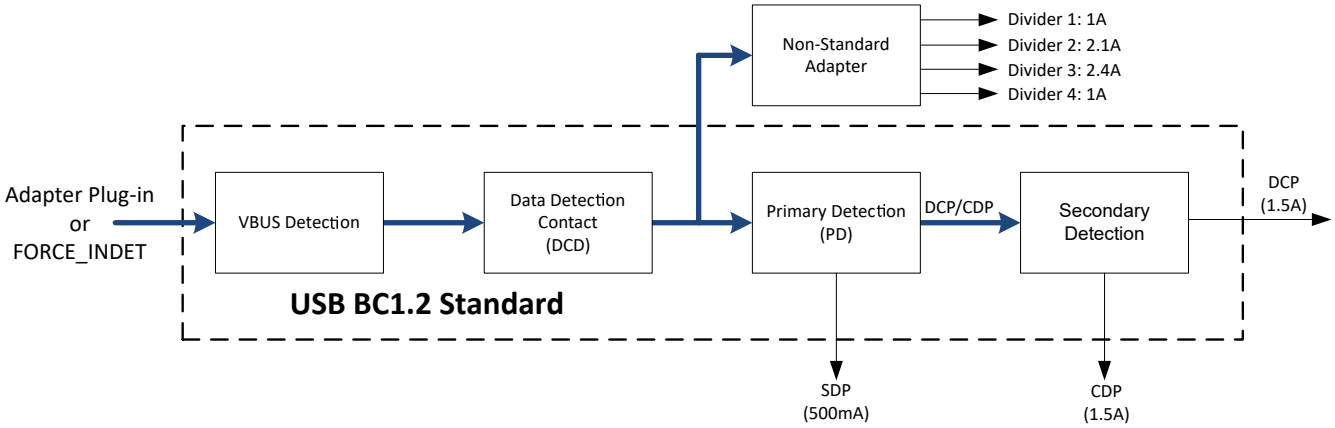



**Figure 9-1. D+/D– Detection Flow**

If DCP is detected (VBUS_STAT = 011), BQ25629 turns on $V_{D+D-\_0p6V\_SRC}$ on D+ if EN_DCP_BIAS is set to 1. Setting EN_DCP_BIAS to 0 while VBUS_STAT = 011 disables the $V_{D+D-\_0p6V\_SRC}$ on D+ pin, and setting EN_DCP_BIAS to 1 while VBUS_STAT = 011 enables the $V_{D+D-\_0p6V\_SRC}$ on D+ pin. The EN_HIZ bit has priority over EN_DCP_BIAS.

The non-standard detection is used to distinguish vendor specific adapters based on their unique dividers on the D+/D- pins. Comparators detect the voltage applied on each pin and determine the input current limit according to Table 9-1.

**Table 9-1. Non-Standard Adapter Detection**

| NON-STANDARD ADAPTER | D+ THRESHOLD | D– THRESHOLD | INPUT CURRENT LIMIT (A) |
|---|---|---|---|
| Divider 1 | $V_{D+}$ within $V_{D+D-\_2p0}$ | $V_{D-}$ within $V_{D+D-\_2p8}$ | 1 |
| Divider 2 | $V_{D+}$ within $V_{D+D-\_2p8}$ | $V_{D-}$ within $V_{D+D-\_2p0}$ | 2.1 |
| Divider 3 | $V_{D+}$ within $V_{D+D-\_2p8}$ | $V_{D-}$ within $V_{D+D-\_2p8}$ | 2.4 |

**Table 9-2. Input Current Limit Setting from D+/D– Detection**

| D+/D– DETECTION | INPUT CURRENT LIMIT (IINLIM) | VBUS_STAT |
|---|---|---|
| USB SDP (USB500) | 500 mA | 0x1 |
| USB CDP | 1.5 A | 0x2 |
| USB DCP | 1.5 A | 0x3 |
| Divider 1 | 1 A | 0x5 |
| Divider 2 | 2.1 A | 0x5 |
| Divider 3 | 2.4 A | 0x5 |
| Unknown 5-V Adapter | 500mA | 0x4 |

#### *9.3.3.4 ILIM Pin (BQ25628 Only)*

The ILIM pin clamps the input current limit to IINREG = $K_{ILIM}$ / $R_{ILIM}$, where $R_{ILIM}$ is connected from the ILIM pin to GND. The ILIM pin can be used to limit the input current limit from 100 mA - 3.2 A. The input current

is limited to the lower of the two values set by the ILIM pin and IINDPM register bits. The ILIM pin can also be used to monitor input current. The input current is proportional to the voltage on the ILIM pin and can be calculated by IIN = ($K_{ILIM}$ x $V_{ILIM}$) / ($R_{ILIM}$ x 0.8). The ILIM pin function is disabled when the EN_EXTILIM bit is set to 0. In BQ25628, if the ILIM pin voltage exceeds $V_{ILIM\_OCP}$ (900mV), the device detects input over current. The converter drives PMID_GD high and clears the OTG_FAULT_STAT bit to 0.

An RC filter in parallel with $R_{ILIM}$ is required when the input current setting on the ILIM pin is either:

- below 400 mA or
- above 2 A when using a 2.2-µH inductor

The value for the RC filter is 1.2 kΩ and 330 nF, respectively.

#### *9.3.3.5 Input Voltage Limit Threshold Setting (VINDPM Threshold)*

BQ25628 and BQ25629 support a wide range of input voltage limit (3.8 V – 16.8V). Its POR default VINDPM threshold is set at 4.6V. BQ25628 and BQ25629 also support dynamic VINDPM tracking, which tracks the battery voltage to ensure a sufficient margin between input and battery voltages for proper operation of the buck converter. This function is enabled via the VINDPM_BAT_TRACK register bit. When enabled, the actual input voltage limit is the higher of the VINDPM register or $V_{INDPM\_BAT\_TRACK}$ (VBAT + 400 mV typical offset.)

#### *9.3.3.6 Converter Power-Up*

After the input current and voltage limits are set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, the BATFET turns off. Otherwise, the BATFET stays on to charge the battery. Converter startup requires the following conditions:

- VBUS has passed poor source qualification ( Section 9.3.3.2 )
- VBUS > $V_{BAT}$ + $V_{SLEEPZ}$
- $V_{VBUS}$ < $V_{VBUS\_OVP}$
- EN_HIZ = 0
- $V_{SYS}$ < $V_{SYS\_OVP}$
- $T_J$ < $T_{SHUT}$

BQ25628 and BQ25629 provide soft start when the system rail is ramped up by setting IINDPM to its lowest programmable value and stepping up through each available setting until reaching the value set by IINDPM register. Concurrently, the system short protection limits the output current to approximately 0.5A when the system rail is below $V_{SYS\_SHORT}$.

These devices use a highly efficient 1.5 MHz, fixed frequency pulse width modulated (PWM) step-down switching regulator. The internally compensated feedback loop keep tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

The device switches to pulse frequency modulation (PFM) control at light load condition. The PFM_FWD_DIS and PFM_OTG_DIS bits can be used to disable the PFM operation in buck and boost respectively.

### 9.3.4 Power Path Management

BQ25628 accommodate a wide range of input sources from USB, wall adapter, wireless charger, to car charger. They provide automatic power path selection to supply the system from input source, battery, or both.

#### *9.3.4.1 Narrow VDC Architecture*

BQ25628 use the Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by VSYSMIN register setting. Even with a fully depleted battery, the system is regulated to the minimum system voltage. If charging is enabled, the BATFET operates in linear mode (LDO mode). The default minimum system voltage at POR is 3.52 V.

As the battery voltage rises above the minimum system voltage, the BATFET is turned fully on. When battery charging is disabled and $V_{BAT}$ is above the minimum system voltage setting, or charging is terminated, the system is regulated 50mV (typical) above battery voltage.

#### 9.3.4.2 Dynamic Power Management

To meet the USB maximum current limit and avoid overloading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When the input source is overloaded, either the current exceeds the input current limit (IINDPM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage by $V_{SUPP}$, the device automatically enters the supplement mode where the BATFET turns on and the battery starts discharging so that the system is supported from both the input source and battery.

#### 9.3.4.3 High Impedance Mode

The host may place BQ25628 into high impedance mode by writing EN_HIZ = 1. In high impedance mode, RBFET (Q1), HSFET (Q2) and LSFET (Q3) are turned off. The RBFET and HSFET block current flow to and from VBUS, putting the VBUS pin into a high impedance state. The BATFET (Q4) is turned on to connect the BAT to SYS. During high impedance mode, REGN is disabled and the digital clock is slowed to conserve power.

BQ25628 drives PMID_GD low in high-impedance mode.

### 9.3.5 Battery Charging Management

BQ25628 and BQ25629 charge 1-cell Li-Ion battery with up to 2.0 A charge current. The 15 mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

#### 9.3.5.1 Autonomous Charging Cycle

When battery charging is enabled (EN_CHG bit = 1 and $\overline{CE}$ pin is LOW), BQ25628 and BQ25629 autonomously complete a charging cycle without host involvement. The device default charging parameters are listed in Table 9-3. The host can always control the charging operations and optimize the charging parameters by writing to the corresponding registers through $I^2C$.

**Table 9-3. Charging Parameter Default Setting**

| | VREG | VRECHG | ITRICKLE | IPRECHG | ICHG | ITERM | TOPOFF TIMER |
|---|---|---|---|---|---|---|---|
| BQ25628 | 4.2V | VREG - 100 mV | 10 mA | 30 mA | 320 mA | 20 mA | Disabled |
| BQ25629 | 4.2V | VREG - 100 mV | 10 mA | 30 mA | 320 mA | 20 mA | Disabled |

A new charge cycle starts when the following conditions are valid:

- Converter starts per the conditions in Section 9.3.3.6
- EN_CHG = 1
- $\overline{CE}$ pin is low
- No thermistor fault on TS
- No safety timer fault

BQ25628 and BQ25629 automatically terminate the charging cycle when the charging current is below termination threshold, battery voltage is above recharge threshold, and device not is in DPM or thermal regulation. When a fully charged battery is discharged below VRECHG, the device automatically starts a new charging cycle. After charging terminates, toggling $\overline{CE}$ pin or EN_CHG bit also initiates a new charging cycle.

The STAT output indicates the charging status. Refer to Section 9.3.8.1 for details of STAT pin operation. In addition, the status register (CHG_STAT) indicates the different charging phases: 00-charging disabled or terminated, 01-constant current, 10 constant voltage, 11-topoff charging.

#### 9.3.5.2 Battery Charging Profile

BQ25628 and BQ25629 charges the battery in five phases: trickle charge, pre-charge, constant current, constant voltage and an optional top-off charging phase. At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

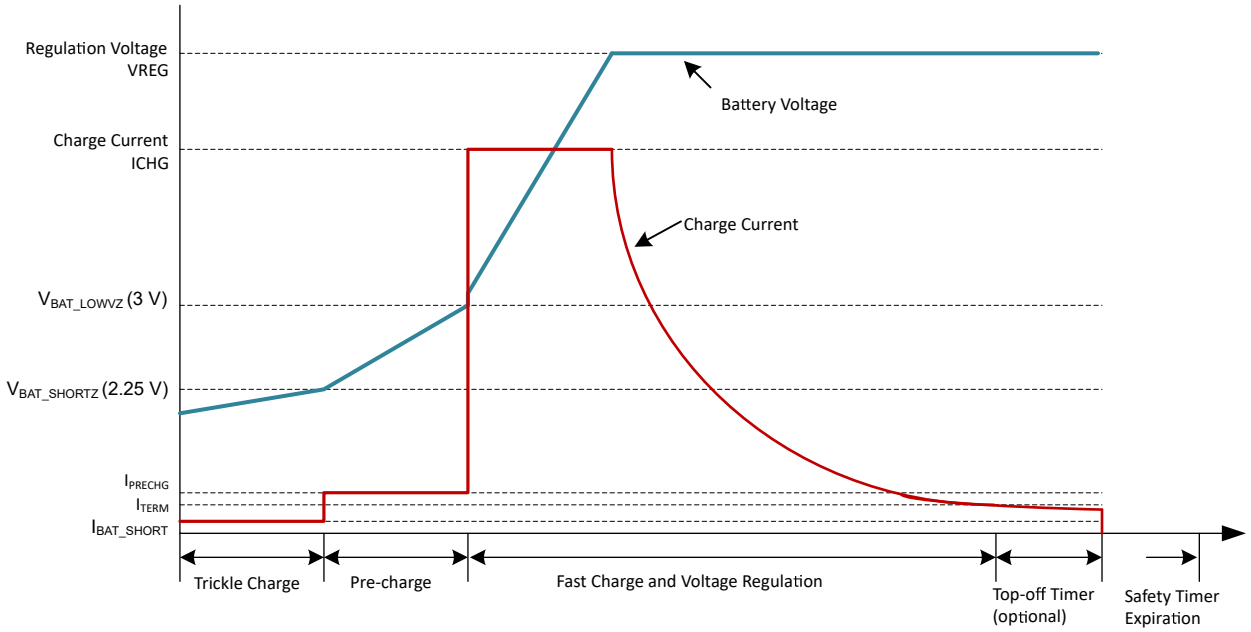



**Figure 9-2. Battery Charging Profile**

### *9.3.5.3 Charging Termination*

BQ25628 and BQ25629 terminate a charge cycle when the battery voltage is above recharge threshold, the converter is in constant-voltage regulation and the current is below ITERM. Because constant-voltage regulation is required for termination, BQ25628 and BQ25629 do not terminate while IINDPM, VINDPM or thermal regulation loops are active. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and the BATFET can turn on again to engage supplement mode. Termination can be permanently disabled by writing 0 to EN_TERM bit prior to charge termination.

At low termination currents, due to the comparator offset, the actual termination current may be 10 mA-20 mA higher than the termination target. in order to compensate for comparator offset, a programmable top-off timer can be applied after termination is detected. The top-off timer follows safety timer constraints, such that if the safety timers suspend, so does the top-off timer. Similarly, if the safety timers count at half-clock rate, so does the top-off timer. Refer to Section 9.3.5.5 for the list of conditions. The host can read CHG_STAT to find out the termination status.

Top-off timer gets reset by any of the following conditions:

1. Charging cycle stop and restart (toggle CE pin, toggle EN_CHG bit, charged battery falls below recharge threshold or adapter removed and replugged)
2. Termination status low to high
3. REG_RST register bit is set

The top-off timer settings are read in after is detected by the charger. Programming a top-off timer value after termination has no effect unless a recharge cycle is initiated. CHG_FLAG is set to 1 when entering top-off timer segment and again when the top-off timer expires.

### *9.3.5.4 Thermistor Qualification*

BQ25628 and BQ25629 provide a single thermistor input for battery temperature monitoring. The TS pin input of the battery temperature can be ignored by the charger if TS_IGNORE = 1. When the TS pin feedback is ignored, the charger considers the TS to always be valid for charging and OTG modes, and TS_STAT always reports 000. The TS pin may be left floating if TS_IGNORE is set to 1.

When TS_IGNORE=1, the TS_ADC channel is disabled, with TS_ADC_DIS forced to 1; Attempting to write to 0 is ignored.

When TS_IGNORE = 0, the charger adjusts the charging profile based on the TS pin feedback information according to the configurable profile described in Section 9.3.5.4.1. When the battery temperature crosses from one temperature range to another, TS_STAT is updated accordingly, and the charger sets the FLAG bit for the newly-entered temperature range. If TS_MASK is set to 0, any change to TS_STAT, including a transition to TS_NORMAL, generates an $\overline{INT}$ pulse.

#### 9.3.5.4.1 Advanced Temperature Profile in Charge Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges. As battery technology continues to evolve, battery manufacturers have released temperature safety specifications that extend beyond the JEITA standard. BQ25628 and BQ25629 feature a highly flexible temperature-based charging profile to meet these advanced specifications while remaining backwards compatible with the original JEITA standard. Figure 8-3 shows the programmability for charger behavior under different battery temperature (TS) operating regions.

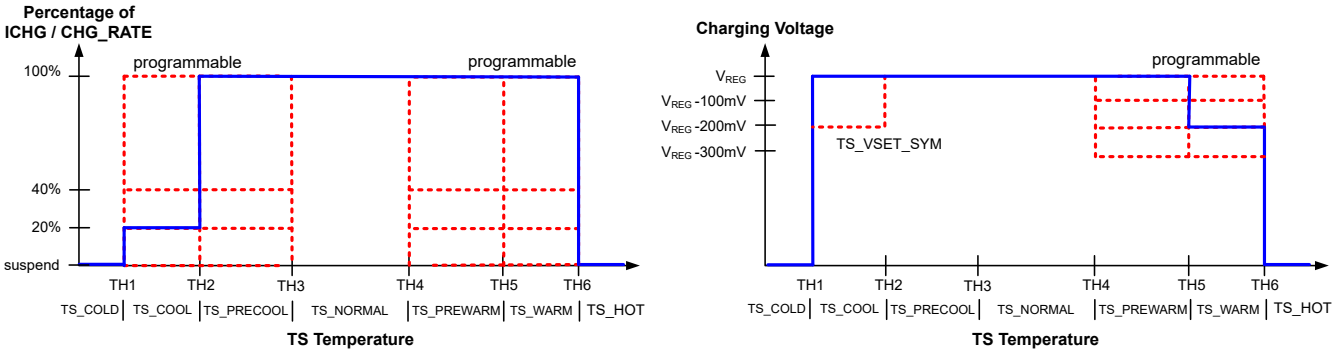



**Figure 9-3. TS Charging Values**

Charging safety timer is adjusted within the temperature zones to reflect changes to the charging current. When IPRECHG and ICHG are reduced to 20% or 40% in the cool or warm temperature zones, the charging safety timer counts at half rate. If charging is suspended, the safety timer is suspended, the STAT pin blinks and CHG_STAT is set to 00 (not charging or charge terminated.)

#### 9.3.5.4.2 TS Pin Thermistor Configuration

The typical TS resistor network is illustrated below.

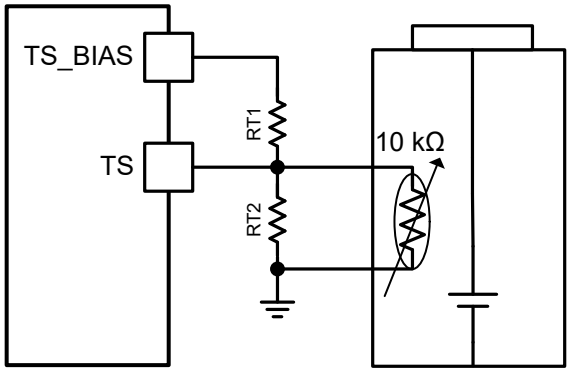



**Figure 9-4. TS Resistor Network**

The value of RT1 and RT2 are determined from the resistance of the thermistor at 0 and 60 ºC ($RTH_{0degC}$ and $RTH_{60degC}$) and the corresponding voltage thresholds $V_{TS\_0degC}$ and $V_{TS\_60degC}$ (expressed as percentage of REGN with value between 0 and 1.) For the most accurate thermistor curve fitting, use the rising threshold for

$V_{TS\_COLD}$ at 0 ºC and the falling threshold for $V_{TS\_HOT}$ at 60 ºC, regardless of the actual register settings for TS_TH1_TH2_TH3 and TS_TH4_TH5_TH6.

$$RT2 = \frac{RTH_{0degC} \times RTH_{60degC} \times \left(\frac{1}{V_{TS\_0degC}} - \frac{1}{V_{TS\_60degC}}\right)}{RTH_{60degC} \times \left(\frac{1}{V_{TS\_60degC}} - 1\right) - RTH_{0degC} \times \left(\frac{1}{V_{TS\_0degC}} - 1\right)} \quad (1)$$

$$RT1 = \frac{\frac{1}{V_{TS\_0degC}} - 1}{\frac{1}{R_{T2}} + \frac{1}{RTH_{0degC}}} \quad (2)$$

Assuming a 103AT NTC thermistor on the battery pack, the RT1 and RT2 are calculated to be 5.30 kΩ and 31.1 kΩ respectively.

If the thermistor is biased from TS_BIAS, the maximum current should be checked against $I_{TS\_BIAS\_FAULT}$. For the worst-case condition of thermistor at 0 Ω impedance (very hot), the bias current is :

$$I_{BIAS\_MAX} = \frac{V_{REGN}}{RT1} \quad (3)$$

For 5.30 kΩ RT1, this has a maximum $I_{BIAS}$ of 0.94 mA, which is well below the minimum $I_{TS\_BIAS\_FAULT}$ threshold. The 103AT NTC thermistor is the recommended thermistor and has 10 kΩ nominal impedance. Using a lower impedance thermistor will change the value of R1 and may produce a bias current that exceeds the TS_BIAS pin fault threshold. TS_STAT[2:0] is set to 111.

#### 9.3.5.4.3 Cold/Hot Temperature Window in OTG Mode

For battery protection during boost OTG and bypass OTG modes, BQ25628 and BQ25629 monitor the battery temperature to be within the TS_TH_OTG_COLD to TS_TH_OTG_HOT register settings. For a 103AT NTC thermistor with RT1 of 5.3 kΩ and RT2 of 31.1 kΩ, TS_TH_OTG_COLD default is -10°C and TS_TH_OTG_HOT default is 60°C. When temperature is outside of this range, the OTG mode is suspended with REGN remaining on. In addition, VBUS_STAT bits are set to 000, TS_STAT is set to 001 (TS_OTG_COLD) or 010 (TS_OTG_HOT), and TS_FLAG is set. In bypass OTG, PMID_GD drives low and the HSFET is disabled. Once the battery temperature returns to normal temperature, the boost OTG or bypass OTG is restarted and TS_STAT returns to 000 (TS_NORMAL).

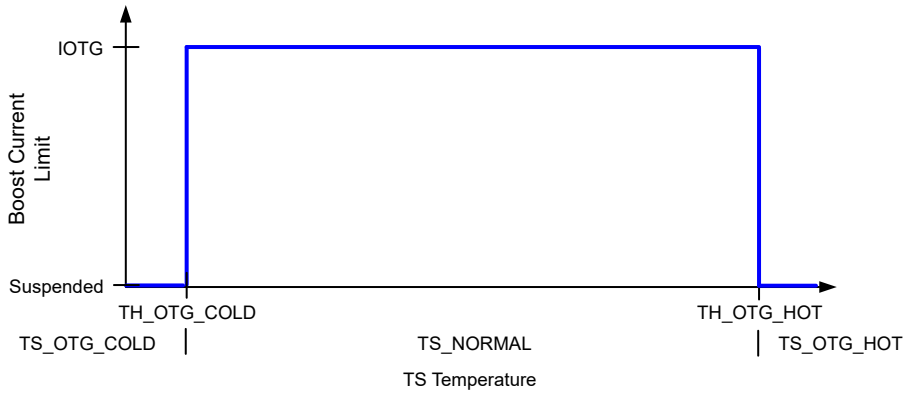



**Figure 9-5. TS Pin Thermistor Sense Threshold in Boost Mode**

#### 9.3.5.4.4 JEITA Charge Rate Scaling

The TS_ISET_PRECOOL, TS_ISET_COOL, TS_ISET_PREWARM and TS_ISET_WARM cool and warm charge current fold backs are based on a 1C charging rate.

A setting of TS_ISET_COOL = 01 sets $I_{CHG\_COOL}$ = 20% $ICHG_{1C}$. When the battery enters the TS_COOL temperature zone, the current is reduced to 20% of the 1C charging rate. In order to convert the charging

foldback, the host must set the CHG_RATE register to the C rate for the battery. This scales the fold back accordingly, producing an $I_{CHG\_COOL}$ as shown in Equation 4:

$$I_{CHG} = \frac{I_{CHG\_COOL}}{CHG\_RATE} \times JEITA\_ISETC \quad (4)$$

When TS_ISET_PRECOOL, TS_ISET_COOL, TS_ISET_PREWARM or TS_ISET_WARM is set to either 00 (suspend) or 11 (unchanged), the CHG_RATE setting has no effect. A summary is provided in Table 9-4.

**Table 9-4. ICHG Fold Back**

| TS_ISET_PRECOOL, TS_ISET_COOL, TS_ISET_PREWARM or TS_ISET_WARM | CHG_RATE | FOLD-BACK CURRENT AS PERCENTAGE OF ICHG |
|---|---|---|
| 00 | Any | 0% (Suspended) |
| 01 (20%) | 00 (1C) | 20% |
| | 01 (2C) | 10% |
| | 10 (4C) | 5% |
| | 11 (6C) | 3.3% |
| 10 (40%) | 00 (1C) | 40% |
| | 01 (2C) | 20% |
| | 10 (4C) | 10% |
| | 11 (6C) | 6.6% |
| 11 | Any | 100% |

#### 9.3.5.4.5 TS_BIAS Pin

The BQ25628 has the TS_BIAS pin to isolate the battery temperature sensing thermistor and associated resistor-divider from REGN. The 103AT thermistor with typical resistor-divider network requires about 400 µA to bias. The BQ25628 provides the TS_BIAS pin, which is internally connected to the REGN LDO via a back-to-back MOSFET switch. When no temperature measurement is being taken, the switch is disabled to disconnect the thermistor and resistor-divider from the REGN LDO, saving the 400 µA bias current from being expended unnecessarily.

The TS_BIAS pin has short-circuit protection. If a short is detected on the TS_BIAS pin, the switch is disabled to disconnect the short from REGN. If this condition occurs, TS_STAT register is set to 0x3. Charging and OTG modes are suspended until the short is removed.

### *9.3.5.5 Charging Safety Timers*

BQ25628 and BQ25629 have three built-in safety timers to prevent extended charging cycle due to abnormal battery conditions. The fast charge safety timer and pre-charge safety timers are set through $I^2C$ CHG_TMR and PRECHG_TMR fields, respectively. The trickle charge timer is fixed at 1 hour.

The trickle charging, pre-charging and fast charging safety timers can be disabled by setting EN_SAFETY_TMRS = 0. EN_SAFETY_TMRS can be enabled anytime regardless of which charging stage the charger is in. Each timer starts to count as soon as the following two conditions are simultaneously true: EN_SAFETY_TMRS=1 and the corresponding charging stage is active.

When either the fast charging, trickle charging or pre-charging safety timer expires, the SAFETY_TMR_STAT and SAFETY_TMR_FLAG bits are set to 1.

Events that cause a reduction in charging current also cause the charging safety timer to count at half-clock rate if TMR2X_EN bit is set.

During faults which suspend charging, the charge, pre-charge and trickle safety timers are also suspended, regardless of the state of the TMR2X_EN bit. Once the fault goes away, charging resumes and the safety timer resumes from where it stopped.

The charging safety timer and the charging termination can be disabled at the same time. Under this condition, the charging keeps running until it is disabled by the host.

### 9.3.6 USB On-The-Go (OTG)

#### *9.3.6.1 Boost OTG Mode*

BQ25628 and BQ25629 support boost converter operation to deliver power from the battery to PMID. The output voltage is set in VOTG. VBUS_STAT is set to 111 upon a successful entry into boost OTG. The boost operation is enabled when the following conditions are met:

1. BAT above $V_{BAT\_OTG}$
2. VBUS less than $V_{BAT}$+$V_{SLEEP}$
3. Boost mode operation is enabled (EN_OTG = 1)
4. $V_{TS\_OTG\_HOT} < V_{TS} < V_{TS\_OTG\_COLD}$
5. $V_{REGN} > V_{REGN\_OK}$
6. 30 ms delay after EN_OTG = 1
7. Boost mode regulation voltage in REG0x0C is greater than 105% of battery voltage.

#### *9.3.6.2 Bypass OTG Mode*

In addition to boost OTG mode, the BQ25628 and BQ25629 provide bypass mode to directly connect the battery to PMID pin through BATFET and HSFET. The low impedance path in bypass mode achieves the highest efficiency when powering up external accessories, and maximizes the battery run time. During bypass OTG mode, the status register VBUS_STAT is set to 111.

Bypass OTG mode is entered when:

- $V_{BAT} > V_{BAT\_OTG}$
- $V_{VBUS} < V_{BAT}$+$V_{SLEEP}$
- OTG mode has been enabled (EN_OTG=1) and bypass mode is enabled (EN_BYPASS_OTG=1).
- $V_{TS\_OTG\_HOT} < V_{TS} < V_{TS\_OTG\_COLD}$
- $V_{REGN} > V_{REGN\_OK}$
- 30 ms delay after EN_OTG = EN_BYPASS_OTG = 1, bypass OTG is enabled by turning on HSFET and BATFET.

Any of the following conditions will exit from bypass OTG. Unless otherwise indicated, exit from bypass mode leads into battery-only mode by setting EN_OTG = EN_BYPASS_OTG = 0:

- OTG mode is disabled (EN_OTG=0)
- Bypass OTG mode is disabled (EN_BYPASS_OTG = 0) will cause exit into boost OTG mode if EN_OTG remains at 1.
- Entry into shutdown, ship mode or system power reset will exit from bypass OTG by setting EN_OTG = EN_BYPASS_OTG = 0 and then enter into shutdown, ship mode or system power reset as selected.

BQ25628 and BQ25629 can be configured to automatically transition between charging mode and bypass OTG mode by setting EN_CHG = 1, EN_OTG = 1 and EN_BYPASS_OTG = 1. When the adapter plugs in, and all conditions to start a new charge cycle are valid, the device automatically transitions to charging mode. If the adapter is removed and bypass enable conditions are valid, the device automatically transitions to bypass OTG mode to power the accessories connected to PMID.

#### *9.3.6.3 PMID Voltage Indicator ( PMID_GD)*

In BQ25628 and BQ25629, accessory devices can be connected to charger PMID pin to get power either from the adapter through Q1 direct path or from battery boost mode. An optional external PMOS FET can be placed between the PMID pin and accessory input to disconnect the power path during over-current and over-voltage conditions. PMID_GD is used to drive this external PMOS FET through an inverter. PMID_GD HIGH turns on an inverter to pull the PMOS FET gate low to turn on PMOS FET, and PMID_GD LOW turns off the PMOS FET.

Upon adapter plug-in, PMID_GD goes from LOW to HIGH when VBUS rises above $V_{BAT}$ but below $V_{PMID\_OVP}$ and passes poor source detection. An adapter voltage that is greater than $V_{PMID\_OVP}$ but less than $V_{VBUS\_OVP}$ will drive PMID_GD low, but will charge the battery if all other conditions are valid. In this state, the external PMOS FET will stay off to protect the accessory from over-voltage fault.

When the adapter is removed, PMID_GD goes LOW before battery boost mode starts. In battery boost mode, the device regulates PMID voltage to the VOTG register setting as a stable power supply to the accessory devices. PMID_GOOD goes from LOW to HIGH when PMID voltage rises above $V_{OTG\_UVPZ}$. Once PMID voltage is out of this range, PMID_GOOD goes LOW to disconnect the accessory device from PMID. During boost mode, any of the conditions to exit boost mode will also drive PMID_GD from HIGH to LOW. See Section 9.3.6.1 for a list of these conditions.

If the device enters bypass OTG mode, the PMID_GD goes from LOW to HIGH when HSFET (Q2) is enabled. During bypass OTG mode, any conditions to exit will also drive PMID_GD from HIGH to LOW. See Section 9.3.6.2 for a list of these conditions.

### 9.3.7 Integrated 12-Bit ADC for Monitoring

BQ25628 provide an integrated 12-bit ADC for the host to monitor various system parameters.

To enable the ADC, the ADC_EN bit must be set to ‘1’. The ADC is disabled by default (ADC_EN=0) to conserve power. The ADC is allowed to operate if either VBUS > $V_{POORSRC}$ or VBAT > $V_{BAT\_LOWV}$ is valid. If ADC_EN is set to ‘1’ before VBUS or VBAT reach their respective valid thresholds, then ADC_EN stays '0'. When the charger enters HIZ mode, the ADC is disabled. The host can re-enable the ADC during HIZ mode by setting ADC_EN =1.

At battery only condition, if the TS_ADC channel is enabled, the ADC only operates when the battery voltage is higher than 3.2V (the minimal value to turn on REGN), otherwise, the ADC operates when the battery voltage is higher than $V_{BAT\_LOWV}$.

The ADC_DONE_STAT, ADC_DONE_FLAG bits are set when a conversion is complete in one-shot mode only. During continuous conversion mode, the ADC_DONE_STAT, ADC_DONE_FLAG bits have no meaning and remain at 0. In one-shot mode, the ADC_EN bit is set to 0 at the completion of the conversion, at the same time as the ADC_DONE_FLAG bit is set. In continuous mode, the ADC_EN bit remains at 1 until the user disables the ADC by setting it to 0.

### 9.3.8 Status Outputs ( STAT, $\overline{INT}$)

#### *9.3.8.1 Charging Status Indicator (STAT)*

BQ25628 indicates charging state on the open drain STAT pin. The STAT pin can drive an LED. The STAT pin function can be disabled via the DIS_STAT bit.

**Table 9-5. STAT Pin State**

| CHARGING STATE | STAT INDICATOR |
|---|---|
| Charging in progress (including recharge) | LOW |
| Not charging, no fault detected. (Includes charging complete, Charge Disabled, no adapter present, in OTG mode.) | HIGH |
| Charge suspend<br>Boost Mode suspend | Blinking at 1 Hz |

#### *9.3.8.2 Interrupt to Host ( $\overline{INT}$)*

In many applications, the host does not continually poll the charger status registers. Instead, the INT pin may be used to notify the host of a status change with a 256-µs $\overline{INT}$ pulse. Upon receiving the interrupt pulse, the host may read the flag registers (Charger_Flag_X and FAULT_Flag_X) to determine the event that caused the interrupt, and for each flagged event, read the corresponding status registers (Charger_Status_X and FAULT_Status_X) to determine the current state. Once set to 1, the flag bits remain latched at 1 until they are read by the host, which clears them. The status bits, however, are updated whenever there is a change to status and always represent the current state of the system.

All of the $\overline{INT}$ events can be masked off to prevent $\overline{INT}$ pulses from being sent out when they occur, with the exception of the initial power-up interrupt. Interrupt events are masked by setting their mask bit in registers (Charger_Mask_X and FAULT_Mask_X.) Events always cause the corresponding flag bit to be set to 1, regardless of whether or not the interrupt pulse has been masked.

### 9.3.9 BATFET Control

BQ25628 and BQ25629 have an integrated, bi-directionally blocking BATFET that can be turned off to remove leakage current from the battery to the system. The BATFET is controlled by the BATFET_CTRL register bits, and supports shutdown mode, ship mode and system power reset.

**Table 9-6. BATFET Control Modes**

| MODE | BATFET | I²C | ENTRY, NO ADAPTER | ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS = 0 | ENTRY, WITH ADAPTER, BATFET_CTRL_WVBUS = 1 | EXIT |
|---|---|---|---|---|---|---|
| Normal | On | Active | N/A | N/A | N/A | N/A |
| Ship mode | Off | Off | Writing BATFET_CTRL = 10 turns off BATFET after BATFET_DLY and enters ship mode. | Writing BATFET_CTRL = 10 has no effect while adapter is present. When both BATFET_DLY has expired and the adapter is removed, the device turns off BATFET and enters ship mode. Writing BATFET_CTRL = 00 before adapter is removed aborts ship mode. | Writing BATFET_CTRL = 10 turns off BATFET after BATFET_DLY. When both BATFET_DLY has expired and adapter is removed, the device enters ship mode. Writing BATFET_CTRL = 00 before adapter is removed turns BATFET on and aborts ship mode. | $\overline{QON}$ or adapter plug-in |
| System reset | On to Off to On | Active | Writing BATFET_CTRL = 11 initiates system reset after BATFET_DLY. Holding $\overline{QON}$ low for $t_{QON\_RST}$ initiates immediate reset (BATFET_DLY is not applied.) | Writing BATFET_CTRL = 11 is ignored and BATFET_CTRL resets to 00. Holding $\overline{QON}$ low for $t_{QON\_RST}$ is ignored. | Writing BATFET_CTRL = 11 initiates system reset after BATFET_DLY. Holding $\overline{QON}$ low for $t_{QON\_RST}$ initiates immediate reset. Converter is placed in HIZ during system reset and exits HIZ when system reset completes. | N/A |
| Shutdown mode | Off | Off | Writing BATFET_CTRL = 01 turns off BATFET after BATFET_DLY and enters shutdown. | Writing BATFET_CTRL = 01 with adapter present is ignored, regardless of BATFET_CTRL_WVBUS setting, and BATFET_CTRL is reset to 00. | | Adapter plug-in |

#### *9.3.9.1 Shutdown Mode*

For the lowest battery leakage current, the host can shut down BQ25628 and BQ25629 by setting the register bits BATFET_CTRL to 01. In this mode, the BATFET is turned off to prevent the battery from powering the system, the I2C is disabled and the charger is totally shut down. BQ25628 and BQ25629 can only be woken up by plugging in an adapter. When the adapter is plugged in, BQ25628 and BQ25629 start back up with all register settings in their POR default.

After the host sets BATFET_CTRL to 01, the BATFET turns off after waiting either 20 ms or 10 s as configured by BATFET_DLY register bit. Shutdown mode can only be entered when $V_{VBUS} < V_{VBUS\_UVLO}$, regardless of the BATFET_CTRL_WVBUS setting, which has no effect on shutdown mode entry. If the host writes BATFET_CTRL = 01 with $V_{VBUS} > V_{VBUS\_UVLOZ}$, the request is ignored and the BATFET_CTRL bits are set back to 00.

If the host writes BATFET_CTRL to 01 while boost OTG or bypass OTG is active, BQ25628 and BQ25629 first exit from boost OTG by setting EN_OTG = 0 or exits from bypass OTG by setting EN_OTG = EN_BYPASS_OTG = 0 and then enters shutdown mode.

$\overline{QON}$ has no effect during shutdown mode. The internal pull-up on the $\overline{QON}$ pin is disabled during shutdown to prevent leakage through the pin.

#### 9.3.9.2 Ship Mode

The host may place BQ25628 and BQ25629 into ship mode by setting BATFET_CTRL = 10. In ship mode, the BATFET is turned off to prevent the battery from powering the system, and the I2C is disabled. Ship mode has slightly higher quiescent current than shutdown mode, but $\overline{QON}$ may be used to exit from ship mode. BQ25628 and BQ25629 are taken out of ship mode by either of these methods:

- Pulling the $\overline{QON}$ pin low for $t_{SM\_EXIT}$
- $V_{VBUS} > V_{VBUS\_UVLOZ}$ (adapter plug-in)

When BQ25628 and BQ25629 exit from ship mode, the registers are reset to their POR values.

Ship mode is only entered when the adapter is not present. Setting BATFET_CTRL = 10 while $V_{VBUS} > V_{VBUS\_UVLOZ}$ (adapter present) either disables the BATFET or has no immediate effect depending on the setting of BATFET_CTRL_WVBUS.

#### 9.3.9.3 System Power Reset

The BATFET functions as a load switch between battery and system when the converter is not running. By changing the state of BATFET from on to off, systems connected to SYS can be power cycled. Any of the following conditions initiates a system power reset:

- BATFET_CTRL_WVBUS = 1 and $\overline{QON}$ is pulled low for tQON_RST
- BATFET_CTRL_WVBUS = 1 and BATFET_CTRL = 11
- BATFET_CTRL_WVBUS = 0 and VBUS < $V_{VBUS\_UVLO}$ simultaneously with $\overline{QON}$ pulled low for tQON_RST
- BATFET_CTRL_WVBUS = 0 and VBUS < $V_{VBUS\_UVLO}$ and BATFET_CTRL = 11

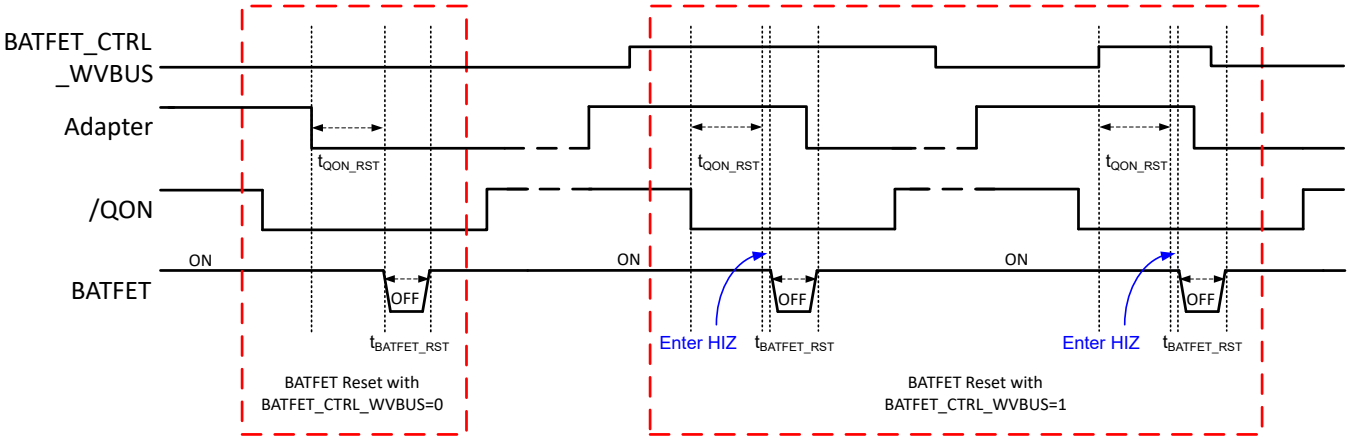



**Figure 9-6. System Power Reset Timing**

When BATFET_CTRL_WVBUS is set to 1, system power reset proceeds if either BATFET_CTRL is set to 11 or $\overline{QON}$ is pulled low for $t_{QON\_RST}$, regardless of whether VBUS is present or not . There is a delay of $t_{BATFET\_DLY}$ before initiating the system power reset. If $\overline{QON}$ is pulled low, there is no delay after the tQON_RST completes, regardless of BATFET_DLY setting.

The system power reset can be initiated from the battery only condition, from OTG mode or from the forward charging mode with adapter present. If the system power is reset when the charger is in boost OTG mode, the boost OTG mode is first stopped by setting EN_OTG = 0. If the system power is reset when the charger is in bypass OTG mode, the bypass OTG mode will first be terminated by setting EN_OTG = EN_BYPASS_OTG = 0.

## 9.4 Device Functional Modes

### 9.4.1 Host Mode and Default Mode

The device is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WD_STAT bit becomes HIGH, WD_FLAG is set to 1, and an $\overline{INT}$ is asserted low to alert the host (unless masked by WD_MASK). The WD_FLAG bit would read as 1 upon the first read and then 0 upon subsequent reads. When the charger is in host mode, WD_STAT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired. All the registers are in the default settings.

In default mode, the device keeps charging the battery with default 1-hour trickle charging safety timer, 2-hour pre-charging safety timer and the 12-hour fast charging safety timer. At the end of the 1-hour or 2-hour or 12-hour timer expired, the charging is stopped and the buck converter continues to operate to supply system load.

A write to any $I^2C$ register transitions the charger from default mode to host mode, and initiates the watchdog timer. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WD_STAT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog expires, the device returns to default mode. The ICHG value is divided in half when the watchdog timer expires, and a number of other fields are reset to their POR default values as shown in the notes column of the register tables in Section 9.6. When watchdog timer expires, WD_STAT and WD_FLAG is set to 1, and an $\overline{INT}$ is asserted low to alert the host (unless masked by WD_MASK).

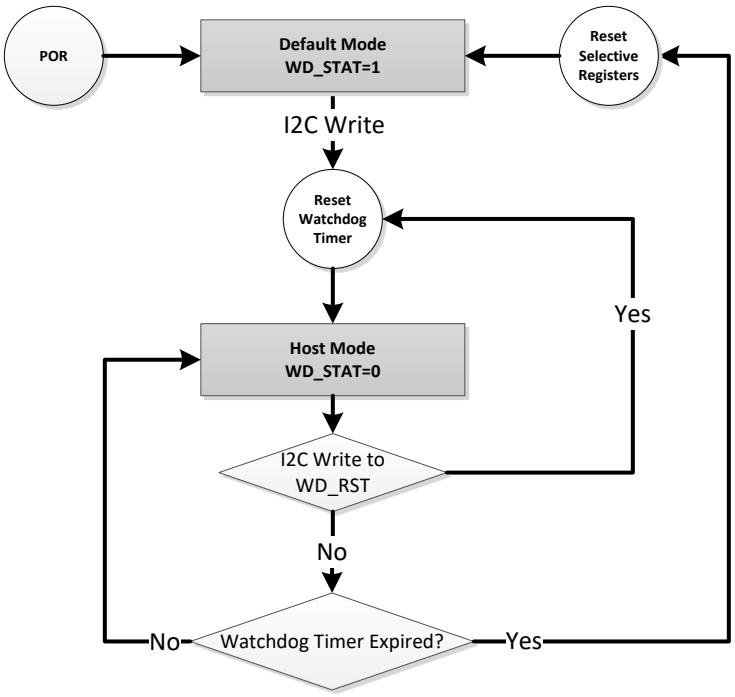



**Figure 9-7. Watchdog Timer Flow Chart**

### 9.4.2 Register Bit Reset

Beside the register reset by the watchdog timer in the default mode, the register and the timer could be reset to the default value by writing the REG_RST bit to 1. The register bits, which can be reset by the REG_RST bit, are noted in the Register Map section. After the register reset, the REG_RST bit goes back from 1 to 0 automatically.

## 9.5 Programming

### 9.5.1 Serial Interface

BQ25628 and BQ25629 uses I$^2$C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I$^2$C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA), and a serial clock line (SCL).

The device has 7-bit I$^2$C address 0x6A , receiving control inputs from a host device such as a micro-controller or digital signal processor through register addresses 0x02 – 0x38. The host device initiates all transfers and the charger responds. Register reads outside of these addresses return 0xFF. When the bus is free, both SDA and SCL lines are HIGH.

The I$^2$C interface supports standard mode (up to 100 kbits/s), fast mode (up to 400 kbits/s) and fast mode plus (up to 1 Mbits/s.) These lines are pulled up to a reference voltage via pull-up resistor. The device I$^2$C detection thresholds support a communication reference voltage from 1.2 V to 5 V.

#### *9.5.1.1 Data Validity*

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

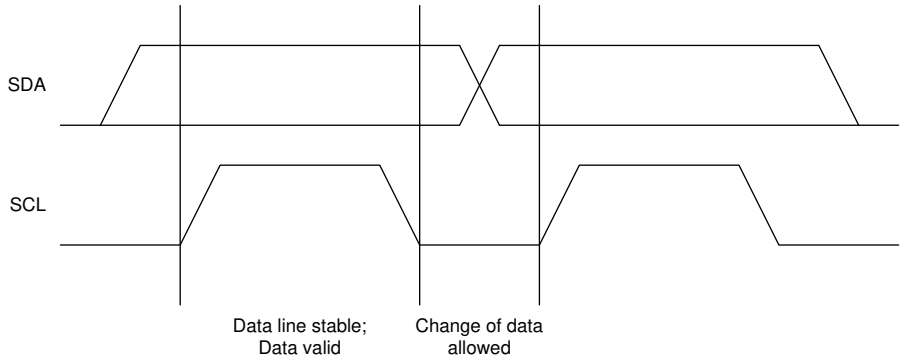



**Figure 9-8. Bit Transfer on the I$^2$C Bus**

#### *9.5.1.2 START and STOP Conditions*

All transactions begin with a START (S) and are terminated with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the host. The bus is considered busy after the START condition, and free after the STOP condition.

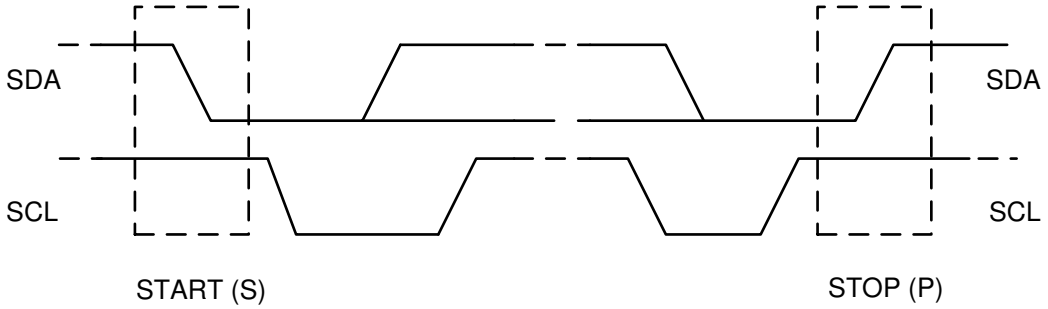



**Figure 9-9. START and STOP Conditions on the I$^2$C Bus**

#### 9.5.1.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an ACKNOWLEDGE (ACK) bit. Data is transferred with the Most Significant Bit (MSB) first. If target cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the SCL line low to force the host into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and releases the SCL line.

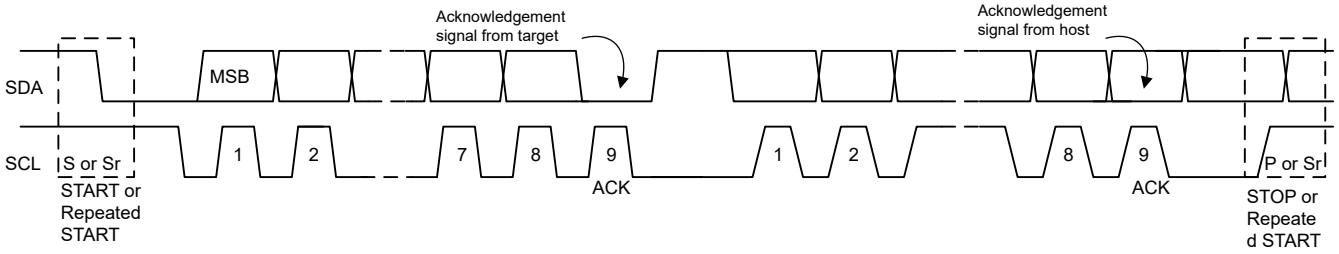



**Figure 9-10. Data Transfer on the I²C Bus**

#### 9.5.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The ACK signaling takes place after each transmitted byte. The ACK bit allows the target to signal the host that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the host.

The host releases the SDA line during the acknowledge clock pulse so the target can pull the SDA line LOW and it remains stable LOW during the HIGH period of this 9th clock pulse.

A NACK is signaled when the SDA line remains HIGH during the 9th clock pulse. The host can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

#### 9.5.1.5 Target Address and Data Direction Bit

After the START signal, a target address is sent. This address is 7 bits long, followed by the 8 bit as a data direction bit (bit R/ $\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The device 7-bit address is defined as

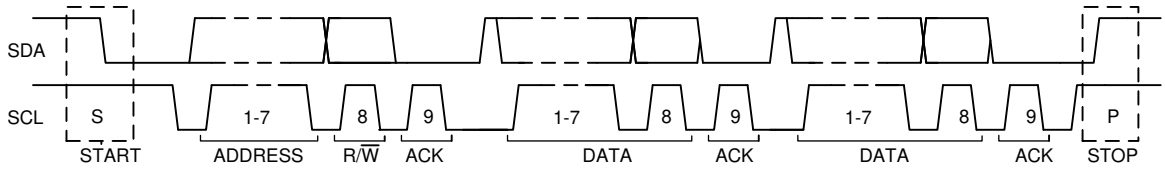



**Figure 9-11. Complete Data Transfer on the I²C Bus**

#### 9.5.1.6 Single Write and Read

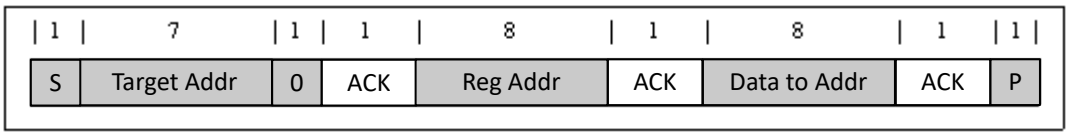



**Figure 9-12. Single Write**

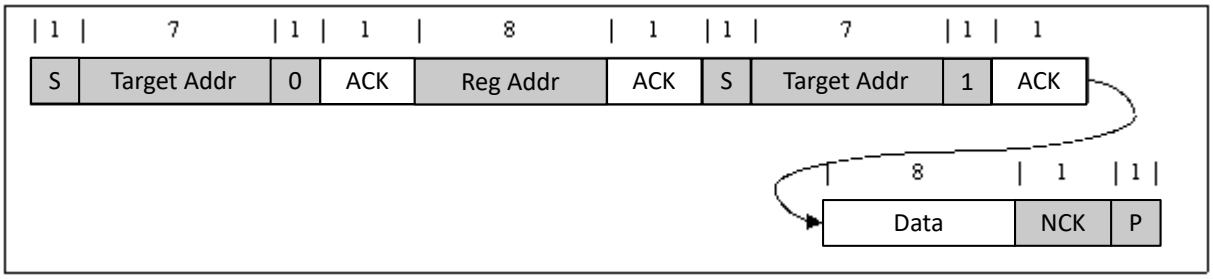



**Figure 9-13. Single Read**

If the register address is not defined, the charger IC sends back NACK and returns to the idle state.

#### *9.5.1.7 Multi-Write and Multi-Read*

The charger device supports multi-byte read and multi-byte write of all registers. These multi-byte operations are allowed to cross register boundaries. For instance, the entire register map may be read in a single operation with a 39-byte read that starts at register address 0x01.

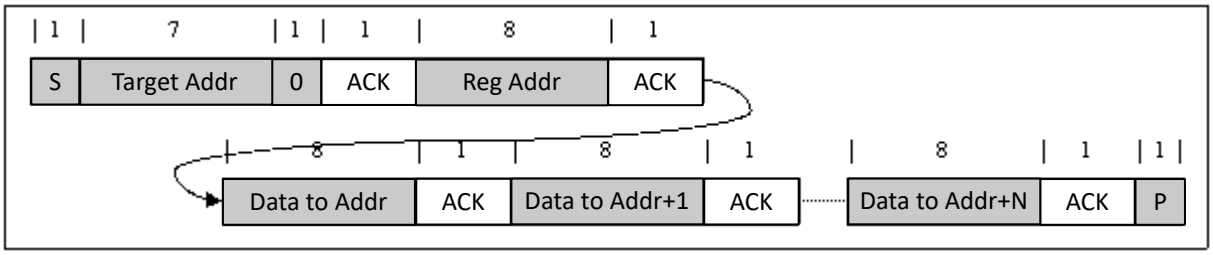



**Figure 9-14. Multi-Write**

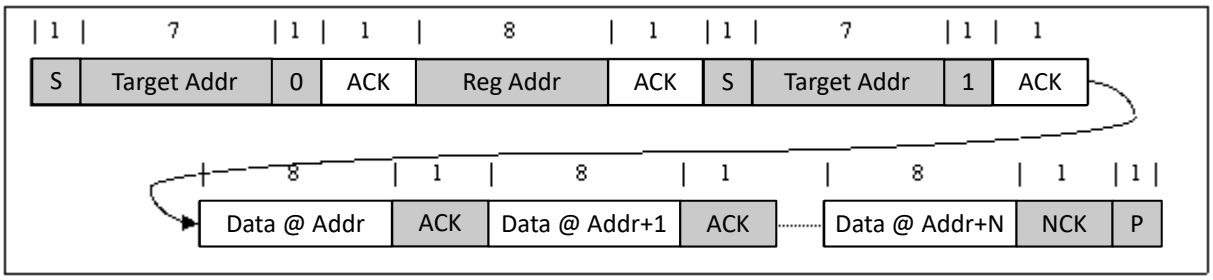



**Figure 9-15. Multi-Read**

## 9.6 Register Maps

$I^2C$ Device Address: 0x6A.

### 9.6.1 Register Programming

The BQ25628 and BQ25629 contain 8-bit and 16-bit registers. When writing to 16-bit registers, $I^2C$ transactions follow the little endian format, starting at the address of the least significant byte and writing both register bytes in a single 16-bit transaction.

### 9.6.2 BQ25628 Registers

Table 9-7 lists the memory-mapped registers for the BQ25628 registers. All register offset addresses not listed in Table 9-7 should be considered as reserved locations and the register contents should not be modified.

**Table 9-7. BQ25628 Registers**

| Address | Acronym | Register Name | Section |
|---|---|---|---|
| 0x2 | REG0x02_Charge_Current_Limit | Charge Current Limit | Go |
| 0x4 | REG0x04_Charge_Voltage_Limit | Charge Voltage Limit | Go |
| 0x6 | REG0x06_Input_Current_Limit | Input Current Limit | Go |
| 0x8 | REG0x08_Input_Voltage_Limit | Input Voltage Limit | Go |
| 0xC | REG0x0C_VOTG_regulation | VOTG regulation | Go |
| 0xE | REG0x0E_Minimal_System_Voltage | Minimal System Voltage | Go |
| 0x10 | REG0x10_Pre-charge_Control | Pre-charge Control | Go |
| 0x12 | REG0x12_Termination_Control | Termination Control | Go |
| 0x14 | REG0x14_Charge_Control | Charge Control | Go |
| 0x15 | REG0x15_Charge_Timer_Control | Charge Timer Control | Go |
| 0x16 | REG0x16_Charger_Control_0 | Charger Control 0 | Go |
| 0x17 | REG0x17_Charger_Control_1 | Charger Control 1 | Go |
| 0x18 | REG0x18_Charger_Control_2 | Charger Control 2 | Go |
| 0x19 | REG0x19_Charger_Control_3 | Charger Control 3 | Go |
| 0x1A | REG0x1A_NTC_Control_0 | NTC Control 0 | Go |
| 0x1B | REG0x1B_NTC_Control_1 | NTC Control 1 | Go |
| 0x1C | REG0x1C_NTC_Control_2 | NTC Control 2 | Go |
| 0x1D | REG0x1D_Charger_Status_0 | Charger Status 0 | Go |
| 0x1E | REG0x1E_Charger_Status_1 | Charger Status 1 | Go |
| 0x1F | REG0x1F_FAULT_Status_0 | FAULT Status 0 | Go |
| 0x20 | REG0x20_Charger_Flag_0 | Charger Flag 0 | Go |
| 0x21 | REG0x21_Charger_Flag_1 | Charger Flag 1 | Go |
| 0x22 | REG0x22_FAULT_Flag_0 | FAULT Flag 0 | Go |
| 0x23 | REG0x23_Charger_Mask_0 | Charger Mask 0 | Go |
| 0x24 | REG0x24_Charger_Mask_1 | Charger Mask 1 | Go |
| 0x25 | REG0x25_FAULT_Mask_0 | FAULT Mask 0 | Go |
| 0x26 | REG0x26_ADC_Control | ADC Control | Go |
| 0x27 | REG0x27_ADC_Function_Disable_0 | ADC Function Disable 0 | Go |
| 0x28 | REG0x28_IBUS_ADC | IBUS ADC | Go |
| 0x2A | REG0x2A_IBAT_ADC | IBAT ADC | Go |
| 0x2C | REG0x2C_VBUS_ADC | VBUS ADC | Go |
| 0x2E | REG0x2E_VPMID_ADC | VPMID ADC | Go |
| 0x30 | REG0x30_VBAT_ADC | VBAT ADC | Go |
| 0x32 | REG0x32_VSYS_ADC | VSYS ADC | Go |
| 0x34 | REG0x34_TS_ADC | TS ADC | Go |
| 0x36 | REG0x36_TDIE_ADC | TDIE ADC | Go |
| 0x38 | REG0x38_Part_Information | Part Information | Go |

Complex bit access types are encoded to fit into small table cells. Table 9-8 shows the codes that are used for access types in this section.

**Table 9-8. BQ25628 Access Type Codes**

| Access Type | Code | Description |
|---|---|---|
| **Read Type** | | |
| R | R | Read |
| **Write Type** | | |
| W | W | Write |
| **Reset or Default Value** | | |
| *-n* | | Value after reset or the default value |

### 9.6.2.1 REG0x02_Charge_Current_Limit Register (Address = 0x2) [Reset = X]

REG0x02_Charge_Current_Limit is shown in Figure 9-16 and described in Table 9-9.

Return to the Summary Table.

Charge Current Limit

**Figure 9-16. REG0x02_Charge_Current_Limit Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | ICHG | | | |
| R-0x0 | | | | R/W-X | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ICHG | | | | RESERVED | | | |
| R/W-X | | | | R-0x0 | | | |

**Table 9-9. REG0x02_Charge_Current_Limit Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:12 | RESERVED | R | 0x0 | | Reserved |
| 11:5 | ICHG | R/W | X | WATCHDOG Timer Expiration sets ICHG to 1/2 its previous value (rounded down)<br>Reset by:<br>REG_RESET | Charge Current Regulation Limit:<br>This 16-bit register follows the little-endian convention. ICHG[5:3] falls in REG0x03[2:0], and ICHG[2:0] falls in REG0x02[7:5].<br>POR: 320mA (8h)<br>Range: 40mA-2000mA (1h-32h)<br>Clamped Low<br>Clamped High<br>Bit Step: 40mA (1h)<br>NOTE: When Q4_FULLON=1, this register has a minimum value of 80mA |
| 4:0 | RESERVED | R | 0x0 | | Reserved |

### 9.6.2.2 REG0x04_Charge_Voltage_Limit Register (Address = 0x4) [Reset = 0x0D20]

REG0x04_Charge_Voltage_Limit is shown in Figure 9-17 and described in Table 9-10.

Return to the Summary Table.

Charge Voltage Limit

**Figure 9-17. REG0x04_Charge_Voltage_Limit Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | VREG | | | |
| R-0x0 | | | | R/W-0x1A4 | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VREG | | | | | RESERVED | | |
| R/W-0x1A4 | | | | | R-0x0 | | |

**Figure 9-17. REG0x04_Charge_Voltage_Limit Register (continued)**

**Table 9-10. REG0x04_Charge_Voltage_Limit Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:12 | RESERVED | R | 0x0 | | Reserved |
| 11:3 | VREG | R/W | 0x1A4 | Reset by:<br>REG_RESET | Battery Voltage Regulation Limit:<br>This 16-bit register follows the little-endian convention. VREG[8:5] falls in REG0x05[3:0], and VREG[4:0] falls in REG0x04[7:3].<br>POR: 4200mV (1A4h)<br>Range: 3500mV-4800mV (15Eh-1E0h)<br>Clamped Low<br>Clamped High<br>Bit Step: 10mV |
| 2:0 | RESERVED | R | 0x0 | | Reserved |

### 9.6.2.3 REG0x06_Input_Current_Limit Register (Address = 0x6) [Reset = 0x0A00]

REG0x06_Input_Current_Limit is shown in Figure 9-18 and described in Table 9-11.

Return to the Summary Table.

Input Current Limit

**Figure 9-18. REG0x06_Input_Current_Limit Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | IINDPM | | | |
| R-0x0 | | | | R/W-0xA0 | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IINDPM | | | | RESERVED | | | |
| R/W-0xA0 | | | | R-0x0 | | | |

**Table 9-11. REG0x06_Input_Current_Limit Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:12 | RESERVED | R | 0x0 | | Reserved |
| 11:4 | IINDPM | R/W | 0xA0 | Reset by:<br>REG_RESET<br>Adapter Removal | Input Current Regulation Limit:<br>This 16-bit register follows the little-endian convention. IINDPM[7:4] falls in REG0x07[3:0], and IINDPM[3:0] falls in REG0x06[7:4]. Based on D+/D- detection results:<br>USB SDP = 500mA<br>USB CDP = 1.5A<br>USB DCP = 1.5A<br>Unknown Adapter = 500mA<br>Non-Standard Adapter = 1A/2.1A/2.4A<br>POR: 3200mA (A0h)<br>Range: 100mA-3200mA (5h-A0h)<br>Clamped Low<br>Clamped High<br>Bit Step: 20mA<br>When the adapter is removed, IINDPM is reset to its POR value of 3.2 A. |
| 3:0 | RESERVED | R | 0x0 | | Reserved |

### 9.6.2.4 REG0x08_Input_Voltage_Limit Register (Address = 0x8) [Reset = 0x0E60]

REG0x08_Input_Voltage_Limit is shown in Figure 9-19 and described in Table 9-12.

Return to the Summary Table.

Input Voltage Limit

**Figure 9-19. REG0x08_Input_Voltage_Limit Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | VINDPM | | | |
| R-0x0 | | | | R/W-0x73 | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VINDPM | | | | RESERVED | | | |
| R/W-0x73 | | | | R-0x0 | | | |

**Table 9-12. REG0x08_Input_Voltage_Limit Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:14 | RESERVED | R | 0x0 | | Reserved |
| 13:5 | VINDPM | R/W | 0x73 | | Absolute Input Voltage Regulation Limit:<br>This 16-bit register follows the little-endian convention. VINDPM[8:3] falls in REG0x09[5:0], and VINDPM[2:0] falls in REG0x08[7:5].<br>POR: 4600mV (73h)<br>Range: 3800mV-16800mV (5Fh-1A4h)<br>Clamped Low<br>Clamped High<br>Bit Step: 40mV |
| 4:0 | RESERVED | R | 0x0 | | Reserved |

### 9.6.2.5 REG0x0C_VOTG_regulation Register (Address = 0xC) [Reset = 0x0FC0]

REG0x0C_VOTG_regulation is shown in Figure 9-20 and described in Table 9-13.

Return to the Summary Table.

VOTG regulation

**Figure 9-20. REG0x0C_VOTG_regulation Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | VOTG | | | |
| R-0x0 | | | | R/W-0x3F | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VOTG | | | | RESERVED | | | |
| R/W-0x3F | | | | R-0x0 | | | |

**Table 9-13. REG0x0C_VOTG_regulation Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:13 | RESERVED | R | 0x0 | | Reserved |
| 12:6 | VOTG | R/W | 0x3F | Reset by:<br>REG_RESET | Boost mode regulation voltage:<br>This 16-bit register follows the little-endian convention. VOTG[6:2] falls in REG0x0D[4:0], and VOTG[1:0] falls in REG0x0C[7:6].<br>POR: 5040mV (3Fh)<br>Range: 3840mV-5200mV (30h-41h)<br>Clamped Low<br>Clamped High<br>Bit Step: 80mV |
| 5:0 | RESERVED | R | 0x0 | | Reserved |

### 9.6.2.6 REG0x0E_Minimal_System_Voltage Register (Address = 0xE) [Reset = 0x0B00]

REG0x0E_Minimal_System_Voltage is shown in Figure 9-21 and described in Table 9-14.

Return to the Summary Table.

Minimal System Voltage

**Figure 9-21. REG0x0E_Minimal_System_Voltage Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | VSYSMIN | | | |
| R-0x0 | | | | R/W-0x2C | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VSYSMIN | | | RESERVED | | | | |
| R/W-0x2C | | | R-0x0 | | | | |

**Table 9-14. REG0x0E_Minimal_System_Voltage Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:12 | RESERVED | R | 0x0 | | Reserved |
| 11:6 | VSYSMIN | R/W | 0x2C | Reset by:<br>REG_RESET | Minimal System Voltage:<br>This 16-bit register follows the little-endian convention. VSYSMIN[5:2] falls in REG0x0F[3:0], and VSYSMIN[1:0] falls in REG0x0E[7:6].<br>POR: 3520mV (2Ch)<br>Range: 2560mV-3840mV (20h-30h)<br>Clamped Low<br>Clamped High<br>Bit Step: 80mV |
| 5:0 | RESERVED | R | 0x0 | | Reserved |

### 9.6.2.7 REG0x10_Pre-charge_Control Register (Address = 0x10) [Reset = 0x0018]

REG0x10_Pre-charge_Control is shown in Figure 9-22 and described in Table 9-15.

Return to the Summary Table.

Pre-charge Control

**Figure 9-22. REG0x10_Pre-charge_Control Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | IPRECHG |
| R-0x0 | | | | | | | R/W-0x3 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IPRECHG | | | | | RESERVED | | |
| R/W-0x3 | | | | | R-0x0 | | |

**Table 9-15. REG0x10_Pre-charge_Control Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:9 | RESERVED | R | 0x0 | | Reserved |
| 8:3 | IPRECHG | R/W | 0x3 | Reset by:<br>REG_RESET | Pre-charge current regulation limit:<br>This 16-bit register follows the little-endian convention.<br>IPRECHG[4:0] falls in REG0x10[7:3]<br>POR: 30mA (3h)<br>Range: 10mA-310mA (1h-1Fh)<br>Clamped Low<br>Bit Step: 10mA (1h)<br>NOTE: When Q4_FULLON=1, this register has a minimum value of 80mA, so Reset value becomes 80mA in this case |
| 2:0 | RESERVED | R | 0x0 | | Reserved |

### 9.6.2.8 REG0x12_Termination_Control Register (Address = 0x12) [Reset = 0x0010]

REG0x12_Termination_Control is shown in Figure 9-23 and described in Table 9-16.

Return to the Summary Table.

Termination Control

**Figure 9-23. REG0x12_Termination_Control Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | ITERM |
| R-0x0 | | | | | | | R/W-0x4 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ITERM | | | | | | RESERVED | |
| R/W-0x4 | | | | | | R-0x0 | |

**Table 9-16. REG0x12_Termination_Control Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:9 | RESERVED | R | 0x0 | | Reserved |
| 8:2 | ITERM | R/W | 0x4 | Reset by:<br>REG_RESET | Termination Current Threshold:<br>This 16-bit register follows the little-endian convention. ITERM[5:0] falls in REG0x12[7:2].<br>POR: 20mA (4h)<br>Range: 5mA-310mA (1h-3Eh)<br>Clamped Low<br>Bit Step: 5mA (1h)<br>NOTE: When Q4_FULLON=1, this register has a minimum value of 60mA, so Reset value becomes 60mA in this case |
| 1:0 | RESERVED | R | 0x0 | | Reserved |

### 9.6.2.9 REG0x14_Charge_Control Register (Address = 0x14) [Reset = 0x06]

REG0x14_Charge_Control is shown in Figure 9-24 and described in Table 9-17.

Return to the Summary Table.

Charge Control

**Figure 9-24. REG0x14_Charge_Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Q1_FULLON | Q4_FULLON | ITRICKLE | TOPOFF_TMR | | EN_TERM | VINDPM_BAT_TRACK | VRECHG |
| R-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | | R/W-0x1 | R/W-0x1 | R/W-0x0 |

**Table 9-17. REG0x14_Charge_Control Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | Q1_FULLON | R | 0x0 | | Forces RBFET (Q1) into low resistance state (26 mΩ) , regardless of IINDPM setting.<br>0x0 = RBFET RDSON determined by IINDPM setting (default)<br>0x1 = RBFET RDSON is always 26 mΩ |
| 6 | Q4_FULLON | R/W | 0x0 | | Forces BATFET (Q4) into low resistance state (15 mΩ), regardless of ICHG setting (Only applies when VBAT > VSYSMIN).<br>0x0 = BATFET RDSON determined by charge current (default)<br>0x1 = BATFET RDSON is always 15 mΩ |
| 5 | ITRICKLE | R/W | 0x0 | Reset by:<br>REG_RESET | Trickle charging current setting:<br>0b = 10mA (default)<br>1b = 40mA |

**Table 9-17. REG0x14_Charge_Control Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 4:3 | TOPOFF_TMR | R/W | 0x0 | Reset by:<br>REG_RESET | Top-off timer control:<br>0x0 = Disabled (default)<br>0x1 = 15 mins<br>0x2 = 30 mins<br>0x3 = 45 mins |
| 2 | EN_TERM | R/W | 0x1 | Reset by:<br>REG_RESET<br>WATCHDOG | Enable termination:<br>0x0 = Disable<br>0x1 = Enable (default) |
| 1 | VINDPM_BAT_TRACK | R/W | 0x1 | Reset by:<br>REG_RESET | Sets VINDPM to track BAT voltage. Actual VINDPM is higher of the VINDPM register value and VBAT + VINDPM_BAT_TRACK.<br>0x0 = Disable function (VINDPM set by register)<br>0x1 = VBAT + 400 mV (default) |
| 0 | VRECHG | R/W | 0x0 | Reset by:<br>REG_RESET | Battery Recharge Threshold Offset (Below VREG)<br>0x0 = 100mV (default)<br>0x1 = 200mV |

### 9.6.2.10 REG0x15_Charge_Timer_Control Register (Address = 0x15) [Reset = 0x5C]

REG0x15_Charge_Timer_Control is shown in Figure 9-25 and described in Table 9-18.

Return to the Summary Table.

Charge Timer Control

**Figure 9-25. REG0x15_Charge_Timer_Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DIS_STAT | EN_AUTO_INDET | FORCE_INDET | EN_DCP_BIAS | TMR2X_EN | EN_SAFETY_TMRS | PRECHG_TMR | CHG_TMR |
| R/W-0x0 | R/W-0x1 | R/W-0x0 | R/W-0x1 | R/W-0x1 | R/W-0x1 | R/W-0x0 | R/W-0x0 |

**Table 9-18. REG0x15_Charge_Timer_Control Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | DIS_STAT | R/W | 0x0 | Reset by:<br>REG_RESET | Disable the STAT pin output<br>0x0 = Enable (default)<br>0x1 = Disable |
| 6 | EN_AUTO_INDET | R/W | 0x1 | Reset by:<br>REG_RESET<br>WATCHDOG | Automatic D+/D- Detection Enable<br>0x0 = Disable DPDM detection when VBUS is plugged-in<br>0x1 = Enable DPDM detection when VBUS is plugged-in (default) |
| 5 | FORCE_INDET | R/W | 0x0 | Reset by:<br>REG_RESET<br>WATCHDOG | Force D+/D- detection<br>0x0 = Do not force DPDM detection (default)<br>0x1 = Force DPDM algorithm, when DPDM detection is done, this bit is reset to 0 |
| 4 | EN_DCP_BIAS | R/W | 0x1 | Reset by:<br>REG_RESET<br>WATCHDOG | Enable 600 mV bias on D+ pin whenever DCP is detected by BC1.2 detection algorithm (VBUS_STAT = 011b.)<br>0x0 = Disable 600 mV bias on D+ pin<br>0x1 = Enable 600 mV bias on D+ pin if DCP detected |
| 3 | TMR2X_EN | R/W | 0x1 | Reset by:<br>REG_RESET | 2X charging timer control<br>0x0 = Trickle charge, pre-charge and fast charge timer not slowed by 2X during input DPM or thermal regulation.<br>0x1 = Trickle charge, pre-charge and fast charge timer slowed by 2X during input DPM or thermal regulation (default) |

**Table 9-18. REG0x15_Charge_Timer_Control Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 2 | EN_SAFETY_TMRS | R/W | 0x1 | Reset by:<br>REG_RESET<br>WATCHDOG | Enable fast charge, pre-charge and trickle charge timers<br>0x0 = Disable<br>0x1 = Enable (default) |
| 1 | PRECHG_TMR | R/W | 0x0 | Reset by:<br>REG_RESET | Pre-charge safety timer setting<br>0x0 = 2 hrs (default)<br>0x1 = 0.5 hrs |
| 0 | CHG_TMR | R/W | 0x0 | Reset by:<br>REG_RESET | Fast charge safety timer setting<br>0x0 = 12 hrs (default)<br>0x1 = 24 hrs |

### 9.6.2.11 REG0x16_Charger_Control_0 Register (Address = 0x16) [Reset = 0xA1]

REG0x16_Charger_Control_0 is shown in Figure 9-26 and described in Table 9-19.

Return to the Summary Table.

Charger Control 0

**Figure 9-26. REG0x16_Charger_Control_0 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EN_AUTO_IBATDIS | FORCE_IBATDIS | EN_CHG | EN_HIZ | FORCE_PMID_DIS | WD_RST | WATCHDOG | |
| R/W-0x1 | R/W-0x0 | R/W-0x1 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x1 | |

**Table 9-19. REG0x16_Charger_Control_0 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | EN_AUTO_IBATDIS | R/W | 0x1 | Reset by:<br>REG_RESET | Enable the auto battery discharging during the battery OVP fault<br>0x0 = The charger does NOT apply a discharging current on BAT during battery OVP triggered<br>0x1 = The charger does apply a discharging current on BAT during battery OVP triggered (default) |
| 6 | FORCE_IBATDIS | R/W | 0x0 | Reset by:<br>REG_RESET<br>WATCHDOG | Force a battery discharging current (~30mA)<br>0x0 = IDLE (default)<br>0x1 = Force the charger to apply a discharging current on BAT |
| 5 | EN_CHG | R/W | 0x1 | Reset by:<br>REG_RESET<br>WATCHDOG | Charger enable configuration<br>0x0 = Charge Disable<br>0x1 = Charge Enable (default) |
| 4 | EN_HIZ | R/W | 0x0 | Reset by:<br>REG_RESET<br>WATCHDOG<br>Adapter Plug In | Enable HIZ mode.<br>0x0 = Disable (default)<br>0x1 = Enable |
| 3 | FORCE_PMID_DIS | R/W | 0x0 | Reset by:<br>REG_RESET<br>WATCHDOG | Force a PMID discharge current (~30mA.)<br>0x0 = Disable (default)<br>0x1 = Enable |
| 2 | WD_RST | R/W | 0x0 | Reset by:<br>REG_RESET | I2C watch dog timer reset<br>0x0 = Normal (default)<br>0x1 = Reset (this bit goes back to 0 after timer reset) |
| 1:0 | WATCHDOG | R/W | 0x1 | Reset by:<br>REG_RESET | Watchdog timer setting<br>0x0 = Disable<br>0x1 = 40s (default)<br>0x2 = 80s<br>0x3 = 160s |

### 9.6.2.12 REG0x17_Charger_Control_1 Register (Address = 0x17) [Reset = 0x4F]

REG0x17_Charger_Control_1 is shown in Figure 9-27 and described in Table 9-20.

Return to the Summary Table.

Charger Control 1

**Figure 9-27. REG0x17_Charger_Control_1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| REG_RST | TREG | SET_CONV_FREQ | | SET_CONV_STRN | | RESERVED | VBUS_OVP |
| R/W-0x0 | R/W-0x1 | R/W-0x0 | | R/W-0x3 | | R/W-0x1 | R/W-0x1 |

**Table 9-20. REG0x17_Charger_Control_1 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | REG_RST | R/W | 0x0 | REG_RESET | Reset registers to default values and reset timer Value resets to 0 after reset completes.<br>0x0 = Not reset (default)<br>0x1 = Reset |
| 6 | TREG | R/W | 0x1 | Reset by:<br>REG_RESET | Thermal regulation thresholds.<br>0x0 = 60C<br>0x1 = 120C (default) |
| 5:4 | SET_CONV_FREQ | R/W | 0x0 | Reset by:<br>REG_RESET | Adjust switching frequency of the converter<br>0x0 = Nominal, 1.5 MHz (default)<br>0x1 = -10%, 1.35 MHz<br>0x2 = +10%, 1.65 MHz<br>0x3 = RESERVED |
| 3:2 | SET_CONV_STRN | R/W | 0x3 | Reset by:<br>REG_RESET | Adjust the high side and low side drive strength of the converter to adjust efficiency versus EMI.<br>0x0 = weak<br>0x1 = normal<br>0x2 = RESERVED<br>0x3 = strong |
| 1 | RESERVED | R/W | 0x1 | | Reserved |
| 0 | VBUS_OVP | R/W | 0x1 | Reset by:<br>REG_RESET | Sets VBUS overvoltage protection threshold<br>0x0 = 6.3 V<br>0x1 = 18.5 V (default) |

### 9.6.2.13 REG0x18_Charger_Control_2 Register (Address = 0x18) [Reset = 0x04]

REG0x18_Charger_Control_2 is shown in Figure 9-28 and described in Table 9-21.

Return to the Summary Table.

Charger Control 2

**Figure 9-28. REG0x18_Charger_Control_2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EN_BYPASS_OTG | EN_OTG | PFM_OTG_DIS | PFM_FWD_DIS | BATFET_CTRL_WVBUS | BATFET_DLY | BATFET_CTRL | |
| R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R-0x0 | R/W-0x1 | R/W-0x0 | |

**Table 9-21. REG0x18_Charger_Control_2 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | EN_BYPASS_OTG | R/W | 0x0 | Reset by:<br>REG_RESET<br>WATCHDOG | Enable the Boost bypass mode<br>0x0 = Disable (default)<br>0x1 = Enable |
| 6 | EN_OTG | R/W | 0x0 | Reset by:<br>REG_RESET<br>WATCHDOG | Boost mode control<br>0b = OTG Disable (default)<br>1b = OTG Enable |

**Table 9-21. REG0x18_Charger_Control_2 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 5 | PFM_OTG_DIS | R/W | 0x0 | Reset by:<br>REG_RESET | Disable PFM in boost mode<br>0x0 = Enable (Default)<br>0x1 = Disable |
| 4 | PFM_FWD_DIS | R/W | 0x0 | Reset by:<br>REG_RESET | Disable PFM in forward buck mode<br>0x0 = Enable (Default)<br>0x1 = Disable |
| 3 | BATFET_CTRL_WVBUS | R | 0x0 | | Optionally allows BATFET off or system power reset with adapter present.<br>0x0 = 0x0<br>0x1 = 0x1 |
| 2 | BATFET_DLY | R/W | 0x1 | Reset by:<br>REG_RESET | Delay time added to the taking action in bits [1:0] of the BATFET_CTRL<br>0x0 = Add 20 ms delay time<br>0x1 = Add 10s delay time (default) |
| 1:0 | BATFET_CTRL | R/W | 0x0 | Reset by:<br>REG_RESET | BATFET control<br>The control logic of the BATFET to force the device enter different modes.<br>0x0 = Normal (default)<br>0x1 = Shutdown Mode<br>0x2 = Ship Mode<br>0x3 = System Power Reset |

### 9.6.2.14 REG0x19_Charger_Control_3 Register (Address = 0x19) [Reset = 0xC4]

REG0x19_Charger_Control_3 is shown in Figure 9-29 and described in Table 9-22.

Return to the Summary Table.

Charger Control 3

**Figure 9-29. REG0x19_Charger_Control_3 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| IBAT_PK | | VBAT_UVLO | VBAT_OTG_MIN | RESERVED | EN_EXTILIM | CHG_RATE | |
| R/W-0x3 | | R/W-0x0 | R/W-0x0 | R-0x0 | R/W-0x1 | R/W-0x0 | |

**Table 9-22. REG0x19_Charger_Control_3 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7:6 | IBAT_PK | R/W | 0x3 | Reset by:<br>REG_RESET | Battery discharging peak current protection threshold setting<br>0x0 = 1.5A<br>0x1 = 3A<br>0x2 = 6A<br>0x3 = 12A (default) |
| 5 | VBAT_UVLO | R/W | 0x0 | Reset by:<br>REG_RESET | Select the VBAT_UVLO falling threshold and VBAT_SHORT threshold<br>0x0 = VBAT_UVLO 2.2V, VBAT_SHORT 2.05V (default)<br>0x1 = VBAT_UVLO 1.8V, VBAT_SHORT 1.85V |
| 4 | VBAT_OTG_MIN | R/W | 0x0 | Reset by:<br>REG_RESET | Select the minimal battery voltage to start the boost mode<br>0x0 = 3V rising / 2.8 falling (default)<br>0x1 = 2.6V rising / 2.4 falling |
| 3 | RESERVED | R | 0x0 | | Reserved |
| 2 | EN_EXTILIM | R/W | 0x1 | Reset by:<br>REG_RESET<br>WATCHDOG | **BQ25628:**<br>Enable the external ILIM pin input current regulation<br>0b = Disabled<br>1b = Enabled (default)<br>**BQ25629: Reserved with default 0** |

**Table 9-22. REG0x19_Charger_Control_3 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 1:0 | CHG_RATE | R/W | 0x0 | Reset by:<br>REG_RESET | The charge rate definition for the fast charge stage. The charging current fold back value is equal to ICHG register setting times the fold back ratio, then divided by the charge rate.<br>0x0 = 1C (default)<br>0x1 = 2C<br>0x2 = 4C<br>0x3 = 6C |

### 9.6.2.15 REG0x1A_NTC_Control_0 Register (Address = 0x1A) [Reset = 0x3D]

REG0x1A_NTC_Control_0 is shown in Figure 9-30 and described in Table 9-23.

Return to the Summary Table.

NTC Control 0

**Figure 9-30. REG0x1A_NTC_Control_0 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TS_IGNORE | TS_TH_OTG_HOT | | TS_TH_OTG_COLD | TS_ISET_WARM | | TS_ISET_COOL | |
| R/W-0x0 | R/W-0x1 | | R/W-0x1 | R/W-0x3 | | R/W-0x1 | |

**Table 9-23. REG0x1A_NTC_Control_0 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | TS_IGNORE | R/W | 0x0 | Reset by:<br>REG_RESET<br>WATCHDOG | Ignore the TS feedback: the charger considers the TS is always good to allow charging and OTG modes, TS_STAT reports TS_NORMAL condition.<br>0x0 = Not ignore (Default)<br>0x1 = Ignore |
| 6:5 | TS_TH_OTG_HOT | R/W | 0x1 | Reset by:<br>REG_RESET | OTG Mode TS_HOT rising temperature threshold to transition from normal operation into suspended OTG mode when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ.<br>0x0 = 55°C<br>0x1 = 60°C (default)<br>0x2 = 65°C<br>0x3 = Disable |
| 4 | TS_TH_OTG_COLD | R/W | 0x1 | Reset by:<br>REG_RESET | OTG Mode TS_COLD falling temperature threshold to transition from normal operation into suspended OTG mode when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ.<br>0x0 = -20°C<br>0x1 = -10°C (default) |
| 3:2 | TS_ISET_WARM | R/W | 0x3 | Reset by:<br>REG_RESET | TS_WARM Current Setting<br>0x0 = Charge Suspend<br>0x1 = Set ICHG to 20%<br>0x2 = Set ICHG to 40%<br>0x3 = ICHG unchanged (default) |
| 1:0 | TS_ISET_COOL | R/W | 0x1 | Reset by:<br>REG_RESET | TS_COOL Current Setting<br>0x0 = Charge Suspend<br>0x1 = Set ICHG to 20% (default)<br>0x2 = Set ICHG to 40%<br>0x3 = ICHG unchanged |

### 9.6.2.16 REG0x1B_NTC_Control_1 Register (Address = 0x1B) [Reset = 0x25]

REG0x1B_NTC_Control_1 is shown in Figure 9-31 and described in Table 9-24.

Return to the Summary Table.

NTC Control 1

**Figure 9-31. REG0x1B_NTC_Control_1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TS_TH1_TH2_TH3 | | | TS_TH4_TH5_TH6 | | | TS_VSET_WARM | |
| R/W-0x1 | | | R/W-0x1 | | | R/W-0x1 | |

**Table 9-24. REG0x1B_NTC_Control_1 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7:5 | TS_TH1_TH2_TH3 | R/W | 0x1 | Reset by:<br>REG_RESET | TH1, TH2 and TH3 comparator falling temperature thresholds when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ.<br>0x0 = TH1 is 0°C, TH2 is 5°C, TH3 is 15°C<br>0x1 = TH1 is 0°C, TH2 is 10°C, TH3 is 15°C (default)<br>0x2 = TH1 is 0°C, TH2 is 15°C, TH3 is 20°C<br>0x3 = TH1 is 0°C, TH2 is 20°C, TH3 20°C<br>0x4 = TH1 is -5°C, TH2 is 5°C, TH3 is 15°C<br>0x5 = TH1 is -5°C, TH2 is 10°C, TH3 is 15°C<br>0x6 = TH1 is -5°C, TH2 is 10°C, TH3 is 20°C<br>0x7 = TH1 is 0°C, TH2 is 10°C, TH3 is 20°C |
| 4:2 | TS_TH4_TH5_TH6 | R/W | 0x1 | Reset by:<br>REG_RESET | TH4, TH5 and TH6 comparator rising temperature thresholds when a 103AT NTC thermistor is used, RT1=5.24kΩ and RT2=30.31kΩ.<br>0x0 = TH4 is 35°C, TH5 is 40°C, TH6 is 60°C<br>0x1 = TH4 is 35°C, TH5 is 45°C, TH6 is 60°C (default)<br>0x2 = TH4 is 35°C, TH5 is 50°C, TH6 is 60°C<br>0x3 = TH4 is 40°C, TH5 is 55°C, TH6 is 60°C<br>0x4 = TH4 is 35°C, TH5 is 40°C, TH6 is 50°C<br>0x5 = TH4 is 35°C, TH5 is 45°C, TH6 is 50°C<br>0x6 = TH4 is 40°C, TH5 is 45°C, TH6 is 60°C<br>0x7 = TH4 is 40°C, TH5 is 50°C, TH6 is 60°C |
| 1:0 | TS_VSET_WARM | R/W | 0x1 | Reset by:<br>REG_RESET | TS_WARM Voltage Setting<br>0x0 = Set VREG to VREG-300mV<br>0x1 = Set VREG to VREG-200mV (default)<br>0x2 = Set VREG to VREG-100mV<br>0x3 = VREG unchanged |

### 9.6.2.17 REG0x1C_NTC_Control_2 Register (Address = 0x1C) [Reset = 0x3F]

REG0x1C_NTC_Control_2 is shown in Figure 9-32 and described in Table 9-25.

Return to the Summary Table.

NTC Control 2

**Figure 9-32. REG0x1C_NTC_Control_2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | TS_VSET_SYM | TS_VSET_PREWARM | | TS_ISET_PREWARM | | TS_ISET_PRECOOL | |
| R-0x0 | R/W-0x0 | R/W-0x3 | | R/W-0x3 | | R/W-0x3 | |

**Table 9-25. REG0x1C_NTC_Control_2 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | RESERVED | R | 0x0 | | RESERVED |
| 6 | TS_VSET_SYM | R/W | 0x0 | Reset by:<br>REG_RESET | When this bit is set to 0, the voltage regulation for TS_PRECOOL and TS_COOL is unchanged. When this bit is set to 1, TS_PRECOOL uses the TS_VSET_PREWARM setting of TS_PREWARM and TS_COOL uses the TS_VSET_WARM setting of TS_WARM .<br>0x0 = VREG unchanged (default)<br>0x1 = TS_COOLx matches TS_WARMx |

**Table 9-25. REG0x1C_NTC_Control_2 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 5:4 | TS_VSET_PREWARM | R/W | 0x3 | Reset by: REG_RESET | Advanced temperature profile voltage setting for TS_PREWARM (TH4 - TH5)<br>0x0 = Set VREG to VREG-300mV<br>0x1 = Set VREG to VREG-200mV<br>0x2 = Set VREG to VREG-100mV<br>0x3 = VREG unchanged (default) |
| 3:2 | TS_ISET_PREWARM | R/W | 0x3 | Reset by: REG_RESET | Advanced temperature profile current setting for TS_PREWARM zone(TH4 - TH5)<br>0x0 = Charge Suspend<br>0x1 = Set ICHG to 20%<br>0x2 = Set ICHG to 40%<br>0x3 = ICHG unchanged (default) |
| 1:0 | TS_ISET_PRECOOL | R/W | 0x3 | Reset by: REG_RESET | Advanced temperature profile current setting for TS_PRECOOL zone (TH2 - TH3)<br>0x0 = Charge Suspend<br>0x1 = Set ICHG to 20%<br>0x2 = Set ICHG to 40%<br>0x3 = ICHG unchanged (default) |

### 9.6.2.18 REG0x1D_Charger_Status_0 Register (Address = 0x1D) [Reset = 0x00]

REG0x1D_Charger_Status_0 is shown in Figure 9-33 and described in Table 9-26.

Return to the Summary Table.

Charger Status 0

**Figure 9-33. REG0x1D_Charger_Status_0 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | ADC_DONE_STAT | TREG_STAT | VSYS_STAT | IINDPM_STAT | VINDPM_STAT | SAFETY_TMR_STAT | WD_STAT |
| R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 |

**Table 9-26. REG0x1D_Charger_Status_0 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | RESERVED | R | 0x0 | | Reserved |
| 6 | ADC_DONE_STAT | R | 0x0 | | ADC Conversion Status (in one-shot mode only)<br>Note: Always reads 0 in continuous mode<br>0x0 = Conversion not complete<br>0x1 = Conversion complete |
| 5 | TREG_STAT | R | 0x0 | | IC Thermal regulation status<br>0x0 = Normal<br>0x1 = Device in thermal regulation |
| 4 | VSYS_STAT | R | 0x0 | | VSYS Regulation Status (forward mode)<br>0x0 = Not in VSYSMIN regulation (BAT>VSYSMIN)<br>0x1 = In VSYSMIN regulation (BAT<VSYSMIN) |
| 3 | IINDPM_STAT | R | 0x0 | | In forward mode, indicates that either IINDPM regulation is active or ILIM pin regulation is active<br>In OTG mode, indicates that IOTG regulation is active<br>0x0 = Normal<br>0x1 = In IINDPM/ILIM regulation or IOTG regulation |
| 2 | VINDPM_STAT | R | 0x0 | | VINDPM status (forward mode) or VOTG status (OTG mode, backup mode)<br>0x0 = Normal<br>0x1 = In VINDPM regulation or VOTG regulation |
| 1 | SAFETY_TMR_STAT | R | 0x0 | | Fast charge, trickle charge and pre-charge timer status<br>0x0 = Normal<br>0x1 = Safety timer expired |

**Table 9-26. REG0x1D_Charger_Status_0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 0 | WD_STAT | R | 0x0 | | I2C watch dog timer status<br>0x0 = Normal<br>0x1 = WD timer expired |

### 9.6.2.19 REG0x1E_Charger_Status_1 Register (Address = 0x1E) [Reset = 0x00]

REG0x1E_Charger_Status_1 is shown in Figure 9-34 and described in Table 9-27.

Return to the Summary Table.

Charger Status 1

**Figure 9-34. REG0x1E_Charger_Status_1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | CHG_STAT | | VBUS_STAT | | |
| R-0x0 | | | R-0x0 | | R-0x0 | | |

**Table 9-27. REG0x1E_Charger_Status_1 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7:5 | RESERVED | R | 0x0 | | Reserved |
| 4:3 | CHG_STAT | R | 0x0 | | Charge Status bits<br>0x0 = Not Charging or Charge Terminated<br>0x1 = Trickle Charge, Pre-charge or Fast charge (CC mode)<br>0x2 = Taper Charge (CV mode)<br>0x3 = Top-off Timer Active Charging |
| 2:0 | VBUS_STAT | R | 0x0 | | VBUS status bits<br>BQ25629:<br>000b = No qualified adapter, or EN_AUTO_INDET = 0.<br>001b = USB SDP Adapter (500mA)<br>010b = USB CDP Adapter (1.5A)<br>011b = USB DCP Adapter (1.5A)<br>100b = Unknown Adapter (500mA)<br>101b = Non-Standard Adapter (1A/2.1A/2.4A)<br>110b = Reserved<br>111b = In boost OTG mode<br>BQ25628:<br>100b = Unknown Adapter (default IINDPM setting) |

### 9.6.2.20 REG0x1F_FAULT_Status_0 Register (Address = 0x1F) [Reset = 0x00]

REG0x1F_FAULT_Status_0 is shown in Figure 9-35 and described in Table 9-28.

Return to the Summary Table.

FAULT Status 0

**Figure 9-35. REG0x1F_FAULT_Status_0 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VBUS_FAULT_STAT | BAT_FAULT_STAT | SYS_FAULT_STAT | OTG_FAULT_STAT | TSHUT_STAT | TS_STAT | | |
| R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | | |

**Table 9-28. REG0x1F_FAULT_Status_0 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | VBUS_FAULT_STAT | R | 0x0 | | VBUS fault status, VBUS OVP and sleep comparator<br>0x0 = Normal<br>0x1 = Device not switching due to over voltage protection or sleep comparator |

**Table 9-28. REG0x1F_FAULT_Status_0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 6 | BAT_FAULT_STAT | R | 0x0 | | BAT fault status, IBAT OCP and VBAT OVP<br>0x0 = Normal<br>0x1 = Device in battery over current protection or battery overvoltage protection |
| 5 | SYS_FAULT_STAT | R | 0x0 | | VSYS under voltage and over voltage status<br>0x0 = Normal<br>0x1 = SYS in SYS short circuit or over voltage |
| 4 | OTG_FAULT_STAT | R | 0x0 | | Forward mode: IBUS overcurrent or PMID overvoltage<br>Boost mode: PMID and VBUS reverse-current, under voltage and over voltage status<br>0x0 = Normal<br>0x1 = Fault detected |
| 3 | TSHUT_STAT | R | 0x0 | | IC temperature shutdown status<br>0x0 = Normal<br>0x1 = Device in thermal shutdown protection |
| 2:0 | TS_STAT | R | 0x0 | | The TS temperature zone.<br>0x0 = TS_NORMAL<br>0x1 = TS_COLD or TS_OTG_COLD or TS resistor string power rail is not available.<br>0x2 = TS_HOT or TS_OTG_HOT<br>0x3 = TS_COOL<br>0x4 = TS_WARM<br>0x5 = TS_PRECOOL<br>0x6 = TS_PREWARM<br>0x7 = TS pin bias reference fault |

### 9.6.2.21 REG0x20_Charger_Flag_0 Register (Address = 0x20) [Reset = 0x00]

REG0x20_Charger_Flag_0 is shown in Figure 9-36 and described in Table 9-29.

Return to the Summary Table.

Charger Flag 0

**Figure 9-36. REG0x20_Charger_Flag_0 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | ADC_DONE_FLAG | TREG_FLAG | VSYS_FLAG | IINDPM_FLAG | VINDPM_FLAG | SAFETY_TMR_FLAG | WD_FLAG |
| R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 |

**Table 9-29. REG0x20_Charger_Flag_0 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | RESERVED | R | 0x0 | | Reserved |
| 6 | ADC_DONE_FLAG | R | 0x0 | | ADC conversion flag (only in one-shot mode)<br>0x0 = Conversion not completed<br>0x1 = Conversion completed |
| 5 | TREG_FLAG | R | 0x0 | | IC Thermal regulation flag<br>0x0 = Normal<br>0x1 = TREG signal rising threshold detected |
| 4 | VSYS_FLAG | R | 0x0 | | VSYS min regulation flag<br>0x0 = Normal<br>0x1 = Entered or existed VSYS min regulation |
| 3 | IINDPM_FLAG | R | 0x0 | | Indicates that either the IINDPM regulation loop, ILIM pin regulation or IOTG regulation loop has been entered.<br>0x0 = Normal<br>0x1 = IINDPM, ILIM or IOTG regulation signal rising edge detected |

**Table 9-29. REG0x20_Charger_Flag_0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 2 | VINDPM_FLAG | R | 0x0 | | VINDPM or VOTG flag<br>0x0 = Normal<br>0x1 = VINDPM or VOTG regulation signal rising edge detected |
| 1 | SAFETY_TMR_FLAG | R | 0x0 | | Fast charge, trickle charge and pre-charge timer flag<br>0x0 = Normal<br>0x1 = Fast charge timer expired rising edge detected |
| 0 | WD_FLAG | R | 0x0 | | I2C watchdog timer flag<br>0x0 = Normal<br>0x1 = WD timer signal rising edge detected |

### 9.6.2.22 REG0x21_Charger_Flag_1 Register (Address = 0x21) [Reset = 0x00]

REG0x21_Charger_Flag_1 is shown in Figure 9-37 and described in Table 9-30.

Return to the Summary Table.

Charger Flag 1

**Figure 9-37. REG0x21_Charger_Flag_1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | CHG_FLAG | RESERVED | | VBUS_FLAG |
| R-0x0 | | | | R-0x0 | R-0x0 | | R-0x0 |

**Table 9-30. REG0x21_Charger_Flag_1 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7:4 | RESERVED | R | 0x0 | | Reserved |
| 3 | CHG_FLAG | R | 0x0 | | Charge status flag<br>0x0 = Normal<br>0x1 = Charge status changed |
| 2:1 | RESERVED | R | 0x0 | | Reserved |
| 0 | VBUS_FLAG | R | 0x0 | | VBUS status flag<br>0x0 = Normal<br>0x1 = VBUS status changed |

### 9.6.2.23 REG0x22_FAULT_Flag_0 Register (Address = 0x22) [Reset = 0x00]

REG0x22_FAULT_Flag_0 is shown in Figure 9-38 and described in Table 9-31.

Return to the Summary Table.

FAULT Flag 0

**Figure 9-38. REG0x22_FAULT_Flag_0 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VBUS_FAULT_FLAG | BAT_FAULT_FLAG | SYS_FAULT_FLAG | OTG_FAULT_FLAG | TSHUT_FLAG | RESERVED | | TS_FLAG |
| R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | R-0x0 | | R-0x0 |

**Table 9-31. REG0x22_FAULT_Flag_0 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | VBUS_FAULT_FLAG | R | 0x0 | | VBUS over-voltage or sleep flag<br>0x0 = Normal<br>0x1 = Entered VBUS OVP or sleep |
| 6 | BAT_FAULT_FLAG | R | 0x0 | | IBAT over-current and VBAT over-voltage flag<br>0x0 = Normal<br>0x1 = Entered battery discharged OCP or VBAT OVP |

**Table 9-31. REG0x22_FAULT_Flag_0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 5 | SYS_FAULT_FLAG | R | 0x0 | | VSYS over voltage and SYS short flag<br>0x0 = Normal<br>0x1 = Stopped switching due to system over-voltage or SYS short fault |
| 4 | OTG_FAULT_FLAG | R | 0x0 | | Forward mode: IBUS overcurrent or PMID overvoltage<br>Boost mode: PMID and VBUS reverse-current, under voltage and over voltage flag<br>0x0 = Normal<br>0x1 = Turned off PMID_GD or stopped boost mode due to forward over-current, over-voltage or boost mode reverse-current, under-voltage or over-voltage faults |
| 3 | TSHUT_FLAG | R | 0x0 | | IC thermal shutdown flag<br>0x0 = Normal<br>0x1 = TS shutdown signal rising threshold detected |
| 2:1 | RESERVED | R | 0x0 | | Reserved |
| 0 | TS_FLAG | R | 0x0 | | TS status flag<br>0x0 = Normal<br>0x1 = A change to TS status was detected |

### 9.6.2.24 REG0x23_Charger_Mask_0 Register (Address = 0x23) [Reset = 0x00]

REG0x23_Charger_Mask_0 is shown in Figure 9-39 and described in Table 9-32.

Return to the Summary Table.

Charger Mask 0

**Figure 9-39. REG0x23_Charger_Mask_0 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RSERVED | ADC_DONE_MASK | TREG_MASK | VSYS_MASK | IINDPM_MASK | VINDPM_MASK | SAFETY_TMR_MASK | WD_MASK |
| R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 |

**Table 9-32. REG0x23_Charger_Mask_0 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | RSERVED | R/W | 0x0 | | Reserved |
| 6 | ADC_DONE_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | ADC conversion mask flag (only in one-shot mode)<br>0x0 = ADC conversion done does produce $\overline{INT}$ pulse<br>0x1 = ADC conversion done does not produce $\overline{INT}$ pulse |
| 5 | TREG_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | IC thermal regulation mask flag<br>0x0 = Entering TREG does produce $\overline{INT}$<br>0x1 = Entering TREG does not produce $\overline{INT}$ |
| 4 | VSYS_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | VSYS min regulation mask flag<br>0x0 = Enter or exit VSYSMIN regulation does produce $\overline{INT}$ pulse<br>0x1 = Enter or exit VSYSMIN regulation does not produce $\overline{INT}$ pulse |
| 3 | IINDPM_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | IINDPM, ILIM or IOTG mask<br>0x0 = Enter IINDPM, ILIM or IOTG does produce $\overline{INT}$ pulse<br>0x1 = Enter IINDPM, ILIM or IOTG does not produce $\overline{INT}$ pulse |

**Table 9-32. REG0x23_Charger_Mask_0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 2 | VINDPM_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | VINDPM or VOTG mask<br>0x0 = Enter VINDPM or VOTG does produce $\overline{INT}$ pulse<br>0x1 = Enter VINDPM or VOTG does not produce $\overline{INT}$ pulse |
| 1 | SAFETY_TMR_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | Fast charge, trickle charge and pre-charge timer mask flag<br>0x0 = Fast charge, trickle charge or pre-charge timer expiration does produce $\overline{INT}$<br>0x1 = Fast charge, trickle charge or pre-charge timer expiration does not produce $\overline{INT}$ |
| 0 | WD_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | I2C watch dog timer mask<br>0x0 = I2C watch dog timer expired does produce $\overline{INT}$ pulse<br>0x1 = I2C watch dog timer expired does not produce $\overline{INT}$ pulse |

### 9.6.2.25 REG0x24_Charger_Mask_1 Register (Address = 0x24) [Reset = 0x00]

REG0x24_Charger_Mask_1 is shown in Figure 9-40 and described in Table 9-33.

Return to the Summary Table.

Charger Mask 1

**Figure 9-40. REG0x24_Charger_Mask_1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | CHG_MASK | RESERVED | | VBUS_MASK |
| R-0x0 | | | | R/W-0x0 | R-0x0 | | R/W-0x0 |

**Table 9-33. REG0x24_Charger_Mask_1 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7:4 | RESERVED | R | 0x0 | | Reserved |
| 3 | CHG_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | Charge status mask flag<br>0x0 = Charging status change does produce $\overline{INT}$<br>0x1 = Charging status change does not produce $\overline{INT}$ |
| 2:1 | RESERVED | R | 0x0 | | Reserved |
| 0 | VBUS_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | VBUS status mask flag<br>0x0 = VBUS status change does produce $\overline{INT}$<br>0x1 = VBUS status change does not produce $\overline{INT}$ |

### 9.6.2.26 REG0x25_FAULT_Mask_0 Register (Address = 0x25) [Reset = 0x00]

REG0x25_FAULT_Mask_0 is shown in Figure 9-41 and described in Table 9-34.

Return to the Summary Table.

FAULT Mask 0

**Figure 9-41. REG0x25_FAULT_Mask_0 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VBUS_FAULT_MASK | BAT_FAULT_MASK | SYS_FAULT_MASK | OTG_FAULT_MASK | TSHUT_MASK | RESERVED | | TS_MASK |
| R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R-0x0 | | R/W-0x0 |

**Table 9-34. REG0x25_FAULT_Mask_0 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | VBUS_FAULT_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | VBUS over-voltage and sleep comparator mask flag<br>0x0 = Entering VBUS OVP or sleep does produce $\overline{INT}$<br>0x1 = Entering VBUS OVP or sleep does not produce $\overline{INT}$ |
| 6 | BAT_FAULT_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | IBAT over current and VBAT overvoltage mask flag<br>0x0 = IBAT OCP fault or VBAT OVP fault does produce $\overline{INT}$<br>0x1 = Neither IBAT OCP fault nor VBAT OVP fault produces $\overline{INT}$ |
| 5 | SYS_FAULT_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | SYS over voltage and SYS short mask<br>0x0 = System over-voltage or SYS short fault does produce $\overline{INT}$<br>0x1 = Neither system over voltage nor SYS short fault produces $\overline{INT}$ |
| 4 | OTG_FAULT_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | Forward mode: IBUS overcurrent or PMID overvoltage<br>Boost mode: PMID and VBUS reverse-current, under voltage and over voltage mask<br>0x0 = OTG VBUS or PMID reverse-current, under voltage fault or over voltage fault does produce $\overline{INT}$<br>0x1 = Neither reverse-current fault, OTG PMID or VBUS under voltage nor over voltage fault produces $\overline{INT}$ |
| 3 | TSHUT_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | IC thermal shutdown mask flag<br>0x0 = TSHUT does produce $\overline{INT}$<br>0x1 = TSHUT does not produce $\overline{INT}$ |
| 2:1 | RESERVED | R | 0x0 | | Reserved |
| 0 | TS_MASK | R/W | 0x0 | Reset by:<br>REG_RESET | Temperature charging profile interrupt mask<br>0x0 = A change to TS temperature zone does produce $\overline{INT}$<br>0x1 = A change to the TS temperature zone does not produce $\overline{INT}$ |

### 9.6.2.27 REG0x26_ADC_Control Register (Address = 0x26) [Reset = 0x30]

REG0x26_ADC_Control is shown in Figure 9-42 and described in Table 9-35.

Return to the Summary Table.

ADC Control

**Figure 9-42. REG0x26_ADC_Control Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADC_EN | ADC_RATE | ADC_SAMPLE | | ADC_AVG | ADC_AVG_INIT | RESERVED | |
| R/W-0x0 | R/W-0x0 | R/W-0x3 | | R/W-0x0 | R/W-0x0 | R-0x0 | |

**Table 9-35. REG0x26_ADC_Control Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | ADC_EN | R/W | 0x0 | Reset by:<br>REG_RESET<br>WATCHDOG | ADC Control<br>The registers POR to all 0 's, then after that always retain the last measurement, and never clear.<br>0x0 = Disable (default)<br>0x1 = Enable |
| 6 | ADC_RATE | R/W | 0x0 | Reset by:<br>REG_RESET | ADC conversion rate control<br>0x0 = Continuous conversion (default)<br>0x1 = One shot conversion |

**Table 9-35. REG0x26_ADC_Control Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 5:4 | ADC_SAMPLE | R/W | 0x3 | Reset by:<br>REG_RESET | ADC sample speed<br>0x0 = 12 bit effective resolution<br>0x1 = 11 bit effective resolution<br>0x2 = 10 bit effective resolution<br>0x3 = 9 bit effective resolution (default) |
| 3 | ADC_AVG | R/W | 0x0 | Reset by:<br>REG_RESET | ADC average control<br>0x0 = Single value (default)<br>0x1 = Running average |
| 2 | ADC_AVG_INIT | R/W | 0x0 | Reset by:<br>REG_RESET | ADC average initial value control<br>0x0 = Start average using the existing register value (default)<br>0x1 = Start average using a new ADC conversion |
| 1:0 | RESERVED | R | 0x0 | | Reserved |

### 9.6.2.28 REG0x27_ADC_Function_Disable_0 Register (Address = 0x27) [Reset = 0x00]

REG0x27_ADC_Function_Disable_0 is shown in Figure 9-43 and described in Table 9-36.

Return to the Summary Table.

ADC Function Disable 0

**Figure 9-43. REG0x27_ADC_Function_Disable_0 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| IBUS_ADC_DIS | IBAT_ADC_DIS | VBUS_ADC_DIS | VBAT_ADC_DIS | VSYS_ADC_DIS | TS_ADC_DIS | TDIE_ADC_DIS | VPMID_ADC_DIS |
| R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x0 |

**Table 9-36. REG0x27_ADC_Function_Disable_0 Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7 | IBUS_ADC_DIS | R/W | 0x0 | Reset by:<br>REG_RESET | IBUS ADC control<br>0x0 = Enable (Default)<br>0x1 = Disable |
| 6 | IBAT_ADC_DIS | R/W | 0x0 | Reset by:<br>REG_RESET | IBAT ADC control<br>0x0 = Enable (Default)<br>0x1 = Disable |
| 5 | VBUS_ADC_DIS | R/W | 0x0 | Reset by:<br>REG_RESET | VBUS ADC control<br>0x0 = Enable (Default)<br>0x1 = Disable |
| 4 | VBAT_ADC_DIS | R/W | 0x0 | Reset by:<br>REG_RESET | VBAT ADC control<br>0x0 = Enable (Default)<br>0x1 = Disable |
| 3 | VSYS_ADC_DIS | R/W | 0x0 | Reset by:<br>REG_RESET | VSYS ADC control<br>0x0 = Enable (Default)<br>0x1 = Disable |
| 2 | TS_ADC_DIS | R/W | 0x0 | Reset by:<br>REG_RESET | TS ADC control<br>0x0 = Enable (Default)<br>0x1 = Disable |
| 1 | TDIE_ADC_DIS | R/W | 0x0 | Reset by:<br>REG_RESET | TDIE ADC control<br>0x0 = Enable (Default)<br>0x1 = Disable |
| 0 | VPMID_ADC_DIS | R/W | 0x0 | Reset by:<br>REG_RESET | VPMID ADC control<br>0x0 = Enable (Default)<br>0x1 = Disable |

### 9.6.2.29 REG0x28_IBUS_ADC Register (Address = 0x28) [Reset = 0x0000]

REG0x28_IBUS_ADC is shown in Figure 9-44 and described in Table 9-37.

Return to the Summary Table.

IBUS ADC

**Figure 9-44. REG0x28_IBUS_ADC Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| IBUS_ADC | | | | | | | |
| R-0x0 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IBUS_ADC | | | | | | | RESERVED |
| R-0x0 | | | | | | | R-0x0 |

**Table 9-37. REG0x28_IBUS_ADC Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:1 | IBUS_ADC | R | 0x0 | | IBUS ADC reading<br>Reported in 2 's Complement.<br>When the current is flowing from VBUS to PMID, IBUS ADC reports positive value, and when the current is flowing from PMID to VBUS, IBUS ADC reports negative value.<br>POR: 0mA (0h)<br>Format: 2s Complement<br>Range: -4000mA-4000mA (7830h-7FFFh), (0h-7D0h)<br>Clamped Low<br>Clamped High<br>Bit Step: 2mA |
| 0 | RESERVED | R | 0x0 | | Reserved |

### 9.6.2.30 REG0x2A_IBAT_ADC Register (Address = 0x2A) [Reset = 0x0000]

REG0x2A_IBAT_ADC is shown in Figure 9-45 and described in Table 9-38.

Return to the Summary Table.

IBAT ADC

**Figure 9-45. REG0x2A_IBAT_ADC Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| IBAT_ADC | | | | | | | |
| R-0x0 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IBAT_ADC | | | | | | RESERVED | |
| R-0x0 | | | | | | R-0x0 | |

**Table 9-38. REG0x2A_IBAT_ADC Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:2 | IBAT_ADC | R | 0x0 | | IBAT ADC reading<br>Reported in 2 's Complement.<br>The IBAT ADC reports positive value for the battery charging current, and negative value for the battery discharging current.<br>The IBAT ADC resets to zero when EN_CHG=0.<br>POR: 0mA (0h)<br>Format: 2s Complement<br>Range: -7500mA-4000mA (38ADh-3FFFh), (0h-3E8h)<br>Clamped Low<br>Clamped High<br>Bit Step: 4mA<br>If polarity of battery current changes from charging to discharging or vice-versa during the ADC measurement, the conversion is aborted and the register reports code 0x8000 (which is code 0x2000 for IBAT_ADC field) |
| 1:0 | RESERVED | R | 0x0 | | Reserved |

### 9.6.2.31 REG0x2C_VBUS_ADC Register (Address = 0x2C) [Reset = 0x0000]

REG0x2C_VBUS_ADC is shown in Figure 9-46 and described in Table 9-39.

Return to the Summary Table.

VBUS ADC

**Figure 9-46. REG0x2C_VBUS_ADC Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | VBUS_ADC | | | | | | |
| R-0x0 | R-0x0 | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VBUS_ADC | | | | | | RESERVED | |
| R-0x0 | | | | | | R-0x0 | |

**Table 9-39. REG0x2C_VBUS_ADC Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15 | RESERVED | R | 0x0 | | Reserved |
| 14:2 | VBUS_ADC | R | 0x0 | | VBUS ADC reading<br>POR: 0mV (0h)<br>Range: 0mV-19850mV (0h-1388h)<br>Clamped High<br>Bit Step: 3.97mV |
| 1:0 | RESERVED | R | 0x0 | | Reserved |

### 9.6.2.32 REG0x2E_VPMID_ADC Register (Address = 0x2E) [Reset = 0x0000]

REG0x2E_VPMID_ADC is shown in Figure 9-47 and described in Table 9-40.

Return to the Summary Table.

VPMID ADC

**Figure 9-47. REG0x2E_VPMID_ADC Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | VPMID_ADC | | | | | | |
| R-0x0 | R-0x0 | | | | | | |

**Figure 9-47. REG0x2E_VPMID_ADC Register (continued)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| VPMID_ADC | | | | | | RESERVED | |
| R-0x0 | | | | | | R-0x0 | |

**Table 9-40. REG0x2E_VPMID_ADC Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15 | RESERVED | R | 0x0 | | Reserved |
| 14:2 | VPMID_ADC | R | 0x0 | | VPMID ADC reading<br>POR: 0mV (0h)<br>Range: 0mV-19850mV (0h-1388h)<br>Clamped High<br>Bit Step: 3.97mV |
| 1:0 | RESERVED | R | 0x0 | | Reserved |

### 9.6.2.33 REG0x30_VBAT_ADC Register (Address = 0x30) [Reset = 0x0000]

REG0x30_VBAT_ADC is shown in Figure 9-48 and described in Table 9-41.

Return to the Summary Table.

VBAT ADC

**Figure 9-48. REG0x30_VBAT_ADC Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | VBAT_ADC | | | | |
| R-0x0 | | | R-0x0 | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VBAT_ADC | | | | | | | RESERVED |
| R-0x0 | | | | | | | R-0x0 |

**Table 9-41. REG0x30_VBAT_ADC Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:13 | RESERVED | R | 0x0 | | Reserved |
| 12:1 | VBAT_ADC | R | 0x0 | | VBAT ADC reading<br>POR: 0mV (0h)<br>Range: 0mV-5572mV (0h-AF0h)<br>Clamped High<br>Bit Step: 1.99mV |
| 0 | RESERVED | R | 0x0 | | Reserved |

### 9.6.2.34 REG0x32_VSYS_ADC Register (Address = 0x32) [Reset = 0x0000]

REG0x32_VSYS_ADC is shown in Figure 9-49 and described in Table 9-42.

Return to the Summary Table.

VSYS ADC

**Figure 9-49. REG0x32_VSYS_ADC Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | VSYS_ADC | | | | |
| R-0x0 | | | R-0x0 | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VSYS_ADC | | | | | | | RESERVED |
| R-0x0 | | | | | | | R-0x0 |

**Table 9-42. REG0x32_VSYS_ADC Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:13 | RESERVED | R | 0x0 | | Reserved |
| 12:1 | VSYS_ADC | R | 0x0 | | VSYS ADC reading<br>POR: 0mV (0h)<br>Range: 0mV-5572mV (0h-AF0h)<br>Clamped High<br>Bit Step: 1.99mV |
| 0 | RESERVED | R | 0x0 | | Reserved |

### 9.6.2.35 REG0x34_TS_ADC Register (Address = 0x34) [Reset = 0x0000]

REG0x34_TS_ADC is shown in Figure 9-50 and described in Table 9-43.

Return to the Summary Table.

TS ADC

**Figure 9-50. REG0x34_TS_ADC Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | TS_ADC | | | |
| R-0x0 | | | | R-0x0 | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TS_ADC | | | | | | | |
| R-0x0 | | | | | | | |

**Table 9-43. REG0x34_TS_ADC Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:12 | RESERVED | R | 0x0 | | Reserved |
| 11:0 | TS_ADC | R | 0x0 | | TS ADC reading as TS pin voltage in percentage of bias reference. Valid with TS pin bias reference active.<br>POR: 0%(0h)<br>Range: 0% - 98.3103% (0h-3FFh)<br>Clamped High<br>Bit Step: 0.0961% |

### 9.6.2.36 REG0x36_TDIE_ADC Register (Address = 0x36) [Reset = 0x0000]

REG0x36_TDIE_ADC is shown in Figure 9-51 and described in Table 9-44.

Return to the Summary Table.

TDIE ADC

**Figure 9-51. REG0x36_TDIE_ADC Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | TDIE_ADC | | | |
| R-0x0 | | | | R/W-0x0 | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TDIE_ADC | | | | | | | |
| R/W-0x0 | | | | | | | |

**Table 9-44. REG0x36_TDIE_ADC Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 15:12 | RESERVED | R | 0x0 | | Reserved |

**Table 9-44. REG0x36_TDIE_ADC Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 11:0 | TDIE_ADC | R/W | 0x0 | | TDIE ADC reading<br>Reported in 2 's Complement.<br>POR: 0°C(0h)<br>Format: 2s Complement<br>Range: -40°C - 150°C (FB0h-12Ch)<br>Clamped Low<br>Clamped High<br>Bit Step: 0.5°C |

### 9.6.2.37 REG0x38_Part_Information Register (Address = 0x38) [Reset = 0x02]

REG0x38_Part_Information is shown in Figure 9-52 and described in Table 9-45.

Return to the Summary Table.

Part Information

**Figure 9-52. REG0x38_Part_Information Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | PN | | | | DEV_REV | |
| R-0x0 | | R-0x0 | | | | R-0x2 | |

**Table 9-45. REG0x38_Part_Information Register Field Descriptions**

| Bit | Field | Type | Reset | Notes | Description |
|---|---|---|---|---|---|
| 7:6 | RESERVED | R | 0x0 | | Reserved |
| 5:3 | PN | R | 0x0 | | Device Part number<br>2h = BQ25628<br>6h = BQ25629 |
| 2:0 | DEV_REV | R | 0x2 | | Device Revision |

# 10 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 10.1 Application Information

A typical application consists of the device configured as an $I^2C$ controlled power path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smartphone and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

## 10.2 Typical Application

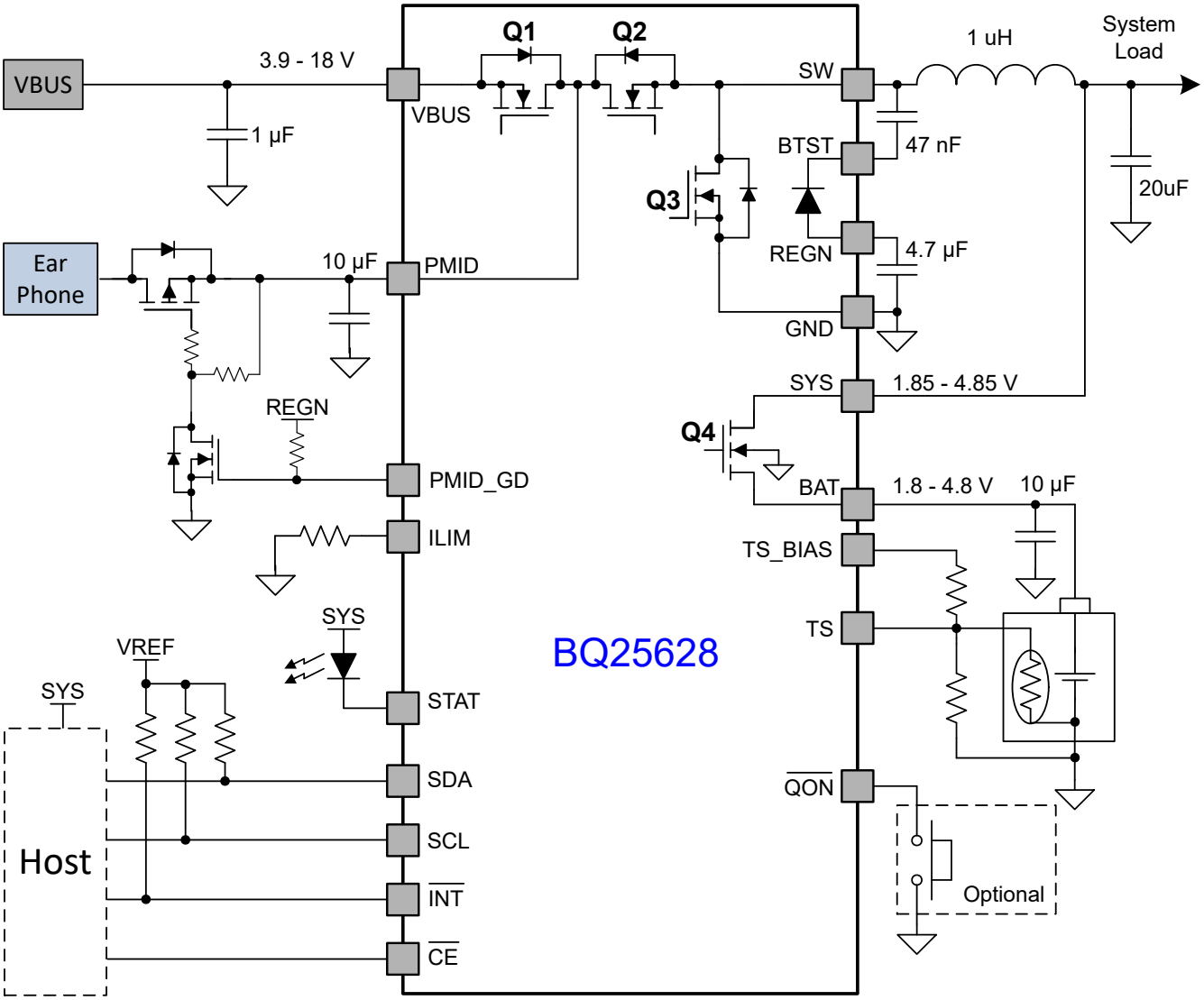



**Figure 10-1. BQ25628 Application Diagram**

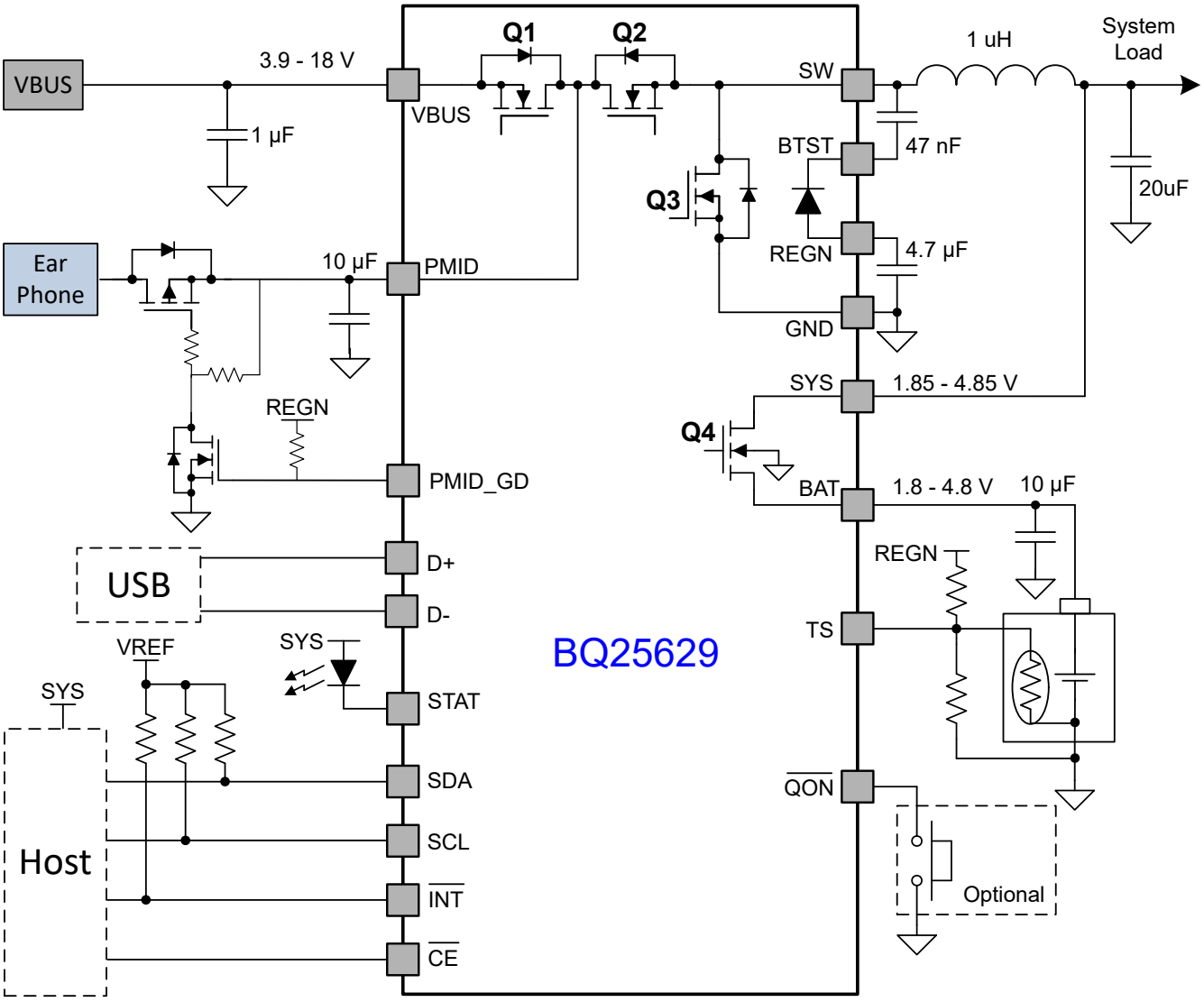



**Figure 10-2. BQ25629 Application Diagram**

### 10.2.1 Design Requirements

**Table 10-1. Design Requirements**

| PARAMETER | VALUE |
|---|---|
| VBUS range | 3.9 -18.0 V |
| Input current limit (REG0x06-0x07) | 3200 mA |
| Fast charge current (REG0x02-0x03) | 320 mA |
| Minimum system voltage (REG0x0E-0x0F) | 3520 mV |
| Battery regulation voltage (REG0x04-0x05) | 4200 mV |

### 10.2.2 Detailed Design Procedure

#### *10.2.2.1 Inductor Selection*

The 1.5-MHz switching frequency allows the use of small inductor and capacitor values to maintain an inductor saturation current higher than the charging current ($I_{CHG}$) plus half the ripple current ($I_{RIPPLE}$):

$$I_{SAT} \geq I_{CHG} + (1/2)\ I_{RIPPLE} \quad (5)$$

The inductor ripple current depends on the input voltage ($V_{VBUS}$), the duty cycle (D = $V_{BAT}/V_{VBUS}$), the switching frequency ($f_S$) and the inductance (L).

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{fs \times L} \quad (6)$$

The maximum inductor ripple current occurs when the duty cycle (D) is approximately 0.5. Usually inductor ripple is designed between 20% and 40% of the maximum charging current as a trade-off between inductor size and efficiency.

#### *10.2.2.2 Input Capacitor*

Design input capacitance to provide enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current $I_{Cin}$ occurs where the duty cycle is closest to 50% and can be estimated using Equation 7.

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \quad (7)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed as close as possible to the drain of the high-side MOSFET (PMID) and source of the low-side MOSFET (GND). Voltage rating of the capacitor must be higher than normal input voltage level. A rating of 25-V or higher capacitor is preferred for 15 V input voltage. 10-µF ceramic capacitor is suggested for typical of 2.0A charging current.

#### *10.2.2.3 Output Capacitor*

Ensure that the output capacitance has enough ripple current rating to absorb the output switching ripple current. Equation 8 shows the output capacitor RMS current $I_{COUT}$ calculation.

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (8)$$

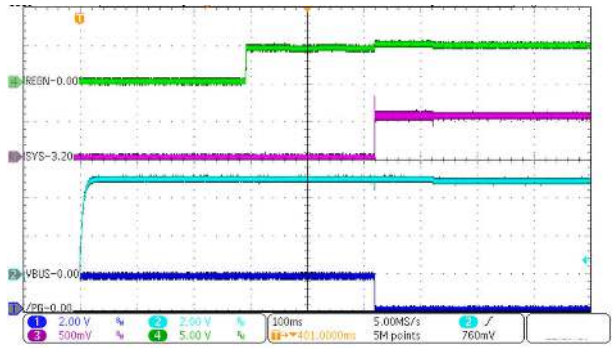
The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_{SYS} = \frac{V_{SYS}}{8 \times L \times C_{SYS} \times f_{SW}^2}\left(1 - \frac{V_{SYS}}{V_{VBUS}}\right) \quad (9)$$

At certain input and output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

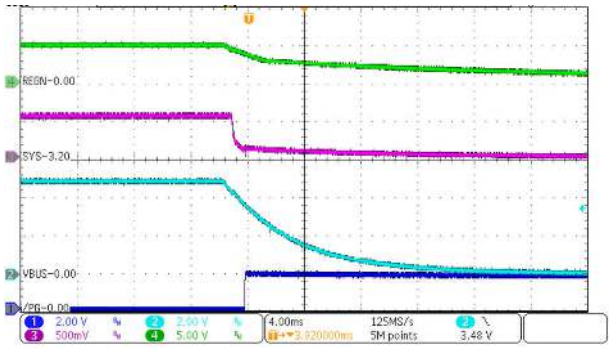
The charger device has internal loop compensation optimized for ≥ 10-µF ceramic output capacitor. The preferred ceramic capacitor is 10-V rating, X7R or X5R.

### 10.2.3 Application Curves



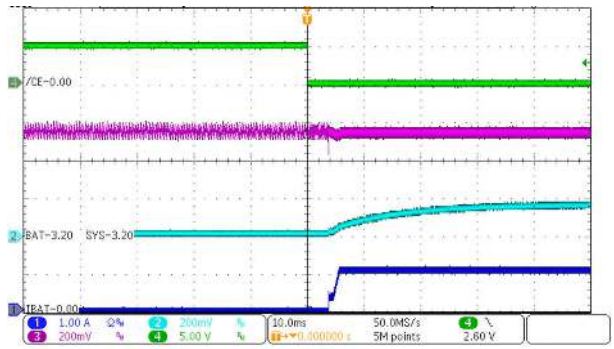

$V_{VBUS}$ = 5 V $V_{BAT}$ = 3.2 V
$I_{CHG}$ = 1 A

**Figure 10-3. Power-Up with Charge Enabled**



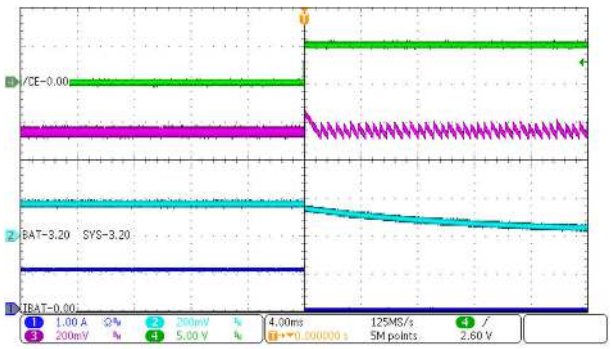

$V_{VBUS}$ = 5 V $V_{BAT}$ = 3.2 V
$I_{CHG}$ = 1 A

**Figure 10-4. Power-Down**



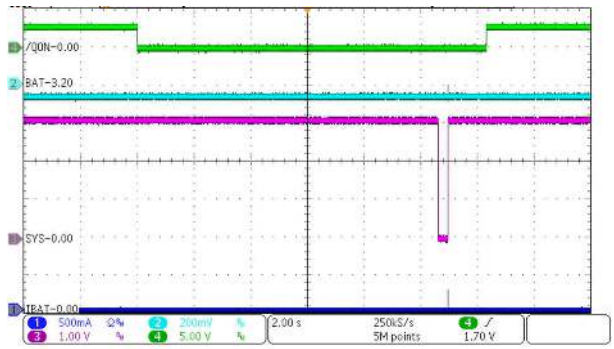

$V_{VBUS}$ = 5 V $V_{BAT}$ = 3.2 V
$I_{CHG}$ = 1 A

**Figure 10-5. Charge Enable**



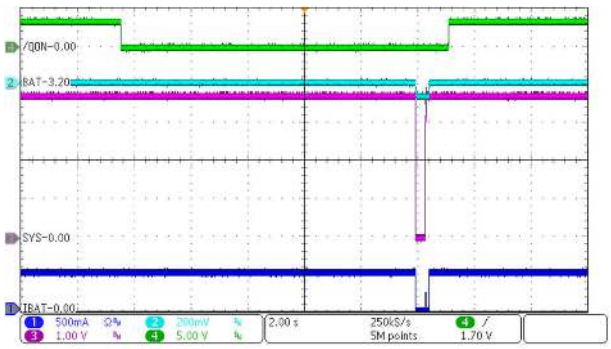

$V_{VBUS}$ = 5 V $V_{BAT}$ = 3.2 V
$I_{CHG}$ = 1 A

**Figure 10-6. Charge Disable**



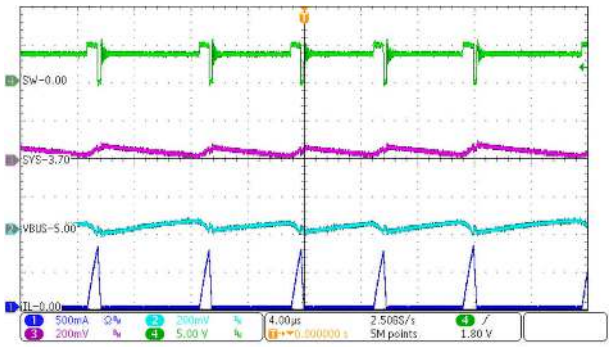

$V_{BAT}$ = 3.2 V

**Figure 10-7. System Reset by QON without VBUS Present**



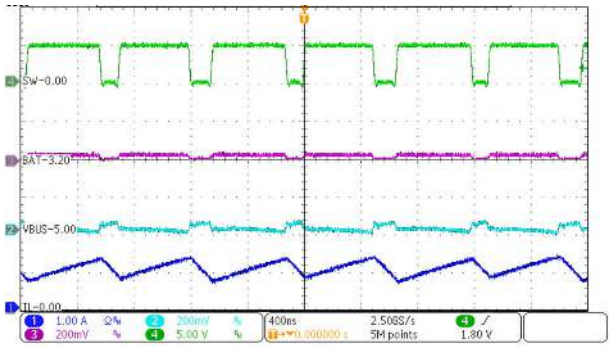

$V_{VBUS}$ = 5 V $V_{BAT}$ = 3.2 V
$I_{CHG}$ = 480mA

**Figure 10-8. System Reset by QON with VBUS Present**



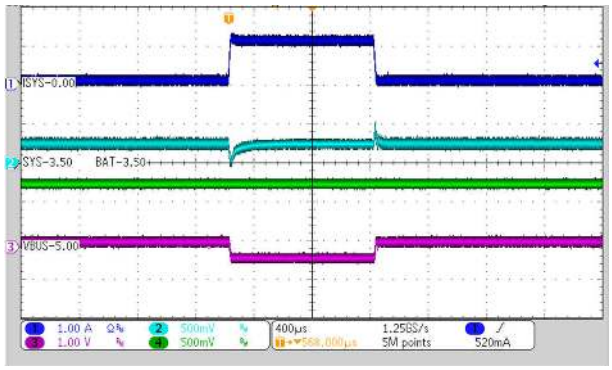

$V_{VBUS}$ = 5 V
$I_{SYS}$ = 50 mA
$V_{BAT}$ = 3.2 V
Charge Disabled

**Figure 10-9. PFM Switching in Buck Mode**



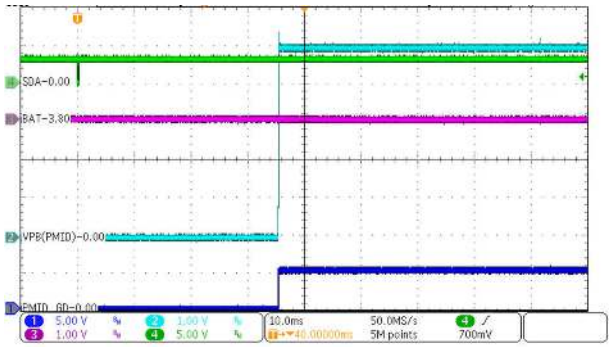

$V_{VBUS}$ = 5 V
$I_{CHG}$ = 1 A
$V_{VBAT}$ = 3.2 V

**Figure 10-10. PWM Switching in Buck Mode**



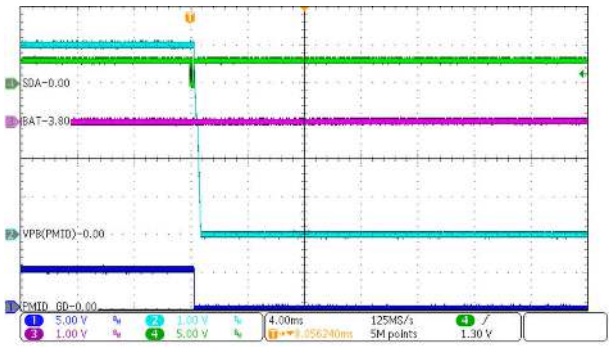

$V_{VBUS}$ = 5 V
$I_{SYS}$ from 0 A to 1 A
$V_{BAT}$ = 3.2 V
Charge Disabled

**Figure 10-11. System Load Transient**



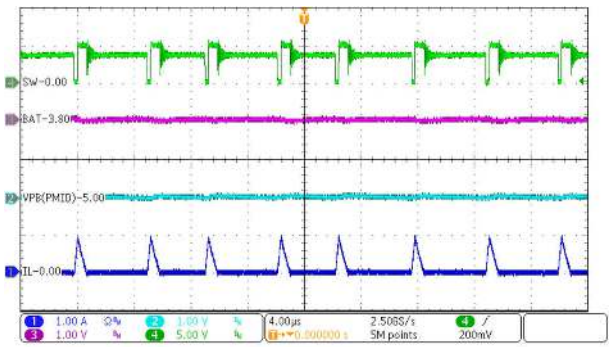

$V_{BAT}$ = 3.8 V
$I_{BOOST}$ = 100 mA
$V_{BOOST}$ = 5.04 V

**Figure 10-12. Boost Mode Power Up**



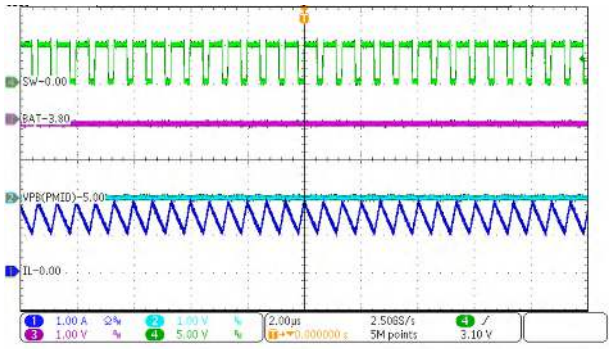

$V_{BAT}$ = 3.8 V
$I_{BOOST}$ = 100 mA
$V_{BOOST}$ = 5.04V

**Figure 10-13. Boost Mode Power Down**



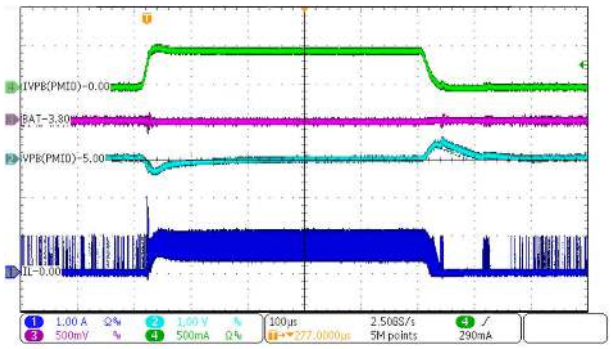

$V_{BAT}$ = 3.8 V
$I_{BOOST}$= 50 mA
$V_{BOOST}$ = 5.04V

**Figure 10-14. PFM Switching in Boost Mode**




$V_{BAT}$ = 3.8 V $V_{BOOST}$ = 5.04V
$I_{BOOST}$= 1 A

**Figure 10-15. PWM Switching in Boost Mode**




$V_{BAT}$ = 3.8 V $V_{BOOST}$ = 5.04 V
$I_{BOOST}$ from 5 mA to 500 mA

**Figure 10-16. Boost Mode Load Transient**

## 11 Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 3.9 V and 18.0 V input with at least 100-mA current rating connected to VBUS or a single-cell Li-Ion battery with voltage > $V_{BATUVLO}$ connected to BAT.

# 12 Layout

## 12.1 Layout Guidelines

The switching node rise and fall times should be minimized for lowest switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 12-1) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

1. For lowest switching noise during forward/charge mode, place the decoupling capacitor CPMID1 and then bulk capacitor CPMID2 positive terminals as close as possible to PMID pin. Place the capacitor ground terminal close to the GND pin using the shortest copper trace connection or GND plane on the same layer as the IC. See Figure 12-2.
2. For lowest switching noise during reverse/OTG mode, place the CSYS1 and CSYS2 output capacitors' positive terminals near the SYS pin. The capacitors' ground terminals must be via'd down through multiple vias to an all ground internal layer that returns to IC GND pin through multiple vias under the IC. See Figure 12-2.
3. Since REGN powers the internal gate drivers, place the CREGN capacitor positive terminal close to REGN pin to minimize switching noise. The capacitor's ground terminal must be via'd down through multiple vias to an all ground internal layer that returns to IC GND pin through multiple vias under the IC. See Figure 12-2.
4. Place the CVBUS and CBAT capacitors positive terminals as close to the VBUS and BAT pins as possible. The capacitors' ground terminals must be via'd down through multiple vias to an all ground internal layer that returns to IC GND pin through multiple vias under the IC. See Figure 12-2.
5. Place the inductor input pin near the positive terminal of the SYS pin capacitors. Due to the PMID capacitor placement requirements, the inductor's switching node terminal must be via'd down with multiple via's to a second internal layer with a wide trace that returns to the SW pin with multiple vias. See Figure 12-3. Using multiple vias ensures that the via's additional resistance is negligible compared to the inductor's dc resistance and therefore does not impact efficiency. The vias additional series inductance is negligible compared to the inductor's inductance.
6. Place the BTST capacitor on the opposite side from the IC using vias to connect to the BTST pin and SW node. See Figure 12-4.
7. A separate analog GND plane for non-power related resistors and capacitors is not required if those components are placed away from the power components traces and planes.
8. Ensure that the I2C SDA and SCL lines are routed away from the SW node.

Additionally, it is important that the PCB footprint and solder mask for BQ25628 cover the entire length of each of the pins. GND, SW, PMID, SYS and BAT pins extend further into the package than the other pins. Using the entire length of these pins reduces parasitic resistance and increases thermal conductivity from the package into the board.

## 12.2 Layout Example

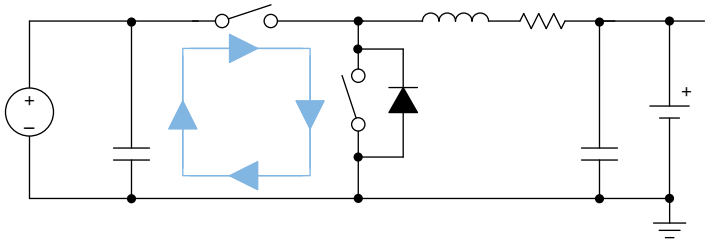


**Figure 12-1. High Frequency Current Path**

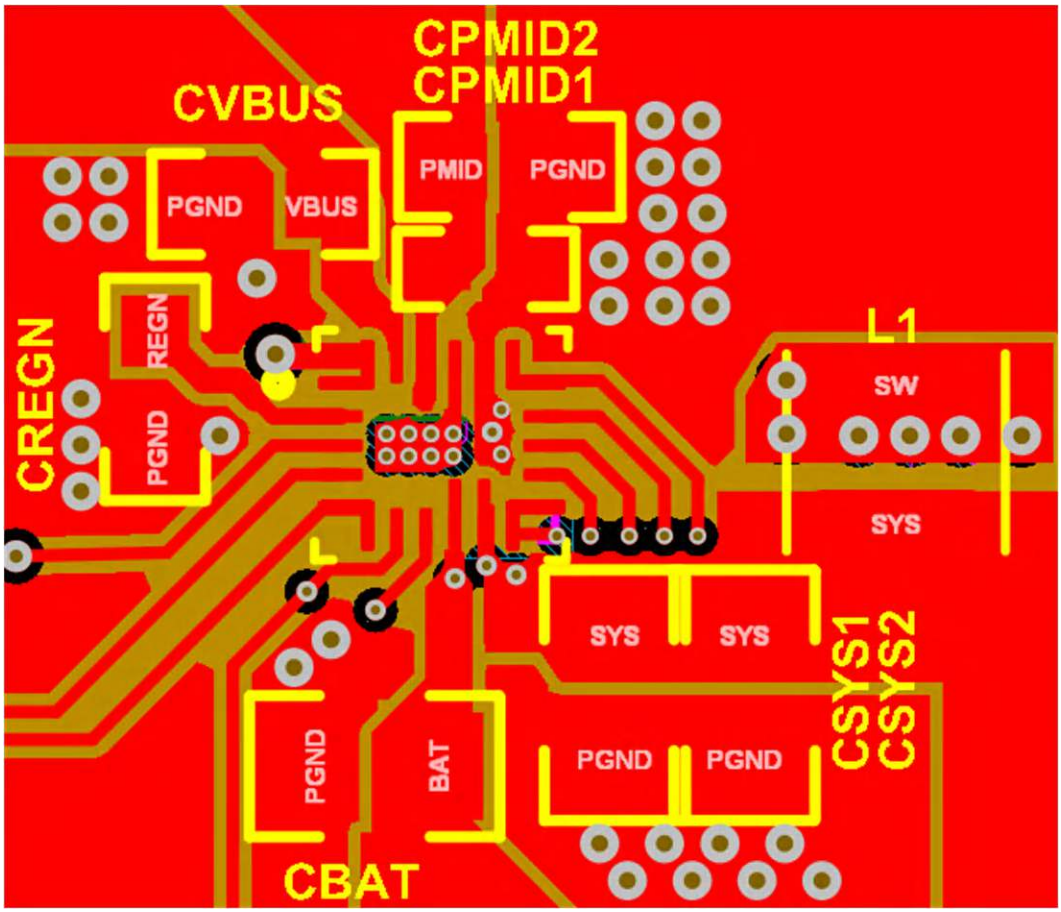



**Figure 12-2. Layout Example: Top Layer (red) and All PGND Internal Layer 2 (brown)**

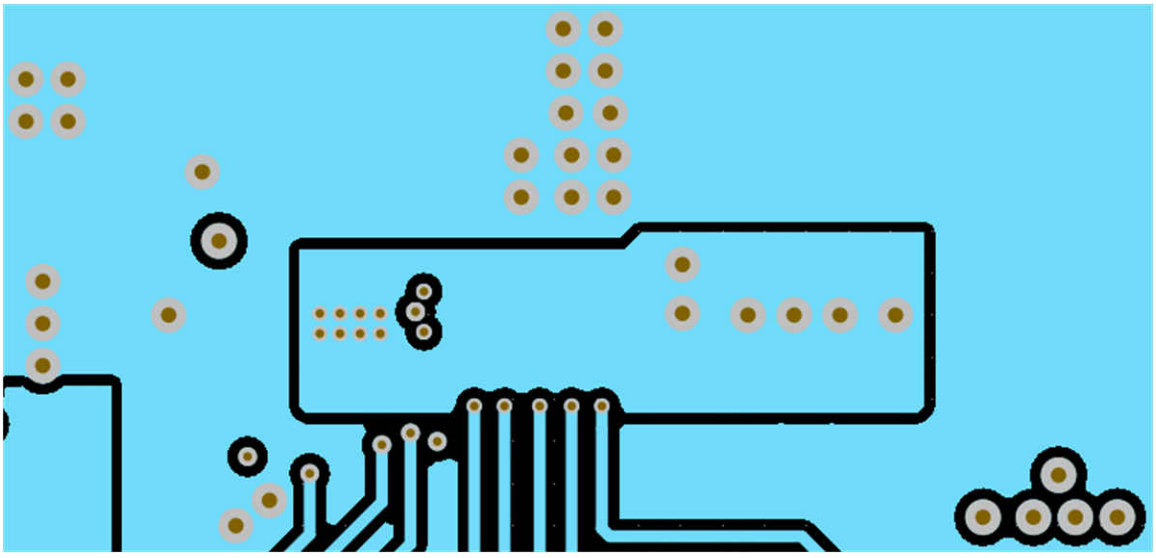


**Figure 12-3. Layout Example: Inner Layer 3 (AGND pour; SW node pour; signal routing)**

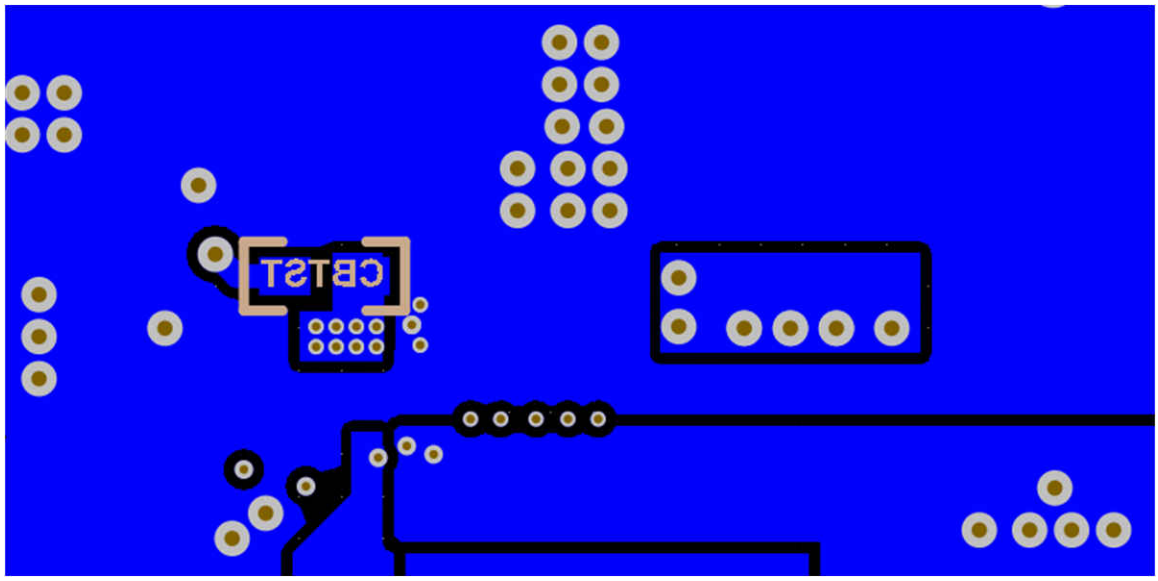



**Figure 12-4. Layout Example: Bottom Layer X-Ray From Top (PGND pour; BTST capacitor; redundant SW, SYS and BAT pours)**

# 13 Device and Documentation Support

## 13.1 Device Support

### 13.1.1 Third-Party Products Disclaimer

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## 13.2 Documentation Support

### 13.2.1 Related Documentation

For related documentation see the following:

- *BQ25601 and BQ25601D (PWR877) Evaluation Module User's Guide*

## 13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 13.5 Trademarks

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## 13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 13.7 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ25628RYKR | ACTIVE | WQFN-HR | RYK | 18 | 3000 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 85 | BQ628 | Samples |
| BQ25629RYKR | ACTIVE | WQFN-HR | RYK | 18 | 3000 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 85 | BQ629 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

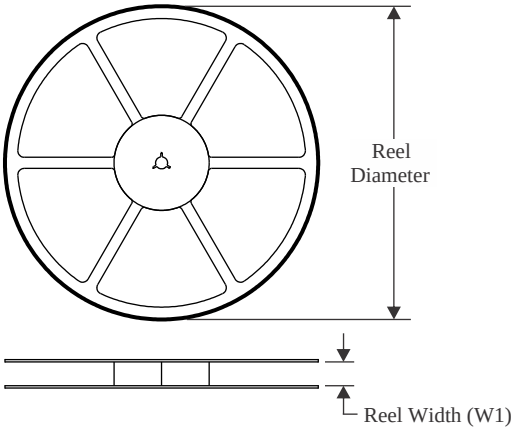
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

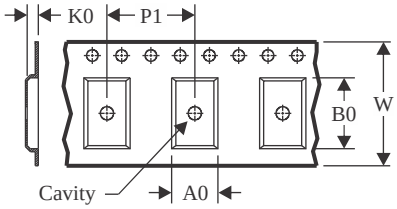
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

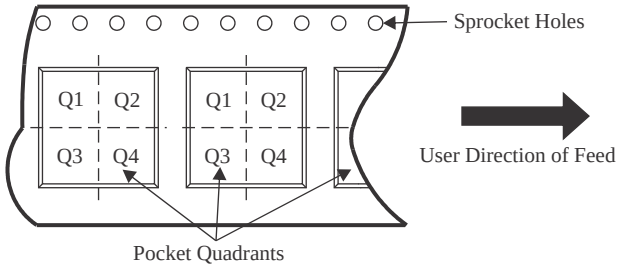



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

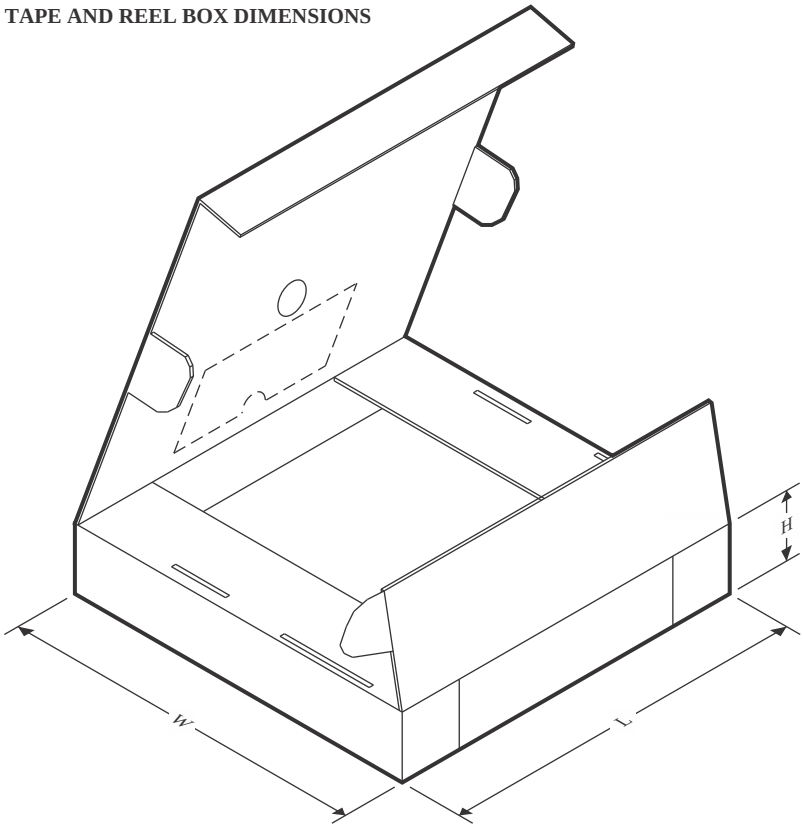
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ25628RYKR | WQFN-HR | RYK | 18 | 3000 | 180.0 | 12.4 | 2.8 | 3.3 | 1.1 | 4.0 | 12.0 | Q2 |
| BQ25629RYKR | WQFN-HR | RYK | 18 | 3000 | 180.0 | 12.4 | 2.8 | 3.3 | 1.1 | 4.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

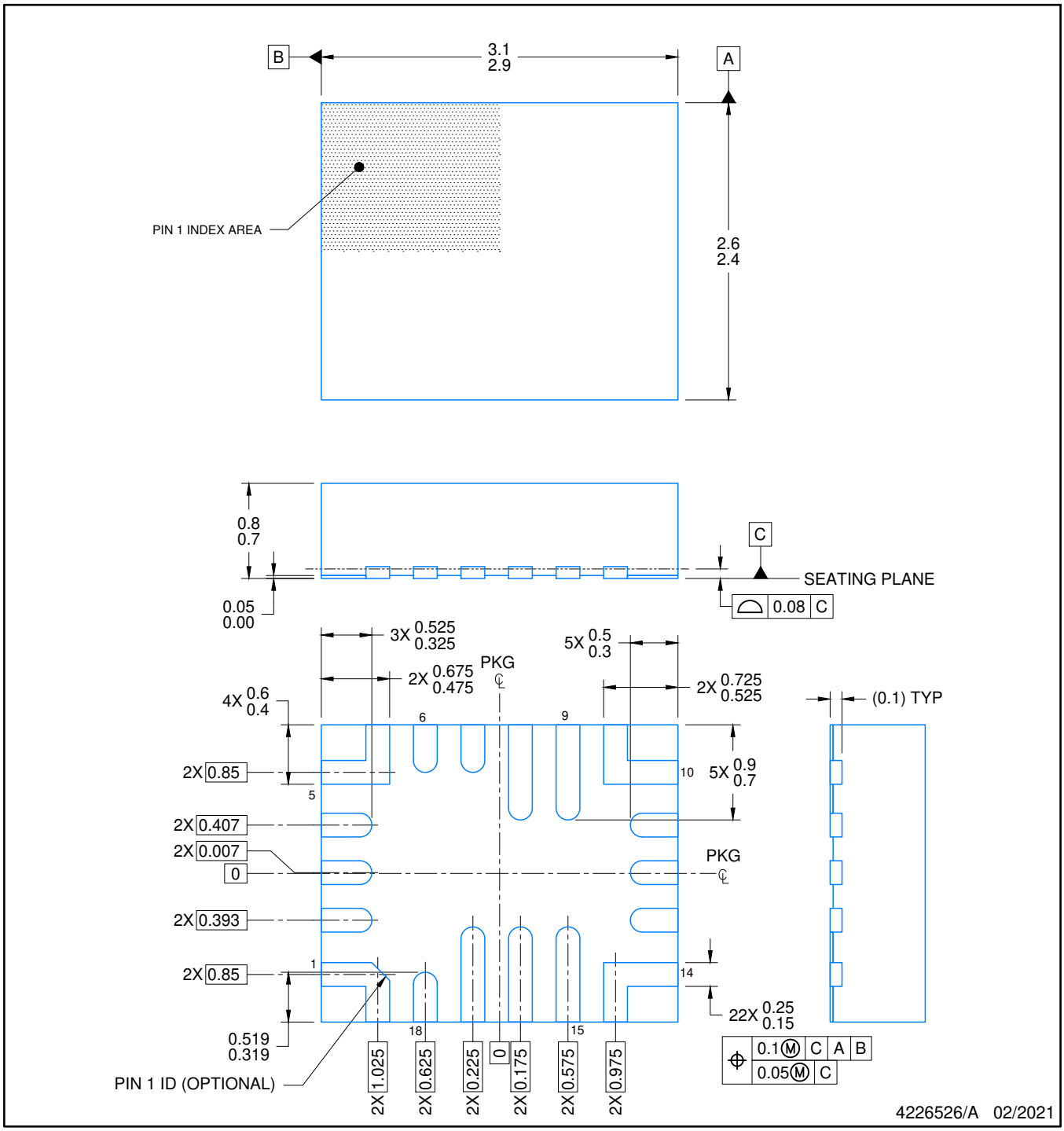
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| BQ25628RYKR | WQFN-HR | RYK | 18 | 3000 | 210.0 | 185.0 | 35.0 |
| BQ25629RYKR | WQFN-HR | RYK | 18 | 3000 | 210.0 | 185.0 | 35.0 |

# PACKAGE OUTLINE

## RYK0018A

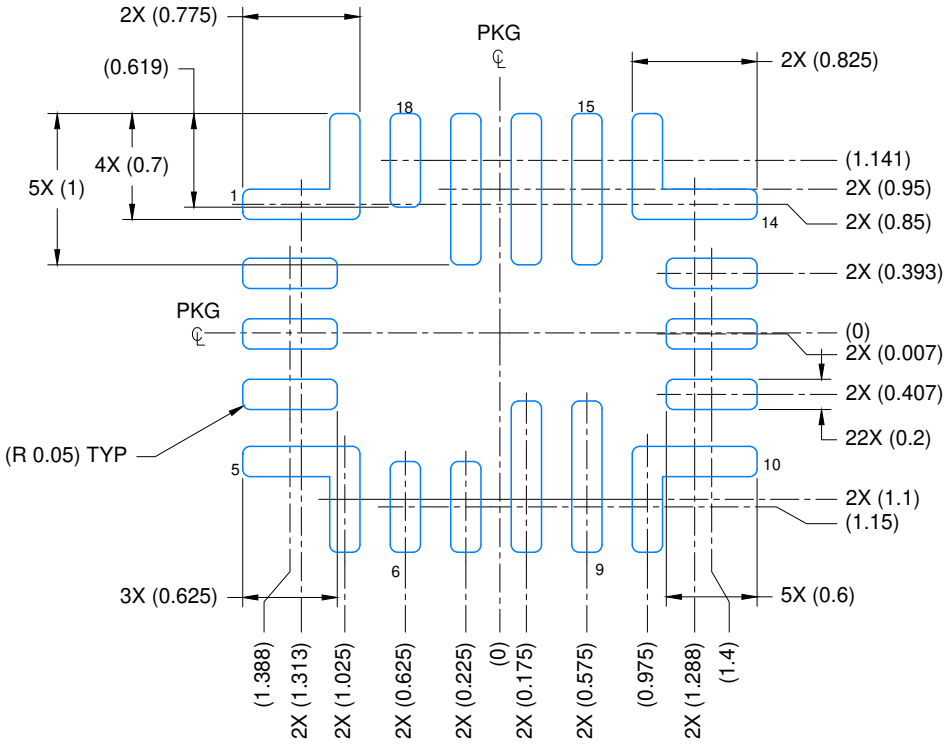
## WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

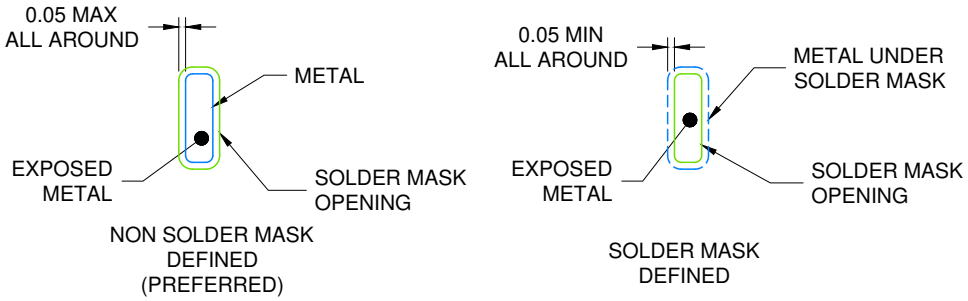



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

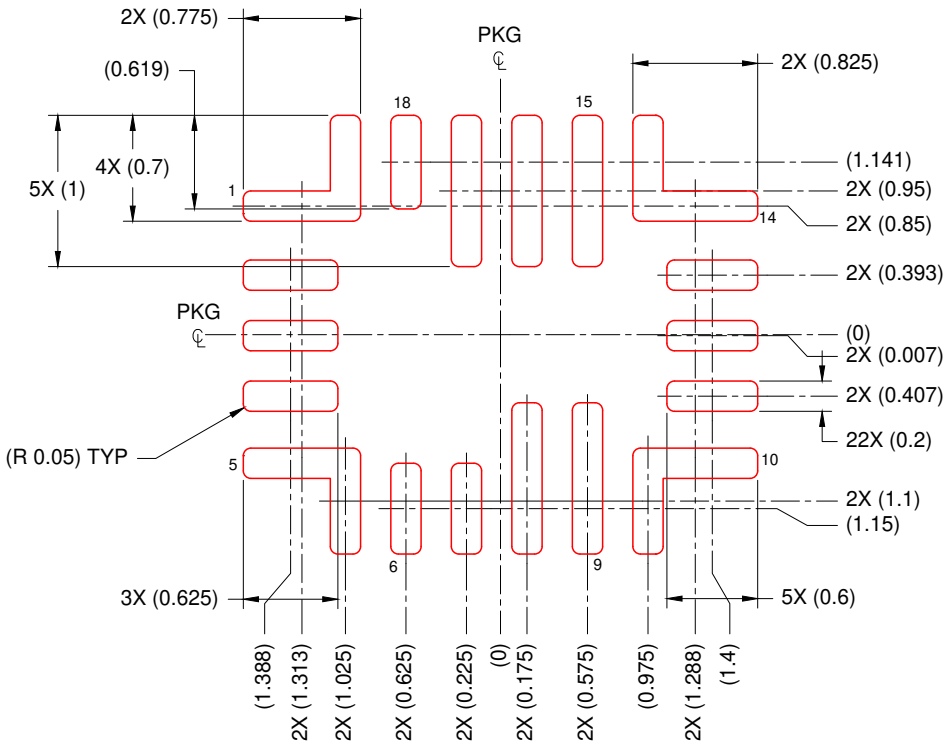



SOLDER MASK DETAILS

4226526/A 02/2021

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 20X

4226526/A 02/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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