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74ABT543
Octal Registered Transceiver with 3-STATE Outputs

General Description

The ABT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

Features

- Back-to-back registers for storage
- Bidirectional data path
- A and B outputs have current sourcing capability of 32 mA and current sinking capability of 64 mA
- Separate controls for data flow in each direction
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

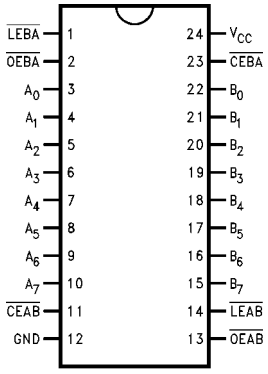
Ordering Code:

Order Number	Package Number	Package Description
74ABT543CSC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ABT543CMSA	MSA24	24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ABT543CMTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



Pin Descriptions

Pin Names	Description
$\overline{OEAB}$, $\overline{OEBA}$	Output Enable Inputs
$\overline{LEAB}$, $\overline{LEBA}$	Latch Enable Inputs
$\overline{CEAB}$, $\overline{CEBA}$	Chip Enable Inputs
A_0–A_7	Side A Inputs or 3-STATE Outputs
B_0–B_7	Side B Inputs or 3-STATE Outputs

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Functional Description

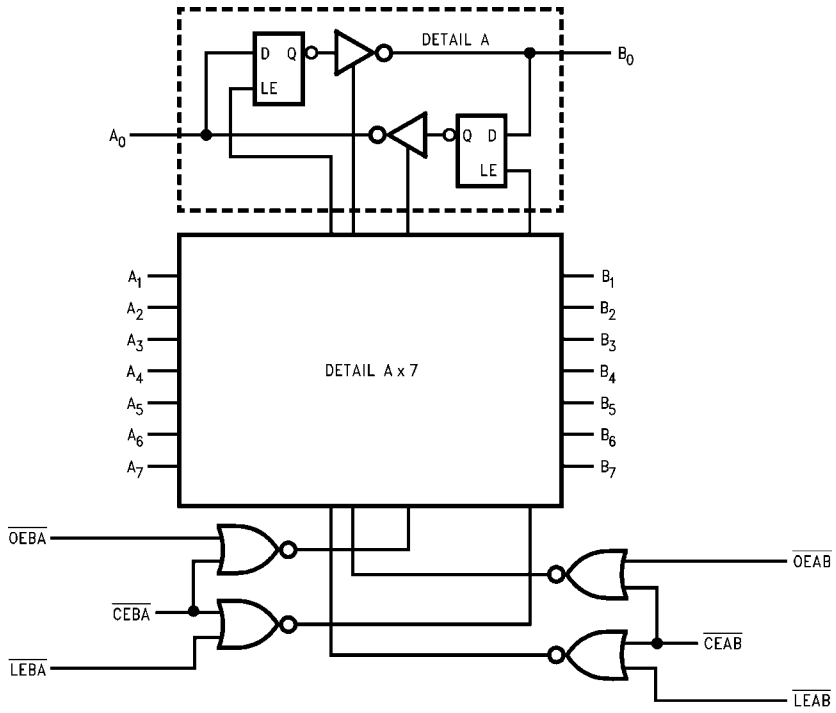
The ABT543 contains two sets of D-type latches, with separate input and output controls for each. For data flow from A to B, for example, the A to B Enable ($\overline{CEAB}$) input must be low in order to enter data from the A Port or take data from the B Port as indicated in the Data I/O Control Table. With $\overline{CEAB}$ low, a low signal on ($\overline{LEAB}$) input makes the A to B latches transparent; a subsequent low to high transition of the $\overline{LEAB}$ line puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the B output buffers are active and reflect the data present on the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	HIGH Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	HIGH Z
L	X	L	—	Driving

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	−40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate (ΔV/Δt)	
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage	0.8			V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V		I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	2.5					I_{OH} = −3 mA, (A_n, B_n)
		2.0					I_{OH} = −32 mA, (A_n, B_n)
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA, (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 µA, (Non-I/O Pins)
							All Other Pins Grounded
I_{IH}	Input HIGH Current			1	µA	Max	V_{IN} = 2.7V (Non-I/O Pins) (Note 3)
				1			V_{IN} = V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	µA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	µA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			−1	µA	Max	V_{IN} = 0.5V (Non-I/O Pins) (Note 3)
				−1			V_{IN} = 0.0V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current			10	µA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OEAB}$ or $\overline{CEAB}$ = 2V
I_{IL} + I_{OZL}	Output Leakage Current			−10	µA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OEAB}$ or $\overline{CEAB}$ = 2V
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	µA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	µA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCLH}	Power Supply Current			50	µA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			50	µA	Max	Outputs 3-STATE; All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	V_I = V_{CC} − 2.1V; All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load (Note 5)			0.18	mA/MHz	Max	Outputs Open, $\overline{CEAB}$ and $\overline{OEAB}$ = GND, $\overline{CEBA}$ = V_{CC}, One Bit Toggling, 50% Duty Cycle, (Note 4)

Note 3: Guaranteed but not tested.

Note 4: For 8-bit toggling. I_{CCD} < 1.4 mA/MHz.

Note 5: Guaranteed, but not tested.

DC Electrical Characteristics

(SOIC Package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.7	1.0	V	5.0	T_A = 25°C (Note 6)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	–1.2	–0.8		V	5.0	T_A = 25°C (Note 6)
V_{OHV}	Minimum HIGH Level Dynamic Output Voltage	2.5	3.0		V	5.0	T_A = 25°C (Note 7)
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	2.0	1.7		V	5.0	T_A = 25°C (Note 8)
V_{ILD}	Maximum LOW Level Dynamic Input Voltage		0.7	0.9	V	5.0	T_A = 25°C (Note 8)

Note 6: Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 7: Max number of outputs defined as (n). n–1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

Note 8: Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

AC Electrical Characteristics

(SOIC and SSOP Packages)

Symbol	Parameter	T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			T_A = –40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	1.5	3.1	4.8	1.5	4.8	ns
t_{PHL}	A_n to B_n or B_n to A_n	1.5		4.8	1.5	4.8	
t_{PLH}	Propagation Delay						
t_{PHL}	$\overline{LEAB}$ to B_n, $\overline{LEBA}$ to A_n	1.6	3.4	5.3	1.6	5.3	ns
	$\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	1.6		5.3	1.6	5.3	
t_{PZH}	Enable Time						
t_{PZL}	$\overline{LEAB}$ to B_n, $\overline{LEBA}$ to A_n	1.5	3.6	5.8	1.5	5.8	ns
	$\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	1.5		5.8	1.5	5.8	
t_{PHZ}	Disable Time	2.0	4.0	6.5	2.0	6.5	ns
t_{PLZ}	$\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	2.0		6.5	2.0	6.5	

AC Operating Requirements

(SOIC and SSOP Packages)

Symbol	Parameter	T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF		T_A = –40°C to +85°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units
		Min	Max	Min	Max	
t_S(H)	Setup Time, HIGH or LOW	1.5		1.5		ns
t_S(L)	A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	1.5		1.5		
t_H(H)	Hold Time, HIGH or LOW	1.0		1.0		ns
t_H(L)	A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	1.0		1.0		
t_S(H)	Setup Time, HIGH or LOW	1.5		1.5		ns
t_S(L)	A_n or B_n to $\overline{CEAB}$ or $\overline{CEBA}$	1.5		1.5		
t_H(H)	Hold Time, HIGH or LOW	1.3		1.3		ns
t_H(L)	A_n or B_n to $\overline{CEAB}$ or $\overline{CEBA}$	1.3		1.3		
t_W(L)	Pulse Width, LOW	3.0		3.0		ns

Extended AC Electrical Characteristics

(SOIC Package)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 9)			$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 1 Output Switching (Note 10)		$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 11)		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{TOGGLE}	Max Toggle Frequency		100						MHz
t_{PLH}	Propagation Delay	1.5		6.2	2.0	7.5	2.5	10.0	ns
t_{PHL}	A_n to B_n or B_n to A_n	1.5		6.2	2.0	7.5	2.5	10.0	
t_{PLH}	Propagation Delay	1.5		6.5	2.0	8.0	2.5	10.5	ns
t_{PHL}	$\overline{LEAB}$ to B_n, $\overline{LEBA}$ to A_n	1.5		6.5	2.0	8.0	2.5	10.5	
t_{PZH}	Output Enable Time								
t_{PZL}	$\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	1.5		7.5	2.0	8.5	2.5	11.0	ns
	$\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	1.5		7.5	2.0	8.5	2.5	11.0	
t_{PHZ}	Output Disable Time								
t_{PLZ}	$\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	1.5		8.5	(Note 12)		(Note 12)		ns
	$\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	1.5		8.5					

Note 9: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 10: This specification is guaranteed but not tested. The limits represent propagation delay with 250pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 11: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 12: The 3-STATE delay times are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet

Skew

(SOIC Package)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 13)	$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 14)	Units
		Max	Max	
t_{OSHL} (Note 15)	Pin to Pin Skew HL Transitions	1.0	2.0	ns
t_{OSLH} (Note 15)	Pin to Pin Skew LH Transitions	1.3	2.0	ns
t_{PS} (Note 16)	Duty Cycle LH–HL Skew	2.0	4.0	ns
t_{OST} (Note 15)	Pin to Pin Skew LH/HL Transitions	2.0	4.0	ns
t_{PV} (Note 17)	Device to Device Skew LH/HL Transitions	2.5	4.5	ns

Note 13: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 14: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 15: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t_{OSHL}), LOW-to-HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (t_{OST}). This specification is guaranteed but not tested.

Note 16: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

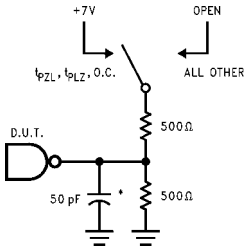
Note 17: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions: $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	V_{CC} = 0V (non I/O pins)
$C_{I/O}$ (Note 18)	Output Capacitance	11.0	pF	V_{CC} = 5.0V (A_n, B_n)

Note 18: $C_{I/O}$ is measured at frequency, f = 1 MHz, PER MLT-STD-883B, METHOD 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

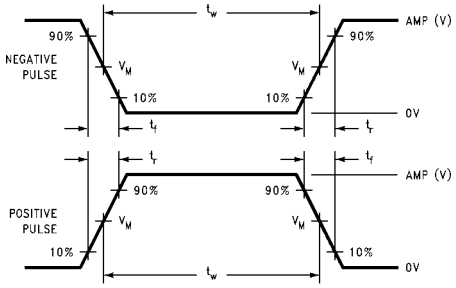


FIGURE 2. V_M = 1.5V Input Pulse Requirements

Amplitude	Rep. Rate	t_W	t_r	t_f
3V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

AC Waveforms

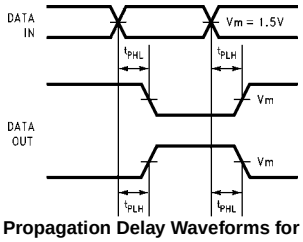


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

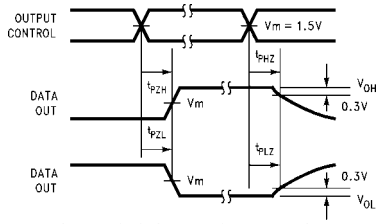


FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times

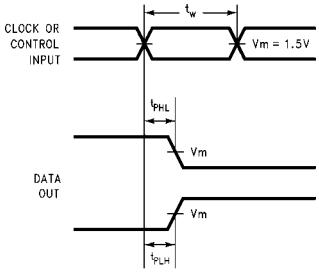


FIGURE 5. Propagation Delay, Pulse Width Waveforms

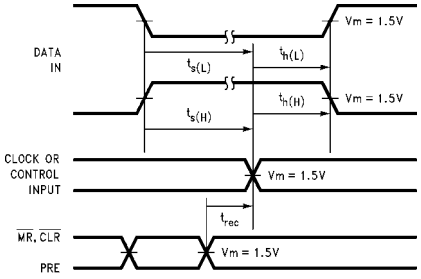
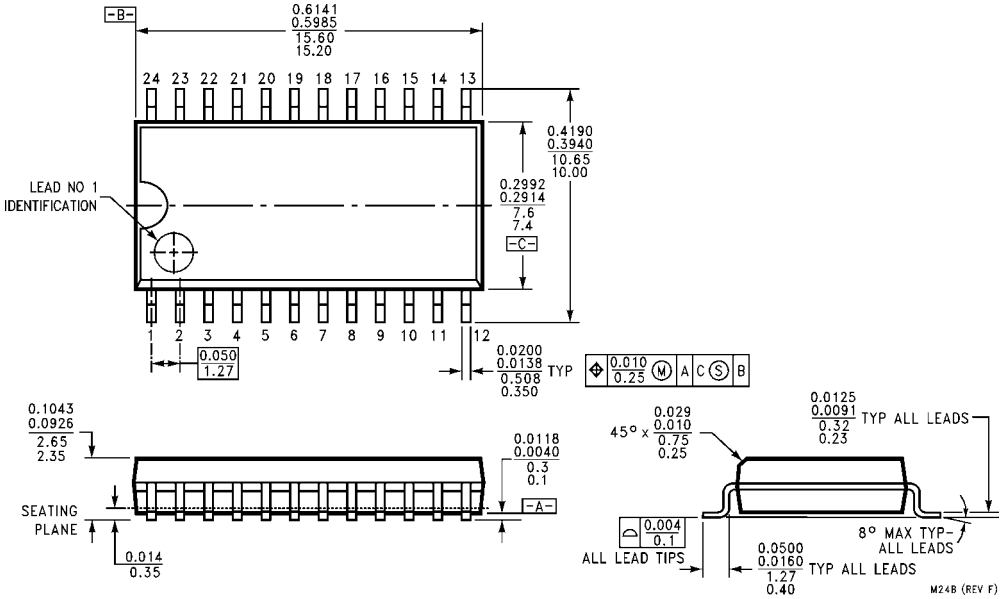
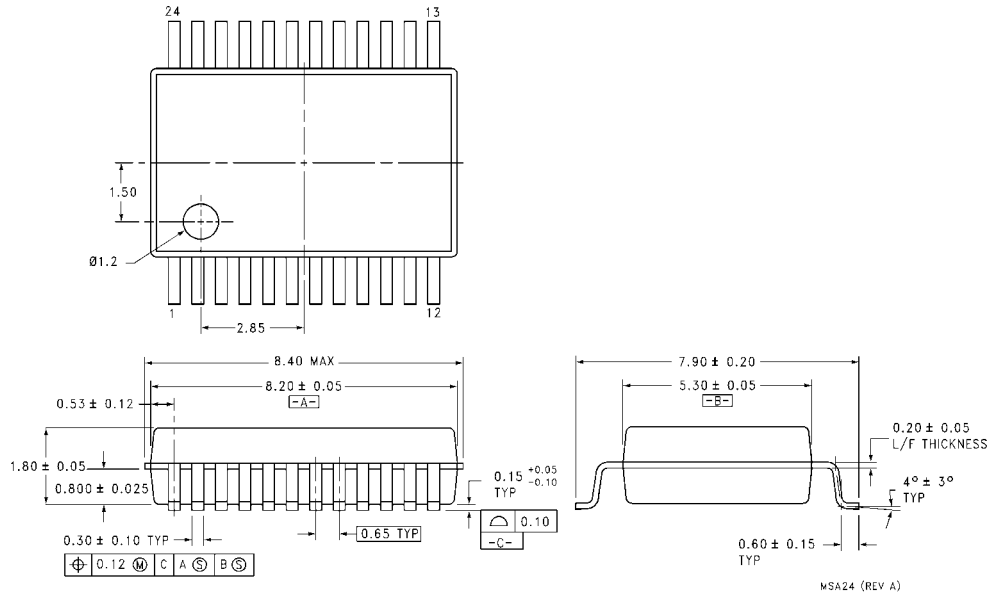


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

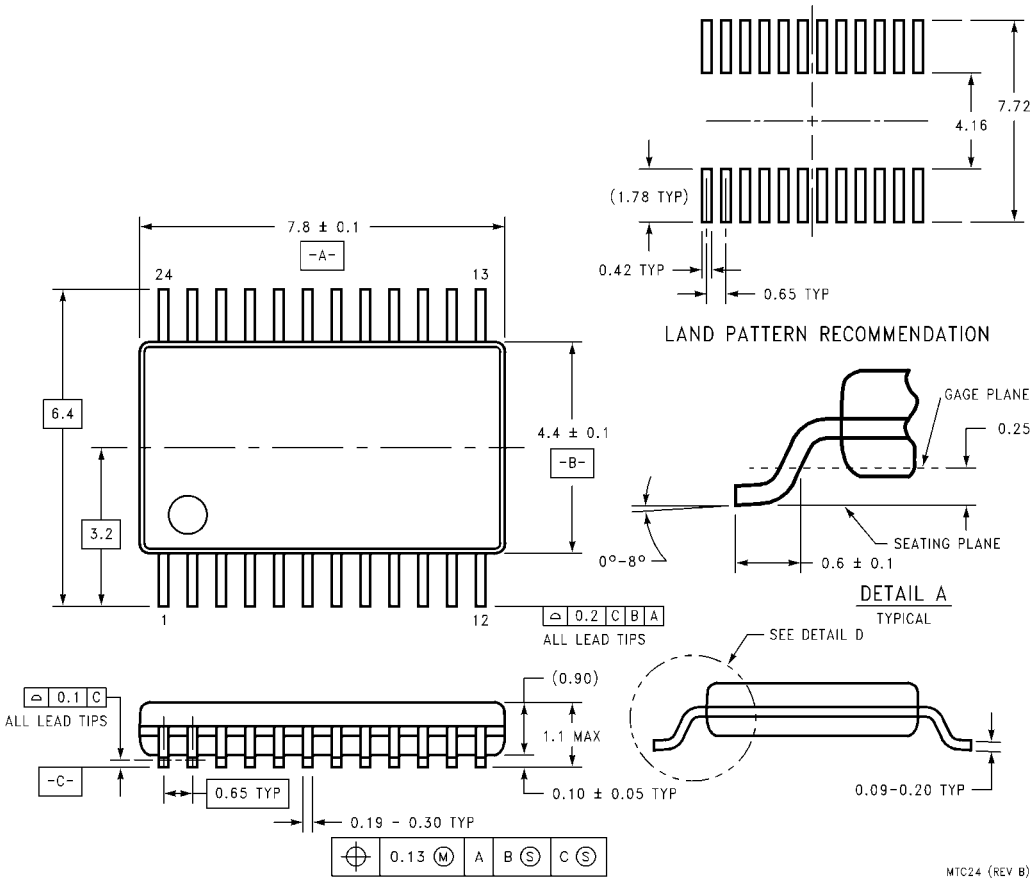


24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
Package Number M24B



24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA24

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24

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