

P-Channel Power MOSFET

-60V, -14.5A, 68 mΩ

FEATURES

- Improved dV/dt capability
- Fast switching
- 100% Eas Guaranteed
- Pb-free plating
- RoHS compliant
- Halogen-Free according to IEC 61249-2-21

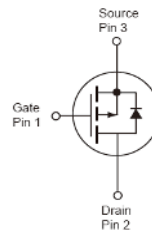
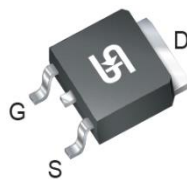
PRODUCT SUMMARY			
PARAMETER	VALUE	UNIT	
V_{DS}	-60	V	
$R_{DS(on)}$ (max)	$V_{GS} = -10V$	68	mΩ
	$V_{GS} = -4.5V$	110	
Q_g	$V_{GS} = -10V$	18	nC

APPLICATIONS

- Motor Drive
- Power Tools
- LED Lighting



TO-252 (DPAK)



Notes: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^(Note 1)	I_D	$T_C = 25^\circ\text{C}$	-14.5
		$T_C = 100^\circ\text{C}$	-9.2
Pulsed Drain Current ^(Note 2)	I_{DM}	-58	A
Single Pulse Avalanche Current ^(Note 3)	I_{AS}	-19.1	A
Single Pulse Avalanche Energy ^(Note 3)	E_{AS}	18.2	mJ
Total Power Dissipation	P_D	20.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

THERMAL RESISTANCE			
PARAMETER	SYMBOL	MAXIMUM	UNIT
Thermal Resistance – Junction to Case	$R_{\theta JC}$	6.1	$^\circ\text{C/W}$
Thermal Resistance – Junction to Ambient	$R_{\theta JA}$	62	$^\circ\text{C/W}$

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	BV_{DSS}	-60	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu A$	$V_{GS(TH)}$	-1.2	-1.4	-2.2	V
Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
Drain-Source Leakage Current	$V_{GS} = 0V, V_{DS} = -60V$	I_{DSS}	--	--	-1	μA
	$V_{GS} = 0V, V_{DS} = -48V$ $T_J = 125^\circ\text{C}$		--	--	-10	
Drain-Source On-State Resistance (Note 3)	$V_{GS} = -10V, I_D = -6A$	$R_{DS(on)}$	--	53.2	68	m Ω
	$V_{GS} = -4.5V, I_D = -3A$		--	67.4	110	
Forward Transconductance	$V_{DS} = -10V, I_D = -6A$	g_{fs}	--	15.3	--	S
Dynamic (Note 5)						
Total Gate Charge	$V_{GS} = -10V, V_{DS} = -30V,$ $I_D = -6A$	Q_g	--	18	--	nC
Gate-Source Charge		Q_{gs}	--	2.8	--	
Gate-Drain Charge		Q_{gd}	--	3.2	--	
Input Capacitance	$V_{GS} = 0V, V_{DS} = -30V,$ $f = 1.0\text{MHz}$	C_{iss}	--	929	--	pF
Output Capacitance		C_{oss}	--	68	--	
Reverse Transfer Capacitance		C_{rss}	--	55	--	
Gate Resistance	$f = 1.0\text{MHz}$	R_g	--	14	--	Ω
Switching (Note 6)						
Turn-On Delay Time	$V_{GS} = -10V, V_{DS} = -30V,$ $I_D = -1A, R_G = 6\Omega$	$t_{d(on)}$	--	6.7	--	nS
Rise Time		t_r	--	8.5	--	
Turn-Off Delay Time		$t_{d(off)}$	--	53	--	
Fall Time		t_f	--	35	--	
Source-Drain Diode						
Diode Forward Voltage (Note 4)	$V_{GS} = 0V, I_S = -1A$	V_{SD}	--	--	-1	V
Reverse Recovery Time	$I_S = -1A,$ $di/dt = 100A/\mu s$	t_{rr}	--	11.9	--	nS
Reverse Recovery Charge		Q_{rr}	--	6.2	--	nC

Notes:

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. $L = 0.1\text{mH}, V_{GS} = -10V, R_G = 25\Omega, \text{Starting } T_J = 25^\circ\text{C}$
4. Pulse test: $PW \leq 300\mu s, \text{duty cycle} \leq 2\%$
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

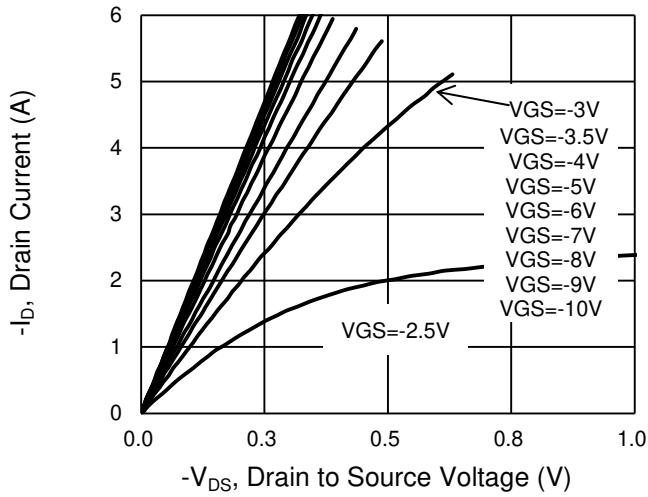
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM680P06CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

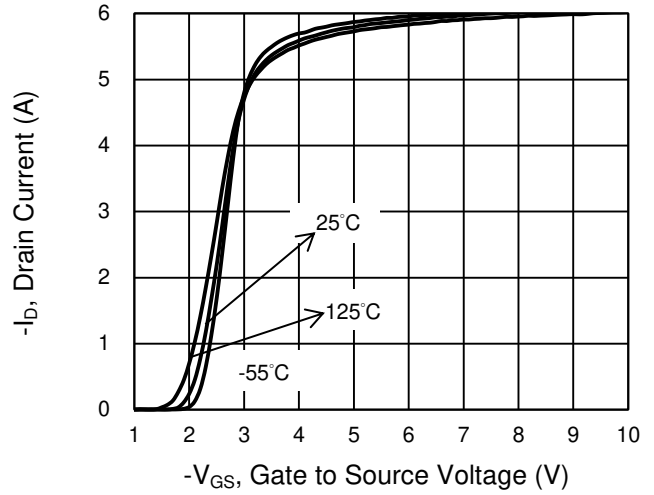
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

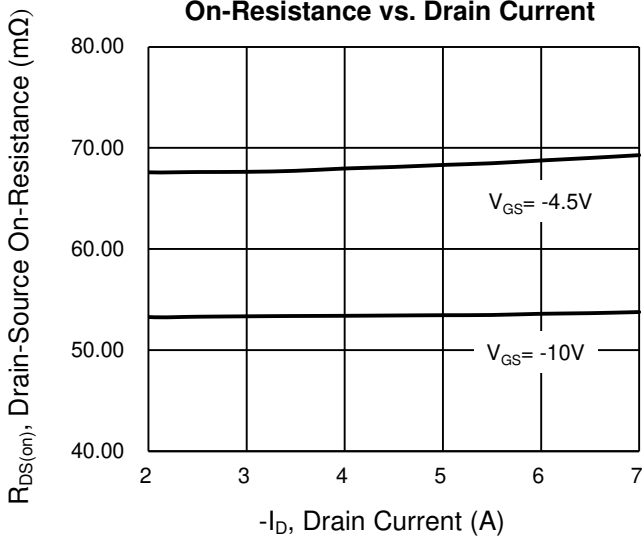
Output Characteristics



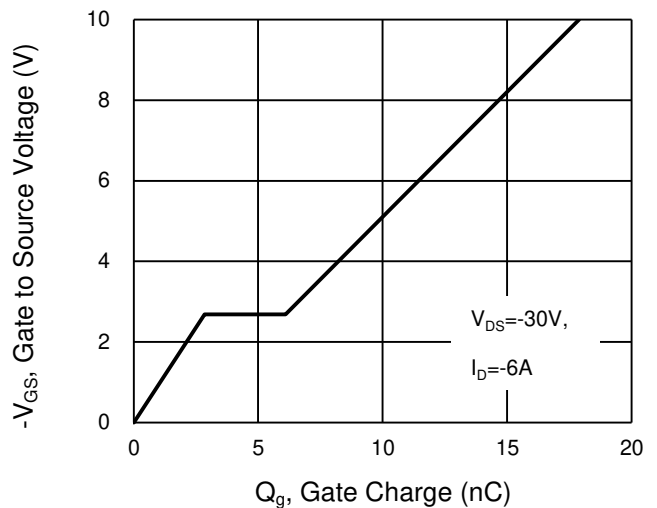
Transfer Characteristics



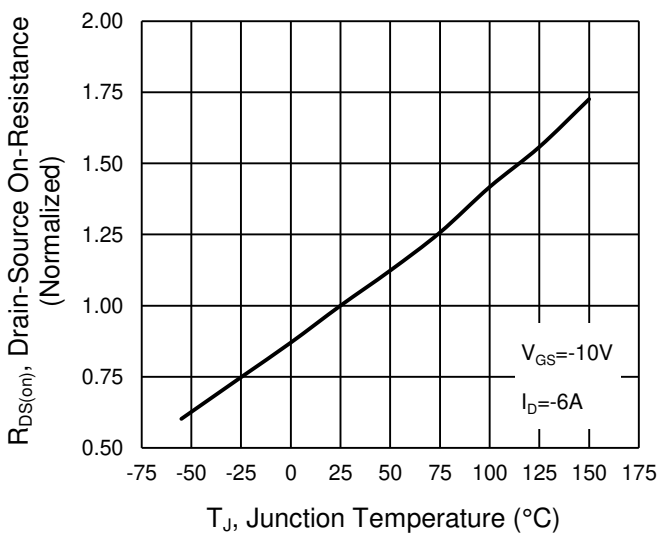
On-Resistance vs. Drain Current



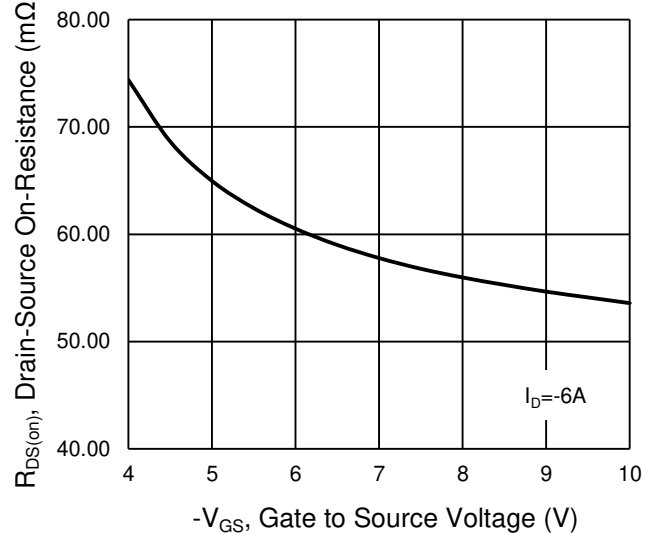
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



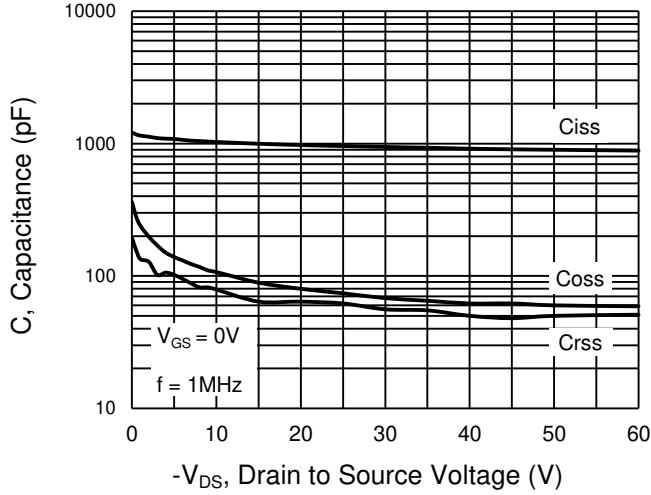
On-Resistance vs. Gate-Source Voltage



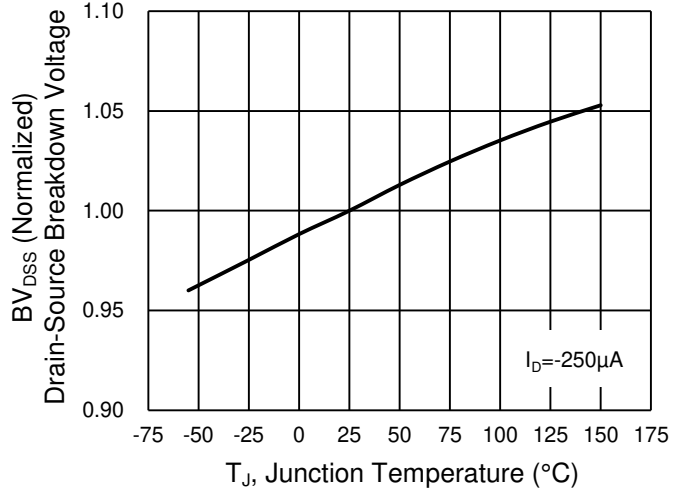
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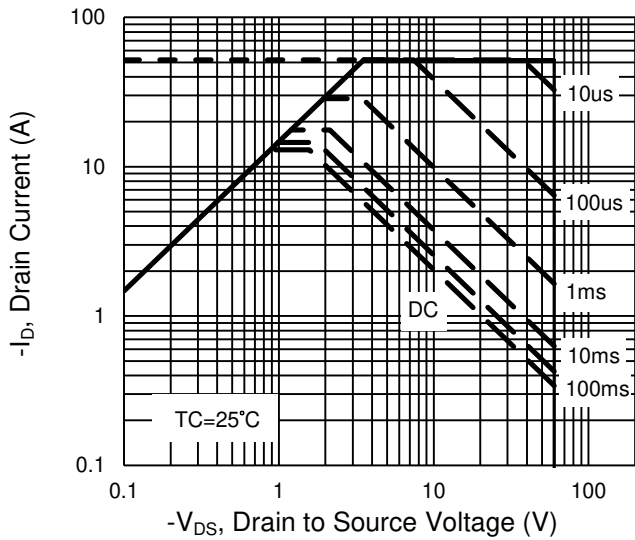
Capacitance vs. Drain-Source Voltage



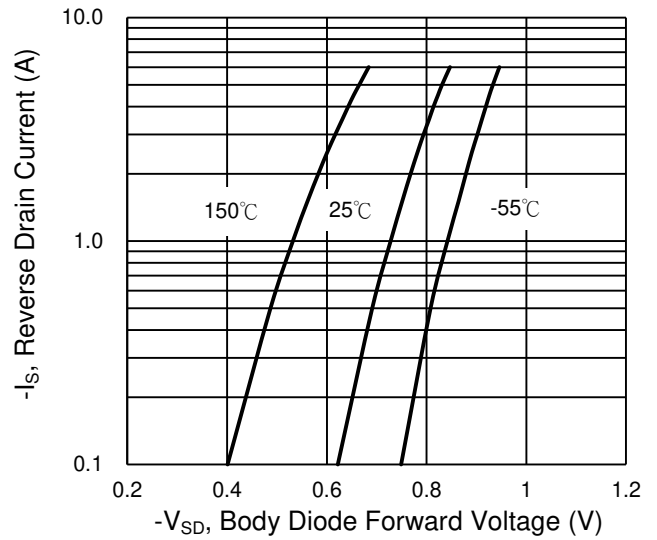
BV_{DSS} vs. Junction Temperature



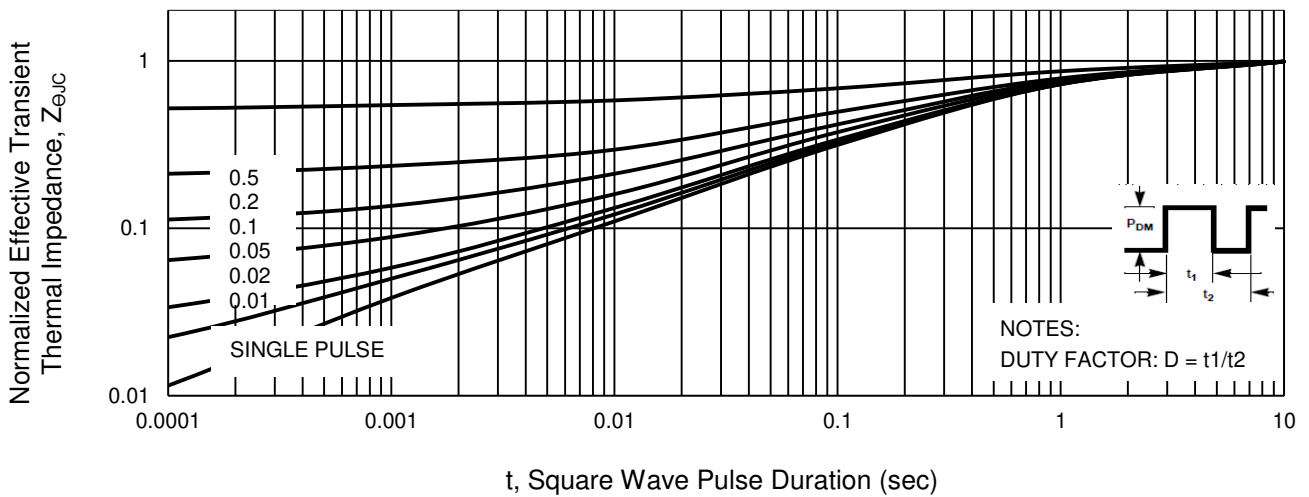
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

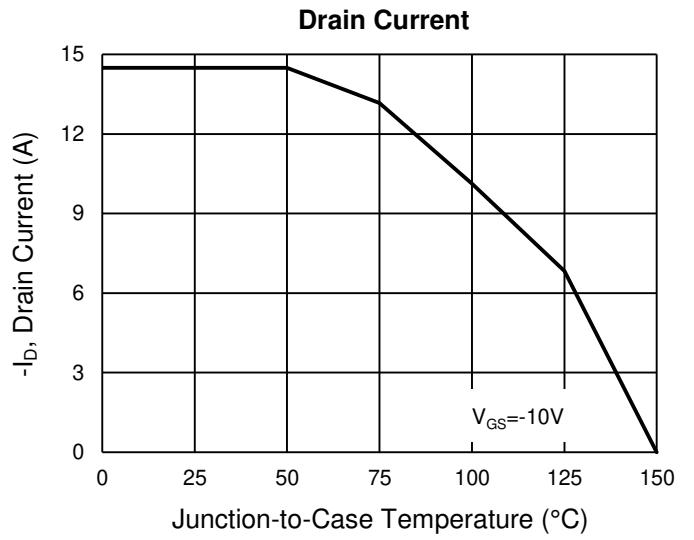
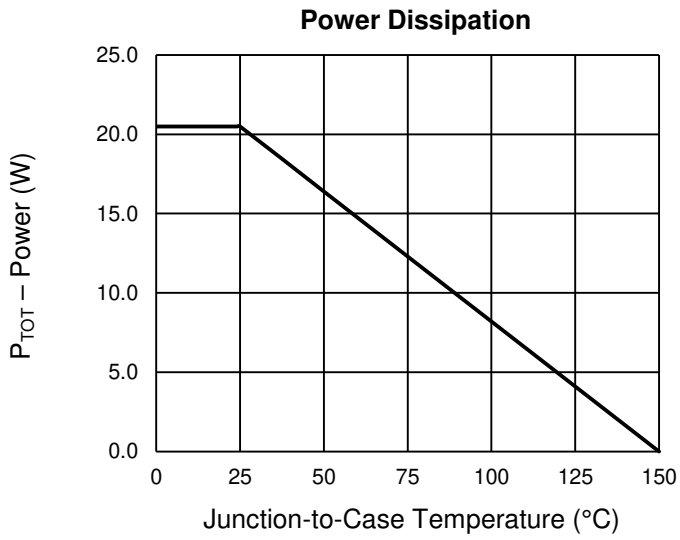


Normalized Thermal Transient Impedance, Junction-to-Case

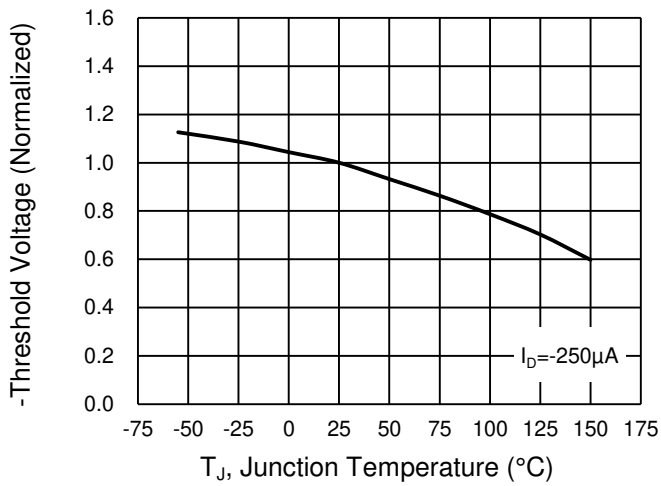


CHARACTERISTICS CURVES

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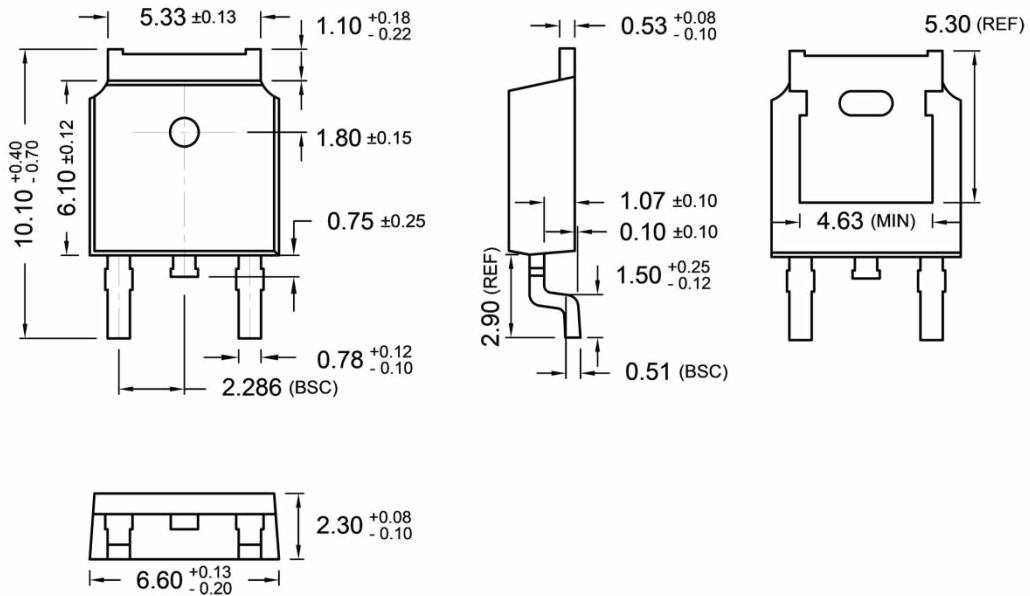


Normalized gate threshold voltage vs Temperature

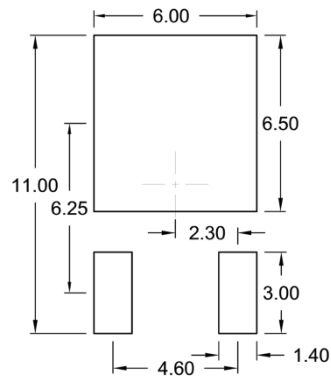


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-252 (DPAK)



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- Y** = Year Code
- M** = Month Code
- O** =Jan **P** =Feb **Q** =Mar **R** =Apr
- S** =May **T** =Jun **U** =Jul **V** =Aug
- W** =Sep **X** =Oct **Y** =Nov **Z** =Dec
- L** = Lot Code (1~9, A~Z)

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