ExpressLane PEX 8624-AA, AB, and BB 24-Lane/6-Port PCI Express Gen 2 Switch Data Book

Version 1.3

June 2012

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Revision History

Version	Date	Description of Changes
1.0	February, 2009	Production release, Silicon Revision BB. Support for pre-Production Silicon Revisions AA and AB is also included.
1.1	September, 2009	Production update, Silicon Revision BB. Applied miscellaneous corrections, changes, and enhancements throughout data book.
1.2	October, 2010	Production update, Silicon Revision BB. Added support for Industrial temperature. Updated PEX 8624 part ordering information. Applied miscellaneous corrections, changes, and enhancements throughout data book.
1.3	June, 2012	Production update, Silicon Revision BB. Corrected the JTAG IDCODE version number. Updated the thermal matrix table. Updated the ordering part number. Applied miscellaneous corrections, changes, and enhancements throughout data book.

Copyright Information

Document Number: 8624-AA/AB/BB-SIL-DB-P1-1.3

Preface

The information in this data book is subject to change without notice. This PLX data book to be updated periodically as new information is made available.

Audience

This data book provides functional details of PLX Technology's ExpressLane PEX 8624-AA, AB, and BB 24-Lane/6-Port PCI Express Gen 2 Switch, for hardware designers and software/firmware engineers. The information provided pertains to all Silicon Revisions (AA, AB, and BB), unless specified otherwise.

Supplemental Documentation

This data book assumes that the reader is familiar with the following documents:

- PLX Technology, Inc. (PLX), www.plxtech.com

  The PLX PEX 8624 Toolbox includes this data book and other supporting documentation, *such as* errata, and design and application notes.
- The Institute of Electrical and Electronics Engineers, Inc. (IEEE), www.ieee.org
  - *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Standard 1149.1-1994, Specifications for Vendor-Specific Extensions*
  - *IEEE Standard 1149.6-2003, IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions*
- NXP Semiconductors, ics.nxp.com
  - *The I2C-Bus Specification, Version 2.1*
- PCI Special Interest Group (PCI-SIG), www.pcisig.com
  - *PCI Local Bus Specification, Revision 3.0*
  - *PCI Bus Power Management Interface Specification, Revision 1.2*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.2*
  - *PCI Express Base Specification, Revision 1.1*
  - *PCI Express Base Specification, Revision 2.0*
  - *PCI Express Base Specification, Revision 2.0 Errata*
  - *PCI Express Card Electromechanical Specification, Revision 2.0*
  - *PCI Express Mini Card Electromechanical Specification, Revision 1.1*
  - *PCI Express Architecture PCI Express Jitter and BER White Paper, Revision 1.0*
- Personal Computer Memory Card International Association (PCMCIA), www.pcmcia.org
  - *ExpressCard Standard Release 1.0*
- PXI Systems Alliance (PXI), www.pxisa.org
  - *PXI-5 PXI Express Hardware Specification, Revision 1.0*

Note: *In this data book, shortened titles are associated with the previously listed documents. The following table lists these abbreviations.*

Abbreviation	Document
PCI r3.0	*PCI Local Bus Specification, Revision 3.0*
PCI Power Mgmt. r1.2	*PCI Bus Power Management Interface Specification, Revision 1.2*
PCI-to-PCI Bridge r1.2	*PCI to PCI Bridge Architecture Specification, Revision 1.2*
PCI Express Base r1.1	*PCI Express Base Specification, Revision 1.1*
PCI Express Base r2.0	*PCI Express Base Specification, Revision 2.0*
PCI ExpressCard CEM r2.0	*PCI Express Card Electromechanical Specification, Revision 2.0*
PCI ExpressCard Mini CEM r1.1	*PCI Express Mini Card Electromechanical Specification, Revision 1.1*
IEEE Standard 1149.1-1990	*IEEE Standard Test Access Port and Boundary-Scan Architecture*
IEEE Standard 1149.6-2003	*IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions*
I^2C Bus v2.1 *I2C Bus v2.1*[a]	*The I^2C-Bus Specification, Version 2.1*

a. Due to formatting limitations, the specification name may appear without the superscripted "2" in its title.

Terms and Abbreviations

The following table lists common terms and abbreviations used in this data book. Terms and abbreviations defined in the *PCI Express Base r2.0* are not included in this table.

Terms and Abbreviations	Definitions
8b/10b	Data-encoding scheme used on data transferred across a Link that is operating at either Gen 1 or Gen 2 Link speed (2.5 or 5.0 GT/s, respectively).
ACK	Acknowledge Control Packet. Control packet used by a destination to acknowledge data packet receipt. Signal that acknowledges signal receipt.
AMCAM	Address-mapping CAM that determines a memory Request route. Contains mirror copies of the PCI-to-PCI bridge **Memory Base** and **Memory Limit** registers in the PEX 8624.
ARI	Alternative Routing-ID Interpretation.
BAR	Base Address register.
BER	Bit error rate.
BusNoCAM	Bus Number-mapping CAM that determines the Completion route. Contains mirror copies of the PCI-to-PCI bridge **Secondary Bus Number** and **Subordinate Bus Number** registers in the PEX 8624.
CAM	Content-Addressable Memory.
CDR	Clock Data Recovery.
CRC	Cyclic Redundancy Check.
CSR	Configuration Space register.
DLL	Data Link Layer.
DMA	Direct Memory Access.
Downstream Station	Station that contains only downstream Ports.
ECC	Error-Correcting Code.
ECRC	End-to-end Cyclic Redundancy Check.
EIOS	Electrical Idle Ordered-Set.
EP	Endpoint.
Field	Multiple register bits that are combined for a single function.
FC	Flow Control.
GPIO	General-Purpose Input/Output.
GT/s	Giga-Transfers per second.
INCH	Ingress Credit Handler.
InitFC	Initialization Flow Control.
IOCAM	I/O-mapping CAM that determines an I/O Request route. Contains mirror copies of the PCI-to-PCI bridge **I/O Base** and **I/O Limit** registers in the PEX 8624.
JTAG	Joint Test Action Group.
Lane	Bidirectional pair of differential PCI Express I/O signals.
LCRC	Link Cyclic Redundancy Check.
Link Interface	Primary side of the NT Port, connects to external device pins. The secondary side of the NT Port is referred to as the *NT Port Virtual Interface*, and connects to the internal virtual PCI Express interface.

Terms and Abbreviations	Definitions
Local	Reference to PCI Express attributes (*such as* credits) that belong to the PCI Express Station.
LTSSM	Link Training and Status State Machine.
LUT	Lookup Table.
MRL	Manually operated Retention Latch.
NAK	Negative Acknowledge.
N_FTS	Number of Fast Training Sequences field in Training Sets.
NT	Non-Transparent. A bridging technique used in the PCI Express Switch to isolate Memory spaces by presenting the processor as an endpoint rather than another memory system. The PEX 8624 supports one NT Port.
PCI Express Station	Functional unit that provides the PCI Express conforming system interface. Includes the Serializer/De-Serializer (SerDes) hardware interface modules and PCI Express interface, which provides the Physical Layer (PHY), Data Link Layer (DLL), and Transaction Layer (TL) logic.
PEX	PCI Express.
PHY	Physical Layer.
PLL	Phase-Locked Loop.
PM	Power Management.
PME	Power Management Event.
Port	Interface to a group of SerDes and supporting logic that is capable of creating a Link, for communication with another Port.
P-P	PCI-to-PCI.
PRBS	Pseudo-Random Bit Sequence.
QoS	Quality of Service.
RAS	Reliability, Availability, and Serviceability.
RoHS	Restrictions on the use of certain Hazardous Substances (RoHS) Directive.
RR	Round-Robin scheduling.
Rx	Receiver.
SerDes	Serializer/De-Serializer. A high-speed differential-signaling parallel-to-serial and serial-to-parallel conversion logic attached to Lane pads.
SPI	Serial Peripheral Interface.
Sticky bits	Register bits in which the current values are unchanged by a Hot Reset, Link Down event, or Secondary Bus Reset, while the PEX 8624 is powered. Sticky bits are reset to default values by a Fundamental Reset. Applies to ROS, RW1CS, and RWS CSR types, and sometimes HwInit. (Refer to Table 12-5, “Register Types, Grouped by User Accessibility,” for CSR type definitions.)
TC	Traffic Class.
TCB	Training Control Bit field in Training Sets.

Terms and Abbreviations	Definitions
TL	Transaction Layer.
TLC	Transaction Layer Control. The module performing PCI Express Transaction Layer functions.
TLP	Transaction Layer Packet. PCI Express packet formation and organization.
Transparent	Refers to standard PCI Express upstream-to-downstream routing protocol.
TS1	Type 1 Training Sequence Ordered-Set.
TS2	Type 2 Training Sequence Ordered-Set.
Tx	Transceiver.
UI	Unit Interval – 400 ps at 2.5 GT/s, 200 ps at 5.0 GT/s.
Upstream Station	Contains the component's upstream Port. An upstream Station can also contain one or more downstream Ports.
UTP	User Test Pattern.
VC	Virtual Channel.
Vector	Address and data.
Virtual Interface	Secondary side of the NT Port, connects to the internal virtual PCI Express interface.
WRR	Weighted Round-Robin scheduling.

Data Book Notations and Conventions

Notation / Convention	Description
Blue text	Indicates that the text is hyperlinked to its description elsewhere in the data book. Left-click the blue text to learn more about the hyperlinked information. This format is often used for register names, register bit and field names, register offsets, chapter and section titles, figures, and tables.
PEX_XXXn[*x*] PEX_XXXp[*x*]	When the signal name appears in all CAPS, with the primary Port description listed first, field [*x*] indicates the number associated with the signal balls/ pads assigned to a specific SerDes module/Lane. The lowercase "n" (negative) or "p" (positive) suffix indicates the differential pair of signals, which are always used together.
# = Active-Low signals	Unless specified otherwise, Active-Low signals are identified by a "#" appended to the term (*for example*, PEX_PERST#).
`Program/code samples`	`Monospace font` (*`program or code samples`*) is used to identify code samples or programming references. These code samples are case-sensitive, unless specified otherwise.
`command_done`	Interrupt format.
Command/Status	Register names.
Parity Error Detected	Register parameter [bit or field] or control function.
Upper Base Address[31:16]	Specific Function in 32-bit register bounded by bits [31:16].
Number multipliers	k = 1,000 (10^3) is generally used with frequency response. K = 1,024 (2^{10}) is used for Memory size references. KB = 1,024 bytes. M = meg. = 1,000,000 when referring to frequency (decimal notation) = 1,048,576 when referring to Memory sizes (binary notation)
255d	d = Suffix that identifies decimal values.
1Fh	h = Suffix that identifies hex values. Each prefix term is equivalent to a 4-bit binary value (Nibble). Legal prefix terms are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F.
1010b	b = suffix which identifies binary notation (*for example*, 01b, 010b, 1010b, and so forth). Not used with single-digit values of 0 nor 1.
0 through 9	Decimal numbers, or single binary numbers.
byte	Eight bits – abbreviated to "B" (*for example*, 4B = 4 bytes).
LSB	Least-Significant Byte.
lsb	Least-significant bit.
MSB	Most-Significant Byte.
msb	Most-significant bit.
DWord	Double-Word (32 bits) is the primary register size in these devices.
QWord	Quad-Word (64 bits).
Reserved	Do not modify ***reserved*** bits and words. Unless specified otherwise, these bits read as 0 and must be written as 0.
word	16 bits.

Contents

Registers

Transparent Port Registers

NT Port Virtual Interface Registers – NT Mode Only

NT Port Link Interface Registers – NT Mode Only

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Chapter 1 Introduction

1.1 Overview

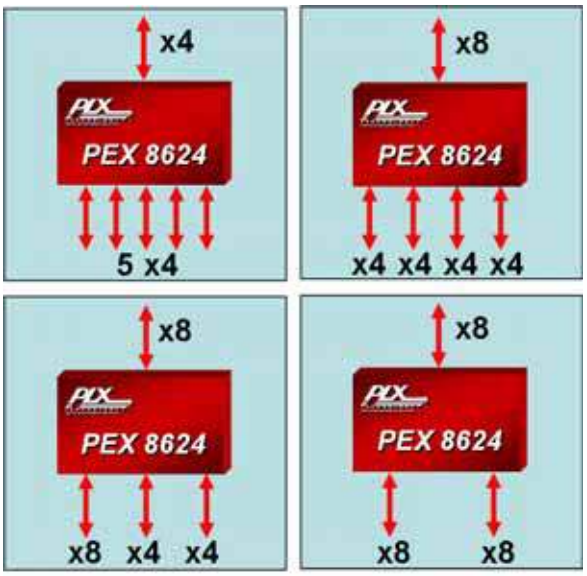
This data book describes PLX Technology's ExpressLane™ PEX 8624, a fully non-blocking, low-latency, low-cost, and low-power 24-Lane, 6-Port PCI Express Gen 2 switch. Conforming to the *PCI Express Base r2.0*, the PEX 8624 enables users to add high-bandwidth I/O to various products, including workstations, storage systems, communications platforms, embedded systems, and intelligent I/O modules. The PEX 8624's flexible hardware configuration and software programmability allows the switch to be tailored for a wide variety of application requirements.

The PEX 8624 is principally aimed at fan-in/out or aggregation applications; however, it is also well-suited for peer-to-peer communication traffic. The PEX 8624 supports multiple Port configuration options, to provide flexible solutions for optimal product design. *For example*, if using the PEX 8624 in a fan-out application (illustrated in Figure 1-1), configure the switch as:

- One x4 upstream Port and five x4 downstream Ports
- One x8 upstream Port and four x4 downstream Ports
- One x8 upstream Port, and one x8 and two x4 downstream Ports
- One x8 upstream Port and two x8 downstream Ports

or other combinations, up to the maximum number of Lanes (24) or Ports (6). The PEX 8624 can also support x1 and x2 Link widths, by auto-negotiating its Ports to the Link width of the PCI Express device with which it is interfacing.

Figure 1-1. Common Port Configurations



Note: *The six PEX 8624 Ports that connect to PCI Express Transmitters and Receivers are Ports 0, 1, 5, 6, 8, and 9, and each Port has its own set of registers. An additional set of Port 4 registers is visible to software, although the Port is not connected to external signals. The Port 4 registers include:*

- *Other Device-Specific registers.*
- *"Station" registers, that control all Ports in Station 1 (Ports 5 and 6), and are identical to the Port 0 registers that control all Ports in Station 0 (Ports 0 and 1) and Port 8 registers that control all Ports in Station 2 (Ports 8 and 9). The Station registers include Physical Layer registers, Device-Specific Error registers, and internal mapping (CAM) registers.*

1.2 Features

The PEX 8624 supports the following features:

- 6-Port PCI Express switch
  - 24 Lanes with integrated on-chip SerDes
  - Low-power SerDes (under 90 mW per Lane)
  - Fully Non-Blocking Switch architecture
  - Device-Specific Relaxed Ordering
  - Port configuration
    - 6 independent Ports
    - Choice of Link width (number of Lanes) per unique Link/Port – x4 or x8; Link widths of x1 and x2 are also supported
    - Configurable with serial EEPROM, I^2C, or Host software
    - Designate any Port as the *upstream Port* (Port 0 is recommended)
- High Performance
  - 240 GT/s aggregate bandwidth (5.0 GT/s/Lane x 24 SerDes x 2 (full duplex))
  - Integrated 5.0 GT/s SerDes speed negotiation, for each Port
  - Non-blocking Crossbar Switch interface supports TLP bandwidth capacity of each x8 Link
  - Full line rate on all Ports
  - Cut-Thru packet latency of less than 160 ns between symmetric (x8 to x8)
  - Maximum Payload Size – 2,048 bytes
- *performance*PAK™
  - Read Pacing™ (intelligent bandwidth allocation)
  - Dual Cast™
  - Dynamic Buffer Pool Architecture for faster credit updates
- *vision*PAK™
  - Performance Monitoring
    - Per-Port Payload and Header Counters
    - Per-traffic type (Write, Read, Completion) Counters
  - PCI Express Packet Generator
    - Capable of saturating a x8 Gen 2 Link
  - Error Injection and Pseudo-Random Bit Sequence (PRBS)
  - SerDes Loopback
  - SerDes Eye Capture
- Access Control Services (ACS) – Protection mechanisms for added data integrity in peer-to-peer transactions
- Alternative Routing-ID Interpretation (ARI) – Enables virtualized systems and/or highly integrated multi-function devices
- Quality of Service (QoS) support
  - All Ports support one, full-featured Virtual Channel (VC0)
  - All Ports support eight Traffic Class (TC[7:0]) mapping, independently of the other Ports
  - Round-Robin (RR) and Weighted Round-Robin (WRR) Port arbitration

- Non-Transparent Bridging
  - Program any one downstream Station 0 Port as the *Non-Transparent (NT) Port*
  - Enables Dual-Host, Dual-Fabric, Host-Failover applications
  - Moveable *upstream Port*
  - Cross-link Port capability
- Reliability, Availability, Serviceability (RAS) features
  - PCI Express Standard Hot Plug Controller for three Transparent downstream Ports, including optional usage models for Manually operated Retention Latch, by way of Manually operated Retention Latch (MRL) Sensor and Attention Button support
  - Serial Hot Plug, by way of I^2C, for Hot Plug capability on all Transparent downstream Ports
  - End-to-end Cyclic Redundancy Check (ECRC) and Poison bit support
  - Data path protection
  - Memory (RAM) error correction
  - Electromechanical Interlock supported with Power Enable output
  - Baseline and Advanced Error Reporting capability
  - Port (Link) Status bits and GPIO available
  - Per-Port error diagnostics
  - Joint Test Action Group (JTAG) AC/DC boundary scan
- INTA# (PEX_INTA#) and FATAL ERROR (FATAL_ERR#) (Conventional PCI SERR# equivalent) ball support
- 20 General-Purpose Input/Output (GPIO) balls, which can be used for Link Status LEDs, GPIO, and/or Interrupt inputs
- Port Status balls (PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]#)
- Other PCI Express Capabilities
  - Lane reversal
  - Polarity reversal
  - Conventional PCI-compatible Link Power Management states – L0, L0s, L1, L2/L3 Ready, and L3 (with Vaux ***not supported***)
  - Conventional PCI-compatible Device Power Management states – D0 and D3hot
  - Active State Power Management (ASPM)
  - Dynamic speed (2.5 or 5.0 GT/s) negotiation, for each Port
  - Dynamic Link width negotiation
- Out-of-Band Initialization options
  - Serial EEPROM
  - I^2C (7-bit Slave address with 100 Kbps)
- Testability – JTAG support for DC
- 19 x 19 mm^2, 324-ball Flip-Chip Ball Grid Array (FCBGA) package with Heat Spreader
- Typical power – 2.62W

- Compliant to the following specifications:
  - *PCI Local Bus Specification, Revision 3.0 (PCI r3.0)*
  - *PCI Bus Power Management Interface Specification, Revision 1.2 (PCI Power Mgmt. r1.2)*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.2 (PCI-to-PCI Bridge r1.2)*
  - *PCI Express Base Specification, Revision 1.1 (PCI Express Base r1.1)*
  - *PCI Express Base Specification, Revision 2.0 (PCI Express Base r2.0)*
  - *PCI Express Base Specification, Revision 2.0 Errata*
  - *PCI Express Card Electromechanical Specification, Revision 2.0 (PCI ExpressCard CEM r2.0)*
  - *PCI Express Mini Card Electromechanical Specification, Revision 1.1 (PCI ExpressCard Mini CEM r1.1)*
  - *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (IEEE Standard 1149.1-1990)*
  - *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Standard 1149.1-1994, Specifications for Vendor-Specific Extensions*
  - *IEEE Standard 1149.6-2003, IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions (IEEE Standard 1149.6-2003)*
  - *The I^2C-Bus Specification, Version 2.1 (I^2C Bus v2.1)*

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Chapter 2 Features and Applications

2.1 Flexible and Feature-Rich 24-Lane, 6-Port Switch

2.1.1 Highly Flexible Port Configurations

The PLX ExpressLane PEX 8624 PCI Express Gen 2 Switch offers highly configurable Ports. A maximum of 6 Ports (two per Station, three Stations total) can be configured to x1, x2, x4, or x8 Link widths, in any combination, to support specific bandwidth needs. The Ports can be symmetric (each Port has the same Link width) or asymmetric (the Ports have different Link widths). Any one Port can be designated as, or dynamically changed to be, the upstream Port (Port 0 is recommended).

The PEX 8624 supports a large number of Port configurations. *For example*, the PEX 8624 can be used in a fan-out application, with Link widths of x1, x2, x4, or x8, where any Port can be designated as the upstream Port and the remaining available Lanes are divided among five downstream Ports, of varying Link widths.

The PEX 8624 architecture allows for the combining of smaller Ports, to create larger Ports. *For example*, two x4 Ports can be combined to create a x8 Port. Furthermore, the PEX 8624 supports auto-negotiation, which allows the switch to train down to smaller Link widths (x4, x2, or x1). Link widths can be individually configured from each Port through auto-negotiation, hardware strapping, an optional serial EEPROM, and/or the I^2C Slave interface.

2.1.2 Non-Blocking Crossbar Switch Architecture

The Non-Blocking Crossbar Switch architecture is an on-chip interconnect switching fabric, which is built upon the existing PLX Switch Fabric Architecture technology. In addition to addressing simultaneous multiple flows, the Crossbar Switch architecture incorporates functions required to support an efficient PCI Express switch fabric, including:

- Deadlock avoidance
- Priority preemption
- PCI Express Ordering rules
- Packet fair queuing
- Oldest first scheduling

The Crossbar Switch interconnect physical topology is that of a packet-based Crossbar Switch fabric (internal fabric) designed to simultaneously connect multiple on-chip Stations. The Crossbar Switch protocol is sufficiently flexible and robust to support a variety of embedded system requirements. The protocol is specifically designed to ease chip integration, by strongly enforcing Station boundaries and standardizing communication between Stations. The Crossbar Switch architecture basic features include:

- Multiple concurrent Data transfers
- Global ordering within the PEX 8624
- Three types of transactions – Posted, Non-Posted, and Completion (P, NP, and Cpl, respectively) – meet PCI and PCI Express Ordering and Deadlock Avoidance rules
- Optional weighting of source Ports, to support Source Port arbitration

2.1.3 Low Packet Latency and High Performance

The PEX 8624 architecture supports packet Cut-Thru with a latency of less than 160 ns between symmetric (x8 to x8) ingress and egress Ports. This, combined with large Packet memory, support for larger packet payloads (programmable 128- to 2,048-byte Maximum Payload Size), and Non-Blocking Internal Switch architecture, allows high Transaction Layer Packet (TLP) throughput on each Link for performance-hungry applications, *such as* storage servers or storage switch fabrics.

2.1.3.1 Data Payloads

The Data Payloads are variable length with a maximum of 2,048 bytes, as defined by the *Maximum Payload Size* field (available sizes are 128, 256, 512, 1,024, and 2,048, depending upon the quantity of enabled Ports). Read Requests ***do not*** include a Data Payload.

Note: *Refer to the **Device Control** register Maximum Payload Size field (offset 70h[7:5]) for Maximum Payload Size Port limitations.*

2.1.3.2 Cut-Thru Mode

Cut-Thru mode can reduce latency, especially for longer packets, because the entire packet does not need to be stored before being forwarded. Instead, after the Header is decoded, the packet can be immediately forwarded. The PEX 8624 is designed to cut through TLPs, to and from every Port. By default, all Ports are enabled for Cut-Thru. Cut-Thru mode can be disabled for all Ports, by Clearing the **Debug Control** register *Cut-Thru Enable* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1DCh[21]).

Cut-Thru mode, if enabled, is supported for the PEX 8624's NT Port Link Interface, if the PEX 8624 is configured for NT mode.

Note: *The **Debug Control** register Cut-Thru Enable bit affects the entire switch. If Cut-Thru is enabled, all Ports use Cut-Thru. If Cut-Thru is **not** enabled, no Ports use Cut-Thru.*

Caution: ***One of the drawbacks to using Cut-Thru mode is that the TLP is not known to be good until the last byte. If the TLP proves to be bad, the Cut-Thru packet must be discarded. If the TLP has already been forwarded to another device, that TLP will be framed with an EDB (End Data Bad), as opposed to the standard END.***

2.1.4 Virtual Channel and Traffic Classes

The PEX 8624 supports one Virtual Channel (VC0) and eight Traffic Classes (TC[7:0]). VC0 and TC0 are required by the *PCI Express Base r2.0*, and configured at device start-up.

2.1.5 End-to-End Packet Integrity

To enable designs that require **guaranteed error-free packets**, the PEX 8624 provides **End-to-end Cyclic Redundancy Check** (ECRC) protection and **Poison** bit support, as well as **Error-Correcting Code** (ECC) protection on the internal data paths and memory (RAM). ECC maintains packet integrity through the PEX 8624, by providing automatic correction of any 1-bit errors. These features are optional in the *PCI Express Base r2.0*; however, PLX provides them across its entire ExpressLane PCI Express Gen 2 switch product line.

2.1.6 Configuration Flexibility

The PEX 8624 provides several ways to configure its operations. *For example*, the PEX 8624 can be configured through Strapping inputs, CPU Configuration Requests, an optional serial EEPROM, or the I^2C Slave interface. Additionally, the I^2C Slave interface allows for easy debug during the Development phase, performance monitoring during the Operation phase, and driver or software upgrade.

2.1.7 Interoperability

The PEX 8624 is designed to be fully compliant with the *PCI Express Base r2.0*, and is backward-compatible to the *PCI Express Base r1.1* and *PCI Express Base r1.0a*. Additionally, the switch supports **auto-negotiation**, **Lane reversal**, and **polarity reversal**, for maximum board design and board layout flexibility. Furthermore, the PEX 8624 is designed to be interoperable with many popular motherboards and server boards with PCI Express connections, and PCI Express endpoints (Ethernet, RAID Controllers), as well as PLX's family of PCI Express switches and bridges. All PLX ExpressLane devices undergo thorough interoperability testing at PLX's **Interoperability Lab** and compliance testing at the **PCI-SIG Compliance Workshop**, to ensure compatibility with PCI Express devices in the market.

2.1.8 Low Power with Granular SerDes Control

The PEX 8624 provides **low-power** capability that is fully compliant with the *PCI Express Base r2.0* and *PCI Power Mgmt. r1.2* Power Management (PM) specifications. Unused SerDes can be automatically powered down, to further reduce power consumption.

The PEX 8624 supports **SerDes output software control**, to allow power and signal strength optimization within a system. The PLX SerDes implementation supports four power levels – *Off*, *Low*, *Typical*, and *High*. The SerDes block also supports **Loopback modes** and **Advanced Error Reporting**, which enables efficient system debug and management.

2.1.9 Dynamic Lane Reversal

The PEX 8624 supports dynamic Lane reversal during the Link training process. Lane reversal capability allows flexibility in determining board routing, so that PCI Express components can be connected without having to crisscross wires. If the wiring of Lanes to a device is reversed (on both Transmitters and Receivers), only one of the two connected devices must support Lane reversal.

Either of the outside Lanes (Transmitter and Receiver pairs) of the PEX 8624 programmed Link width must be identified as being Lane 0. During Link training, both devices on the Link negotiate the Lane numbering. During the Link Training and Status State Machine (LTSSM)'s *Configuration* state, the upstream device sends TS1 Ordered-Sets, in which each connected Lane is identified by a consecutive Lane Number, starting with Lane 0 corresponding to the physical Lane Number of the Port.

The Port reverses its Lane Numbers and attempts to re-train when any of the following conditions occur:

- No Receiver is detected on preferred Lane 0
- No valid Training Sets are received on preferred Lane 0 during the LTSSM's *Polling* state
- TS1 with a non-zero Lane Number Port is received on the Port's Lane 0

To confirm successful Lane Number negotiation, both devices exchange TS2 Ordered-Sets with identical Lane Numbers on each connected Lane.

2.1.10 *performance*PAK

Exclusive to PLX, *performance*PAK is a suite of unique and innovative performance features that enable PLX's Gen 2 switches to be the highest-performing Gen 2 switches available in the market today. The *performance*PAK features consist of Read Pacing, Dual Cast, and Dynamic Buffer Pool.

2.1.10.1 Read Pacing

The Read Pacing feature allows users to throttle the number of Read Requests being made by downstream devices. When a downstream device requests several long Reads back-to-back, the Root Complex services the Read Requests from this downstream Port in a sequential order. If this Port has a narrow Link and is therefore slow in receiving these Read packets from the Root Complex, other downstream Ports may become starved, thus negatively impacting performance. This feature enhances performance by allowing for the adequate servicing of all downstream devices, by intelligent handling of Read Requests.

For further details, refer to Section 8.7, "Read Pacing."

2.1.10.2 Dual Cast

The Dual Cast feature allows for the copying of data (packets) from one ingress Port to two egress Ports, in a single transaction, allowing for higher performance in storage, security, and mirroring applications. The feature relieves the CPU from having to conduct two separate transactions, resulting in higher system performance.

For further details, refer to Section 8.8, "Using the Dual Cast Feature."

2.1.10.3 Dynamic Buffer Pool

The PEX 8624 uses a dynamic buffer pool for FC management, which uses a common pool of FC Credits that is shared among other Ports within a Station. This shared buffer pool is user-programmable, so FC credits can be allocated among the enabled Ports, as needed. Not only does this prevent wasted buffers and inappropriate buffer assignments, any un-allocated buffers remain in the common buffer pool, which can then be used by other Ports within the same Station, for faster FC credit updates.

For further details, refer to Section 8.4.2, "Dynamic Buffering."

2.1.11 *vision*PAK

Another PLX exclusive, *vision*PAK is a debug diagnostics suite of integrated hardware and software instruments that users can use to help bring their systems to market faster. *vision*PAK features consist of Performance Monitoring, Error Injection, SerDes Loopback, SerDes Eye Capture, and more.

2.1.11.1 Performance Monitoring

The PEX 8624's real-time performance monitoring allows users to literally "see" ingress and egress performance on each Port as traffic passes through the switch, using PLX's Software Development Kit (SDK). The monitoring is completely passive, and therefore, has no effect on overall system performance. Internal Counters provide extensive granularity down to traffic and packet type, and even allow for the filtering of traffic (*that is*, count only Memory Writes).

2.1.11.2 Error Injection

Using the PEX 8624's Error Injection feature, users can inject malformed packets and/or Fatal errors into their system, then evaluate the system's ability to detect and recover from such errors.

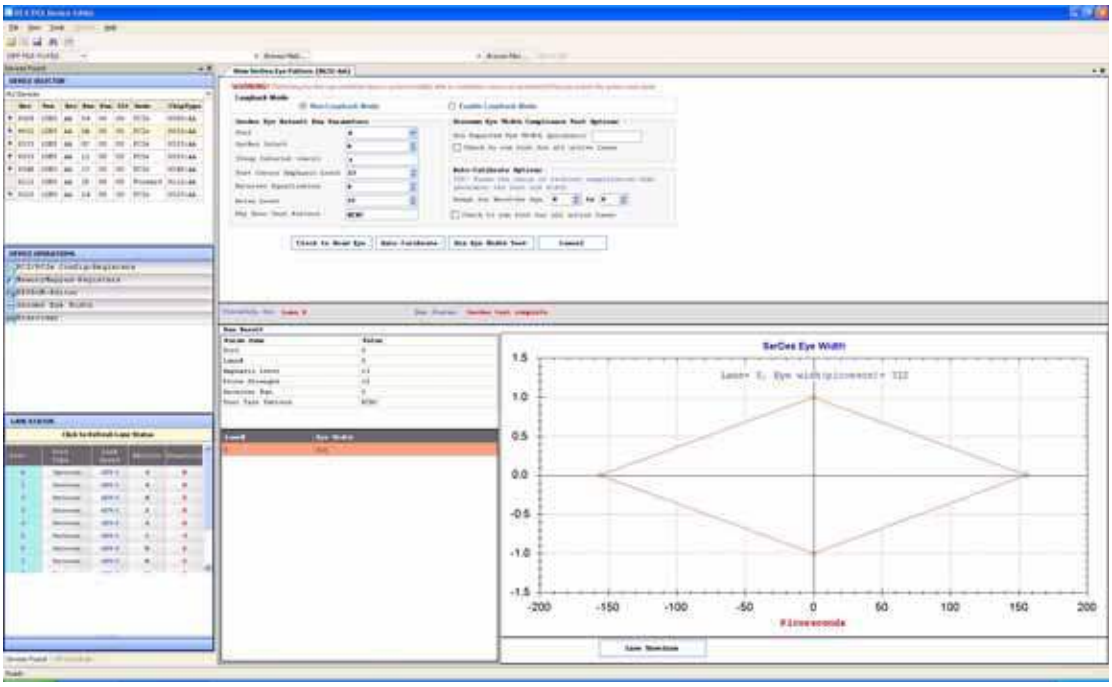
2.1.11.3 SerDes Loopback

The PEX 8624 supports External Tx, Recovered Clock, and Recovered Data Loopback modes.

2.1.11.4 SerDes Eye Capture

Users can evaluate their system's signal integrity at the Physical Layer (PHY), using the PEX 8624's SerDes Eye Capture feature. Using PLX's SDK, users can view the Receiver eye width of any Lane on the PEX 8624. Users can then modify SerDes Settings and see the impact on the Receiver eye. Figure 2-1 presents a screenshot of the SDK's SerDes Eye Capture feature.

Figure 2-1. PLX SDK SerDes Eye Capture Feature



2.1.12 Hot Plug for High Availability

Hot Plug capability allows users to replace hardware modules and perform maintenance, without having to power down the system. The PEX 8624 Hot Plug Capability and Advanced Error Reporting features make the switch suitable for High-Availability (HA) applications. The PEX 8624 automatically manages Hot Plug events on its Transparent downstream Ports/slots. Additionally, the upstream Port and NT Port Link Interface are fully compliant Hot Plug clients, and the PEX 8624 used on hot-pluggable adapter boards, docking Stations, and line cards.

Each PEX 8624 Transparent downstream Port includes a Hot Plug Controller. Each Station in the PEX 8624 includes one set of 10 Hot Plug signals that associated to any single Port within that Station (default association is to Ports 1, 5, and 9, except when a Station is configured as a single x8 Port, default association is to that single Port within the Station). If more than one Port per Station requires Hot Plug signals, the additional Ports can use an external I^2C I/O Expander (one 16-pin Maxim MAX7311, NXP PCA9555, or TI PCA9555 per slot (no serial EEPROM is required), –or–, if a programmed serial EEPROM is present, one 40-pin NXP PCA9698 per two slots), to provide the external signals (11 pins for Hot Plug, four pins for Slot ID, and one pin as General-Purpose Input/Output (GPIO)).

For further details, refer to Chapter 10, "Hot Plug Support."

2.1.13 Fully Compliant Power Management

The PEX 8624 supports Link (L0, L0s, L1, L2/L3 Ready, and L3) and Device (D0 and D3hot) PM states, in compliance with the *PCI Express Base r2.0* and *PCI Power Mgmt. r1.2* PM specifications.

For further details, refer to Chapter 11, "Power Management."

2.1.14 General-Purpose Input/Output Signals

The PEX 8624 contains 20 General-Purpose Input/Output (GPIO) balls and associated registers, that can be programmed to function as GPIO, Link Status (PORT_GOOD) indicators, and/or Interrupt inputs. Default functionality is GPIO input; however, serial EEPROM, I^2C, and/or software can program the GPIO registers to define functionality for each I/O. Default functionality can also be modified by the logical value of the STRAP_TESTMODE[3:0] inputs, sampled at Fundamental Reset. Because typical designs implement PORT_GOOD functionality for enabled Ports, GPIO[9, 8, 6, 5, 1, 0] are renamed as PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]# outputs.

For details, refer to the GPIO[19:12], GPIO[11, 10, 7, 4:2], PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]#, and STRAP_TESTMODE[3:0] signal descriptions in Section 3.4, "Signal Ball Descriptions."

2.1.15 PCI Express Switch Non-Transparent Bridging

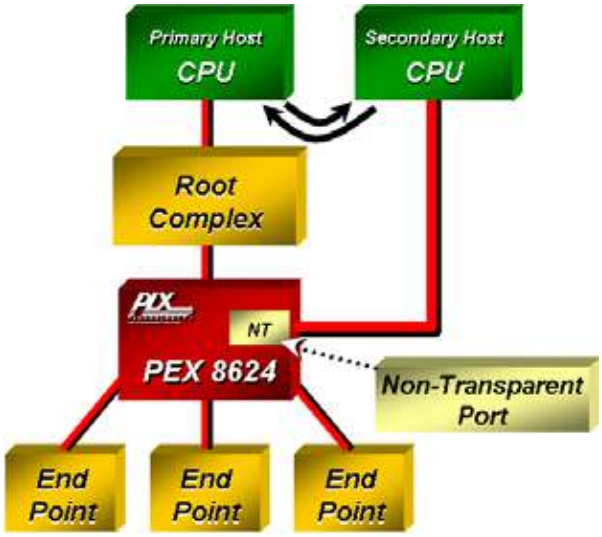
The PEX 8624 supports full Non-Transparent Bridging (NTB) functionality, to allow implementation of **multi-Host systems** and **intelligent I/O modules** in applications *such as* **storage**. To ensure prompt product migration, Non-Transparency features are implemented in the same way as Conventional PCI applications.

NT bridges allow systems to isolate Host memory domains, by presenting the processor subsystem as an endpoint, rather than another memory system:

- **Base Address** registers (BARs) are used to translate addresses
- **Doorbell** registers are used to signal interrupts between the address domains
- **Scratchpad** registers are accessible from both address domains, to allow inter-processor communication

Figure 2-2 illustrates use of the NT Port. For further details regarding NT mode, refer to Chapter 13, "Non-Transparent Bridging – NT Mode Only."

Figure 2-2. Non-Transparent Port



2.2 Applications

Suitable for **Host-centric** and **peer-to-peer traffic**, the PEX 8624 can be configured for a wide variety of form factors and applications.

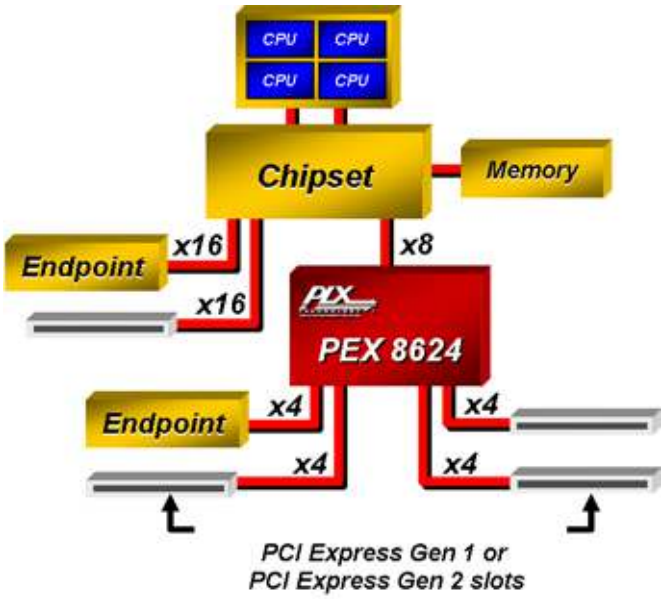
2.2.1 Host-Centric Fan-Out

The PEX 8624, with its symmetric or asymmetric Lane configuration capability, allows user-specific tuning to a variety of Host-centric applications.

Figure 2-3 illustrates a typical server fan-out design, where the Root Complex provides a PCI Express Link that needs to be expanded to a larger number of smaller Ports for a variety of I/O functions. In this example, the PEX 8624 has an 8-Lane upstream Port and four downstream Ports, using x4 Links. The downstream Ports can be of differing widths, if required.

The PEX 8624 is backward-compatible with PCI Express Gen 1 devices. Each PEX 8624 Port can independently negotiate the Link speed to 2.5 GT/s (Gen 1) or 5.0 GT/s (Gen 2), depending upon the other device's capabilities. Thus, the PEX 8624 can be used to create Gen 1 (2.5 GT/s) Ports, or to bridge Gen 1 devices to PCI Express Gen 2 systems (and vice versa). In Figure 2-3, the PCI Express slots connected to the PEX 8624's downstream Ports can be populated with either Gen 1 or Gen 2 devices. Conversely, the PEX 8624 can also be used to create Gen 2 Ports on a Gen 1 native chipset in the same manner.

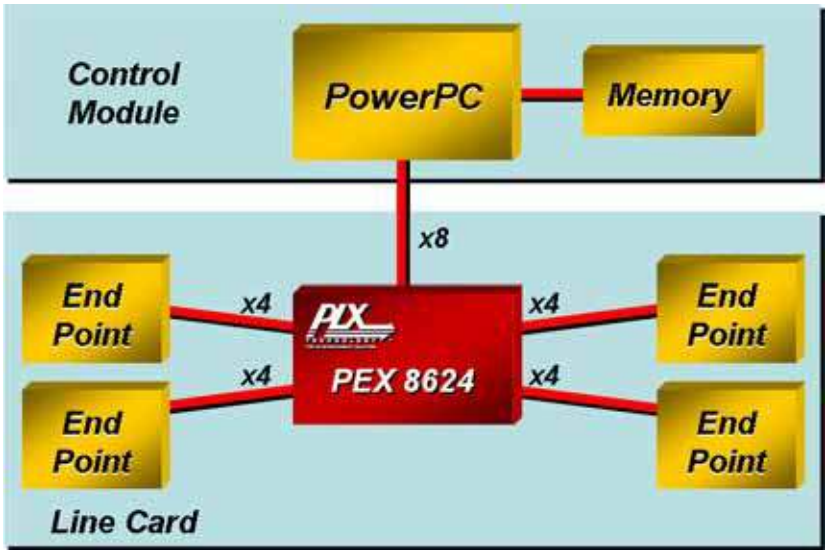
Figure 2-3. Fan-In/Fan-Out Usage



2.2.2 Communications Systems

The PEX 8624 can also be used in communications applications. Figure 2-4 illustrates a PEX 8624 being used in a router, to fan-out to multiple endpoints in a line card from a control module using PowerPC. The Link widths for each endpoint can be configured as required. The PEX 8624's peer-to-peer communication feature allows the endpoints to communicate with one another, without Host intervention or management.

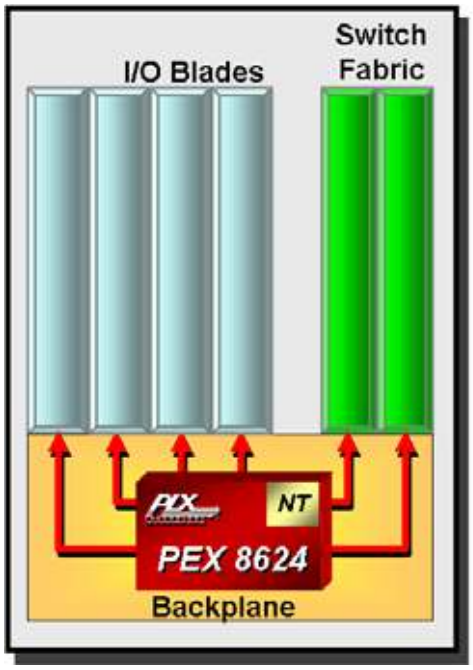
Figure 2-4. Communications Systems



2.2.3 Embedded Systems

The PEX 8624 is well-suited for embedded applications as well. Embedded applications, such as the example illustrated in Figure 2-5, commonly use a number of independent modules for functions *such as* control plane processing, data acquisition, or image processing. Figure 2-5 represents a bladed embedded system using a PEX 8624 for backplane connectivity between the CPU and I/O blades.

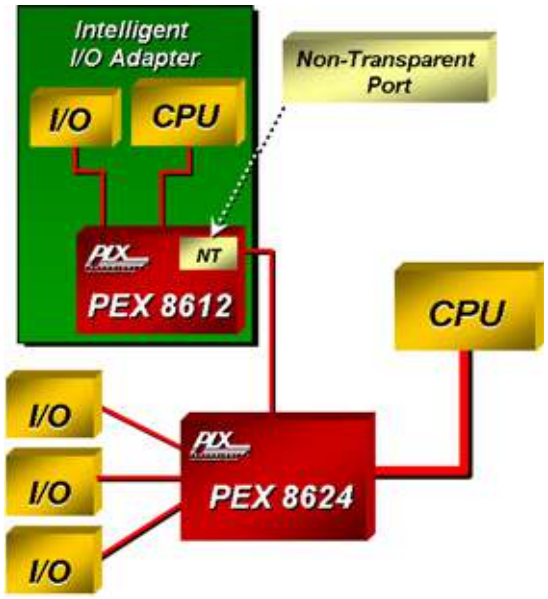
Figure 2-5. Embedded Systems – PCI Express Used in Bladed Systems for Backplane Connectivity between CPU and I/O Blades



2.2.4 Intelligent Adapter Board Usage

The PEX 8624 supports Non-Transparency Bridging (NTB). Figure 2-6 illustrates a Host system using an intelligent adapter board, where the adapter board CPU is isolated from the Host CPU. The PEX 8624 NT Port allows the two CPUs to be isolated, but communicate with one another through registers designed specifically for that purpose. The Host CPU can dynamically re-assign the upstream Port and NT Port, allowing system re-configuration.

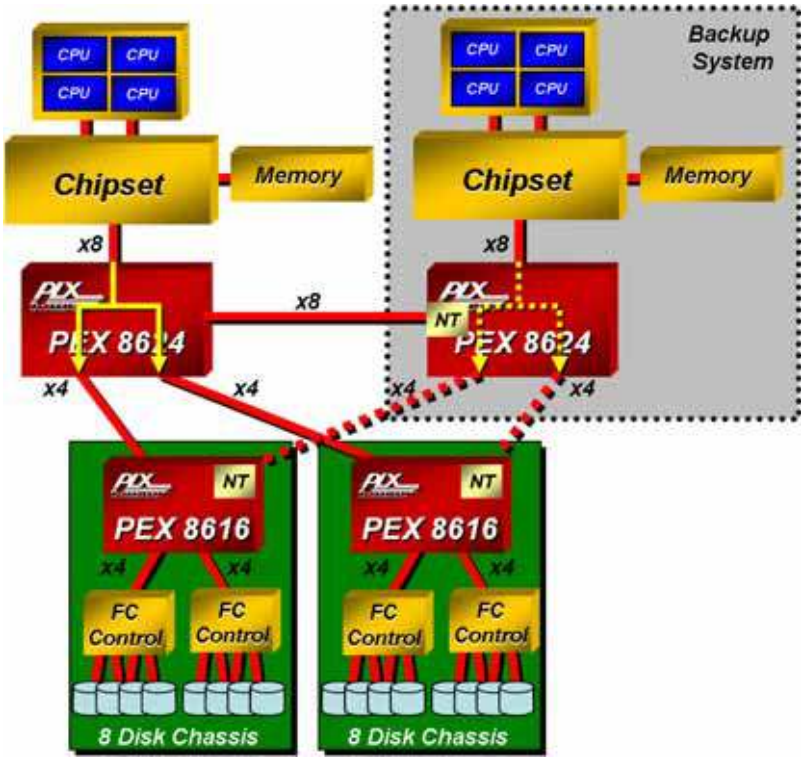
Figure 2-6. Intelligent Adapter Board Usage



2.2.5 Failover Storage Systems with Dual Cast

The PEX 8624's Dual Cast feature is useful in storage systems. In the example illustrated in Figure 2-7, Dual Cast enables the PEX 8624 to copy data coming from the Host to two downstream Ports (indicated in the figure as the yellow traffic patterns) in one transaction, as opposed to having to execute two separate transactions to send data to the redundant chassis. By offloading the task of backing up data onto the secondary system, processor and system performance is enhanced. The PEX 8624's NT Port is used to isolate the backup system from the primary system.

Figure 2-7. Failover Storage Systems



2.3 Software Usage Model

From the system model viewpoint, each PCI Express Port is a virtual PCI-to-PCI bridge, with its own set of PCI Express Configuration registers. The recommended upstream Port is Port 0; however, any Port can be configured as the upstream Port through optional configuration, by way of a serial EEPROM, the I^2C Slave interface, or Strapping inputs. The BIOS or Host can configure the other Ports, by way of the upstream Port, using Conventional PCI enumeration.

2.3.1 System Configuration

The virtual PCI-to-PCI bridges within the PEX 8624 are compliant to the PCI and PCI Express system models. The Configuration Space registers (CSRs) in a virtual primary/secondary PCI-to-PCI bridge are accessible by Type 0 or Type 1 Configuration Requests, through the virtual primary bus interface (matching Bus Number, Device Number, and Function Number).

2.3.2 Interrupt Sources and Events

The PEX 8624 supports the INT*x* Interrupt Message type (compatible with *PCI r3.0* Interrupt signals) or Message Signaled Interrupts (MSIs), when enabled. The PEX 8624 generates interrupts/Messages for the following:

- Hot Plug or Link State events
- PCI Express Hot Plug events
- Device-Specific errors and events
- GPIO-generated events
- NT Doorbell-generated events
- Baseline and Advanced Error Reporting

Internally generated interrupts and interrupts forwarded from downstream Ports are re-mapped and collapsed at the upstream Port.

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Chapter 3 Signal Ball Description

3.1 Introduction

This chapter provides descriptions of the 324 PEX 8624 signal balls. The signal name, type, location, and a brief description are provided for each signal ball. A map of the PEX 8624's physical layout is also provided.

3.2 Abbreviations

The following abbreviations are used in the signal tables provided in this chapter.

Table 3-1. Ball Assignment Abbreviations

Abbreviation	Description
#	Active-Low signal
A	Analog Input signal
APWR	Power (VDD10A) balls for SerDes Analog circuits
CMLCLKn[a]	Differential low-voltage, high-speed, CML negative Clock inputs
CMLCLKp[a]	Differential low-voltage, high-speed, CML positive Clock inputs
CMLRn	Differential low-voltage, high-speed, CML negative Receiver inputs
CMLRp	Differential low-voltage, high-speed, CML positive Receiver inputs
CMLTn	Differential low-voltage, high-speed, CML negative Transmitter outputs
CMLTp	Differential low-voltage, high-speed, CML positive Transmitter outputs
CPWR	1.0V Power (VDD10) balls for low-voltage Core circuits
GND	Common Ground (VSS) for all circuits
I	Input
I/O	Bidirectional (Input or Output)
I/OPWR	2.5V Power (VDD25) balls for Input and Output interfaces
O	Output
OD	Open Drain output
PD	Weak internal pull-down resistor
PLLPWR	2.5V Power (VDD25A) balls for Phase-Locked Loop (PLL) circuits
PU	Weak internal pull-up resistor
SerDes	Serializer/De-Serializer differential low-voltage, high-speed, I/O signal pairs (negative and positive)
STRAP	Input signals used for PEX 8624 configuration, operational mode Setting, and ***Factory Test***; these signals generally are not toggled at runtime

a. For REFCLK input, CML source is recommended; however, LVDS source is supported.

3.3 Internal Pull-Up/Pull-Down Resistors

The PEX 8624 contains I/O buffers that have weak internal pull-up or pull-down resistors, indicated in this chapter by PU or PD, respectively, in the signal ball tables (**Type** column). If a signal with this notation is used and no board trace is connected to the ball, the internal resistor is usually sufficient to keep the signal from toggling. However, if a signal with this notation is not used, but is connected to a board trace and is not used nor driven by an external source at all times, the internal resistors might not be sufficiently strong to hold the signal in the inactive state. In cases such as these, it is recommended that the signal be pulled or tied High to VDD25, or Low to Ground (VSS), as appropriate, through a 3KΩ to 10KΩ resistor.

Table 3-2 lists the internal pull-up and pull-down resistor values.

Table 3-2. Internal Resistor Values

Internal Resistor	Minimum	Typical	Maximum	Units
PU	74K	111K	178K	Ω
PD	62K	99K	179K	Ω

3.4 Signal Ball Descriptions

Note: *If there is more than one ball per signal name that includes a numbered range, the locations are listed in the same sequence in which the range is listed, starting at the top row, from left to right. For example, PEX_PERn11 is located at AC17, PEX_PERn10 is located at AC16, and so forth.*

If there is more than one ball per signal name that does not include a numbered range (such as VDD10), the locations are listed in ascending alphanumeric order.

The PEX 8624 signals are divided into the following groups:

- PCI Express Signals
- Parallel Hot Plug Signals for Ports C, B, and A
- Serial Hot Plug Signals
- Serial EEPROM Signals
- Strapping Signals
- JTAG Interface Signals
- I2C Slave Interface Signals
- Device-Specific Signals
- External Resistor Signals
- No Connect Signals
- Power and Ground Signals

3.4.1 PCI Express Signals

Table 3-3 defines the PCI Express SerDes and Control signals.

Table 3-3. PCI Express Signals – 99 Balls

Signal Name	Type	Location	Description
PEX_PERn[7:0]	CMLRn	R11, R10, R9, R8, R6, R5, R4, R3	**Negative Half of PCI Express Receiver Differential Signal Pairs for Station 0 (8 Balls)**
PEX_PERn[31:24]	CMLRn	D11, D10, D9, D8, D6, D5, D4, D3	**Negative Half of PCI Express Receiver Differential Signal Pairs for Station 1 (8 Balls)**
PEX_PERn[39:32]	CMLRn	E15, F15, G15, H15, K15, L15, M15, N15	**Negative Half of PCI Express Receiver Differential Signal Pairs for Station 2 (8 Balls)**
PEX_PERp[7:0]	CMLRp	P11, P10, P9, P8, P6, P5, P4, P3	**Positive Half of PCI Express Receiver Differential Signal Pairs for Station 0 (8 Balls)**
PEX_PERp[31:24]	CMLRp	E11, E10, E9, E8, E6, E5, E4, E3	**Positive Half of PCI Express Receiver Differential Signal Pairs for Station 1 (8 Balls)**
PEX_PERp[39:32]	CMLRp	E14, F14, G14, H14, K14, L14, M14, N14	**Positive Half of PCI Express Receiver Differential Signal Pairs for Station 2 (8 Balls)**
PEX_PERST#	I/O PU	M3	**PCI Express Reset** Used to cause a Fundamental Reset. (Refer to Chapter 5, "Reset and Initialization," for further details.)
PEX_PETn[7:0]	CMLTn	V11, V10, V9, V8, V6, V5, V4, V3	**Negative Half of PCI Express Transmitter Differential Signal Pairs for Station 0 (8 Balls)**
PEX_PETn[31:24]	CMLTn	A11, A10, A9, A8, A6, A5, A4, A3	**Negative Half of PCI Express Transmitter Differential Signal Pairs for Station 1 (8 Balls)**
PEX_PETn[39:32]	CMLTn	E18, F18, G18, H18, K18, L18, M18, N18	**Negative Half of PCI Express Transmitter Differential Signal Pairs for Station 2 (8 Balls)**
PEX_PETp[7:0]	CMLTp	U11, U10, U9, U8, U6, U5, U4, U3	**Positive Half of PCI Express Transmitter Differential Signal Pairs for Station 0 (8 Balls)**
PEX_PETp[31:24]	CMLTp	B11, B10, B9, B8, B6, B5, B4, B3	**Positive Half of PCI Express Transmitter Differential Signal Pairs for Station 1 (8 Balls)**
PEX_PETp[39:32]	CMLTp	E17, F17, G17, H17, K17, L17, M17, N17	**Positive Half of PCI Express Transmitter Differential Signal Pairs for Station 2 (8 Balls)**

Table 3-3. PCI Express Signals – 99 Balls *(Cont.)*

Signal Name	Type	Location	Description
PEX_REFCLKn	CMLCLKn	V7	**Negative Half of 100-MHz PCI Express Reference Clock Input Signal Pair** PEX_REFCLKn must be AC-coupled. Use a 0.01 to 0.1 µF capacitor.
PEX_REFCLKp	CMLCLKp	U7	**Positive Half of 100-MHz PCI Express Reference Clock Input Signal Pair** PEX_REFCLKp must be AC-coupled. Use a 0.01 to 0.1 µF capacitor.

3.4.2 Hot Plug Signals

The PEX 8624 includes signals for both Parallel and Serial Hot Plug support.

Parallel Hot Plug can be implemented on one Port per Station, as selected by the *HP Parallel Port* field in each Station (Port 0, 4, or 8, offset 1E0h[14:13]).

Serial Hot Plug can be implemented on any Transparent downstream Port that is not designated as a Parallel Hot Plug Port by the Station's *HP Parallel Port* field.

Hot Plug signals are enabled, configured, and accessed through the **Slot Capability** and **Slot Status and Control** registers (offsets 7Ch and 80h, respectively), in each Port. Also, each Port's **Power Management Hot Plug User Configuration** register (offset 1E0h) provides additional Device-Specific configuration and control, for both Parallel and Serial Hot Plug implementations.

Both signal types are discussed in the sections that follow.

3.4.2.1 Parallel Hot Plug Signals

The PEX 8624 includes 10 signal balls, per Station, that support the Parallel Hot Plug Controller (HP_), as defined in Table 3-4. These signals are active only for Hot Plug-capable Transparent downstream Ports configured at start-up.

For further details regarding Hot Plug, refer to Chapter 10, "Hot Plug Support."

Notes: *All Parallel Hot Plug signals are I/O; however, their logical operation is either input or output, as described for each signal.*

All Parallel Hot Plug signals are duplicated for each Hot Plug-capable Port, as A, B, and C signals, which map to one Port in each Station (Stations 0, 1, and 2, respectively), as designated in the HP Parallel Port field of each Station (Port 0, 4, or 8, offset 1E0h[14:13]).

Table 3-4. Parallel Hot Plug Signals[a] for Ports C, B, and A – 30 Balls

Signal Name	Type	Location	Description
HP_ATNLED_[C, B, A]#	I/O PU	A13, K2, U16	**Hot Plug Attention LED Outputs (3 Balls)** Active-Low Slot Control Logic output that is used to drive the Attention Indicator. Output is asserted Low to turn On (illuminate) the LED. Enabled when the **Slot Capability** register *Attention Indicator Present* bit (offset 7Ch[3]) is Set and controlled by the **Slot Control** register *Attention Indicator Control* field (offset 80h[7:6]). When software writes to the *Attention Indicator Control* field, a Command Completed interrupt can be generated to notify the Host that the command has been executed. When the following conditions exist: • **Slot Capability** register *Attention Indicator Present* bit (offset 7Ch[3]) is Set, and • **Slot Control** register *Command Completed Interrupt Enable* bit is not masked (offset 80h[4], is Set), and • **Slot Control** register *Hot Plug Interrupt Enable* bit (offset 80h[5]) is Set, an interrupt (MSI, INT*x* Message, or PEX_INTA# output, all mutually exclusive, on a per-Port basis) can be generated to the Host. **If HP_ATNLED_*x*# are used, each requires an external current-limiting resistor.** ***Note:*** *Although this is an I/O signal, its logical operation is output.*

Table 3-4. Parallel Hot Plug Signals[a] for Ports C, B, and A – 30 Balls *(Cont.)*

Signal Name	Type	Location	Description
HP_BUTTON_[C, B, A]#	I/O PU	A14, M1, U17	**Hot Plug Attention Button Inputs (3 Balls)** Active-Low Slot Control Logic input that is connected directly to the Attention Button, with input assertion status latched in the **Slot Status** register *Attention Button Pressed* bit (offset 80h[16]). Enabled when the **Slot Capability** register *Attention Button Present* bit (offset 7Ch[0]) is Set. When the following conditions exist: • HP_BUTTON_*x*# are not masked (**Slot Control** register *Attention Button Pressed Enable* bit, offset 80h[0], is Set), and • **Slot Capability** register *Hot Plug Capable* bit (offset 7Ch[6]) is Set, and • **Slot Control** register *Hot Plug Interrupt Enable* bit (offset 80h[5]) is Set, an interrupt (MSI, INT*x* Message, or PEX_INTA# output, all mutually exclusive, on a per-Port basis) can be generated, to notify the Host of intended board insertion or removal. ***Notes:*** *HP_BUTTON_x# is internally de-bounced, but must remain stable for at least 10 ms.* *Although this is an I/O signal, its logical operation is input.*
HP_CLKEN_[C, B, A]#	I/O PU	A18, R1, V15	**Hot Plug Reference Clock Enable Outputs (3 Balls)** Active-Low Slot Control Logic output that, when enabled, controls the connection of the external REFCLK to the slot. Enabled when the **Slot Capability** register *Power Controller Present* bit (offset 7Ch[1]) is Set, and controlled by the **Slot Control** register *Power Controller Control* bit (offset 80h[10]). The time delay from HP_PWREN_*x* output assertion to HP_CLKEN_*x*# output assertion is programmable (through serial EEPROM load) from 128 to 512 ms, in the *HPC Tpepv* field (offset 1E0h[4:3]). When the register field is programmed to 00b (default), HP_PWR_GOOD_*x* input assertion controls the time delay from HP_PWREN_*x* output assertion to HP_CLKEN_*x*# output assertion. ***Note:*** *Although this is an I/O signal, its logical operation is output.*

Table 3-4. Parallel Hot Plug Signals[a] for Ports C, B, and A – 30 Balls *(Cont.)*

Signal Name	Type	Location	Description
HP_MRL_[C, A]#	I/O PU	D13, R15	**Hot Plug Manually Operated Retention Latch Sensor Inputs (2 Balls)** Active-Low Slot Control Logic input that is connected directly to an optional Manually operated Retention Latch (MRL) Sensor that is logic Low when the latch is closed. Enabled when the **Slot Capability** register *MRL Sensor Present* bit (offset 7Ch[2]) is Set. When enabled, HP_MRL_[C, A]# input assertion enables Hot Plug output sequencing to turn On the slot's power (HP_PWREN_[C, A] and HP_PWRLED_[C, A]#) and clock (HP_CLKEN_[C, A]#), and de-assert Reset (HP_PERST_[C, A]#) after reset, as illustrated in Figure 10-2, "Hot Plug Outputs When Power Controller Present and Power Controller Control Bits Are Cleared," or under software control. A change in the HP_MRL_[C, A]# signal state is latched in the **Slot Status** register *MRL Sensor Changed* bit (offset 80h[18]), and the state change can assert an interrupt to notify the Host of a change in the MRL Sensor state. When the following conditions exist: • HP_MRL_[C, A]# are not masked (**Slot Control** register *MRL Sensor Changed Enable* bit, offset 80h[2], is Set), and • **Slot Control** register *Hot Plug Interrupt Enable* bit (offset 80h[5]) is Set, an interrupt (MSI, INT*x* Message, or PEX_INTA# output, all mutually exclusive, on a per-Port basis) can be generated. If the associated Hot Plug-capable Transparent downstream Port connects to a PCI Express board slot that does not implement an MRL Sensor, HP_MRL_[C, A]# is typically connected to HP_PRSNT_[C, A]# and a pull-up resistor, with the common node connected to the PRSNT2# signal(s) at the slot. If the associated Hot Plug-capable Transparent downstream Port instead connects directly to a device, and Hot Plug signals (*such as* HP_PERST_*x*#) are used, pull HP_MRL_[C, A]# Low to enable the automatic Hot Plug output sequencing following switch Reset (PEX_PERST# or Hot Reset) de-assertion. Otherwise, if Hot Plug signals are not used, pull HP_MRL_[C, A]# High, to hold the Hot Plug outputs in their inactive states. When HP_MRL_HP_MRL_[C, A]# is enabled and the input is sampled High on a powered slot, REFCLK to the slot is automatically disconnected and the slot power is automatically turned Off, as illustrated in Figure 10-3, "Hot Plug Automatic Power-Down Sequence." ***Notes:*** *HP_MRL_[C, A]# is internally de-bounced, but must remain stable for at least 10 ms. HP_MRL_[C, A]#, if enabled, is not de-bounced when sampled immediately after reset.* *Although this is an I/O signal, its logical operation is input.*

Table 3-4. Parallel Hot Plug Signals[a] for Ports C, B, and A – 30 Balls *(Cont.)*

Signal Name	Type	Location	Description
HP_MRL_B#	I	L2	**Hot Plug Manually Operated Retention Latch Sensor Input** Active-Low Slot Control Logic input that is connected directly to an optional MRL Sensor that is logic Low when the latch is closed. Enabled when the **Slot Capability** register *MRL Sensor Present* bit (offset 7Ch[2]) is Set. When enabled, HP_MRL_B# input assertion enables Hot Plug output sequencing to turn On the slot's power (HP_PWREN_B and HP_PWRLED_B#) and clock (HP_CLKEN_B#), and de-assert Reset (HP_PERST_B#) after reset, as illustrated in Figure 10-2, "Hot Plug Outputs When Power Controller Present and Power Controller Control Bits Are Cleared," or under software control. A change in the HP_MRL_B# signal state is latched in the **Slot Status** register *MRL Sensor Changed* bit (offset 80h[18]), and the state change can assert an interrupt to notify the Host of a change in the MRL Sensor state. When the following conditions exist: • HP_MRL_B# is not masked (**Slot Control** register *MRL Sensor Changed Enable* bit, offset 80h[2], is Set), and • **Slot Control** register *Hot Plug Interrupt Enable* bit (offset 80h[5]) is Set, an interrupt (MSI, INT*x* Message, or PEX_INTA# output, all mutually exclusive, on a per-Port basis) can be generated. If the associated Hot Plug-capable Transparent downstream Port connects to a PCI Express board slot that does not implement an MRL Sensor, HP_MRL_B# is typically connected to HP_PRSNT_B# and a pull-up resistor, with the common node connected to the PRSNT2# signal(s) at the slot. If the associated Hot Plug-capable Transparent downstream Port instead connects directly to a device, and Hot Plug signals (*such as* HP_PERST_*x*#) are used, pull HP_MRL_B# Low to enable the automatic Hot Plug output sequencing following switch Reset (PEX_PERST# or Hot Reset) de-assertion. Otherwise, if Hot Plug signals are not used, pull HP_MRL_B# High, to hold the Hot Plug outputs in their inactive states. When HP_MRL_HP_MRL_B# is enabled and the input is sampled High on a powered slot, REFCLK to the slot is automatically disconnected and the slot power is automatically turned Off, as illustrated in Figure 10-3, "Hot Plug Automatic Power-Down Sequence." **HP_MRL_B# requires an external resistor, as follows:** • **If Station 1 Parallel Hot Plug is not used, but HP_PERST_B# output is used (to reset a downstream device), connect HP_MRL_B# to an external pull-down resistor** • **Otherwise, connect HP_MRL_B# to an external pull-up resistor** ***Notes:*** *HP_MRL_B# is internally de-bounced, but must remain stable for at least 10 ms. HP_MRL_B#, if enabled, is not de-bounced when sampled immediately after reset.* *Although this is an I/O signal, its logical operation is input.*

Table 3-4. Parallel Hot Plug Signals[a] for Ports C, B, and A – 30 Balls *(Cont.)*

Signal Name	Type	Location	Description
HP_PERST_[C, B, A]#	I/O PU	B13, N1, V16	**Hot Plug Reset Outputs (3 Balls)** Active-Low Slot Control Logic output that is used to reset the slot. When the **Slot Capability** register *Power Controller Present* bit (offset 7Ch[1]) is Set, the HP_PERST_*x*# output state can be controlled by software, using the **Slot Control** register *Power Controller Control* bit (offset 80h[10]). ***Note:*** *Although this is an I/O signal, its logical operation is output.*
HP_PRSNT_[C, B, A]#	I/O PU	A16, M2, V18	**Hot Plug PRSNT2# Inputs (3 Balls)** Active-Low Slot Control Logic input that connects to the slot's PRSNT2# signal, which on the add-in board connects to the slot's PRSNT1# signal, which is typically grounded on the motherboard. A change in the HP_PRSNT_*x*# input state is latched in the **Slot Status** register *Presence Detect Changed* bit (offset 80h[19]), and the state change can assert an interrupt to notify the Host of board presence or absence. When the following conditions exist: • HP_PRSNT_*x*# are not masked (**Slot Control** register *Presence Detect Changed Enable* bit (offset 80h[3], is Set), and • **Slot Control** register *Hot Plug Interrupt Enable* bit (offset 80h[5]) is Set, an interrupt (MSI, INT*x* Message, or PEX_INTA# output, all mutually exclusive, on a per-Port basis) can be generated. ***Notes:*** *HP_PRSNT_x# is internally de-bounced, but must remain stable for at least 10 ms.* *Although this is an I/O signal, its logical operation is input.*

Table 3-4. Parallel Hot Plug Signals[a] for Ports C, B, and A – 30 Balls *(Cont.)*

Signal Name	Type	Location	Description
HP_PWREN_[C, B, A]	I/O PU	B14, M4, U15	**Hot Plug Power Enable Outputs (3 Balls)** Active-High Slot Control Logic output that controls the slot power state. When this output is High, power is enabled to the slot. Enabled when the **Slot Capability** register *Power Controller Present* bit (offset 7Ch[1]) is Set. When software turns the slot's Power Controller On or Off (**Slot Control** register *Power Controller Control* bit, offset 80h[10]), a Command Completed interrupt can be generated to notify the Host that the command has been executed. When the following conditions exist: • **Slot Control** register *Command Completed Interrupt Enable* bit is not masked (offset 80h[4], is Set), and • **Slot Control** register *Hot Plug Interrupt Enable* bit (offset 80h[5]) is Set, an interrupt (MSI, INT*x* Message, or PEX_INTA# output, all mutually exclusive, on a per-Port basis) can be generated to the Host. When HP_MRL_*x*# is enabled (**Slot Capability** register *MRL Sensor Present* bit, offset 7Ch[2], is Set), HP_MRL_*x*# input assertion enables Hot Plug output sequencing to turn On the slot's power, by asserting HP_PWREN_*x* after reset, as illustrated in Figure 10-2, "Hot Plug Outputs When Power Controller Present and Power Controller Control Bits Are Cleared," or under software control. ***Notes:*** *HP_PWREN_x polarity is inverted with respect to HP_PWRENx# functionality in PLX ExpressLane Gen 1 switches.* *Although this is an I/O signal, its logical operation is output.*
HP_PWRFLT_[C, B, A]#	I/O PU	C14, M5, V17	**Hot Plug Power Fault Inputs (3 Balls)** Active-Low Slot Control Logic input that, when asserted Low, indicates that the slot's external Power Controller detected a power fault on one or more supply rails. Enabled when the **Slot Capability** register *Power Controller Present* bit (offset 7Ch[1]) is Set, and input assertion status is latched in the **Slot Status** register *Power Fault Detected* bit (offset 80h[17]). When the following conditions exist: • HP_PWRFLT_*x*# are not masked (**Slot Control** register *Power Fault Detector Enable* bit, offset 80h[1], is Set), and • **Slot Control** register *Hot Plug Interrupt Enable* bit (offset 80h[5]) is Set, an interrupt (MSI, INT*x* Message, or PEX_INTA# output, all mutually exclusive, on a per-Port basis) can be generated, to notify the Host of a power fault. ***Notes:*** *If HP_PWREN_x and HP_CLKEN_x# are not used, HP_PWRFLT_x# can be used as a general-purpose input with status reflected in the Port's **Slot Status** register Power Fault Detected bit (offset 80h[17]), provided that the Port's **Slot Capability** register Power Controller Present bit (offset 7Ch[1]) is Set.* *Although this is an I/O signal, its logical operation is input.*

Table 3-4. Parallel Hot Plug Signals[a] for Ports C, B, and A – 30 Balls *(Cont.)*

Signal Name	Type	Location	Description
HP_PWR_GOOD_[C, B, A]	I PD	C16, K4, R14	**Hot Plug Power Good Inputs (3 Balls)** Active-High (default) input that when enabled (default), causes the Slot Control Logic to delay HP_CLKEN_*x*# output assertion to turn On REFCLK to the slot, until HP_PWR_GOOD_*x* input is asserted to indicate that the installed module's power supplies are active and stable. Signal polarity can be changed to Active-Low, by programming the serial EEPROM to Set the Port's *HP_PWR_GOOD_x Active-Low Enable* bit (offset 1E0h[6]). Polarity must not be changed by I^2C, because that is too slow for initialization. HP_PWR_GOOD_*x* is disabled when the Port's *HPC Tpepv* field (offset 1E0h[4:3]) is programmed to a value other than 00b, to cause HP_CLKEN_*x*# output assertion to follow HP_PWREN_*x* assertion, by a fixed delay (128, 256, or 512 ms).
HP_PWRLED_[C, B, A]#	I/O PU	B16, N2, T14	**Hot Plug Power LED Outputs (3 Balls)** Active-Low Slot Control Logic output that is used to drive the Power Indicator. This output is asserted Low to turn On (illuminate) the LED. Enabled when the **Slot Capability** register *Power Indicator Present* bit (offset 7Ch[4]) is Set, and controlled by the **Slot Control** register *Power Indicator Control* field (offset 80h[9:8]). When software writes to the *Power Indicator Control* field, a Command Completed interrupt can be generated to notify the Host that the command has been executed. When the following conditions exist: • **Slot Capability** register *Power Indicator Present* bit (offset 7Ch[4]) is Set, and • **Slot Control** register *Command Completed Interrupt Enable* bit is not masked (offset 80h[4], is Set), and • **Slot Control** register *Hot Plug Interrupt Enable* bit (offset 80h[5]) is Set, an interrupt (MSI, INT*x* Message, or PEX_INTA# output, all mutually exclusive, on a per-Port basis) can be generated to the Host. **If HP_PWRLED_*x*# are used, each requires an external current-limiting resistor.** ***Note:*** *Although this is an I/O signal, its logical operation is output.*

a. If Hot Plug outputs are used and HP_MRL_x# inputs are not used, pull the HP_MRL_x# inputs Low, so that Hot Plug outputs will properly sequence if the serial EEPROM is blank or missing. Default register values enable HP_MRL_x#, which must then be asserted, to cause Hot Plug outputs to toggle (for example, to de-assert HP_PERST_x# and assert HP_PWRLED_x#).

3.4.2.2 Serial Hot Plug Signals

Transparent downstream Ports can implement Hot Plug by using external I^2C I/O Expanders (one 16-pin Maxim MAX7311, NXP PCA9555, or TI PCA9555 per slot –or– one 40-pin NXP PCA9698 per two slots, provided that the PEX 8624 serial EEPROM Sets the **Power Management Hot Plug User Configuration** register *40-Pin I/O Expander Enable* bit (Port 0, or NT Port Virtual Interface if Port 0 is the NT Port, offset 1E0h[17]). All Ports implementing Serial Hot Plug must use the same type of I/O Expander (either 16-pin or 40-pin, but not both concurrently).

Table 3-4 defines the three signal balls that support Serial Hot Plug. Additionally, the PEX 8624 supports external Serial Hot Plug signals on the I^2C I/O Expander. (Refer to Section 10.8.2, "I2C I/O Expander Parts Selection and Pin Definition.")

These signals are active only for Serial Hot Plug-capable Ports configured at start-up. For further details regarding Hot Plug, refer to Chapter 10, "Hot Plug Support."

Table 3-5. Serial Hot Plug Signals – 3 Balls

Signal Name	Type	Location	Description
I2C_SCL1	OD	U14	**I^2C Serial Clock Line for Serial Hot Plug Support** I^2C Clock source. Used with the external I^2C I/O Expander, and must be bused to each I/O Expander's Clock (SCL) pin. In combination with I2C_SDA1, forms the PEX 8624 I^2C Master interface. **I2C_SCL1 requires an external pull-up resistor.**
I2C_SDA1	OD	U13	**I^2C Serial Data Line for Serial Hot Plug Support** Transmits and receives I^2C data. Used with the external I^2C I/O Expander, and must be bused to each I/O Expander's Data (SDA) pin. In combination with I2C_SCL1, forms the PEX 8624 I^2C Master interface. **I2C_SDA1 requires an external pull-up resistor.**
SHPC_INT#	I	A1	**Serial Hot Plug Controller Interrupt Input** Active-Low interrupt input from external I^2C I/O Expanders. Used only by Serial Hot Plug-capable Transparent downstream Ports. The I/O Expander asserts its INT# output whenever any of its inputs change state, and de-asserts its INT# output when the corresponding Input Port Data register (that changed state) is read. When the SHPC_INT# Interrupt input (connected to the INT# output of all I/O Expanders) is asserted, the I^2C Master interface begins reading the Input Port registers of all I/O Expanders, and copies the values to the appropriate bits in the corresponding Port's **Slot Status** register (offset 80h). The I^2C Master interface halts the reading of I/O Expander registers when the SHPC_INT# input de-asserts. **SHPC_INT# requires an external pull-up resistor.** ***Note:*** *SHPC_INT# is internally de-bounced, but must remain stable for at least 10 ms.*

3.4.3 Serial EEPROM Signals

The PEX 8624 includes four signals for interfacing to a serial EEPROM, defined in Table 3-6. For information regarding serial EEPROM use, refer to Chapter 6, "Serial EEPROM Controller."

Table 3-6. Serial EEPROM Signals – 4 Balls

Signal Name	Type	Location	Description
EE_CS#	I/O PU	B18	**Active-Low Serial EEPROM Chip Select I/O** ***Note:*** *Although this is an I/O signal, its logical operation is output.*
EE_DI	O	C15	**PEX 8624 Output to Serial EEPROM Data Input**
EE_DO	I/O PU	C17	**PEX 8624 I/O from Serial EEPROM Data Output** Should be pulled High to VDD25. ***Note:*** *Although this is an I/O signal, its logical operation is input.*
EE_SK	I/O PU	B17	**Serial EEPROM Clock Frequency Output** Programmable (by way of the **Serial EEPROM Clock Frequency** register *EepFreq[2:0]* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 268h[2:0]), to the following: • 1 MHz (default) • 1.98 MHz • 5 MHz • 9.62 MHz • 12.5 MHz • 15.6 MHz • 17.86 MHz ***Note:*** *Although this is an I/O signal, its logical operation is output.*

3.4.4 Strapping Signals

The PEX 8624 Strapping inputs, defined in Table 3-7, Set the configuration of upstream Port and NT Port assignment, Link width, and various setup and test modes. These inputs must be pulled or tied High to VDD25 or Low to Ground (VSS), as indicated in the table. After a Fundamental Reset, the **Link Capability**, **Debug Control**, and **Port Configuration** registers (offsets 74h, 1DCh, and 574h, respectively) capture ball status. Strapping input Configuration data can be changed by writing new data to these registers from the serial EEPROM. I^2C can also change Strapping input Configuration data; however, it should first Set the Port's **Port Control** register *Disable Port x* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 234h[18:16]), to prevent linkup and Host enumeration. Then, when I^2C programming is complete, I^2C should lastly Clear the upstream Port's *Disable Port x* bit.

Table 3-7. Strapping Signals – 29 Balls

Signal Name	Type	Location	Description
STRAP_DEBUG_SEL[1:0]	I	N3, U2	***Factory Test Only* (2 Balls)** Must be pulled or tied High to VDD25.
STRAP_FAST_BRINGUP#	I	P12	***Factory Test Only*** Must be pulled or tied High to VDD25.
STRAP_NT_ENABLE#	I	A2	**Enable NT Mode** Active-Low input that enables and disables NT mode. The STRAP_NT_ENABLE# input can be overridden by the serial EEPROM programming of the **Debug Control** register *NT Mode Enable* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1DCh[18]). **If the register is programmed by serial EEPROM, that must be the first serial EEPROM entry.** I^2C can enable or disable NT mode, by writing to the **Debug Control** register, after the upstream Port Link is brought down, by Setting the upstream device's **Link Control** register *Link Disable* bit (PCI Express Capability, offset 10h[4]). After I^2C configures the PEX 8624, the upstream Link can be restored by Clearing the *Link Disable* bit in the device connected to the upstream Port. Software can enable or disable NT mode, by writing to the **Debug Control** register, if the register's *Hardware/ Software Configuration Mode Control* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1DCh[15]) is already Set. L = Enables NT mode H = Disables NT mode (default)

Table 3-7. Strapping Signals – 29 Balls *(Cont.)*

Signal Name	Type	Location	Description
STRAP_NT_UPSTRM_PORTSEL[1:0]	I	D2, C2	**Select Upstream Non-Transparent Port (2 Balls)** Select any Station 0 Port as the upstream NT Port. The STRAP_NT_UPSTRM_PORTSEL[1:0] inputs can be overridden by the serial EEPROM value for the **Debug Control** register *NT Port Number* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1DCh[25:24]). **If the register is programmed by serial EEPROM, that must be the first serial EEPROM entry.** I^2C can select a Port to be the upstream NT Port, by writing to the **Debug Control** register. I^2C should first Set the Port's **Port Control** register *Disable Port x* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 234h[18:16]), to prevent linkup and Host enumeration. After I^2C re-configures the PEX 8624, I^2C should lastly Clear the upstream Port's *Disable Port x* bit. Software can also change which Port is configured to be the NT Port, by writing to the **Debug Control** register, if the register's *Hardware/Software Configuration Mode Control* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1DCh[15]) is already Set. Refer to Section 13.8, "Port Programmability," for further details. LL = Port 0 LH = Port 1 HL = ***Reserved*** HH = NT is not implemented ***Note:*** *If NT mode is not used (STRAP_NT_ENABLE#=H, and/or the serial EEPROM or I^2C programs NT mode (**Debug Control** register, NT Mode Enable bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1DCh[18]) is Set (thereby overriding STRAP_NT_ENABLE#))), value should be HH. and/or if the **Debug Control** register is programmed by serial EEPROM (thereby overriding STRAP_NT_UPSTRM_PORTSEL[1:0]), field [25:24] should be programmed to 11b.*
STRAP_PLL_BYPASS#	I	P18	***Factory Test Only*** Must be pulled or tied High to VDD25.
STRAP_PROBE_MODE#	I	U12	***Factory Test Only*** Must be pulled or tied High to VDD25.
STRAP_RESERVED[16, 8, 7, 4:0]	I	T13, E12, F3, V12, E2, K5, P2, J4	***Factory Test Only* (8 Balls)** ***Reserved for future use*** Refer to Table 3-8 for specific resistor requirements.
STRAP_RESERVED17#	I	D18	***Factory Test Only*** ***Reserved for future use*** Refer to Table 3-8 for specific resistor requirements.

Table 3-7. Strapping Signals – 29 Balls *(Cont.)*

Signal Name	Type	Location	Description
STRAP_SERDES_MODE_EN#	I	P17	***Factory Test Only*** Must be pulled or tied High to VDD25.
STRAP_STN0_PORTCFG1	I	R12	**Strapping Signal to Select Port Configuration for Station 0 (Number of Enabled Ports (1 or 2), and Maximum Number of Lanes for Each Specific Port)** Defines the enabled Port Numbers and their Link widths, for Station 0. Programs the **Port Configuration** register *Port Configuration for Station 0* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[1]; 574h[0] value must be 0) default value. L = Port 0 = x4, Port 1 = x4 H = Port 0 = x8, Port 1 is not enabled
STRAP_STN1_PORTCFG0	I	B2	**Strapping Signal to Select Port Configuration for Station 1 (Number of Enabled Ports (1 or 2), and Maximum Number of Lanes for Each Specific Port)** Defines the enabled Port Numbers and their Link widths, for Station 1. Programs the **Port Configuration** register *Port Configuration for Station 1* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[2]; 574h[3] value must be 1) default value. L = Port 5 = x8, Port 6 is not enabled H = Port 5 = x4, Port 6 = x4 ***Note:*** *Port 4 is visible to software, however, it does **not** connect to PCI Express signals.*
STRAP_STN2_PORTCFG1	I	B12	**Strapping Signal to Select Port Configuration for Station 2 (Number of Enabled Ports (1 or 2), and Maximum Number of Lanes for Each Specific Port)** Defines the enabled Port Numbers and their Link widths, for Station 2. Programs the **Port Configuration** register *Port Configuration for Station 2* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[5]; 574h[4] value must be 0) default value. L = Port 8 = x4, Port 9 = x4 H = Port 8 = x8, Port 9 is not enabled

Table 3-7. Strapping Signals – 29 Balls *(Cont.)*

Signal Name	Type	Location	Description
STRAP_TESTMODE[3:0]	I	J5, V2, T2, R2	**Test Mode Selects (4 Balls)** The STRAP_TESTMODE[3:0] Setting defines PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]#, GPIO[11, 10, 7, 4:2], and GPIO[19:12] signal functionality following a Fundamental Reset. PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]# and GPIO[19:12] signal functionality can also be programmed by serial EEPROM, I^2C, or software. **HLHH (1011b or Bh)** • PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]# default to the PORT_GOOD output function • GPIO[11, 10, 7, 4:2] are GPIO inputs • GPIO[19:12] are inputs, with values reflected in the **GPIO 12_19 Input Data** register (offset 640h) **HHLL (1100b or Ch)** • PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]# default to GPIO inputs, with values reflected in the **GPIO 0_11 Input Data** register (offset 63Ch) • GPIO[11, 10, 7, 4:2] are GPIO inputs • GPIO[19:12] default to the Serial Hot Plug PERST# output function **HHLH (1101b or Dh)** • PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]# default to the PORT_GOOD output function • GPIO[11, 10, 7, 4:2] are GPIO inputs • GPIO[19:12] default to the Serial Hot Plug PERST# output function **HHHH (1111b or Fh)** • PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]# and GPIO[11, 10, 7, 4:2] default to GPIO inputs, with values reflected in the **GPIO 0_11 Input Data** register (offset 63Ch) • GPIO[19:12] are inputs, with values reflected in the **GPIO 12_19 Input Data** register (offset 640h) All other encodings are ***Factory Test Only***.

Table 3-7. Strapping Signals – 29 Balls *(Cont.)*

Signal Name	Type	Location	Description
STRAP_UPSTRM_PORTSEL[3:0]	I	D12, D17, C18, A12	**Strapping Signals to Select Upstream Port (4 Balls)** Select any Port as the upstream Port. The STRAP_UPSTRM_PORTSEL[3:0] inputs can be overridden by the serial EEPROM value for the **Debug Control** register *Upstream Port ID* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1DCh[11:8]). **If the register is programmed by serial EEPROM, that must be the first serial EEPROM entry.** I^2C can also change which Port is configured to be the upstream Port, by writing to the **Debug Control** register. I^2C should first Set the Port's **Port Control** register *Disable Port x* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 234h[18:16]), to prevent linkup and Host enumeration. After I^2C re-configures the PEX 8624, I^2C should lastly Clear the upstream Port's *Disable Port x* bit. Software can also change which Port is configured to be the upstream Port, by writing to the **Debug Control** register, if the register's *Hardware/Software Configuration Mode Control* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1DCh[15]) is already Set. Refer to Section 13.8, "Port Programmability," for further details. LLLL = Port 0 LLLH = Port 1 LHLH = Port 5 HHL = Port 6 HLLL = Port 8 HLLH = Port 9 All other encodings are ***reserved.***

Table 3-8. STRAP_RESERVED17# and STRAP_RESERVED[16, 8, 7, 4:0] Input External Pull-Up/ Pull-Down Resistor Requirements

Ball/Signal Name	Pull-Up/Pull-Down
STRAP_RESERVED17#	Must be pulled or tied High.
STRAP_RESERVED16	Must be tied directly to Ground (VSS).
STRAP_RESERVED8	Must be pulled or tied directly to Ground (VSS).
STRAP_RESERVED7	Must be pulled or tied High.
STRAP_RESERVED4	Must be pulled or tied directly to Ground (VSS).
STRAP_RESERVED3	Must be pulled or tied High.
STRAP_RESERVED2	Must be pulled or tied High.
STRAP_RESERVED1	Must be pulled or tied Low.
STRAP_RESERVED0	Must be pulled or tied Low.

3.4.5 JTAG Interface Signals

The PEX 8624 includes five signals for performing Joint Test Action Group (JTAG) boundary scan, defined in Table 3-9. The JTAG interface is described in Section 16.6, "JTAG Interface."

Table 3-9. JTAG Interface Signals – 5 Balls

Signal Name	Type	Location	Description
JTAG_TCK	I	B1	**JTAG Test Clock Input** JTAG Test Access Port (TAP) Controller clock source. Frequency can be from 0 to 20 MHz.
JTAG_TDI	I	E1	**JTAG Test Data Input** Serial input to the JTAG TAP Controller, for test instructions and data.
JTAG_TDO	O	C1	**JTAG Test Data Output** Serial output from the JTAG TAP Controller test instructions and data.
JTAG_TMS	I	D1	**JTAG Test Mode Select** Input decoded by the JTAG TAP Controller, to control test operations.
JTAG_TRST#	I	F2	**JTAG Test Reset** Active-Low input used to reset the Test Access Port. When JTAG functionality is not used, the JTAG_TRST# input should be driven Low, or pulled Low to Ground (VSS) through a 1.5KΩ resistor, to place the JTAG TAP Controller into the *Test-Logic-Reset* state, which disables the test logic and enables standard logic operation. Alternatively, if JTAG_TRST# input is High, the JTAG TAP Controller can be placed into the *Test-Logic-Reset* state by initializing the JTAG TAP Controller's **Instruction** register to contain the *IDCODE* instruction, or by holding the JTAG_TMS input High for at least five rising edges of the JTAG_TCK input.

3.4.6 I²C Slave Interface Signals

Table 3-10 defines the five signals that support the I²C Slave interface. For further details, refer to Chapter 7, "I2C Slave Interface Operation."

Table 3-10. I²C Slave Interface Signals – 5 Balls

Signal Name	Type	Location	Description
I2C_ADDR[2:0]	I	J2, H1, H2	**I²C Slave Address Bits 2 through 0 Inputs (3 Balls)** Used to configure the PEX 8624 Slave address on the I²C Bus. If I²C configuration is used, I2C_ADDR[2:0] should be strapped to a unique address, to avoid address conflict with any other I²C devices (on the same I²C Bus segment) that have the upper four bits of their 7-bit I²C Slave address also programmed to 1101b. **I2C_ADDR[2:0] require external pull-up or pull-down termination resistors. If I²C is not used, external termination is strongly recommended, to prevent possible Input buffer oscillation.**
I2C_SCL0	OD	G4	**I²C Serial Clock Line** I²C Clock bidirectional Clock line. Data on the I²C-bus can be transferred at rates of up to 100 kbit/s (Standard mode). **I2C_SCL0 requires an external pull-up resistor.** ***Note:*** *The PEX 8624 I²C Slave Interface can stretch the Low period of the I²C clock while a simultaneous in-band Request that also targets PEX 8624 registers is being processed.*
I2C_SDA0	OD	G3	**I²C Serial Data I/O** Transmits and receives I²C data during I²C accesses to PEX 8624 registers. **I2C_SDA0 requires an external pull-up resistor.**

3.4.7 Device-Specific Signals

Table 3-11 defines the Device-Specific signals – signals that are unique to the PEX 8624.

Table 3-11. Device-Specific Signals – 23 Balls

Signal Name	Type	Location	Description
FATAL_ERR#	O	C13	**Fatal Error Output** Asserted Low when a Fatal error is detected in the PEX 8624 and the following conditions exist (all the same conditions that are required to send a Fatal Error Message to the Host): • Specific error is defined as *Fatal* in the **Uncorrectable Error Severity** register (offset FC0h), and • Reporting of the specific error condition is enabled, not masked by the **Uncorrectable Error Mask** register's (offset FBCh) corresponding *Interrupt Mask* bit, and • **Device Control** register *Fatal Error Reporting Enable* bit (offset 70h[2]) –or– **PCI Command** register *SERR# Enable* bit (offset 04h[8]) is Set The **Device Status** register *Fatal Error Detected* bit (offset 70h[18]) is Set, and the specific error is flagged in the **Uncorrectable Error Status** register (offset FB8h).
GPIO[19:12]	I/O PU	P1, U1, T1, V1, R16, U18, A17, B15	**General-Purpose I/O (8 Balls)** Default functionality is determined at Fundamental Reset; however, functionality can be switched by programming the **GPIO** registers using serial EEPROM, I^2C, and/or software. GPIO[19:12] provide GPIO input functionality, by default, when the STRAP_TESTMODE[3:0] inputs, sampled at Fundamental Reset (PEX_PERST# input de-assertion), are a value of 1011b or 1111b (Bh or Fh, respectively). Alternatively, when the STRAP_TESTMODE[3:0] inputs, sampled at Fundamental Reset, are a value of 1100b or 1101b (Ch or Dh, respectively), GPIO[19:12] function as Serial Hot Plug PERST# Reset outputs (similar to HP_PERST_*x*# outputs), by default, for corresponding Ports that include an external I^2C I/O Expander. If an external I^2C I/O Expander is not present for a Port, the corresponding GPIO[19:12] output remains Low (the Serial Hot Plug PERST# output for that Port is not de-asserted). If Serial Hot Plug is implemented (using external I^2C I/O Expanders), it is recommended that the GPIO[19:12] signals be strapped as Serial Hot Plug PERST# Reset outputs and routed to the slots, rather than using the PERST# outputs from the I/O Expanders.
GPIO[11, 10, 7, 4:2]	I/O PU	T17, R17, J1, H5, L5, L1	**General-Purpose I/O (6 Balls)** GPIO[11, 10, 7, 4:2] provide GPIO functionality, determined according to the GPIO registers associated with each GPIO (offsets 62Ch, 630h, and 638h through 654h). ***Note:*** *If PEX_PORT_GOODx# functionality is enabled, GPIO4# output is always High.*

Table 3-11. Device-Specific Signals – 23 Balls *(Cont.)*

Signal Name	Type	Location	Description
PEX_INTA#	OD	G5	**Interrupt Output** PEX_INTA# Interrupt output is enabled if: • INT*x* Messages are enabled and MSIs are disabled (**PCI Command** register *Interrupt Disable* and **MSI Control** register *MSI Enable* bits, offsets 04h[10] and 48h[16], respectively, are both Cleared) • PEX_INTA# output (**ECC Error Check Disable** register *Enable PEX_INTA# Interrupt Output(s) for x Interrupt* bit(s), offset 1C8h[7, 6, 5, and/or 4]) is enabled (refer to the register description, for Port associations) The three interrupt mechanisms, listed below, are mutually exclusive modes of operation, on a per-Port basis, for all interrupt sources: • Conventional PCI INT*x* Message generation • Native MSI transaction generation • Device-Specific PEX_INTA# assertion PEX_INTA# assertion (Low) indicates that one or more of the following events and/or errors (if not masked) were detected: • Hot Plug or Link State events • PCI Express Hot Plug events • General-Purpose Input Interrupt events • Device-Specific errors • NT-Virtual Doorbell events • NT-Link Doorbell events • Device-Specific NT Port Link Interface errors and events Refer to Section 9.1.1, “Interrupt Sources or Events,” for details.
PEX_NT_RESET#	O	V14	**Active-Low Output Used to Propagate Reset in NT Mode** Pulse width is 1 µs.

Table 3-11. Device-Specific Signals – 23 Balls *(Cont.)*

Signal Name	Type	Location	Description
PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]#	I/O PU	T18, R18, H4, H3, F1, G1	**Active-Low PCI Express Port Linkup Status Indicator Outputs for Ports 9, 8, 6, 5, 1, and 0 –or– Programmable General-Purpose I/O (6 Balls)** PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]# function as general-purpose inputs, interrupt inputs, general-purpose outputs, or as the PORT_GOOD output function, as outlined below. If the Port is ***not*** enabled, the signal defaults to GPIO*x* input (default value 0). **General-Purpose Inputs** For PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]# signals that are configured as general-purpose inputs (by STRAP_TESTMODE[3:0] inputs, sampled at Fundamental Reset with a value of 1111b or 1100b, or by subsequent programming (by serial EEPROM, I^2C, and/or software) of the appropriate **GPIO *x* Direction Control** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 62Ch) *Direction Control* bits), input states are reflected in the **GPIO 0_11 Input Data** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 63Ch[9, 8, 6, 5, 1, 0], respectively). Inputs can be internally de-bounced, by Setting the corresponding **GPIO 0_19 Input De-Bounce** register bits (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 638h[11:0], respectively). De-bouncing is disabled, by default; if de-bouncing is enabled, an input must be stable for approximately 1.3 ms to be latched. **Interrupt Inputs** For PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]# signals that are configured as Interrupt inputs in the **GPIO *x* Direction Control** registers, input states are reflected in the **GPIO 0_19 Interrupt Status** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 650h[9, 8, 6, 5, 1, 0] respectively). Inputs can be internally de-bounced, by Setting the corresponding **GPIO 0_19 Input De-Bounce** register bits (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 638h[9, 8, 6, 5, 1, 0], respectively). De-bouncing is disabled, by default; if de-bouncing is enabled, an input must be stable for approximately 1.3 ms to be latched. Interrupt polarity (Active-High or Active-Low) is individually programmable in the **GPIO 0_19 Interrupt Polarity** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 64Ch[9, 8, 6, 5, 1, 0] respectively). Interrupt generation can be selectively masked in the **GPIO 0_19 Interrupt Mask** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 654h[9, 8, 6, 5, 1, 0] respectively). Continued…

Table 3-11. Device-Specific Signals – 23 Balls *(Cont.)*

Signal Name	Type	Location	Description
PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]#	I/O PU	T18, R18, H4, H3, F1, G1	Continued… **General-Purpose Outputs** For PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]# signals that are configured as general-purpose outputs (in the **GPIO *x* Direction Control** registers, output states are controlled by the corresponding **GPIO 0_11 Output Data** register bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 644h[9, 8, 6, 5, 1, 0], respectively) values. **PORT_GOOD Output Function** For PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]# signals that correspond to enabled Ports and are configured for PORT_GOOD functionality (by STRAP_TESTMODE[3:0] inputs, sampled at Fundamental Reset with a value of 1011b or 1101b, or by subsequent programming (by serial EEPROM, I^2C, and/or software) of the appropriate **GPIO *x* Direction Control** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 62Ch) value). The PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]# output states are not directly available from a single register (due to encoded, possibly blinking output); however, software can determine LANE_GOOD status (PHY Link status for each Lane) from the **Station 0/1 Lane Status** and **Station 2 Software Lane Status** registers (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 1F4h and 270h). Software can also determine the Port's Maximum Link Width and Supported Link Speeds from the Port's **Link Capability** register (offset 74h[9:4 and 3:0], respectively, as well as the Port's Negotiated Link Width and Current Link Speed from the Port's **Link Status** register (offset 78h[25:20 and 19:16], respectively). The NT Port Virtual Interface **Link Capability** and **Link Status** registers follow the NT Port Link Interface configuration, and contain the same values as the corresponding NT Port Link Interface registers. If PORT_GOOD functionality is enabled, but some Ports are not enabled due to the STRAP_STN*x*_PORTCFG*x* input levels, the PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]# signals associated with non-enabled Ports function as GPIO*x* input. ***Note:*** *If PEX_PORT_GOODx# functionality is enabled, GPIO4 output is always High.* LED behavior when connected to PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]# signals: • **Off** – Link is down • **On** – Link is up, 5.0 GT/s, all Lanes are up • **Blinking, 0.5 seconds On, 0.5 seconds Off** – Link is up, 5.0 GT/s, reduced Lanes are up • **Blinking, 1.5 seconds On, 0.5 seconds Off** – Link is up, 2.5 GT/s, all Lanes are up • **Blinking, 0.5 seconds On, 1.5 seconds Off** – Link is up, 2.5 GT/s, reduced Lanes are up

3.4.8 External Resistor Signals

Table 3-12. External Resistor Signals – 6 Balls

Signal Name	Type	Location	Description
REXT_A[4, 3, 0]	A	J15, D7, R7	**External Resistor Balls (3 Balls)** One pair per SerDes block (paired with the “B” signal). **Do not connect to any other signal, power, nor Ground.** **Must attach a 1.43KΩ 1% resistor between each REXT_A and REXT_B pair.**
REXT_B[4, 3, 0]	A	J14, E7, P7	**External Resistor Balls (3 Balls)** One pair per SerDes block (paired with the “A” signal). **Do not connect to any other signal, power, nor Ground.** **Must attach a 1.43KΩ 1% resistor between each REXT_A and REXT_B pair.**

3.4.9 No Connect Signals

Caution: ***Do not connect these balls to board electrical paths. These balls are internally connected to the device.***

Table 3-13. No Connect Signals – 15 Balls

Signal Name	Type	Location	Description
N/C	***Reserved***	A7, B7, F7, J13, J17, J18, L3, N7	**No Connect (8 Balls)** Do not connect these balls to board electrical paths.
SPARE[4:0]	I/O PU	R13, L4, K3, K1, G2	**Spare (5 Balls)** ***Reserved for future use*** Do not connect these balls to board electrical paths. **SPARE4 Only:** When SPARE4 is pulled High, the Data Rate Identifier symbol in the TS Ordered-Sets always advertises support for both the Gen 2 data rate and Autonomous Change. When SPARE4 is pulled Low, if this Link training sequence fails during the *Configuration* state, the next time the Link Training and Status State Machine (LTSSM) exits the *Detect* state, TS Ordered-Sets advertise only the Gen 1 data rate, and no Autonomous Change support. The LTSSM then continues to toggle between Gen 1 and Gen 2 advertisement every time it exits the *Detect* state. ***Note: This feature should be enabled only if a non-compliant device will not linkup if these Data Rate Identifier bits are Set.***
THERMAL_DIODEn	***Reserved***	P13	**No Connect** ***Factory Test Only*** Do not connect this ball to board electrical paths.
THERMAL_DIODEp	***Reserved***	V13	**No Connect** ***Factory Test Only*** Do not connect this ball to board electrical paths.

3.4.10 Power and Ground Signals

Table 3-14. Power and Ground Signals – 105 Balls

Signal Name	Type	Location	Description
VDD10	CPWR	G7, G9, G11, H8, H10, H12, J7, J9, J11, K8, K10, K12, L7, L9, L11, M8, M10, M12	**1.0V ±5% Power for Core and SerDes Digital Logic (18 Balls)**
VDD10A	APWR	F6, F10, F12, G13, H6, K6, L13, M6, N9, N11	**1.0V ±5% Power for SerDes Analog Circuits (10 Balls)**
VDD25	I/OPWR	F5, F13, N5, N13, T15	**2.5V ±10% Power for I/O Logic Functions (5 Balls)**
VDD25A	PLLPWR	F8, K13, N8	**2.5V ±10% Power for Phase-Locked Loop (PLL) Circuits (3 Balls)**
VSS	GND	A15, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, D14, D15, D16, E13, E16, F4, F9, F11, F16, G6, G8, G10, G12, G16, H7, H9, H11, H13, H16, J3, J6, J8, J10, J12, J16, K7, K9, K11, K16, L6, L8, L10, L12, L16, M7, M9, M11, M13, M16, N4, N6, N10, N12, N16, P14, P15, P16, T3, T4, T5, T6, T7, T8, T9, T10, T11, T12, T16	**Ground Connections (69 Balls)**

3.5 Physical Layout

Figure 3-1. Physical Ball Assignment (See-Through Top View)

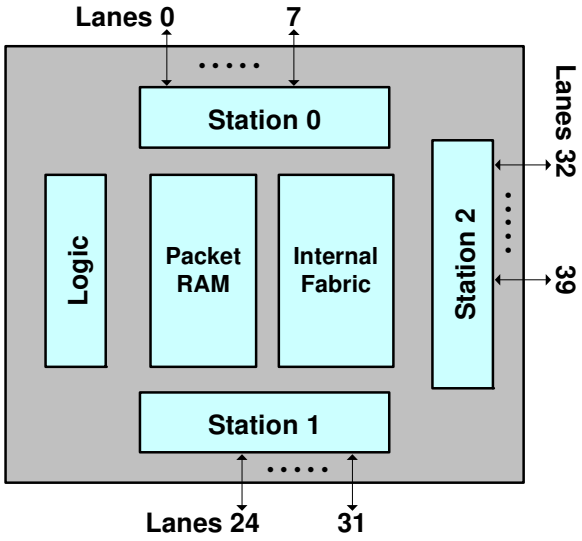
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A	SHPC_INT#	STRAP_NT_ENABLE#	PEX_PETn24	PEX_PETn25	PEX_PETn26	PEX_PETn27	N/C	PEX_PETn28	PEX_PETn29	PEX_PETn30	PEX_PETn31	STRAP_UPSTRM_PORTSEL0	HP_ATNLED_C#	HP_BUTTON_C#	VSS	HP_PRSNT_C#	GPIO13	HP_CLKEN_C#	A
B	JTAG_TCK	STRAP_STN1_PORTCFG0	PEX_PETp24	PEX_PETp25	PEX_PETp26	PEX_PETp27	N/C	PEX_PETp28	PEX_PETp29	PEX_PETp30	PEX_PETp31	STRAP_STN2_PORTCFG1	HP_PERST_C#	HP_PWREN_C	GPIO12	HP_PWRLED_C#	EE_SK	EE_CS#	B
C	JTAG_TDO	STRAP_NT_UPSTRM_PORTSEL0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	FATAL_ERR#	HP_PWRFLT_C#	EE_DI	HP_PWR_GOOD_C	EE_DO	STRAP_UPSTRM_PORTSEL1	C
D	JTAG_TMS	STRAP_NT_UPSTRM_PORTSEL1	PEX_PERn24	PEX_PERn25	PEX_PERn26	PEX_PERn27	REXT_A3	PEX_PERn28	PEX_PERn29	PEX_PERn30	PEX_PERn31	STRAP_UPSTRM_PORTSEL3	HP_MRL_C#	VSS	VSS	VSS	STRAP_UPSTRM_PORTSEL2	STRAP_RESERVED17#	D
E	JTAG_TDI	STRAP_RESERVED3	PEX_PERp24	PEX_PERp25	PEX_PERp26	PEX_PERp27	REXT_B3	PEX_PERp28	PEX_PERp29	PEX_PERp30	PEX_PERp31	STRAP_RESERVED8	VSS	PEX_PERp39	PEX_PERn39	VSS	PEX_PETp39	PEX_PETn39	E
F	PEX_PORT_GOOD1#	JTAG_TRST#	STRAP_RESERVED7	VSS	VDD25	VDD10A	N/C	VDD25A	VSS	VDD10A	VSS	VDD10A	VDD25	PEX_PERp38	PEX_PERn38	VSS	PEX_PETp38	PEX_PETn38	F
G	PEX_PORT_GOOD0#	SPARE0	I2C_SDA0	I2C_SCL0	PEX_INTA#	VSS	VDD10	VSS	VDD10	VSS	VDD10	VSS	VDD10A	PEX_PERp37	PEX_PERn37	VSS	PEX_PETp37	PEX_PETn37	G
H	I2C_ADDR1	I2C_ADDR0	PEX_PORT_GOOD5#	PEX_PORT_GOOD6#	GPIO4	VDD10A	VSS	VDD10	VSS	VDD10	VSS	VDD10	VSS	PEX_PERp36	PEX_PERn36	VSS	PEX_PETp36	PEX_PETn36	H
J	GPIO7	I2C_ADDR2	VSS	STRAP_RESERVED0	STRAP_TESTMODE3	VSS	VDD10	VSS	VDD10	VSS	VDD10	VSS	N/C	REXT_B4	REXT_A4	VSS	N/C	N/C	J
K	SPARE1	HP_ATNLED_B#	SPARE2	HP_PWR_GOOD_B	STRAP_RESERVED2	VDD10A	VSS	VDD10	VSS	VDD10	VSS	VDD10	VDD25A	PEX_PERp35	PEX_PERn35	VSS	PEX_PETp35	PEX_PETn35	K
L	GPIO2	HP_MRL_B#	N/C	SPARE3	GPIO3	VSS	VDD10	VSS	VDD10	VSS	VDD10	VSS	VDD10A	PEX_PERp34	PEX_PERn34	VSS	PEX_PETp34	PEX_PETn34	L
M	HP_BUTTON_B#	HP_PRSNT_B#	PEX_PERST#	HP_PWREN_B	HP_PWRFLT_B#	VDD10A	VSS	VDD10	VSS	VDD10	VSS	VDD10	VSS	PEX_PERp33	PEX_PERn33	VSS	PEX_PETp33	PEX_PETn33	M
N	HP_PERST_B#	HP_PWRLED_B#	STRAP_DEBUG_SEL1	VSS	VDD25	VSS	N/C	VDD25A	VDD10A	VSS	VDD10A	VSS	VDD25	PEX_PERp32	PEX_PERn32	VSS	PEX_PETp32	PEX_PETn32	N
P	GPIO19	STRAP_RESERVED1	PEX_PERp0	PEX_PERp1	PEX_PERp2	PEX_PERp3	REXT_B0	PEX_PERp4	PEX_PERp5	PEX_PERp6	PEX_PERp7	STRAP_FAST_BRINGUP#	THERMAL_DIODEn	VSS	VSS	VSS	STRAP_SERDES_MODE_EN#	STRAP_PLL_BYPASS#	P
R	HP_CLKEN_B#	STRAP_TESTMODE0	PEX_PERn0	PEX_PERn1	PEX_PERn2	PEX_PERn3	REXT_A0	PEX_PERn4	PEX_PERn5	PEX_PERn6	PEX_PERn7	STRAP_STN0_PORTCFG1	SPARE4	HP_PWR_GOOD_A	HP_MRL_A#	GPIO15	GPIO10	PEX_PORT_GOOD8#	R
T	GPIO17	STRAP_TESTMODE1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	STRAP_RESERVED16	HP_PWRLED_A#	VDD25	VSS	GPIO11	PEX_PORT_GOOD9#	T
U	GPIO18	STRAP_DEBUG_SEL0	PEX_PETp0	PEX_PETp1	PEX_PETp2	PEX_PETp3	PEX_REFCLKp	PEX_PETp4	PEX_PETp5	PEX_PETp6	PEX_PETp7	STRAP_PROBE_MODE#	I2C_SDA1	I2C_SCL1	HP_PWREN_A	HP_ATNLED_A#	HP_BUTTON_A#	GPIO14	U
V	GPIO16	STRAP_TESTMODE2	PEX_PETn0	PEX_PETn1	PEX_PETn2	PEX_PETn3	PEX_REFCLKn	PEX_PETn4	PEX_PETn5	PEX_PETn6	PEX_PETn7	STRAP_RESERVED4	THERMAL_DIODEp	PEX_NT_RESET#	HP_CLKEN_A#	HP_PERST_A#	HP_PWRFLT_A#	HP_PRSNT_A#	V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

Chapter 4 Functional Overview

4.1 Hardware Architecture

The PEX 8624 is designed with a flexible, modular architecture. The 24 PCI Express Lanes are implemented equally across three Stations (8 per Station), which are connected to one another by the internal fabric to the central RAM. Figure 4-1 provides a block diagram of the PEX 8624.

Figure 4-1. PEX 8624 Block Diagram



4.1.1 Station and Port Functions

Each Port implements the *PCI Express Base r2.0* Physical, Data Link, and Transaction Layers (PHY, DLL, and TL, respectively). Each PCI Express Station supports up to 8 integrated Serializer/ De-Serializer (SerDes) modules, which provide the 24 PCI Express hardware interface Lanes. The Lanes can be combined, for a total of one to two PCI Express Ports per Station.

4.1.1.1 Port Configurations

Table 4-1 defines the PEX 8624 Port, Station, and Lane configurations. Each Station's Port configuration is independent of the other Stations' Port configurations. Ports that are not configured nor enabled are invisible to software.

The upstream and downstream Ports' Link widths are initially defined by the STRAP_STN*x*_PORTCFG*x* inputs, which are pulled or tied High to VDD25 or Low to VSS (GND). The serial EEPROM option can be used to re-configure the Ports, with the options defined in Table 4-1. Serial EEPROM configuration occurs following a Fundamental Reset, and overrides the configuration defined by the STRAP_STN*x*_PORTCFG*x* inputs at that time. Port configuration can also be changed through the I^2C Slave interface. The final Link width can be automatically negotiated down from the programmed width, through Link-width negotiation for linkup to a device with fewer Lanes. The narrowest Port on one end of the Link determines the maximum Link width. Additionally, if a connection is broken on one of the Lanes, the training sequence removes the broken Lane and negotiates to a narrower Link width. A x8 Port can negotiate down to x4, x2, or x1.

If the Port cannot train to x1 (Lane 0 is broken), the Port reverses its Lanes and attempts to retrain. *For example*, a x8 Port that cannot train to x8 attempts to negotiate down to x4, x2, or x1; if x1 linkup fails, the Port reverses its Lanes and re-attempts linkup negotiation. Either the lowest Lane (Lane 0) or highest Lane (if Lanes are reversed) of the programmed Link width must connect to the other device's Lane 0.

Each Port can run independently at Gen 1 (2.5 GT/s) or Gen 2 (5.0 GT/s) speed.

Notes: *Yellow-highlighted cells in Table 4-1 indicate the default Hot Plug Port for that configuration.*

The six PEX 8624 Ports that connect to PCI Express Transmitters and Receivers are Ports 0, 1, 5, 6, 8, and 9, and each Port has its own set of registers. An additional set of Port 4 registers is visible to software, although the Port is not connected to external signals. The Port 4 registers include:

- *Other Device-Specific registers.*
- *"Station" registers, that control all Ports in Station 1 (Ports 5 and 6), and are identical to the Port 0 registers that control all Ports in Station 0 (Ports 0 and 1) and Port 8 registers that control all Ports in Station 2 (Ports 8 and 9). The Station registers include Physical Layer registers, Device-Specific Error registers, and internal mapping (CAM) registers.*

Table 4-1. Port Configurations

Port Configuration Strapping STRAP_STN0_PORTCFG1, STRAP_RESERVED4	Port Configuration Register Value Port 0, Offset 574h[23:20, 1:0]	Station 0 [Lanes/SerDes]/Port		
		Port 0	Port 1	–
0, 0	0h, 00b	x4 [0-3]	x4 [4-7]	
1, 0	0h, 10b	x8 [0-7]		
Port Configuration Strapping **STRAP_RESERVED7, STRAP_STN1_PORTCFG0**	**Port Configuration Register Value** **Port 0, Offset 574h[27:24, 3:2]**	**Station 1 [Lanes/SerDes]/Port**		
		Port 4	**Port 5**	**Port 6**
1, 0	0h, 10b	***Software Only***	x8 [24-31]	
1, 1	0h, 11b	***Software Only***	x4 [24-27]	x4 [28-31]
Port Configuration Strapping **STRAP_STN2_PORTCFG1, STRAP_RESERVED8**	**Port Configuration Register Value** **Port 0, Offset 574h[31:28, 5:4]**	**Station 2 [Lanes/SerDes]/Port**		
		Port 8	**Port 9**	**–**
0, 0	0h, 00b	x4 [32-35]	x4 [36-39]	
1, 0	0h, 10b	x8 [32-39]		

Notes:

- *The Lanes are assigned to each enabled Port in sequence, as indicated in [brackets].*
- *Refer to Table 4-2 for an explanation of the Port/Physical Lane/SerDes Module/Station to SerDes Quad relationship, when all Ports are enabled.*

Table 4-2. Port/Physical Lane/SerDes Module/Station/SerDes Quad Relationship, when All Ports Are Enabled

Physical Lanes and SerDes Modules, by Port						SerDes Quad
Station 0, Port 0		Station 1, Port 4		Station 2, Port 8		
Port	Physical Lanes and SerDes Modules	Port	Physical Lanes and SerDes Modules	Port	Physical Lanes and SerDes Modules	
0	0-3	–	***Factory Test Only***	8	32-35	0
1	4-7	–	***Factory Test Only***	9	36-39	1
–	***Factory Test Only***	5	24-27	–	***Factory Test Only***	2
–	***Factory Test Only***	6	28-31	–	***Factory Test Only***	3

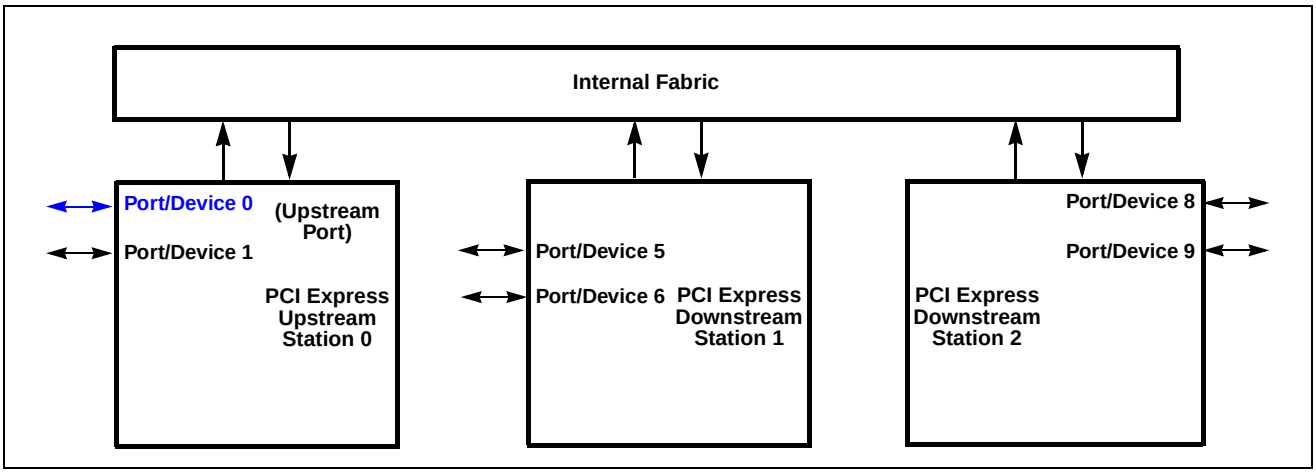
4.1.1.2 Port Numbering

The PEX 8624 Port Numbers are 0 and 1 (Station 0), 5 and 6 (Station 1), and 8 and 9 (Station 2). (Refer to Table 4-1 and Figure 4-2.)

The Port Numbers have a direct relationship to the downstream Ports for the PCI Device Number assigned to the internal PCI-to-PCI bridges on the internal virtual PCI Bus. *For example*, if Port 5 is a downstream Port, the PCI-to-PCI bridge associated with that Port is Device Number 5. Each downstream Device Number matches its corresponding Port Number. *For example*, if Port 0 is the upstream Port, Ports 1, 5, 6, 8, and 9 are the downstream Ports. The Device Numbers for the PCI-to-PCI bridges implemented on the downstream Ports are 1, 5, 6, 8, and 9, respectively. (Refer to Figure 4-2.)

Any PEX 8624 Port can be configured as, or dynamically changed to be, the upstream Port (Port 0 is recommended). The PCI-to-PCI bridge implemented on the upstream Port does not assume a Device Number – it accepts the Device Number assigned by the upstream device. Generally, the upstream device assigns Device Number 0, according to the *PCI Express Base r2.0*.

Figure 4-2. Port Numbering Convention Example (When Port 0 Is Upstream Port)



4.2 PCI Express Station Functional Description

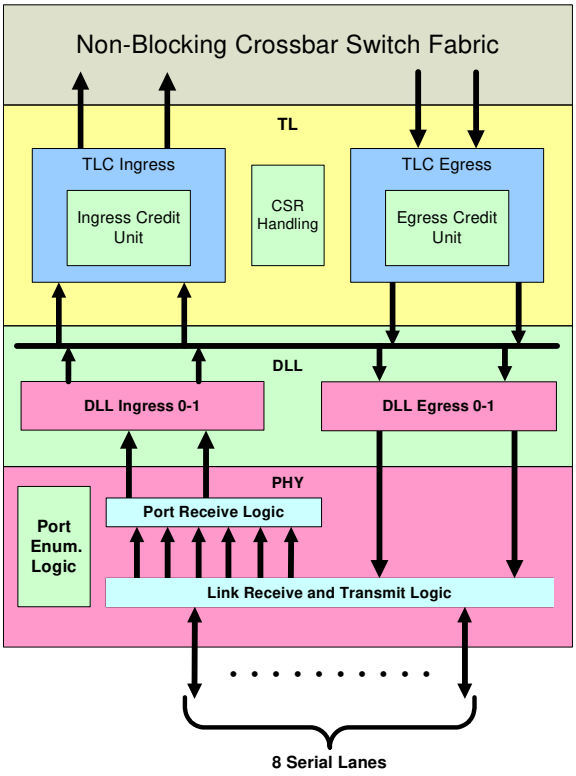
The PEX 8624 groups 8 SerDes together into a Station. Each Station can be comprised of one to two PCI Express Ports. (Refer to Table 4-1.) The Station forwards ingress packets to the internal crossbar fabric and central RAM, and the Station pulls egress packets from the central RAM to send out of the PEX 8624.

Each Station implements the PCI Express PHY and DLL functions for each of its Ports, and aggregates traffic from these Ports onto a transaction-based, non-blocking internal fabric. The PCI Express Station also performs many TL functions, while the packet queuing and ordering aspects of this layer are handled by the Crossbar Switch Control blocks.

During system initialization, software initiates Configuration Requests that set up the PCI Express interfaces, Device Numbers, and Address maps across the various Ports. These maps are used to direct traffic between Ports during standard system operation. Traffic flow between Ports within the same Station, or Ports on different Stations, is supported through the central internal fabric.

At the top level, each Station has a layered organization consisting of the PHY, DLL, and TL blocks, as illustrated in Figure 4-3. The PHY and DLL blocks have Port-specific data paths (one per PCI Express Port) that operate independently of one another. The Transaction Layer Control (TLC) ingress section of the TL block aggregates traffic for all ingress Ports within the Station, then sends the traffic to the internal crossbar fabric. The TLC egress section of the TL block accepts packets, by way of the internal crossbar fabric, from all ingress Ports, and schedules them to be sent out the appropriate egress Port.

Figure 4-3. PCI Express Station Block Diagram



4.3 Physical Layer

The Physical Layer (PHY) converts information received from the DLL into an appropriate serialized format and transmits it across the PCI Express Link. The PHY also receives the serialized input from the Serializer/De-Serializer (SerDes), converts it to parallel data (internal Data Bus), then writes it to the Transaction Layer Control (TLC) Ingress buffer.

The PHY includes all circuitry for PCI Express Link Interface operation, including:

- Driver and input buffers
- Parallel-to-serial and serial-to-parallel conversion
- Phase-Locked Loops (PLLs) and clock circuitry
- Impedance matching circuitry
- Interface initialization and maintenance functions

4.3.1 Physical Layer Features

The PHY module interfaces to the PCI Express Lanes and implements the PHY functions. The number of PCI Express Ports is one to two per Station, with a cumulative Lane bandwidth of x8 on each Station. PHY functions include:

- SerDes modules, which provide all functions required by the *PCI Express Base r2.0*
- User-configurable Port division
- Link widths – x4 or x8; widths of x1 and x2 are also supported
- Link speeds supported
  - 2.5 GT/s
  - 5.0 GT/s
- Hardware Link training and initialization
- Hardware detection of polarity reversal
- Hardware detection of Lane reversal
- Hardware Autonomous Speed Control supported
- Dynamic Link speed control supported
- Dynamic Link width supported
- Data scrambling/de-scrambling and 8b/10b encode/decode
- Packet framing
- Loopback Master and Slave support
- Programmable test pattern with SKIP Ordered-Set insertion and return data checking
- Receiver error checking (Elastic buffer over/underflow, disparity, and symbol encoding)
- Modified Compliance Pattern support with Receiver Error Counters, per Lane
- Link state Power Management (PM) – Supports L0, L0s, L1, L2/L3 Ready, and L3 Link PM states
- Supports cross-linked upstream Port and downstream Ports

4.3.2 Physical Layer Status and Command Registers

The PHY operating conditions are defined in:

- Section 12.14.2, "Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)"
- Section 12.14.4, "Device-Specific Registers – Physical Layer (Offsets 270h – 28Ch)"

The System Host can track the Link operating status and re-configure Link parameters, by way of these registers.

4.3.3 Hardware Link Interface Configuration

The PHY can include up to eight integrated SerDes modules on each Station, which are distributed among four SerDes quads (Quads 0, 1, 2, and 3) and provide the PCI Express hardware interface Lanes. (Refer to Table 4-2, which lists the relationship of the SerDes modules and quads to the Stations and 24 Lanes, when all Ports are enabled.) The SerDes modules also provide all physical communication controls and functions required by the *PCI Express Base r2.0*, as well as the Links (clustered into Ports) that connect the PEX 8624 to other PCI Express devices.

The quantity of Ports, and Link widths associated with those Ports, are configurable, on a Station-by-Station basis. Initial Port configuration is determined by the STRAP_STN*x*_PORTCFG*x* inputs, serial EEPROM, or auto Link-width negotiation. After the PEX 8624 Ports are configured using the auto-negotiation process, the Link widths can narrow or widen (by combining multiple adjacent Lanes within the Station).

4.4 Transaction Layer

The upper layer of the architecture is the Transaction Layer (TL). The TL assembles and disassembles TLPs, which are used to communicate transactions, *such as* Read and Write, as well as certain types of events. The TL also manages credit-based Flow Control (FC) for TLPs.

The TL supports four Address spaces – it includes the three PCI Address spaces (Configuration, Input/Output, and Memory) and adds a Message space. (Refer to Table 4-3.) This specification uses Message space to support all prior sideband signals, *such as* interrupts, Power Management (PM) Requests, and so forth, as in-band Message transactions. PCI Express Message transactions are considered *virtual wires* that support *virtual pins*. As virtual wires, Assert and De-assert Messages are sent when a triggering event changes the wire's state.

Table 4-3. Address Spaces Support Differing Transaction Types

Address Space	Transaction Types	Transaction Functions
Configuration	Read/Write	Device configuration or setup
Input/Output		Transfers data from/to an I/O space
Memory		Transfers data from/to a memory location
Message	Baseline/Virtual Wires	General-purpose Messages Event signaling (status, interrupts, and so forth)

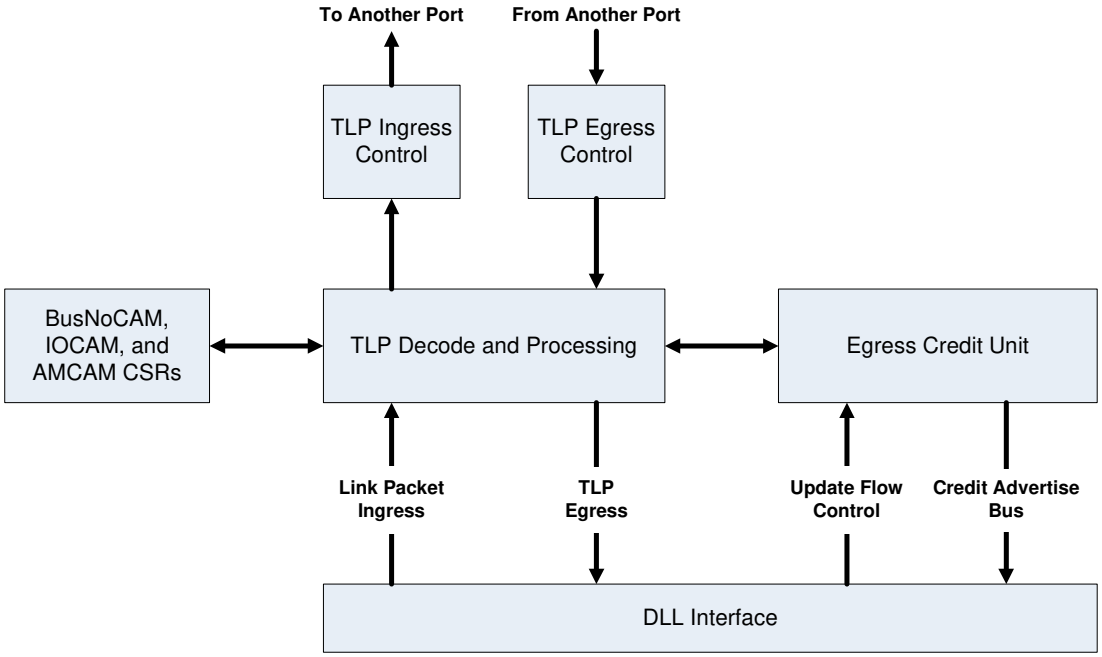
All Request packets requiring a Response packet are implemented as Split Transactions. Each packet has a unique identifier that enables Response packets to be directed to the correct originator. The packet format supports various forms of addressing, depending upon the transaction type – *Memory, I/O, Configuration,* or *Message*.

TL functions include:

- Decoding and checking rules for the incoming TLP
- Memory-Mapped Configuration Space register (CSR) access
- Checking incoming packets for malformed or unsupported packets
- Data Poisoning and end-to-end data integrity detection
- End-to-end Cyclic Redundancy Check (ECRC) of incoming packets
- Error logging and reporting for incoming packets
- TLP dispatching
- Write control to the packet RAM and packet Link List RAM
- Destination lookup and TC-VC mapping
- Shadow CSRs for BusNoCAM/IOCAM/AMCAM/TC-VC mapping
- Credit-based scheduling
- Pipelined full Split Transaction protocol
- PCI/PCI-X-compatible ordering
- Interrupt handling (INT*x* or Message Signaled Interrupts (MSIs))
- Power Management (PM) support
- Hot Plug and PCI Express Hot Plug event support
- Link State event support
- QoS support
- Ordering
- Ingress and Egress credit management

The hardware functions provided by the PEX 8624 to implement the *PCI Express Base r2.0* TL requirements are illustrated in Figure 4-4. The blocks provide a combination of ingress and egress control, as well as the data management at each stage within the flow sequence.

Figure 4-4. TL Controller



4.4.1 Locked Transactions

The PEX 8624 understands Locked transactions; however, it does not lock the resources. This is consistent with limitations for Locked transaction use, as outlined in the *PCI r3.0* (Appendix F, "Exclusive Accesses"), and prevents potential deadlock, as well as serious performance degradation, that could occur with Locked transaction use.

4.4.2 Relaxed Ordering

The PEX 8624 supports Relaxed Ordering for Completions. By default, if the RO attribute is Set within a Completion, then that Completion can bypass Posted transactions, if Posted TLPs are blocked at the egress Port (due to insufficient Posted credits from the connected device). This behavior can be disabled, by Setting the **Ingress Control Shadow** register *No Special Treatment for Relaxed Ordering Traffic* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 664h[5]), in each Station.

4.4.3 TL Transmit/Egress Protocol – End-to-End Cyclic Redundancy Check

End-to-End Cyclic Redundancy Check (*ECRC*) is an optional 32-bit field appended to the end of the outgoing packet. ECRC is calculated over the entire packet, starting with the Header and including the Data Payload, except for the *Endpoint* (*EP*) bit and bit 0 of the *Type* field, which are always considered to be a value of 1 for ECRC calculations. The *ECRC* field is transmitted, unchanged, as it moves through the fabric to the Completer device. The PEX 8624 checks the ECRC on all incoming TLPs, if enabled (**Advanced Error Capabilities and Control** register *ECRC Check Enable* bit, offset FCCh[8], is Set, in each Port), and can optionally report detected errors. (When the ECRC is detected, the **Uncorrectable Error Status** register *ECRC Error Status* bit (offset FB8h[19]) can be used to log ECRC errors.)

Additionally, the PEX 8624 can optionally append ECRC to the end of internally generated TLPs, *such as* Interrupt and Error Messages, if enabled (**Advanced Error Capabilities and Control** register *ECRC Generation Enable* bit, offset FCCh[6], is Set, in each Port).

4.4.4 TL Receive/Ingress Protocol

The ingress side TL collects and stores inbound TLP traffic in the packet RAM. The incoming data is checked for ECRC errors, valid type field, length matching the Header *Transfer Size* field, and other TLP-specific errors defined by the *PCI Express Base r2.0*.

Header and Data Payload information is forwarded to the Source Scheduler, to be routed across the internal fabric, to the egress Port. When ECRC errors are detected, the packet is discarded.

4.4.5 Flow Control Credit Initialization

The initial number of VC0 Flow Control (FC) credits is advertised as programmed for each type of Header and Payload. After VC0 FC initialization is complete, the FC credits received are transferred to the TL egress. The TL ingress must schedule an UpdateFC Data Link Layer Packet (DLLP) for transmission, to replenish the number of advertised credits.

4.4.6 Flow Control Protocol

The PEX 8624 implements FC protocol that ensures that the switch:

- Does not transmit a TLP over a Link to a remote Receiver, unless the receiving device has sufficient VC Buffer space to accommodate the packet
- Generates FC credit updates to the remote Transmitter, to replace credits used to send TLPs to the PEX 8624

This FC is automatically managed by the hardware, and is transparent to software. Software is used only to enable additional Buffer space, to supplement the initial default buffer assignment.

The initial default FC credits, which are enabled after Link training, allow TLP traffic immediately after Link training completes. The Configuration transactions are the first transactions to use the default VC credits, to set up the initial device operating modes and capabilities.

The TL Ingress Credit Unit transmits DLLPs (referred to as *FC packets*) that update the FC to the remote Transmitter device, on a periodic basis. The DLLPs contain FC credit information that updates the Transmitter regarding the amount of available Buffer space in the PEX 8624.

The TL Egress Credit Unit receives DLLPs from the remote device, indicating the amount of Buffer space available in the remote Receiver. The unit uses this credit information to schedule the sending of TLPs to the remote device.

4.5 PCI-Compatible Software Model

The PEX 8624 can be thought of as a hierarchy of PCI-to-PCI bridges, with one upstream PCI-to-PCI bridge and one or more downstream PCI-to-PCI bridges connected by an internal virtual bus. (Refer to Figure 4-5.) PCI-to-PCI bridges are compliant with the PCI and PCI Express system models. Figure 4-5 illustrates the concept of hierarchical PCI-to-PCI bridges, with the bus in the middle being the internal virtual PCI Bus. The Configuration Space registers (CSRs) in the upstream PCI-to-PCI bridge are accessible by Type 0 Configuration Requests that target the upstream bus interface. The upstream Port captures the Type 0 Configuration Write Target Bus Number and Device Number. The upstream Port uses this Captured Bus Number and Captured Device Number as part of the Requester ID and Completer ID for the Requests and Completions generated by the upstream Port.

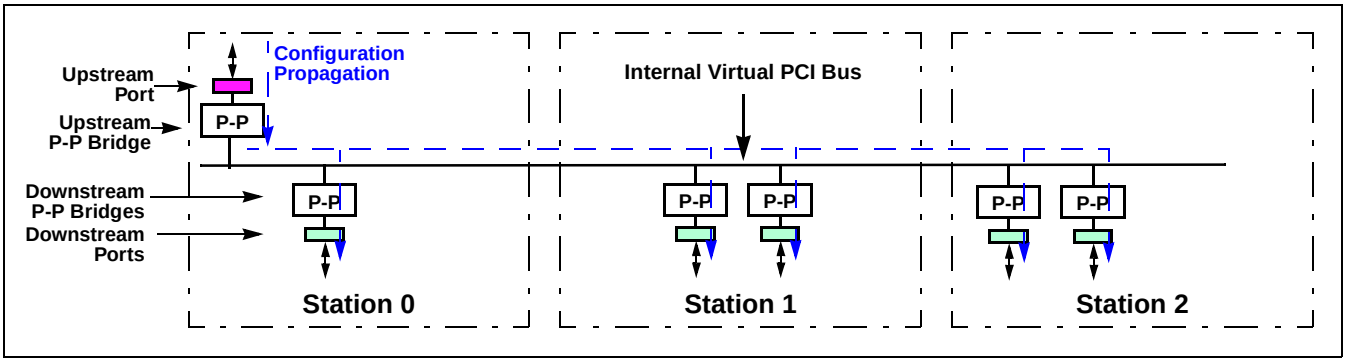
The CSRs in the downstream Port PCI-to-PCI bridges are accessible by Type 1 Configuration Requests received at the upstream Port that target the internal virtual PCI Bus, by having a Bus Number value that matches the upstream bridge's Secondary Bus Number value. Each downstream bridge is associated with a unique Device Number, as explained in Section 4.1.1.2.

The CSRs of downstream devices are hit in two ways. If the Configuration Request matches the PEX 8624 downstream Port Secondary Bus Number, the PEX 8624 converts the Type 1 Configuration Request into a Type 0 Configuration Request. However, if the Bus Number does ***not*** match the Secondary Bus Number, but falls within the Subordinate Bus Number range, the Type 1 Configuration Request is forwarded out of the PEX 8624, unchanged. A Type 1 Configuration Request that targets a Bus Number that is not within range is invalid, and is terminated by the PEX 8624 upstream Port as an Unsupported Request (UR).

After all PCI devices have been located and assigned Bus Numbers and Device Numbers, software can assign a Memory map and I/O map. Requests (Memory or I/O) go downstream if they fall within a bridge's Base and Limit range. In the PEX 8624, each downstream bridge has its own Base and Limit. The Request (Memory or I/O) goes upstream if it does not target anything within the upstream bridge's Base and Limit range.

Completions are routed by the Bus Number established in the Configuration registers. If the Bus Number is in the Secondary or Subordinate range, the packet goes downstream; otherwise, the packet goes upstream.

Figure 4-5. System Configuration Propagation



Chapter 5 Reset and Initialization

5.1 Reset Overview

This section describes the resets that the PEX 8624 supports. (Refer to Table 5-1.) *Reset* is a mechanism that returns a device to its initial state. Reset is propagated from upstream to downstream. Hardware or software mechanisms can trigger three different levels of reset – Fundamental, Hot, or Secondary Bus (each is described in the sections that follow). The re-initialized states following a reset vary, depending upon the reset type.

Table 5-1. Reset Summary

PCI Express Definition	Reset Source	Impact to Different Internal Components (upon De-Assertion)	Impact to Internal Registers
Fundamental Reset • Cold Reset • Warm Reset	PEX_PERST# input assertion	• Initializes everything • Serial EEPROM contents are loaded • HwInit types are evaluated	All registers are initialized
Hot Reset	• TS Ordered-Set *Hot Reset* bit is Set, at the upstream Port • Upstream Port enters the *DL_Down* state	• Initializes all Station Ports • Initializes internal credits and queues • Selectively reloads serial EEPROM contents	All registers, except: • Port Configuration registers • All Sticky bits not affected by Hot Reset (HwInit, ROS, RW1CS, RWS)
Secondary Bus Reset	Downstream Port's **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]) is Set	• Downstream Port Physical Layer (PHY) generates a Hot Reset • Downstream Port Data Link Layer (DLL) is down • Downstream Port Transaction Layer (TL) is initialized, exhibits DL_Down behavior, and TLP Requests to that Port are dropped • Upstream Port and downstream Ports drain traffic, corresponding to the DL_Down condition on the downstream Port, and initialize credits corresponding to that downstream Port	Does not affect registers (other than to initialize credits)
	Upstream Port's **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]) is Set	• All downstream Ports propagate a Hot Reset • DLL of each downstream Port is down • TL of each downstream Port is initialized, exhibits DL_Down behavior, and drops TLP Requests that target downstream Ports • Upstream Port TL exhibits DL_Up behavior	Initializes downstream Ports registers to default values

5.1.1 Fundamental Reset

Fundamental Reset is a hardware mechanism defined by the *PCI Express Base r2.0*, Section 6.6. Fundamental Reset input, through the PEX_PERST# signal, resets all Port states and Configuration registers to default conditions. Reset remains asserted, until the Port's bit is Cleared.

5.1.2 Hot Reset

Hot Reset is an in-band Reset that propagates from an upstream PCI Express Link to all its Transparent downstream Ports, through the Physical Layer (PHY) mechanism. The PHY mechanism communicates a reset to downstream devices through a training sequence (TS1/TS2 Ordered-Set, in which the *Hot Reset* Training Control Bit is Set). Hot Reset is also referred to as a *Soft Reset*.

A Hot Reset initializes all Ports, resets registers that are not defined as Sticky, and resets the serial EEPROM logic to reload registers (except Port Configuration registers) from serial EEPROM, if present[a]. Hot Reset does not reset the Clock logic, and can be caused by any of the following:

- Upstream Port PHY receives two consecutive TS1 Ordered-Sets in which the *Hot Reset* Training Control Bit is Set. Hot Reset is generated from an upstream device, such as by Setting its **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]).
- Upstream Port unexpectedly enters the *DL_Down* state.

  Exception – If the upstream Port Link is in the L2 Link PM state and the Link goes down, the downstream Ports do ***not*** generate Hot Reset.
- Upstream Port PHY enters either the *Loopback* or *Disabled* state, upon receiving two consecutive TS1 or TS2 Ordered-Sets in which either the *Loopback* or *Disable Link* Training Control Bit is Set, respectively. An upstream device can generate the *Disable Link* sequence, by Setting its **Link Control** register *Link Disable* bit (offset 78h[4]).

5.1.3 Secondary Bus Reset

Any virtual upstream or downstream PCI-to-PCI bridge within the PEX 8624 can reset its downstream hierarchy, by Setting the **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]).

When the *Secondary Bus Reset* bit is Set on the upstream Port, all the downstream Ports are initialized to their default states, as defined by the *PCI Express Base r2.0*. Each of the Transparent downstream Ports generates an in-band Hot Reset onto its downstream Links (the NT Port Link Interface does not generate Hot Reset). In addition, writable registers defined by the *PCI Express Base r2.0*, in all downstream Ports, are initialized to default values (upstream Port registers are not reset, and the serial EEPROM does not reload registers).

When the *Secondary Bus Reset* bit is Set on a downstream Port, that Port is reset to its default state as defined by the *PCI Express Base r2.0*, and generates an in-band Hot Reset onto its downstream Link. The registers of that downstream Port are not affected.

5.1.4 Register Bits that Affect Hot Reset

Setting the **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]) generates a Hot Reset to downstream Ports and downstream devices.

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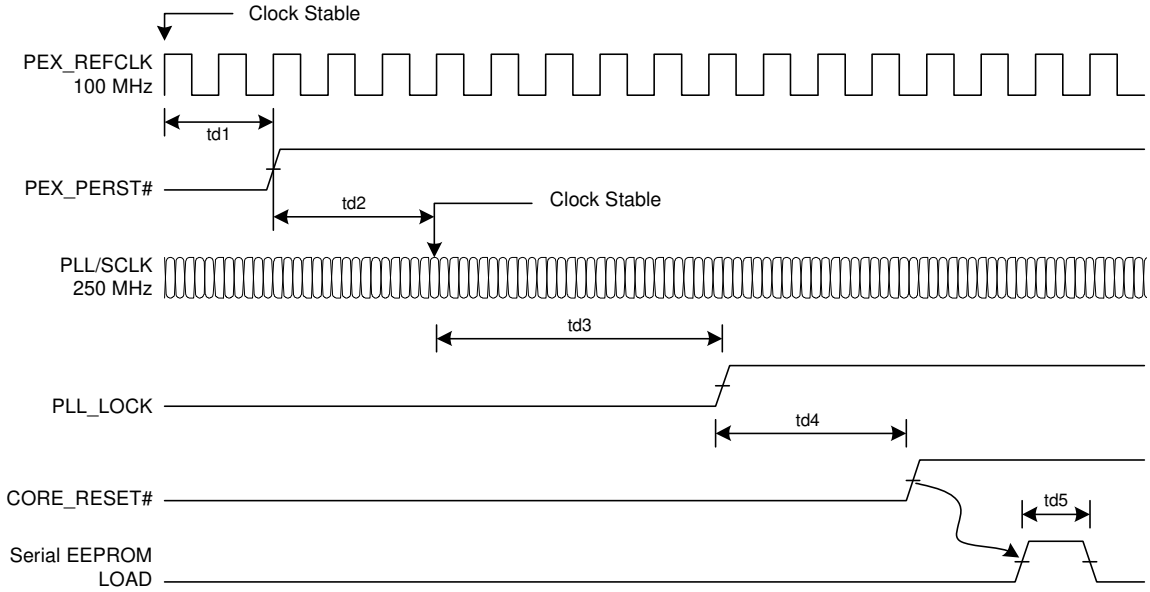
*a. The serial EEPROM is considered to be present if it returns a non-zero value in response to an initial Read Status command of its **Status** register. This value is copied to the **Serial EEPROM Status** register Status Data from Serial EEPROM fields (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 260h[31:24]). Serial EEPROM presence is reported in the register's EepPrsnt[1:0] field (field [17:16]); a value of 01b or 11b indicates that the serial EEPROM is present.*

5.1.5 Reset and Clock Initialization Timing

Table 5-2. Reset and Clock Initialization Timing

Symbol	Description	Typical Delay
td1	REFCLK stable to PEX_Reset release time	100 s
td2	PEX_Reset release to Reset de-bounce	1.32 ms
td3	Reset de-bounce to Phase-Locked Loop (PLL) Lock	105 s
td4	Reset de-bounce to Core Reset release	2.63 ms
td5	Serial EEPROM load time with no serial EEPROM present	17 s

Figure 5-1. Reset and Clock Initialization Timing



5.2 Initialization

The PEX 8624 initialization process starts upon exit from a Fundamental Reset. There are two or more steps in the process, depending upon the availability of an external initialization serial EEPROM and I^2C.

The initialization sequence executed is as follows:

1. PEX 8624 reads the Strapping inputs to determine the upstream Port (STRAP_UPSTRM_PORTSEL[3:0]), and Lane configuration (STRAP_STN*x*_PORTCFG*x*) of each enabled Port.
2. If a serial EEPROM is present, serial EEPROM data is downloaded to the PEX 8624 Configuration registers. The configuration from the Strapping inputs can be changed by serial EEPROM data.

   Alternatively, I^2C can be used to program all the registers to configure the PEX 8624 (the same as would be done with the serial EEPROM), except, if PHY or DLL register values that affect SerDes parameters or Link initialization need to be changed, those registers must be programmed by serial EEPROM, so that the values are loaded prior to initial Link training. Because I^2C is relatively slow, the Links are usually up by the time the first I^2C Write occurs. The first I^2C command might be to block system access while the configuration is being changed, by disabling the upstream Port; Ports can be disabled by Setting the Port's **Port Control** register *Disable Port x* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 234h[18:16]).

   Switch configuration, including Port Configuration (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[5:0]) and/or upstream Port designation (**Debug Control** register *Upstream Port ID* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1DCh[11:8])) can be changed:

   – At runtime, by software, if the **Debug Control** register *Hardware/Software Configuration Mode Control* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1DCh[15]) is Set
   – By I^2C or serial EEPROM reload

   If the **Debug Control** register *Upstream Port ID* field value is to be changed, the register must be written twice, with ***Factory Test Only*** bit 7 Set in the first Write, and Cleared in the second Write. Changes take effect upon subsequent Hot Reset. (Refer to Section 5.1.2.)

Note: *As described in Chapter 7, "I2C Slave Interface Operation," an external I^2C Master can send the register Read/Write Requests to PEX 8624 after reset. To prevent conflict, first disable the upstream Port, by Setting the Port's Disable Port x bit. Restoration of the upstream Port should be the last register Write of the entire I^2C programming procedure.*

3. After configuration from the Strapping signal balls, serial EEPROM, and/or I^2C is complete, the PHY of the configured Ports attempts to bring up the Links. After both components on a Link enter the initial Link Training state, the components proceed through PHY Link initialization and then through Flow Control initialization for VC0, preparing the DLL and TL to use the Link. Following Flow Control initialization for VC0, it is possible for VC0 TLPs and DLL Packets (DLLPs) to be transmitted across the Link.

5.2.1 Default Port Configuration

The default upstream Port selection and overall Link width configuration is determined by Strapping inputs, which must be pulled or tied High to VDD25 or Low to Ground (VSS), to define the default device configuration. (Refer to Section 3.4.4, "Strapping Signals.") The configuration defined by these Strapping inputs can be changed by downloading serial EEPROM data, and/or by I^2C programming followed by a Hot Reset.

5.2.2 Default Register Initialization

Each PEX 8624 Port defined in the Port Configuration process has a set of assigned registers that control Port activities and status during standard operation. These registers are programmed to default/ initial values, as defined in:

- Chapter 12, "Transparent Port Registers"
- Chapter 14, "NT Port Virtual Interface Registers – NT Mode Only"
- Chapter 15, "NT Port Link Interface Registers – NT Mode Only"

Following a Fundamental Reset, the basic PCI Express Support registers are initially programmed to the values specified in the *PCI Express Base r2.0*. The Device-Specific registers are programmed to the values specified in their register description tables. These registers can be changed by loading new data with the attached serial EEPROM, the I^2C Slave interface, and/or by CSR accesses using Configuration or Memory Writes; however, registers identified as Read-Only (RO) ***cannot*** be modified by Configuration nor Memory Write Requests.

The Transparent Ports and NT Port support the following mechanisms for accessing registers by way of the TL, as described in:

- Section 12.4.1, "PCI r3.0-Compatible Configuration Mechanism"
- Section 12.4.2, "PCI Express Enhanced Configuration Access Mechanism"
- Section 12.4.3, "Device-Specific Memory-Mapped Configuration Mechanism"

For NT mode, refer also to Section 14.3.3 or Section 15.3.3, "Device-Specific Cursor Mechanism."

5.2.2.1 Device-Specific Registers

The Device-Specific registers are unique to the PEX 8624, and are not referenced in the *PCI Express Base r2.0*. The registers are organized into the following sections:

- Section 12.14, "Device-Specific Registers (Offsets 1C0h – 51Ch)"
- Section 12.16, "Device-Specific Registers (Offsets 54Ch – F8Ch)"

5.2.3 Serial EEPROM Load Time

Serial EEPROM initialization loads only the Configuration register data that is specifically programmed into the serial EEPROM. Registers that are not included in the serial EEPROM data are initialized to default register values.

Each register entry in the serial EEPROM consists of two Address bytes and four Data bytes (refer to Section 6.4, "Serial EEPROM Data Format"); therefore, each register entry (6 bytes, or 48 bits) requires 48 serial EEPROM clocks to download. Thus, at the serial EEPROM clock default frequency of 1 MHz, after initial overhead to read the **Serial EEPROM Status** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 260h) (16 serial EEPROM clocks, or 16 s), plus another 40 serial EEPROM clocks (40 s) to begin reading the register data, each register entry in the serial EEPROM requires 48 s to download. A serial EEPROM containing 50 register entries (typical configuration, assuming the serial EEPROM is programmed only with non-default register values) and clocked at 1 MHz takes approximately 2.5 ms to load (16 + 40 + 48 x 50) s (5,200 s).

To reduce the serial EEPROM initialization time, the first register entry in the serial EEPROM can increase the clock frequency, by programming the **Serial EEPROM Clock Frequency** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 268h), to a value of 2h (5 MHz), or 3h (9.62 MHz), if the serial EEPROM supports the higher frequency at the serial EEPROM supply voltage (typically 2.5 to 3.3V). At 5 MHz clocking, the serial EEPROM load time for 50 register entries can be reduced to approximately 575 s. Because the *PCI Express Base r2.0* allows a 20-ms budget for system hardware initialization, the default 1-MHz serial EEPROM clock is often sufficient when the quantity of Ports and registers programmed by serial EEPROM is relatively small.

5.2.4 I^2C Load Time

Initialization using I^2C is slower than serial EEPROM initialization, because the I^2C Slave interface operates at a lower clock frequency (100 KHz maximum) and the quantity of bits per Register access is increased (because the Device address is included in the bit stream). Writing one register using 100-KHz clocking takes approximately 830 s (83 clock periods).

Chapter 6 Serial EEPROM Controller

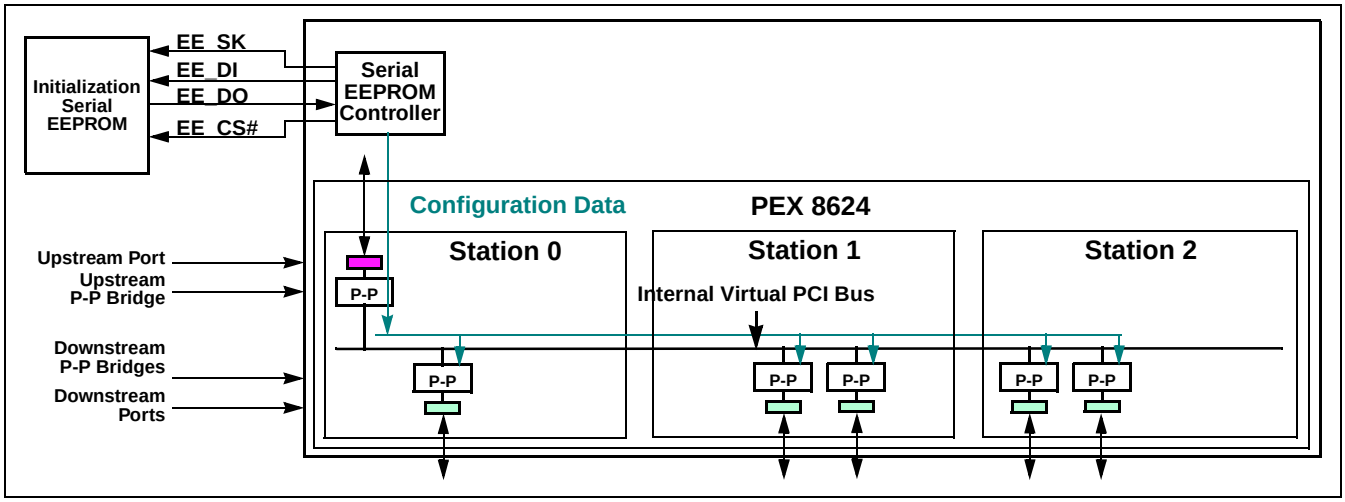
6.1 Overview

The PEX 8624 provides a Serial EEPROM Controller and interface to Serial Peripheral Interface (SPI)-compatible serial EEPROMs, as illustrated in Figure 6-1. This interface consists of a Chip Select, Clock, and Write Data outputs and a Read Data input, and operates at a programmable frequency of up to 17.86 MHz. The PEX 8624 supports serial EEPROMs that use 1-, 2-, or 3-byte addressing (2-byte addressing is recommended). The PEX 8624 automatically determines the appropriate addressing mode.

The Serial EEPROM Controller provides access to non-volatile memory. This external memory can be used for three different purposes:

- The serial EEPROM can be used to store register data, for switch configuration and initialization. When a serial EEPROM device is connected to the PEX 8624, immediately after reset, the Serial EEPROM Controller reads data from the serial EEPROM that is used to update the PEX 8624 register default values.
- System or application data can be stored into, and read from, the serial EEPROM, by software and/or I^2C, initiating random-access Read or Write Requests to the serial EEPROM.
- In NT mode, the serial EEPROM can provide up to 32 KB of Expansion ROM, for the NT Port Link Interface (default) or NT Port Virtual Interface. When software reads the Expansion ROM (starting at the Expansion ROM Base Address), the PEX 8624 reads from the serial EEPROM, to return the requested ROM image.

Figure 6-1. Serial EEPROM Connections



6.2 Features

- Detection of whether a serial EEPROM is present/not present
- Supports high-speed SPI-compatible serial EEPROMs
- Non-volatile storage for register default values loaded during Power-On Reset
- 4-byte Write/Read access to the serial EEPROM, through the upstream Port
- Serial EEPROM data format allows for loading registers by Station/Port/Address location
- Required serial EEPROM size is dependent upon the number of registers being changed
- Automatic support for 1-, 2-, or 3-byte-addressable serial EEPROMs
- Manual override for number of serial EEPROM Address bytes
- Programmable serial EEPROM clock frequency
- Programmable serial EEPROM clock-to-chip select timings
- No Cyclic Redundancy Check (CRC), single *Valid* byte at start of serial EEPROM memory
- Supports Expansion ROM for the NT Port (***not supported*** for 1-byte address serial EEPROMs)

6.3 Serial EEPROM Load Following Upstream Port Reset

The Serial EEPROM Controller performs a serial EEPROM download when the following conditions exist:

- Serial EEPROM is present[a], and
- Validation signature (first byte read from the serial EEPROM) value is 5Ah, and
- One of the following events occur:
  - PEX_PERST# is returned High, following a Fundamental Reset (*such as* a Cold or Warm Reset)
  - Hot Reset is received at the upstream Port (downloading upon this event can be optionally disabled, by Setting the **Debug Control** register *Disable Serial EEPROM Load on Hot Reset* and/or *Upstream Hot Reset Control* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1DCh[17 and/or 16]))
  - Upstream Port exits a *DL_Down* state (downloading upon this event can be optionally disabled, by Setting the **Debug Control** register *Upstream Port and NT-Link DL_Down Reset Propagation Disable* and/or *Upstream Hot Reset Control* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1DCh[20 and/or 16]))

*a. The serial EEPROM is considered to be present if it returns a non-zero value in response to an initial Read Status command of its **Status** register. This value is copied to the **Serial EEPROM Status** register Status Data from Serial EEPROM fields (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 260h[31:24]). Serial EEPROM presence is reported in the register's EepPrsnt[1:0] field (field [17:16]); a value of 01b or 11b indicates that the serial EEPROM is present.*

6.4 Serial EEPROM Data Format

The data in the serial EEPROM is stored in the format defined in Table 6-1. The Validation Signature byte is located in the first address. The Serial EEPROM Controller reads this byte to determine whether a valid serial EEPROM image exists versus a blank image. REG_BYTE_COUNT[15:0] contains the number of bytes of serial EEPROM data to be loaded. It is equal to the number of registers to be loaded times 6 (6 serial EEPROM bytes, per register). If the REG_BYTE_COUNT[15:0] value is not a multiple of 6, the last incomplete register entry is ignored.

For the remaining register-related locations, data is written into a 2-byte address that represents the Configuration register offset and Port Number, and the 4 bytes following are the data loaded for that Configuration register. Only Configuration register data specifically programmed into the serial EEPROM is loaded after the PEX 8624 exits reset.

Table 6-2 defines the Configuration register Address format (REGADDR[15:0] from Table 6-1):

- Bits [9:0] represent bits [11:2] of the Register address
- Bits [15:10] represent the Port Number of the register selected to be programmed by serial EEPROM

Because the PEX 8624 Serial EEPROM Controller always accesses 4 bytes of serial EEPROM data (for DWord-aligned Register addresses), register offsets are stored in the serial EEPROM as DWord address values.

To determine the 2-byte serial EEPROM value that represents the PEX 8624 Port and register offset, shift the register offset 2 bits to the right (divide by 4), then OR the resulting value with the appropriate Port Identifier value from Table 6-2.

For example, to load Port 1 register offset 7Ch, shift the address to the right by 2 bits (this becomes 1Fh) and concatenate 0000_01b. The resulting DWord address in the serial EEPROM will be 0000_0100_0001_1111b, which is 041Fh.

Table 6-1. Serial EEPROM Data

Location	Value	Description
0h	5Ah	Validation Signature
1h	00h	***Reserved***
2h	REG_BYTE_COUNT (LSB)	Configuration register Byte Count (LSB)
3h	REG_BYTE_COUNT (MSB)	Configuration register Byte Count (MSB)
4h	REGADDR (LSB)	1st Configuration Register Address (LSB)
5h	REGADDR (MSB)	1st Configuration Register Address (MSB)
6h	REGDATA (Byte 0)	1st Configuration Register Data (Byte 0)
7h	REGDATA (Byte 1)	1st Configuration Register Data (Byte 1)
8h	REGDATA (Byte 2)	1st Configuration Register Data (Byte 2)
9h	REGDATA (Byte 3)	1st Configuration Register Data (Byte 3)
Ah	REGADDR (LSB)	2nd Configuration Register Address (LSB)
Bh	REGADDR (MSB)	2nd Configuration Register Address (MSB)
Ch	REGDATA (Byte 0)	2nd Configuration Register Data (Byte 0)
Dh	REGDATA (Byte 1)	2nd Configuration Register Data (Byte 1)
Eh	REGDATA (Byte 2)	2nd Configuration Register Data (Byte 2)
Fh	REGDATA (Byte 3)	2nd Configuration Register Data (Byte 3)
…	…	…
FFFFh	REGDATA (Byte 3)	Last Configuration Register Data (Byte 3)

Note: *If the **Debug Control** register (Port 0, offset 1DCh) is programmed by the serial EEPROM, it must be programmed twice by the first two serial EEPROM entries, at locations 4h through 9h, and Ah through Fh, as listed in Table 6-1. The first entry must Set **Factory Test Only** bit 7, to enable Writes to certain fields within the register, and the second entry must Clear bit 7; **all other bit values must be identical in both entries**.*

Table 6-2. Configuration Register Address Format

Port Number	REGADDR Bits [15:10] Value[a]	Port Identifier
Port 0	0000_00b	0000h
Port 1	0000_01b	0400h
Port 4[b]	0010_00b	2000h
Port 5	0010_01b	2400h
Port 6	0010_10b	2800h
Port 8	0100_00b	4000h
Port 9	0100_01b	4400h
NT Port Virtual Interface[c]	0XX0_XXb	XX00h
NT Port Link Interface	1110_00b	E000h

*a. Encodings not listed are **reserved**.*

*b. Port 4 is **Software Only**.*

*c. For NT Port Virtual Interface registers, use the value for the Port Number that is configured as the NT Port (Port 0, 1, 2, or 3, as designated by the STRAP_NT_UPSTRM_PORTSEL[1:0] Strapping signals or **Debug Control** register NT Port Number field (Port 0, offset 1DCh[25:24])).*

6.5 Serial EEPROM Initialization

After the device Reset is de-asserted, the PEX 8624 determines whether a serial EEPROM is present. The serial EEPROM is considered to be present if it returns a non-zero value in response to an initial Read Status command of its **Status** register. A pull-up resistor on the EE_DO input produces a value of FFh if a serial EEPROM is not installed. If a serial EEPROM is detected, the first byte (validation signature) is read. If a value of 5Ah is read, it is assumed that the serial EEPROM is programmed for the PEX 8624. The serial EEPROM address width is determined while the first byte is read. If the first byte's value is not 5Ah, the serial EEPROM is blank or programmed with invalid data. In this case, no more data is read from the serial EEPROM, and the **Serial EEPROM Status** register *EepAddrWidth* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 260h[23:22]) reports a value of 00b (undetermined width).

If the *EepAddrWidth* field reports a value of 00b, any subsequent accesses to the serial EEPROM (through the PEX 8624 Serial EEPROM registers) default to a serial EEPROM address width of 1 byte, unless the **Serial EEPROM Status** register *EepAddrWidth Override* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 260h[21]) is Set. The *EepAddrWidth* field is usually Read-Only (RO); however, it is writable if the *EepAddrWidth Override* bit is Set (both can be programmed by a single Write instruction).

If the serial EEPROM contains valid data, the REG_BYTE_COUNT values in Bytes 2 and 3 determine the number of serial EEPROM locations that contain Configuration register addresses and data. Each Configuration register entry consists of 2 bytes of register Address and 4 bytes of register Write data. The REG_BYTE_COUNT must be a multiple of 6.

The EE_SK output clock frequency is determined by the **Serial EEPROM Clock Frequency** register *EepFreq[2:0]* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 268h[2:0]). The default clock frequency is 1 MHz. At this clock rate, it takes approximately 48 s per DWORD during Configuration register initialization. For faster loading of large serial EEPROMs that support a faster clock, the first Configuration register load from the serial EEPROM could be to the **Serial EEPROM Clock Frequency** register.

6.6 PCI Express Configuration, Control, and Status Registers

The PCI Express Configuration, Control, and Status registers that can be initialized are detailed in:

- Chapter 12, "Transparent Port Registers"
- Chapter 14, "NT Port Virtual Interface Registers – NT Mode Only"
- Chapter 15, "NT Port Link Interface Registers – NT Mode Only"

6.7 Serial EEPROM Registers

The Serial EEPROM register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 260h through 26Ch) parameters defined in Section 12.14.2, "Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)," can be changed, using the serial EEPROM. It is recommended that the first serial EEPROM entry (after the pair of entries for the **Debug Control** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1DCh), if programmed), be used to change the **Serial EEPROM Clock Frequency** register (offset 268h) value, to increase the clock frequency, and thereby reduce the time needed for the remainder of the serial EEPROM load. When the NT Port Expansion ROM feature is used, the serial EEPROM clock frequency must be 5 MHz or higher. At the last serial EEPROM entry, the **Serial EEPROM Status and Control** register (offset 260h) can be programmed to issue a Write Status (WRSR) command, to enable the Write Protection feature(s) within the serial EEPROM data, if needed.

6.8 Serial EEPROM Random Write/Read Access

To access the serial EEPROM, a PCI Express or I^2C Master uses the following registers (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port):

- **Serial EEPROM Status and Control** (offset 260h)
- **Serial EEPROM Buffer** (offset 264h)
- **Serial EEPROM 3rd Address Byte** (offset 26Ch)

Note: *To help streamline the text in the following subsections, the specific Port location/access of each register offset is not repeated – only the offset location is mentioned.*

The Master can only access the serial EEPROM on a DWord basis (4 bytes), aligned to one DWord address.

6.8.1 Writing to Serial EEPROM

To write a DWord to the serial EEPROM:

1. If the 3rd Address byte (Address bits [23:16]) is needed (when the **Serial EEPROM Status** register *EepAddrWidth* field bits (offset 260h[23:22]) are both Set), write the value to the **Serial EEPROM 3rd Address Byte** register *Serial EEPROM 3rd Address Byte* field (offset 26Ch[7:0]).
2. Write the 32-bit data into the **Serial EEPROM Buffer** register (offset 264h).
3. Issue a Write Enable instruction to the serial EEPROM (Command = 110b, Set Write Enable Latch), by writing the value 0000_C000h into the **Serial EEPROM Status and Control** register (offset 260h).
4. Calculate and write the combined Address and Command value to write into the **Serial EEPROM Control** register (offset 260h), by combining the serial EEPROM 3-bit Write Data instruction (value 010b) as bits [15:13], together with the serial EEPROM address. Serial EEPROM Address bits [14:2] must be programmed into **Serial EEPROM Control** register bits [12:0], and serial EEPROM Address bit 15 must be programmed into **Serial EEPROM Status** register bit 20 (*that is*, Set bit 20 if the serial EEPROM address is in the upper 32 KB of any 64-KB address block within the serial EEPROM). The data in the **Serial EEPROM Buffer** register is written to the serial EEPROM when the **Serial EEPROM Status and Control** register is written.
5. The serial EEPROM Write operation is complete when a subsequent read of the **Serial EEPROM Status** register bit 18 returns 0. At this time, another serial EEPROM access can be started.

Because each PEX 8624 Port and Register address value (REGADDR; refer to Section 6.5), and its corresponding data value (REGDATA), require 6 bytes of serial EEPROM memory, and the PEX 8624 serial EEPROM interface accesses 4 bytes at a time, two serial EEPROM Writes may be needed to store each set of REGADDR (1 word) and REGDATA (1 Dword) entries into the serial EEPROM. To avoid overwriting a word of another set of 6-byte REGADDR and REGDATA values, one of the two Serial EEPROM Writes might need to be a Read-Modify-Write type of operation (preserving one word Read from the serial EEPROM, and writing the value back along with a new word value).

6.8.2 Reading from Serial EEPROM

To read a DWord from the serial EEPROM:

1. If the 3rd Address byte (Address bits [23:16]) is needed (when the **Serial EEPROM Status** register *EepAddrWidth* field bits (offset 260h[23:22]) are both Set), write the value to the **Serial EEPROM 3rd Address Byte** register *Serial EEPROM 3rd Address Byte* field (offset 26Ch[7:0]).
2. Calculate the combined Address and Command value to write into the **Serial EEPROM Control** register (offset 260h), by combining the serial EEPROM 3-bit Read Data instruction (value 011b) as bits [15:13], together with the serial EEPROM address. Serial EEPROM Address bits [14:2] must be programmed into **Serial EEPROM Control** register bits [12:0], and serial EEPROM Address bit 15 must be programmed into **Serial EEPROM Status** register bit 20 (*that is*, Set bit 20 if the serial EEPROM address is in the upper 32 KB of any 64-KB address block within the serial EEPROM).
3. Poll the **Serial EEPROM Status** register until the *EepCmdStatus* bit (offset 260h[18]) is Cleared, which signals that the transaction is complete.
4. Read the four bytes of serial EEPROM data from the **Serial EEPROM Buffer** register (offset 264h).

   For example, to read the first DWord in the serial EEPROM, write the value 0000_6000h to Port 0, register offset 260h, and then read Port 0, register offset 264h.

6.8.3 Programming a Blank Serial EEPROM

The PEX 8624 supports 1-, 2-, or 3-byte serial EEPROM addressing. 8-Kbit to 512-Kbit SPI EEPROMs use 2-byte addressing. The PEX 8624 requires that the first byte in the serial EEPROM must be the value 5Ah (ASCII Z), as a Validation Signature.

The 2nd and 3rd bytes contain the number of bytes within the serial EEPROM image, beginning with the first register entry at serial EEPROM address 04h. If this Byte Count value exceeds the actual number of register entries times 6 (*for example*, if the first DWord is programmed to the value 5A00_FFFFh), the system could hang. To simplify programming of a blank EEPROM (*such as* in a typical production build), the serial EEPROM could be pre-programmed with the first DWord, 0000_005Ah.

A 2-byte address serial EEPROM that is blank (or corrupted) can be programmed according to the following procedure (when the PEX 8624 is in 1-Byte Address mode).

To program a blank serial EEPROM:

1. Write the value 0000_005Ah into the **Serial EEPROM Buffer** register at address [upstream Port **BAR0** + 264h].
2. Issue a Write Enable instruction (Command = 110b, Set Write Enable Latch, and enable 2-byte addressing, by writing the value 00A0_C000h into the **Serial EEPROM Status and Control** register (offset 260h).
3. Copy this data value to serial EEPROM location 0, by writing the value 00A0_4000h into the **Serial EEPROM Status and Control** register. At this point, the first four bytes in the serial EEPROM now contain the value 0000_005Ah.
4. Reboot the system, to reset the PEX 8624 so that it re-detects the serial EEPROM.

6.9 Serial EEPROM Loading of NT Port Link Interface Registers

The **Debug Control** register *Load Only EEPROM NT-Link on Hot Reset* and *Inhibit EEPROM NT-Link Load on Hot Reset* bits (NT Port Virtual Interface if Port 0 is the NT Port, offset 1DCh[31:30], respectively) control whether the serial EEPROM is to load registers following a Soft Reset (Hot Reset or DL_Down) to the upstream Port or NT Port Link Interface, as defined in Table 6-3.

Table 6-3. Serial EEPROM Loading of NT Port Link Interface Registers (Offset 1DCh[31:30] Values)

Bit 31 Value	Bit 30 Value	Action
0	0	Load all registers from the serial EEPROM.
0	1	Load all registers, except the NT Port Link Interface registers, from the serial EEPROM.
1	0	Load only NT Port Link Interface registers from the serial EEPROM.
1	1	Disable serial EEPROM loading of all registers.

6.10 NT Port Expansion ROM

The PEX 8624 NT Port Virtual and Link Interfaces support Expansion ROM, as defined in the *PCI r3.0*. Expansion ROM can be implemented for either Port, but not both concurrently. The Expansion ROM image is stored in the serial EEPROM, and its size can be either 16 KB (default, bit is Cleared) or 32 KB (maximum), based upon the **Serial EEPROM Clock Frequency** register *Expansion ROM Size* bit (NT Port Virtual Interface if Port 0 is the NT Port, offset 268h[16]) value. When the NT Port Expansion ROM feature is used, the serial EEPROM clock frequency must be 5 MHz or higher.

By default, the Expansion ROM is enabled on the NT Port Link Interface; however, it can be enabled instead for the NT Port Virtual Interface, by Setting the **Ingress Control** register *Expansion ROM Virtual Side* bit (NT Port Virtual Interface if Port 0 is the NT Port, offset 660h[23]). The **Expansion ROM Base Address** register (BAR) must be enabled, by Setting the register's *Expansion ROM Enable* bit, in either the NT Port Virtual Interface (offset 30h[0]) or NT Port Link Interface (offset 30h[0]).

The Expansion ROM's location in the serial EEPROM is programmed in the **Serial EEPROM 3rd Address Byte** register *Expansion ROM Base Address* field (NT Port Virtual Interface if Port 0 is the NT Port, offset 26Ch[31:16]), of which the lower six bits, [21:16], map to serial EEPROM byte Address bits [15:10] (aligned to a 256-DWord (1-KB) boundary). The Expansion ROM must not straddle a 64-KB boundary within the serial EEPROM.

The default serial EEPROM Base Address value is as follows:

- **16-KB NT Port Expansion ROM (*Expansion ROM Size* bit is Cleared)** – The value is 0020h, which corresponds to serial EEPROM Byte address 2000h (8 KB). The serial EEPROM size must be at least 32 KB.
- **32-KB NT Port Expansion ROM (*Expansion ROM Size* bit is Set)** – The value is 0040h, which corresponds to serial EEPROM byte address 4000h (16 KB). The serial EEPROM size must be at least 64 KB.

Chapter 7 I²C Slave Interface Operation

7.1 I²C Support Overview

Note: *This chapter applies to the I²C Slave interface, which uses the I2C_ADDR[2:0], I2C_SCL0, and I2C_SDA0 signals for PEX 8624 register access by an I²C Master. The I2C_SCL1 and I2C_SDA1 signals form the PEX 8624 I²C Master interface, which is used only for Serial Hot Plug operation. (Refer to Section 10.8, "Serial Hot Plug Controller.")*

Inter-Integrated Circuit (I²C) is a bus used to connect Integrated Circuits (ICs). Multiple ICs can be connected to an I²C Bus, and I²C devices that have I²C mastering capability can initiate a Data transfer. I²C is used for Data transfers between ICs at a relatively low rate (100 Kbps), and is used in a variety of applications. For further details regarding I²C Buses, refer to the *I2C Bus, v2.1*.

The PEX 8624 is an I²C Slave. Slave operations allow the PEX 8624 Configuration registers to be read from or written to by an I²C Master, external from the device. I²C is a sideband mechanism that allows the device Configuration registers to be programmed, read from, or written to, independent of the PCI Express upstream Link.

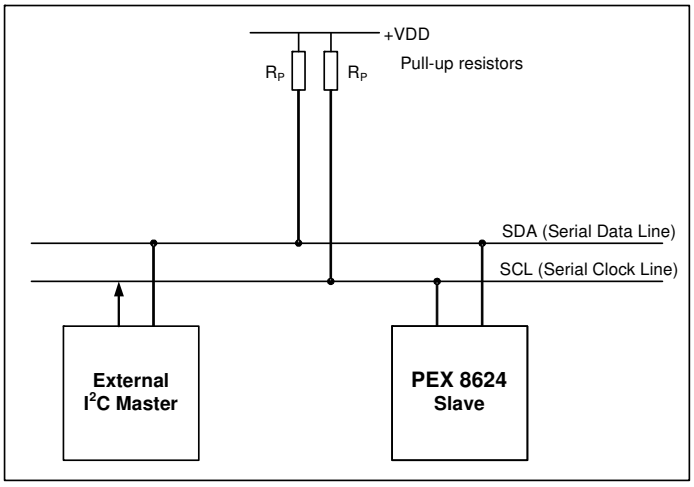
With I²C, users have the option of accessing all PEX 8624 registers through the I²C Slave interface. I²C provides an alternative to using a serial EEPROM. I²C can also be used for debugging, such as if the PEX 8624 upstream Port fails to linkup.

Accordingly, it is recommended that both I²C/SMBus access, and the serial EEPROM (or at least its footprint), be included in designs.

The I2C_SCL0 and I2C_SDA0 signals can be brought out to a 2x2 pin header on the board, to allow PLX software (*for example*, running on a laptop computer) to access the PEX 8624 registers, using an Aardvark USB-I²C adapter connected to this header. (Refer to the *PEX 8624 RDK Hardware Reference Manual* for the header pin design.)

Figure 7-1 provides a block diagram that illustrates how standard devices connect to the I²C Bus.

Figure 7-1. Standard Devices to I²C Bus Connection Block Diagram



7.2 I2C Addressing – Slave Mode Access

To access the PEX 8624 Configuration registers through the I2C Slave interface, the PEX 8624 I2C Slave address must be configured.

The PEX 8624 supports a 7-bit I2C Slave address. The 7-bit I2C Address bits can be configured by the serial EEPROM (recommended, if the default address must be changed), or by a Memory Write, in the **I2C Configuration** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 294h, default value 6Fh or 68h), with the lower three bits of the address derived from the I2C_ADDR[2:0] inputs. Bits [6:0] correspond to Address Byte bits [7:1], with bit 0 of the byte indicating a Write (0) or Read (1).

The I2C_ADDR[2:0] inputs can be pulled or tied High or Low, to select a different Slave address. Up to eight PEX 8624 devices can share the same I2C Bus segment without conflict, provided that each PEX 8624 has its set of I2C_ADDR[2:0] inputs strapped to a unique state. More than eight PEX 8624 devices can share the I2C Bus, however, if the upper Address bits are programmed in the serial EEPROM.

Note: The I2C Slave address must not be changed by an I2C Write command.

7.3 I2C Command Format

An I2C transfer starts as a packet with Address Phase bytes, followed by four Command Phase bytes, and one or more Data Phase bytes. The I2C packet Address Phase Byte format is illustrated in Figure 7-2a. The Command Phase portion must include 4 bytes of data that contain the following:

- I2C Transfer type (Read/Write)
- PCI Express Configuration Register address
- PEX 8624 Port Number being accessed
- Byte Enable(s) of the register data being accessed

When the I2C Master is writing to the PEX 8624, the I2C Master must transmit the Data bytes to be written to that register within the same packet that contains the Command bytes. Table 7-2 describes each I2C Command byte for Write access. Figure 7-2b illustrates the Command phase portion of an I2C Write packet.

When the I2C Master is reading from the PEX 8624, the I2C Master must separately transmit a Command Phase packet and Data Phase packet. Table 7-6 describes each I2C Command byte for Read access. Figure 7-4b illustrates the Command phase portion of an I2C Read packet.

Each I2C packet must contain 4 bytes of data. Pad unused packet Data bytes with zeros (0) to meet this requirement.

7.4 I2C Register Write Access

The PEX 8624 Configuration registers can be read from and written to, based upon I2C register Read and Write operations, respectively. An I2C Write packet consists of Address Phase bytes and Command Phase bytes, followed by one to four additional I2C Data bytes. Table 7-1 defines mapping of the I2C Data bytes to the Configuration register Data bytes. Figure 7-2c illustrates the I2C Data byte format.

The I2C packet starts with the *S* (START condition) bit. Data bytes are separated by the *A* (Acknowledge Control Packet (ACK)) or *N* (Negative Acknowledge (NAK)) bit. The packet ends with the *P* (STOP condition) bit.

If the Master generates an invalid command, the targeted PEX 8624 register is not modified.

The PEX 8624 considers the 1st Data byte of the 4-byte Data phase, following the four Command bytes in the Command phase, as register Byte 3 (bits [31:24]). The next three Data bytes access register Bytes 2 through 0, respectively. Four Data bytes are required, regardless of the Byte Enable Settings in the Command phase. The Master can then generate either a STOP condition (to finish the transfer) or a repeated START condition (to start a new transfer). If the I2C Master sends more than the four Data bytes (violating PEX 8624 protocol), the PEX 8624 returns a NAK for the extra Data byte(s). (For further details regarding I2C protocol, refer to the *I2C Bus, v2.1*.)

Table 7-2 describes each I2C Command byte for Write access. In the packet described in Figure 7-2, Command Bytes 0 through 3 follow the format specified in Table 7-2.

Table 7-1. I2C Register Write Access

I2C Data Byte Order	PCI Express Configuration Register Bytes
0	Written to register Byte 3
1	Written to register Byte 2
2	Written to register Byte 1
3	Written to register Byte 0

Table 7-2. I²C Command Format for Write Access

Byte	Bit(s)	Description
1st (0)	7:3	***Reserved*** Should be Cleared.
	2:0	**Command** 011b = Write register Do not use other encodings for Writes.
2nd (1)	7:4	***Reserved*** Should be Cleared.
	3	**NT Port Link Interface Access** Valid only if NT mode is enabled. 0 = *Station Select* bits (2nd Command byte, bits [2:1]), and *Port Selector* bits (2nd Command byte, bit 0, and 3rd Command byte, bit 7) are used to select 6 Ports. 1 = NT Port Link Interface access is enabled. *Station Select* bits (2nd Command byte, bits [2:1]), and *Port Selector* bits (2nd Command byte, bit 0, and 3rd Command byte, bit 7) should be Cleared.
	2:1	**Station Select** 00b = Station 0 01b = Station 1 10b = Station 2 11b = ***Reserved***
	0	**Port Selector, Bit 1** 2nd Command byte, bit 0, and 3rd Command byte, bit 7, combine to form a 2-bit Port Selector.
3rd (2)	7	**Port Selector, Bit 0** *Port Selector[1:0]* selects the Port to access. 00b = Port 0 of the Station indicated by *Station Select* 01b = Port 1 of the Station indicated by *Station Select* For NT Port Link Interface access, the *Port Selector[1:0]* value must be 00b. For NT Port Virtual Interface access, the *Port Selector[1:0]* value is XXb.
	6	***Reserved*** Should be Cleared.
	5:2	**Byte Enables** **Bit** **Description** 2 Byte Enable for Byte 0 (PEX 8624 register bits [7:0]) 3 Byte Enable for Byte 1 (PEX 8624 register bits [15:8]) 4 Byte Enable for Byte 2 (PEX 8624 register bits [23:16]) 5 Byte Enable for Byte 3 (PEX 8624 register bits [31:24]) 0 = Corresponding PEX 8624 register byte will not be modified 1 = Corresponding PEX 8624 register byte will be modified All 16 combinations are valid values.
	1:0	**PEX 8624 Register Address [11:10]**
4th (3)	7:0	**PEX 8624 Register Address [9:2]** ***Note:*** *All register addresses are DWord-aligned. Therefore, Address bits [1:0] are implicitly Cleared, and then internally incremented for successive I²C byte Writes.*

Figure 7-2. I2C Write Packet

Figure 7-2a I2C Write Packet Address Phase Bytes

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1]	Read/Write Bit 0 = Write	A

Figure 7-2b I2C Write Packet Command Phase Bytes

Command Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK
Command Byte 0	A	Command Byte 1	A	Command Byte 2	A	Command Byte 3	A

Figure 7-2c I2C Write Packet Data Phase Bytes

Write Cycle								
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	STOP
Data Byte 0 (to selected register Byte 3)	A	Data Byte 1 (to selected register Byte 2)	A	Data Byte 2 (to selected register Byte 1)	A	Data Byte 3 (to selected register Byte 0)	A	P

7.4.1 Register Write

The following tables illustrate a sample I²C packet for writing the PEX 8624 **MSI Upper Address** register (offset 50h) for Port 9, with data 1234_5678h.

Notes: *The PEX 8624 has a default I²C Slave address of 6Fh or 68h (68h is used for computing the values provided in this section), according to whether the I2C_ADDR[2:0] inputs have a value of 111b or 000b, respectively. The actual address is reflected in the **I2C Configuration** register Slave Address field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 294h[6:0]).*

The byte sequence on the I²C Bus, as listed in the following tables, occurs after the START and before the STOP bits, by which the I²C Master frames the transfer.

Table 7-3. I²C Register Write Access Example – 1st Cycle

Phase	Value	Description
Address	D0h	**Bits [7:1] for PEX 8624 I²C Slave Address (6Fh or 68h)** Last bit (bit 0) for Write = 0.

Table 7-4. I²C Register Write Access Example – Command Cycle

Byte	Value	Description
0	03h	[7:3] ***Reserved*** Should be Cleared. [2:0] **Command** 011b = Write
1	04h	[7:4] ***Reserved*** Should be Cleared. 3 **If NT Port Link Interface Access** [2:1] **Station Select** 0 **Port Selector, Bit 1**
2	3Ch	7 **Port Selector, Bit 0** 6 ***Reserved*** Should be Cleared. [5:2] **Byte Enables** All active. [1:0] **Register Address, Bits [11:10]**
3	14h	[7:0] **Register Address, Bits [9:2]**

Table 7-5. I²C Register Write Access Example – Write Cycle

Byte	Value	Description
0	12h	**Data to Write for Byte 3**
1	34h	**Data to Write for Byte 2**
2	56h	**Data to Write for Byte 1**
3	78h	**Data to Write for Byte 0**

Figure 7-3. I²C Write Command Packet Example

Figure 7-3a I²C Write Packet Address Phase Bytes

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address 1101_000b	Read/Write Bit 0 0 = Write	A

Figure 7-3b I²C Write Packet Command Phase Bytes

Command Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK
Command Byte 0 0000_0011b	A	Command Byte 1 0000_0001b	A	Command Byte 2 1011_1100b	A	Command Byte 3 0001_0100b	A

Figure 7-3c I²C Write Packet Data Phase Bytes

Write Cycle								
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	STOP
Data Byte 0 0001_0010b	A	Data Byte 1 0011_0100b	A	Data Byte 2 0101_0110b	A	Data Byte 3 0111_1000b	A	P

7.5 I2C Register Read Access

When the I2C Master attempts to read a PEX 8624 register, two packets are transmitted. The 1st packet consists of Address and Command Phase bytes to the Slave. The 2nd packet consists of Address and Data Phase bytes.

According to the *I2C Bus, v2.1*, a Read cycle is triggered when the Read/Write bit (bit 0) of the 1st cycle is Set. The Command phase reads the requested register content into the internal buffer. When the I2C Read access occurs, the internal buffer value is transferred on to the I2C Bus, starting from Byte 3 (bits [31:24]), followed by the subsequent bytes, with Byte 0 (bits [7:0]) being transferred last. If the I2C Master requests more than four bytes, the PEX 8624 re-transmits the same byte sequence, starting from Byte 3 of the internal buffer.

The 1st and 2nd I2C Read packets (illustrated in Figure 7-4 and Figure 7-5, respectively) perform the following functions:

- **1st packet** – Selects the register to read
- **2nd packet** – Reads the register (sample 2nd packet provided is for a 7-bit PEX 8624 I2C Slave address)

Although two packets are shown for the I2C Read, the I2C Master can merge the two packets together into a single packet, by not generating the STOP at the end of the first packet (Master does not relinquish the bus) and generating REPEAT START.

Table 7-6 describes each I2C Command byte for Read access. In the packet described in Figure 7-4, Command Bytes 0 through 3 for Reads follow the format specified in Table 7-6.

Table 7-6. I2C Command Format for Read Access

Byte	Bit(s)	Description
1st (0)	7:3	***Reserved*** Should be Cleared.
	2:0	**Command** 100b = Read register Do not use other encodings for Reads.
2nd (1)	7:4	***Reserved*** Should be Cleared.
	3	**NT Port Link Interface Access** Valid only if NT mode is enabled. 0 = *Station Select* bits (2nd Command byte, bits [2:1]), and *Port Selector* bits (2nd Command byte, bit 0, and 3rd Command byte, bit 7) are used to select 6 Ports. 1 = NT Port Link Interface access is enabled. *Station Select* bits (2nd Command byte, bits [2:1]), and *Port Selector* bits (2nd Command byte, bit 0, and 3rd Command byte, bit 7) should be Cleared.
	2:1	**Station Select** 00b = Station 0 01b = Station 1 10b = Station 2 11b = ***Reserved***
	0	**Port Selector, Bit 1** 2nd Command byte, bit 0, and 3rd Command byte, bit 7, combine to form a 2-bit Port Selector.

Table 7-6. I²C Command Format for Read Access *(Cont.)*

Byte	Bit(s)	Description
3rd (2)	7	**Port Selector, Bit 0** *Port Selector[1:0]* selects the Port to access. 00b = Port 0 of the Station indicated by *Station Select* 01b = Port 1 of the Station indicated by *Station Select* For NT Port Link Interface access, *Port Selector[1:0]* value must be 00b. For NT Port Virtual Interface access, *Port Selector[1:0]* value is XXb.
	6	***Reserved*** Should be Cleared.
	5:2	**Byte Enables** **Bit** **Description** 2 Byte Enable for Byte 0 (PEX 8624 register bits [7:0]) 3 Byte Enable for Byte 1 (PEX 8624 register bits [15:8]) 4 Byte Enable for Byte 2 (PEX 8624 register bits [23:16]) 5 Byte Enable for Byte 3 (PEX 8624 register bits [31:24]) 0 = Corresponding PEX 8624 register byte will not be modified 1 = Corresponding PEX 8624 register byte will be modified All 16 combinations are valid values.
	1:0	**PEX 8624 Register Address [11:10]**
4th (3)	7:0	**PEX 8624 Register Address [9:2]** ***Note:*** *All register addresses are DWord-aligned. Therefore, Address bits [1:0] are implicitly Cleared, and then internally incremented for successive I²C byte Writes.*

Figure 7-4. I2C Read Command Packet (1st Packet)

Figure 7-4a I2C Read Command Packet Address Phase Bytes

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1]	Read/Write Bit 0 = Write	A

Figure 7-4b I2C Read Command Packet Command Phase Bytes

Command Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	STOP
Command Byte 0	A	Command Byte 1	A	Command Byte 2	A	Command Byte 3	P

Figure 7-5. I2C Read Data Packet (2nd Packet)

Figure 7-5a I2C Read Data Packet Address Phase Bytes

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1]	Read/Write Bit, 1 = Read	A

Figure 7-5b I2C Read Data Packet Data Phase Bytes

Read Cycle								
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	STOP
Register Byte 3	A	Register Byte 2	A	Register Byte 1	A	Register Byte 0	N	P

7.5.1 Register Read Address Phase and Command Packet

The following is a sample I²C packet for reading the PEX 8624 **Serial EEPROM Buffer** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 264h) for Port 9, assuming the register value is ABCD_EF01h.

Notes: *The PEX 8624 has a default I²C Slave address of 6Fh or 68h (68h is used for computing the values provided in this section), according to whether the I2C_ADDR[2:0] inputs have a value of 111b or 000b, respectively. The actual address is reflected in the **I2C Configuration** register Slave Address field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 294h[6:0]).*

The byte sequence on the I²C Bus, as listed in the following tables, occurs after the START and before the STOP bits, by which the I²C Master frames the transfer.

Table 7-7. I²C Register Read Access Example – 1st Packet

Phase	Value	Description
Address	D0h	**Bits [7:1] for PEX 8624 I²C Slave Address (6Fh or 68h)** Last bit (bit 0) for Write = 0.

Table 7-8. I²C Register Read Access Example – Command Cycle

Byte	Value	Description
0	04h	[7:3] ***Reserved*** Should be Cleared. [2:0] **Command** 100b = Read
1	04h	[7:4] ***Reserved*** Should be Cleared. 3 **If NT Port Link Interface Access** [2:1] **Station Select** 0 **Port Selector, Bit 1**
2	3Ch	7 **Port Selector, Bit 0** 6 ***Reserved*** Should be Cleared. [5:2] **Byte Enables** All active. [1:0] **Register Address, Bits [11:10]**
3	49h	[7:0] **Register Address, Bits [9:2]**

7.5.2 Register Read Data Packet

Notes: *The PEX 8624 has a default I²C Slave address of 6Fh or 68h (68h is used for computing the values provided in this section), according to whether the I2C_ADDR[2:0] inputs have a value of 111b or 000b, respectively. The actual address is reflected in the **I2C Configuration** register Slave Address field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 294h[6:0]).*

The byte sequence on the I²C Bus, as listed in the following table and figures, occurs after the START and before the STOP bits, by which the I²C Master frames the transfer.

Table 7-9. I²C Register Read Access Example – 1st Cycle

Phase	Value	Description
Address	D1h	**Bits [7:1] for PEX 8624 I²C Slave Address (6Fh or 68h)** Last bit (bit 0) for Read = 1.
Read	ABh	**Byte 3 of Register Read**
	CDh	**Byte 2 of Register Read**
	EFh	**Byte 1 of Register Read**
	01h	**Byte 0 of Register Read**

Figure 7-6. 1st Packet – Command Phase

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address 1101_000b	Read/Write Bit 0 = Write	A

Command Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	STOP
Command Byte 0 0000_0100b	A	Command Byte 1 0000_0010b	A	Command Byte 2 0011_1110b	A	Command Byte 3 1001_1001b	P

Figure 7-7. 2nd Packet – Read Phase

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1] 1101_000b	Read/Write Bit 1 = Read	A

Read Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	STOP
Register Byte 3 1010_1011b	A	Register Byte 2 1100_1101b	A	Register Byte 1 1110_1111b	A	Register Byte 0 0000_0001b	P

Chapter 8 Performance Metrics

8.1 Introduction

This chapter discusses measures of performance, including throughput and latency. It also provides guidelines for programming on-chip registers, to boost performance beyond that provided by the general-purpose default values.

This chapter also differentiates *PCI Express Base r1.1* (Gen 1) rates, 2.5 Giga-Transfers/second (GT/s), from *PCI Express Base r2.0* (Gen 2) rates, 5.0 GT/s, by including "Gen 1" or "Gen 2", as appropriate, after the xWidths (*for example*, "x8 Gen 1" indicates x8 at 2.5 GT/s, and "x8 Gen 2" indicates x8 at 5.0 GT/s).

8.2 Throughput

Throughput measures the amount of Payload bytes transferred per unit time. PCI Express has various possible throughput values, depending upon the Link width, Payload size, traffic distribution, and Transaction Layer Packet (TLP) overhead, all of which are under software control. To comprehend PCI Express throughput, a basic understanding of the underlying PCI Express fundamentals is necessary.

8.2.1 Shared Wire

Bytes are transmitted across PCI Express wires during each symbol time, regardless of traffic load. The bytes are classified into three wire traffic types:

- Transaction Layer Packets (TLPs) that carry Payloads
- Data Link Layer Packets (DLLPs)
- Physical Layer (PHY) Ordered-Sets

Electrical idles (including PADs) are not counted as traffic. To measure throughput and understand how the Link performs, count all three wire traffic types while tracking the amount of time that elapses. PHY SKIP Ordered-Sets occur irregularly and can mostly be ignored. A fully used Link requires 99% TLPs and DLLPs in each direction. The ratio of TLPs to DLLPs depends upon the application.

8.2.2 Unidirectional Throughput

Ideal PCI Express throughput in the unidirectional bandwidth case is illustrated in Figure 8-1 and defined in Table 8-2. Figure 8-4 through Figure 8-6 include each best case with a curve labeled **Calc 0 DLLP/TLP**. Payload size is in bytes (B) for each figure.

Figure 8-1. Ideal PCI Express Throughput in Unidirectional Bandwidth Case

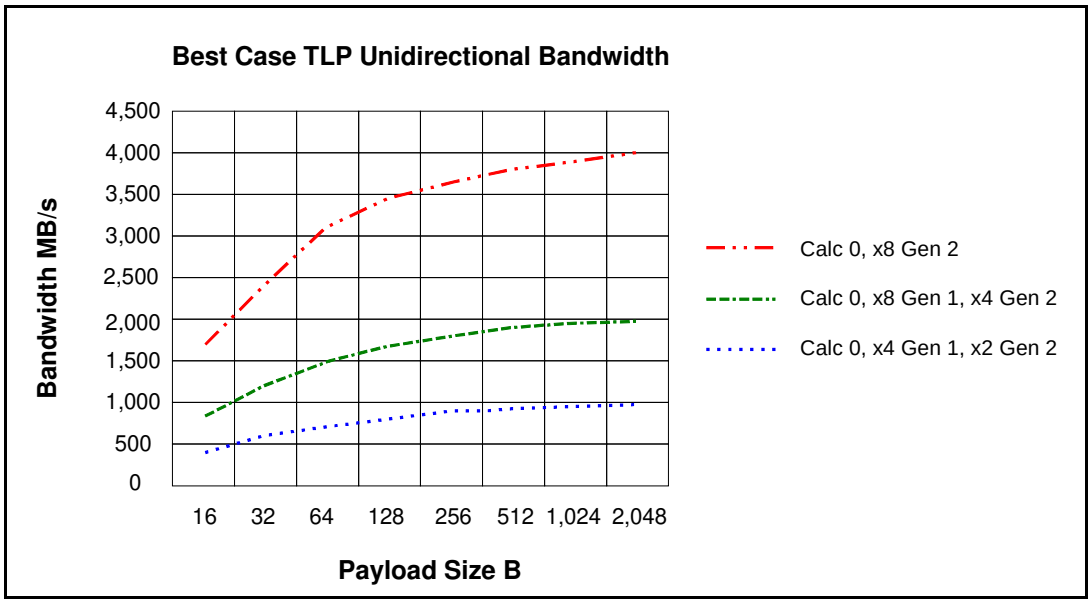


Figure 8-1 illustrates the way in which the maximum throughput increases with larger Payload sizes, and with wider and faster Links. The *PCI Express Base r2.0* allows a default Maximum Payload Size (MPS) of 128 bytes. The PEX 8624, however, supports an MPS of up to 2,048 bytes, to achieve a bandwidth higher than obtainable with the minimum MPS value.

Unidirectional PCI Express throughput has maximal TLPs on the wire going in one direction. The other direction of the bidirectional Link is mostly unused. DLLPs that share the wire (as per the *PCI Express Base r2.0*) are typically transmitted in response to a TLP; therefore, DLLPs travel in the opposite direction of TLPs. Thus, for unidirectional traffic, DLLP traffic does not interfere with TLP bandwidth.

It is useful to make a clarification regarding PCI Express Memory Read (MRd) Requests and their corresponding Completions with Data (CPLD). The *Length* field in the MRd Request can be up to 4 KB. The MRd TLP, however, is only 12 to 20 bytes in length. The Completion for the MRd carries the data. Typically, a Root Complex transmits multiple, partial Completions with 64-byte Payload size (endpoint devices must transmit Completions of at least 128-byte granularity). As a result, even with large Read sizes, the bandwidth expected for the Read is limited by the Completions' data Payload size.

For example, if a series of MRd Requests with large Read sizes are sent upstream, and the Completer sends only Completions with 64-byte Payloads, the maximum bandwidth expected would be close to the unidirectional 64-byte Payload data points in Figure 8-1. (Refer also to Section 8.2.5.)

Table 8-2. Ideal Unidirectional Throughput Numbers (in Gigabytes per Second)

Payload (Bytes)	Calc 0 x8 Gen 2	Calc 0 x8 Gen 1 x4 Gen 2	Calc 0 x4 Gen 1 x2 Gen 2
16	1.771	0.886	0.442
32	2.453	1.226	0.612
64	3.037	1.518	0.757
128	3.447	1.723	0.860
256	3.697	1.848	0.923
512	3.836	1.918	0.958
1,024	3.909	1.955	0.976
2,048	3.947	1.973	0.986

8.2.3 Ideal PCI Express Throughput

This section discusses how to calculate ideal PCI Express throughput, as explained in Section 8.2.2. PEX 8624 signaling operates at 2.5 GT/s/Lane (Gen 1) and 5.0 GT/s/Lane (Gen 2). The PEX 8624 allows Lanes to be grouped into x1, x2, x4, and x8 widths. This bandwidth is de-rated, according to the factors described within this section.

PCI Express protocol has built-in 8b/10b encoding, which immediately removes 20% of the throughput:

$$8b/10b\_encoding\_hit = 8/10 = 0.8$$

TLPs include overhead as part of the PCI Express protocol. Each TLP includes a Header of 12 to 16 bytes (16 bytes only for 64-bit addressing; otherwise, TLPs all include 12-byte Headers). TLPs can also have an optional End-to-end Cyclic Redundancy Check (ECRC) of 4 bytes. All TLPs require a Data Link Layer (DLL) and PHY framing symbol overhead of 8 bytes. The total TLP overhead is as follows:

$$TLP\_overhead\_min = 12 + 8 = 20 \text{ bytes}$$

$$TLP\_overhead\_max = 16 + 4 + 8 = 28 \text{ bytes}$$

Figure 8-2 illustrates a TLP with a 32-byte Data Payload, with 20 bytes of overhead.

Figure 8-2. TLP Packet Structure with 20 Bytes of Overhead and 32 Bytes of Data Payload

STP	SEQ	SEQ	HDR
HDR	HDR	HDR	HDR
HDR	HDR	HDR	ADDR
ADDR	ADDR	ADDR	DATA
DATA	DATA	DATA	DATA
DATA	DATA	DATA	DATA
DATA	DATA	DATA	DATA
DATA	DATA	DATA	DATA
DATA	DATA	DATA	DATA
DATA	DATA	DATA	DATA
DATA	DATA	DATA	DATA
DATA	DATA	DATA	CRC
CRC	CRC	CRC	END

The *PCI Express Base r2.0* requires that DLLPs and SKIP Ordered-Sets share the same wire as TLPs, allowing these other traffic sources to reduce TLP throughput. The best case with the least impact (reduction to TLP bandwidth corresponding to unidirectional traffic scenarios) can be calculated.

To cover lossy Link behavior, the *PCI Express Base r2.0* requires an Acknowledge Control Packet (ACK) and all three types of UpdateFC to be transmitted every 30 s. Each DLLP takes 8 bytes. Figure 8-3 illustrates the DLLP Packet structure. On a x8 Link, a DLLP takes one full symbol time. Therefore, 4 DLLPs cost 4 symbol times every 7,500 symbol times. This hit is much less than 1%. To be complete, however, the throughput decrease from DLLPs in unidirectional Gen 1 traffic is as follows:

DLLP_x8_unidirectional_derating = 7,500/7,504 symbol times

DLLP_x4_unidirectional_derating = 7,500/7,508 symbol times

Figure 8-3. DLLP Packet Structure (8 Bytes)

SDP	DLLP	DLLP	DLLP
DLLP	CRC	CRC	END

A SKIP Ordered-Set can be modeled as occurring once per 1,180 symbol times. The *PCI Express Base r2.0* provides a range of 1,180 to 1,538 symbol times, and the value used by the PEX 8624 is once every 1,180 symbol times. A SKIP Ordered-Set requires 4 symbol times to transmit. Therefore, throughput is decreased by:

SKIP_derating = (1,180 / 1,184)

Placing together all the overhead and throughput de-rating, the ideal PCI Express unidirectional bandwidth can be calculated for any Payload, as follows:

Ideal_pcie_bandwidth = link_rate x 8b/10b_encoding_hit x dllp_derating x skip_derating
x (Payload / (Payload + tlp_overhead))

The above formula, using tlp_overhead_min (for the tlp_overhead variable) and appropriate Link rate, was used to calculate the values for the ideal curves illustrated earlier, in Figure 8-1.

8.2.4 Bidirectional PCI Express Throughput

Although unidirectional flows have virtually no DLLP traffic flowing in the same direction as the TLP, to model bidirectional traffic, DLLPs require prominent consideration. Three different calculated DLLP rates provide a useful reference – 0, 1, and 2 DLLPs per TLP (DLLP/TLP).

The worst case, 2 DLLP/TLP, applies wherein every TLP causes an ACK and UpdateFC DLLP. The ACK acknowledges the TLP arrived and the UpdateFC provides additional credits, allowing additional TLPs of the same type to be transmitted.

Note: *Worst case is approximate. There can be an additional UpdateFC time every 7,500 symbol times.*

The best case, 0 DLLP/TLP, is the unidirectional traffic case, because no DLLPs travel in the same direction as the TLP flow.

Table 8-3 summarizes the amount of Link bandwidth used by the Payload, for various DLLP policies and Payload sizes when using TLPs with the minimum overhead of 20 bytes (32-bit addressing and no ECRC). The values calculated used the following formula:

(data payload bytes / (data payload bytes + overhead bytes + DLLP bytes)) x SKIP_derating x 100%

Table 8-3. TLP Data Payload Percent of Link Bandwidth Used for Different DLLP Rates[a]

Payload (Bytes)	0 DLLP/TLP (Ideal) (Percent)	1 DLLP/TLP (Percent)	2 DLLP/TLP (Percent)
0	0.00	0.00	0.00
4	16.61	12.45	9.96
8	28.47	22.14	18.12
16	44.28	36.23	30.66
32	61.31	53.14	46.89
64	75.91	69.31	63.77
128	86.17	81.75	77.76
256	92.42	89.81	87.35
512	95.89	94.47	93.09
1,024	97.73	96.98	96.25
2,048	98.67	98.29	97.92

a. The SKIP_derating factor used was (1,100 / 1,104).

It is expected that in any traffic pattern, a maximally and optimally used Links' throughput will operate in the range of 0, 1, or 2 DLLP/TLP. Because DLLP and TLP Counts are easily measured with standard PCI Express logic analyzers, understanding the DLLP-to-TLP ratio aids in understanding PCI Express Link behavior. If the DLLP Count is more than 2x the TLP Count, the Link is probably underused.

The exact ratio of DLLPs to TLPs depends upon a variety of factors, which to some extent remain outside the *PCI Express Base r2.0* guidelines. Figure 8-4 through Figure 8-6 illustrate the measured PEX 8624 bidirectional throughput, with default register values for their listed Link widths. Table 8-4 through Table 8-6 provide the numbers plotted in Figure 8-4 through Figure 8-6. As a reference, each figure/graph contains throughput curves for three DLLP policies – 0, 1, or 2 DLLP/TLP. The unidirectional and bidirectional curves are the measured performance points of the PEX 8624 when sustained back-to-back TLPs of the same size are indefinitely transferred between any two Ports with the same width.

As illustrated in these graphs and tables (Figure 8-4 through Figure 8-6 and Table 8-4 through Table 8-6), the PEX 8624 unidirectional cases track along the ideal 0 DLLP/TLP curve, for all values, 16 to 2,048 bytes. The bidirectional cases make the PEX 8624 work, because they must process ACKs, UpdateFCs, and TLP traffic, in both directions.

With default values, the PEX 8624 is able to run bidirectional traffic at better (in some cases, significantly better) than 1 DLLP/TLP rates for Payload sizes of 16 to 256 bytes, and maintain better than 2 DLLP/TLP throughput up to 2,048 bytes for x8 Gen 2. For larger Payload sizes, adding additional Payload credits, by tuning the default register values, yields increased throughput. Adjusting the credit values, and the factors/impact of doing so, are discussed in more detail in Section 8.4.

Tuning can improve performance, to a point. The PEX 8624 cannot simultaneously sustain 2,048-byte Payloads on all Ports, due to the amount of on-chip buffering available to maintain a Payload of that size, as illustrated in Figure 8-5. Realistically, it is unlikely to have heavily loaded traffic patterns with 2,048-byte Payloads traveling in both directions.

By default, for all Link widths, the PEX 8624 operates at better than 1 DLLP/TLP for Payload sizes of 32 to 256 bytes. For larger Payload sizes, the default register values require fine-tuning, to allow for improved throughput. Section 8.3 discusses tuning and consideration factors in further detail.

Figure 8-4. Measured Bidirectional Throughput TLP x8 Gen 2 Payload Bandwidth

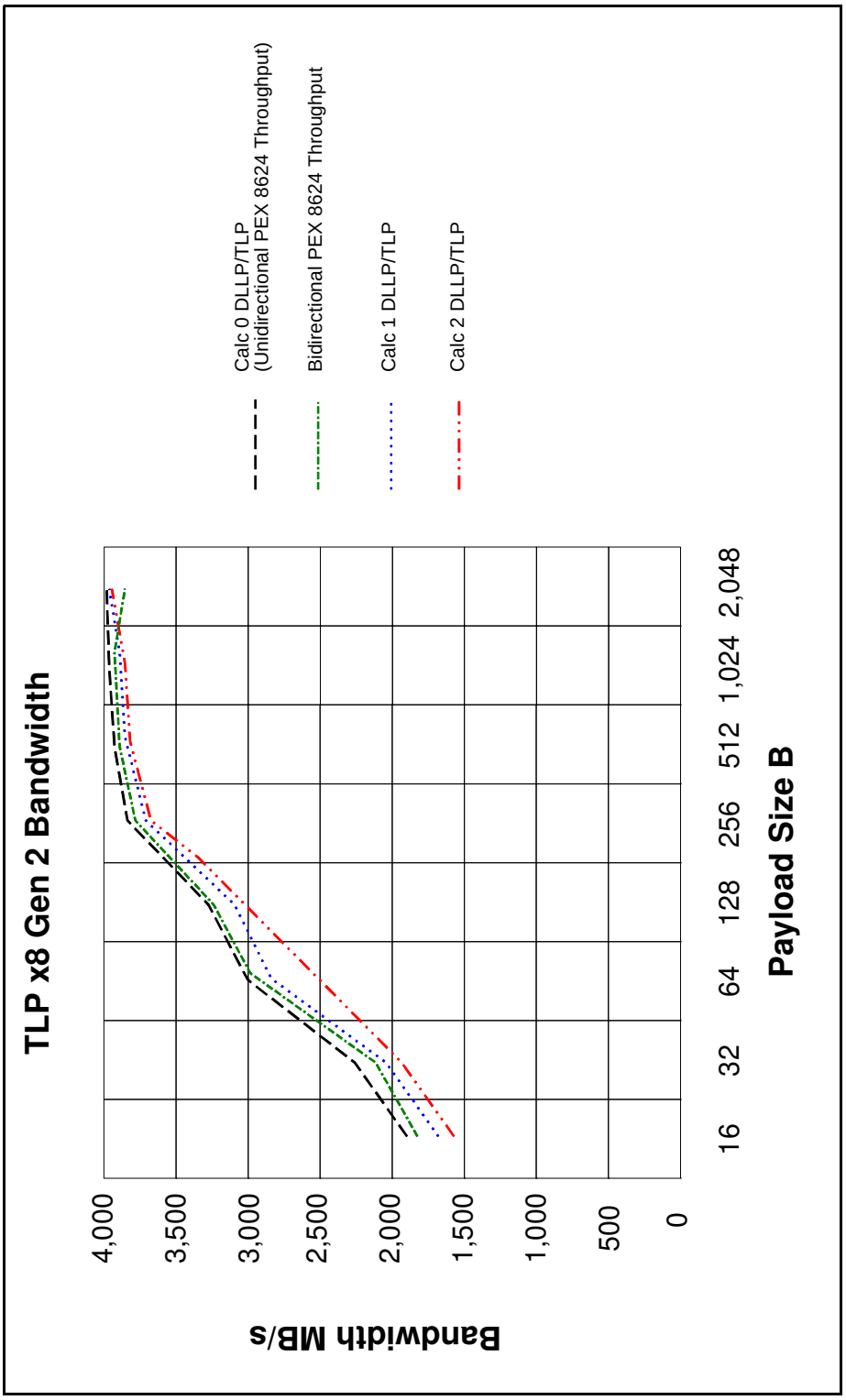


Table 8-4. x8 Gen 2 Throughput Numbers (in Gigabytes per Second)

Payload (Bytes)	x8 Gen 2 Calculated Throughput for Unidirectional and Bidirectional with Calc 0 DLLP/TLP	x8 Gen 2 Calculated Throughput for Bidirectional with Calc 1 DLLP/TLP	x8 Gen 2 Calculated Throughput for Bidirectional with Calc 2 DLLP/TLP	x8 Gen 21 PEX 8624 Throughput for Bidirectional with Default DLLP/TLP Settings/Behavior
16	1.771	1.449	1.226	1.590
32	2.453	2.126	1.876	2.372
64	3.037	2.772	2.551	2.998
128	3.447	3.270	3.111	3.409
256	3.697	3.593	3.494	3.662
512	3.836	3.779	3.724	3.808
1,024	3.909	3.879	3.850	3.881
2,048	3.947	3.932	3.917	3.772

Figure 8-5. Measured Bidirectional Throughput TLP x8 Gen 1 or x4 Gen 2 Payload Bandwidth

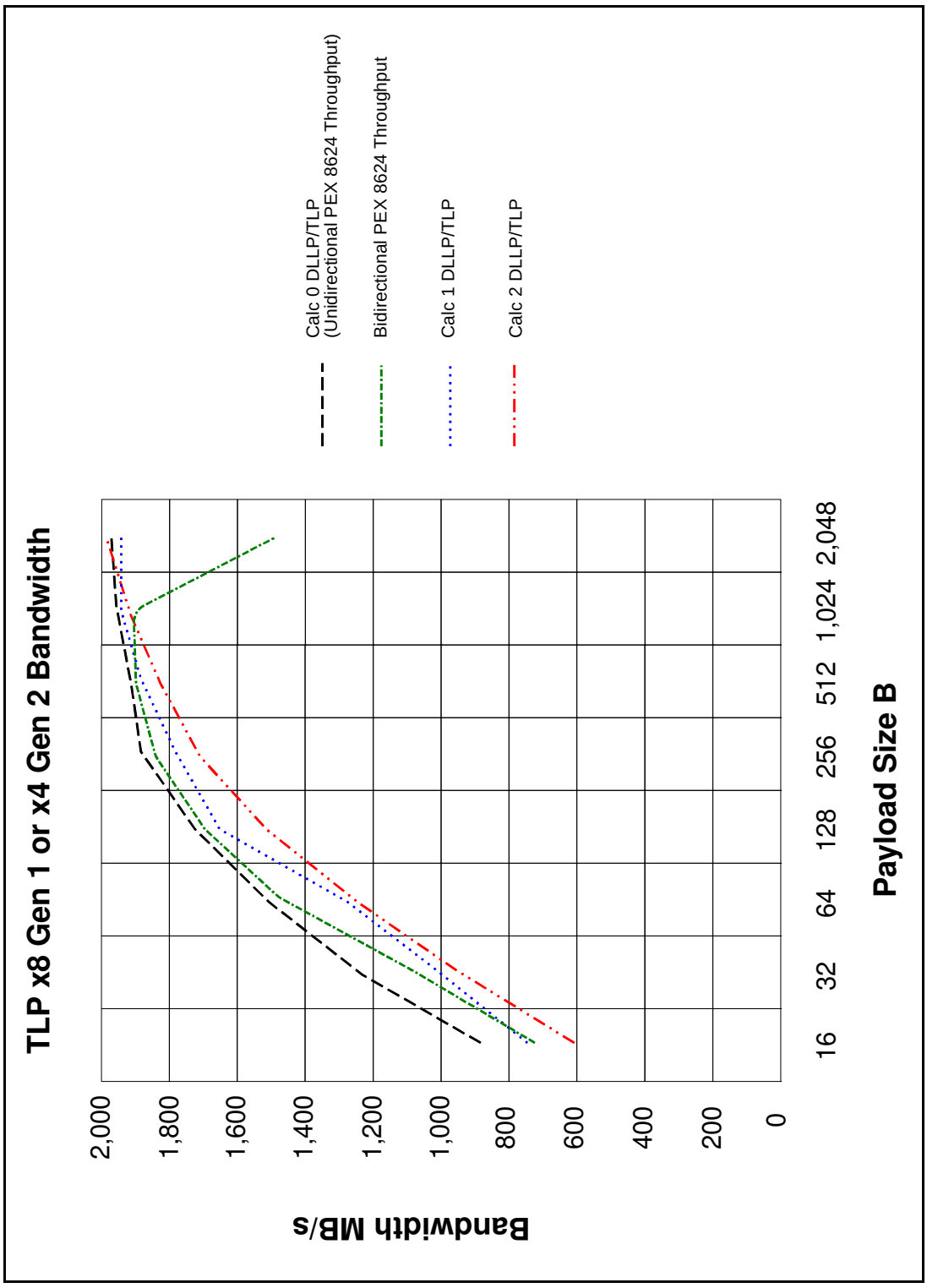


Table 8-5. x8 Gen 1 or x4 Gen 2 Throughput Numbers (in Gigabytes per Second)

Payload (Bytes)	x8 Gen 1 or x4 Gen 2 Calculated Throughput for Unidirectional and Bidirectional with Calc 0 DLLP/TLP	x8 Gen 1 or x4 Gen 2 Calculated Throughput for Bidirectional with Calc 1 DLLP/TLP	x8 Gen 1 or x4 Gen 2 Calculated Throughput for Bidirectional with Calc 2 DLLP/TLP	x8 Gen 1 or x4 Gen 2 PEX 8624 Throughput for Bidirectional with Default DLLP/TLP Settings/Behavior
16	0.886	0.725	0.613	0.716
32	1.226	1.063	0.938	1.125
64	1.518	1.386	1.275	1.486
128	1.723	1.635	1.555	1.692
256	1.848	1.796	1.747	1.822
512	1.918	1.889	1.862	1.894
1,024	1.955	1.940	1.925	1.924
2,048	1.973	1.966	1.985[a]	1.446

a. *The value for this particular entry (as it appears in the table and figure) is incorrect, and will be corrected in a future release.*

Figure 8-6. Measured Bidirectional Throughput TLP x4 Gen 1 or x2 Gen 2 Payload Bandwidth

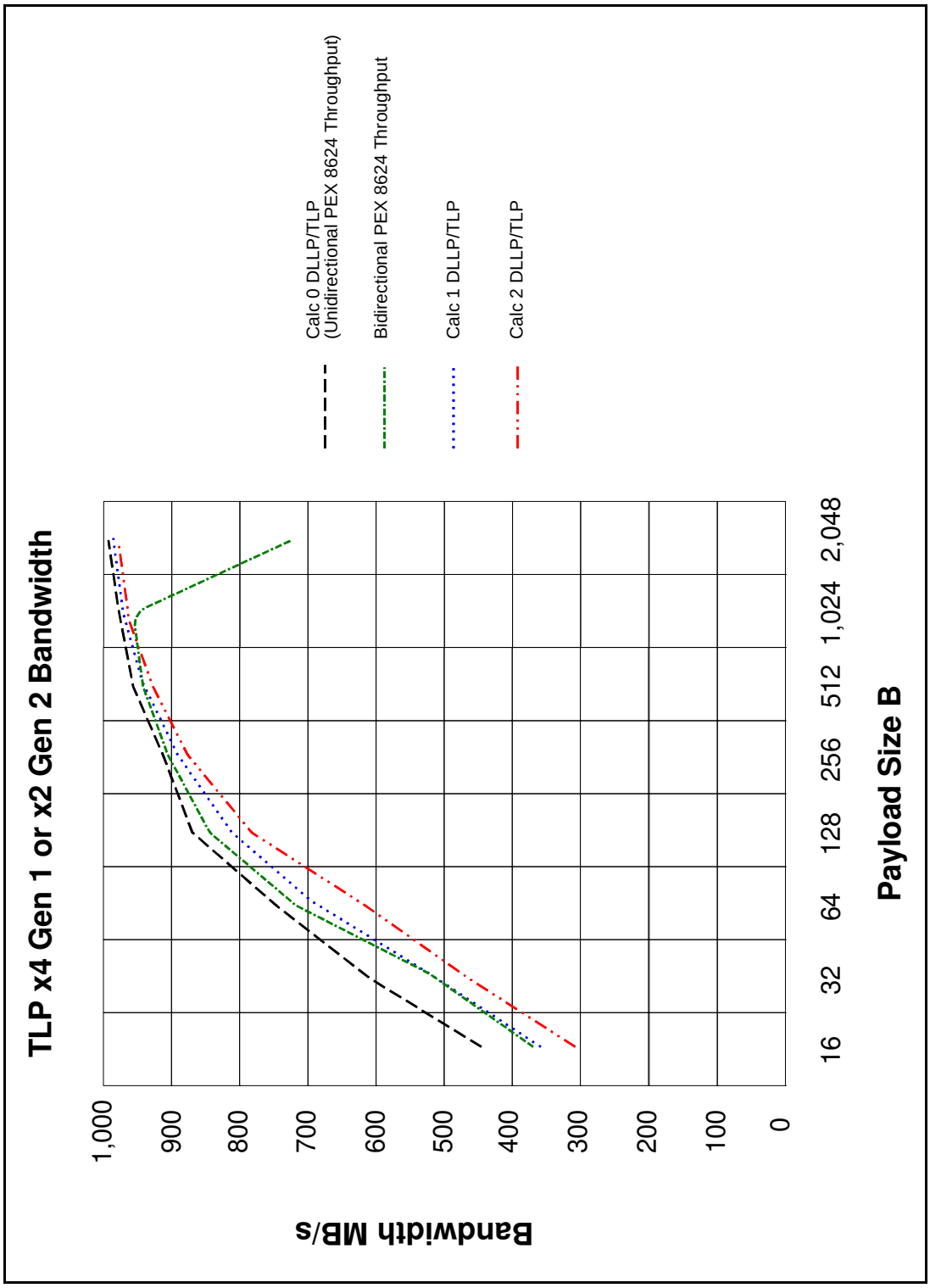


Table 8-6. x4 Gen 1 or x2 Gen 2 Throughput Numbers (in Gigabytes per Second)

Payload (Bytes)	x4 Gen 1 or x2 Gen 2 Calculated Throughput for Unidirectional and Bidirectional with Calc 0 DLLP/TLP	x4 Gen 1 or x2 Gen 2 Calculated Throughput for Bidirectional with Calc 1 DLLP/TLP	x4 Gen 1 or x2 Gen 2 Calculated Throughput for Bidirectional with Calc 2 DLLP/TLP	x4 Gen 1 or x2 Gen 2 PEX 8624 Throughput for Bidirectional with Default DLLP/TLP Settings/Behavior
16	0.442	0.362	0.307	0.376
32	0.612	0.532	0.469	0.532
64	0.757	0.693	0.638	0.737
128	0.860	0.818	0.778	0.843
256	0.923	0.898	0.874	0.909
512	0.958	0.945	0.931	0.945
1,024	0.976	0.970	0.963	0.957
2,048	0.986	0.983	0.979	0.732

8.2.5 Read Completion Throughput

Read Completion throughput is illustrated in Figure 8-7, with the values listed in Table 8-7. For the calculated curves Calc 0 and Calc 2, note the following:

- Read Completion Payload size matches the Read Request size
- Read throughput does not include time to forward the Read Request

Figure 8-7. Measured Read Completion Throughput x8 Gen 2 Bandwidth

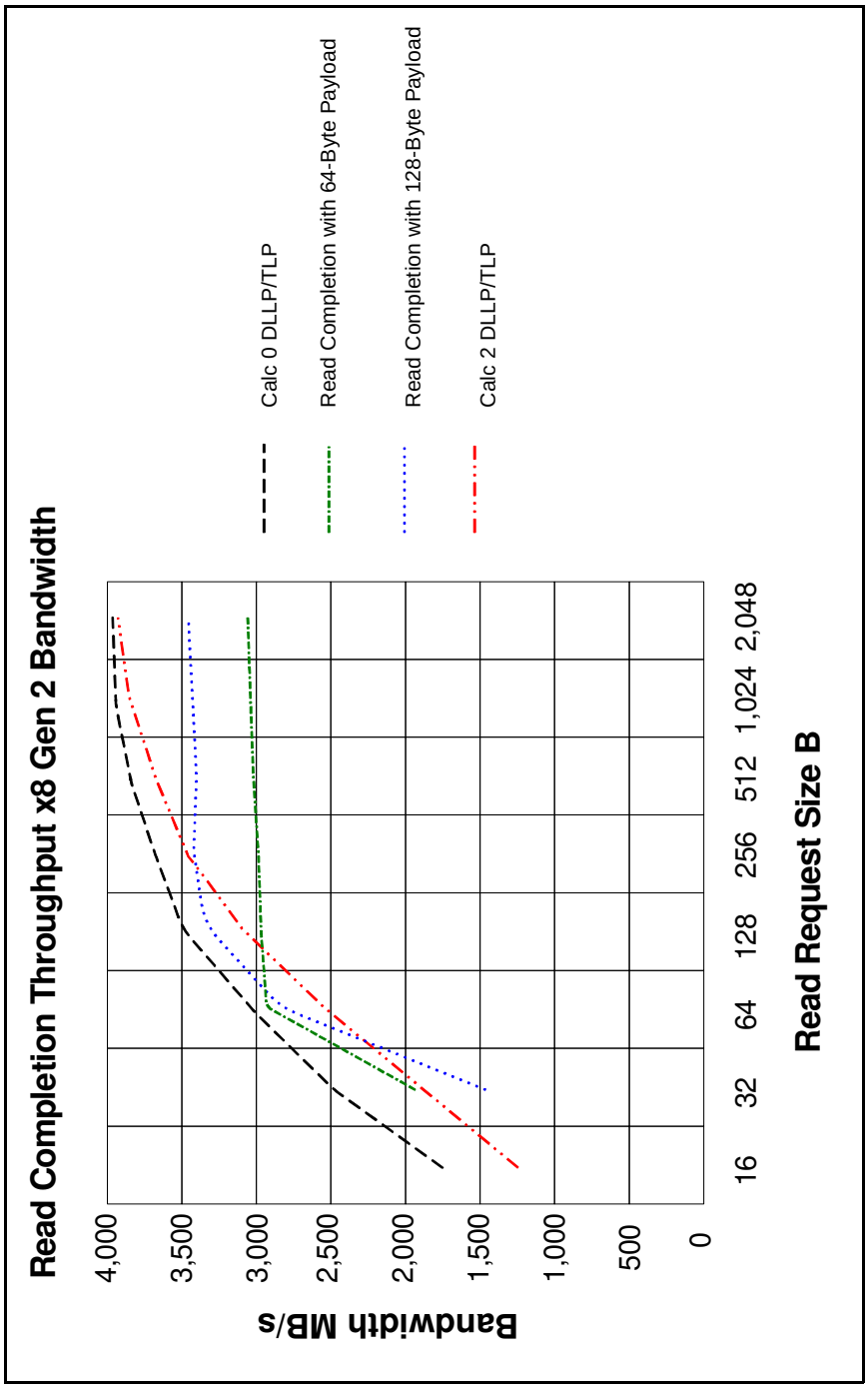


Table 8-7. Measured x8 Gen 2 Read Completion Throughput (in Gigabytes per Second)

Read Request Transfer Size (Bytes)	x8 Gen 2 Calculated Throughput for Calc 0 DLLP/TLP	x8 Gen 2 Calculated Throughput for Calc 2 DLLP/TLP	x8 Gen 2 PEX 8624 Read Throughput When Receiving Completions Containing 64-Byte Payloads with Default Settings/Behavior	x8 Gen 2 PEX 8624 Read Throughput When Receiving Completions Containing 128-Byte Payloads with Default Settings/Behavior
16	1.7715	1.2265	–	–
32	2.4525	1.8755	1.9445	1.9705
64	3.0365	2.5505	2.9350	2.8635
128	3.4470	3.1105	2.9810	3.3795
256	3.6965	3.4940	2.9910	3.4040
512	3.8355	3.7235	3.0020	3.4030
1,024	3.9090	3.8500	3.0040	3.4080
2,048	3.9470	3.9165	3.0060	3.4150

8.3 DLLP Policies

As previously discussed, DLLP rates can vary from 0 to 2 or more DLLPs/TLP. The PEX 8624 allows programming to affect the DLLP rate. Figure 8-4 through Figure 8-6 illustrate that an increase in DLLPs reduces the total TLP throughput. Therefore, for designs that require high performance, minimize DLLP rates. Transmitting fewer DLLPs, however, can result in credit starvation or Replay buffer overfill, which can have a detrimental effect on TLP bandwidth. Care must be taken when changing the default PEX 8624 DLLP transmission rate.

Typically, TLPs have higher transmission priority on the wire than DLLPs. The PEX 8624, however, allows DLLPs to have higher priority under certain conditions, meaning that DLLPs can transmit before starting a new TLP. The decision to transmit a DLLP ahead of a TLP is referred to as *DLLP policy.*

The PEX 8624 can be programmed to alter its default DLLP policies, to emphasize improved TLP throughput, faster acknowledgement, more credit, or simplest behavior. Default policies work for most applications. Choices for a DLLP policy, however, allow for further optimization.

8.3.1 ACK DLLP Policy

An *ACK DLLP* is a response indicating to the TLP Transmitter that the Receiver received a "good" copy of the TLP, meaning that it acknowledged the receipt of the TLP. The simplest policy is to send 1 ACK for every received TLP, resulting in a 1 DLLP/TLP rate for ACK alone. What an ACK means to the TLP Transmitter is that the TLP Transmitter can remove any stored copy of that TLP, because it is unnecessary to resend the TLP. ACK DLLPs can be combined, so that one ACK DLLP can serve to acknowledge multiple TLPs. This collapsing of ACKs is the basis of the ACK DLLP policy choices. Less-frequent, more-collapsed ACKs have the least impact on TLP transmit bandwidth, meaning that less-frequent ACKs result in less than 1 DLLP/TLP.

The PEX 8624 ACK policy consists of two parts – a Timer and TLP Counter. The default ACK Timer policy/value varies according to the negotiated Gen 1 or Gen 2 mode Link width and MPS, as recommended in the *PCI Express Base r1.1* or *PCI Express Base r2.0*, respectively. Table 8-8 defines some of the possible default values, in symbol times.

Table 8-8. Sample ACK Latency Timer Values

Maximum Payload Size (Bytes)	x4 Gen 2 (Symbol Times)	x8 Gen 2 (Symbol Times)
128	124	118
256	169	158
512	205	137

The ACK Transmission Latency Timer loads the appropriate value when a TLP is received and known to be good, meaning a few clocks after the END framing symbol is received. The Timer counts down each symbol time (every 4 ns (*PCI Express Base r1.1*) or 2 ns (*PCI Express Base r2.0*)). When the Timer reaches 0, an ACK DLLP takes higher priority over new TLPs (*that is*, an ACK DLLP is transmitted before a new TLP is started). The ACK DLLP transmitted acknowledges all TLPs, up to the most recently arrived good TLP.

The default value for the TLP Counter is 16, meaning a high-priority ACK is scheduled upon the arrival of 16 TLPs. The **Ingress Control Shadow** register *ACK TLP Counter Timeout* field (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 664h[10:9]) value controls the ACK TLP Counter, as follows:

- 00b – Allows 16 TLPs before a high-priority ACK (default)
- 01b – Allows 8 TLPs before a high-priority ACK
- 10b – Allows 4 TLPs before a high-priority ACK
- 11b – Disables the Counter

Either the Timer or Counter mechanism can cause a high-priority ACK DLLP to be scheduled. The time for 16 TLPs can be less than the ACK Timer above, in which case an ACK is sent earlier. The TLP Counter is useful for any system with a large programmed MPS (resulting in a large timer value), that can send short TLPs, *such as* 12-byte Memory Reads. Rather than require the Transmitter to save possibly 100+ small TLPs, it need only save 16, plus whatever else arrives in the round-trip time.

If there is no TLP traffic being transmitted (*that is*, the Transmit Link is idle), an ACK DLLP can be transmitted before the Timer expires. This is an opportunistic low-priority ACK. When an ACK is transmitted, both the Timer and Counter reset, waiting for a new TLP to arrive to begin counting again.

The PEX 8624 allows a programmable override of the default Ack_Latency_Timer value, on a per Port basis, by programming the **ACK Transmission Latency Limit** register *ACK Transmission Latency Limit* field (offset 1F8h[11:0]). The value in this register is loaded when a new TLP arrives and a high-priority ACK DLLP is attempted when the Timer reaches 0. For fastest ACK response, this Timer can be programmed to 000h, resulting in one DLLP ACK transmitted immediately per each TLP received. For less impact on Transmit TLP bandwidth, a larger value can be programmed, resulting in less-frequent ACKs.

In general, a slower ACK response does not impact the Receive TLP stream, and aids the TLP Transmit stream. Every PCI Express device contains storage (Retry buffer) for storing TLPs while waiting for ACKs. The amount of Retry buffer storage a device contains is vendor-dependent. The number of TLPs the PEX 8624 can store depends upon the type and size of TLPs received. (Refer to Section 8.4.) The PEX 8624 holds TLPs in the Retry buffer while waiting for an ACK. At some point, if the Retry buffer storage fills, then no new TLPs can be sent until a new received ACK frees up space. In this case, the ACK can become a performance bottleneck.

8.3.2 UpdateFC DLLP Policy

An *UpdateFC DLLP* is transmitted in response to a received TLP. The UpdateFC DLLP replenishes the connected device with additional credit, to allow the Transmitter to transmit more TLPs of that type. Each TLP that arrives consumes credit, and eventually, a stream of TLPs consume all the available credit, unless an UpdateFC DLLP provides additional credit. However, if the connected device has sufficient credit to transmit more TLPs, it is not necessary to transmit UpdateFC DLLPs to it. The UpdateFC policy determines how and when to transmit an UpdateFC DLLP.

There are two parts to the UpdateFC policy – frequency of transmitting the updates and credit amount. This section discusses only the frequency. Refer to Section 8.4 for details regarding credit amounts.

If the PEX 8624 is not transmitting TLPs (*that is*, the Transmit Link is idle), and credit to replenish the credit used becomes available, the PEX 8624 immediately transmits an UpdateFC DLLP to the connected device. This is an opportunistic, low-priority UpdateFC DLLP.

However, if the PEX 8624 is busy transmitting TLPs to the connected device, the switch does not transmit an UpdateFC DLLP until a programmed threshold is crossed. The PEX 8624 provides four threshold options – 100%, 75% (default), 50%, and 25%. Whenever the remaining credit drops below the programmed threshold, an UpdateFC DLLP is given high priority, meaning that the UpdateFC DLLP is transmitted before a new TLP is started. There is a separate threshold for Header and Payload credits, for each TLP type – Posted, Non-Posted, and Completion – for each Port in the Station, located in the **Ingress Credit Handler (INCH) Threshold** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets A00h through A38h).

Note: *A Station is an internal grouping of up to eight SerDes Lanes that are bound together. For the PEX 8624, there can be at most two Ports per Station. There can, however, be as few as one Port per Station.*

The example of UpdateFC options (provided in Table 8-9) chart how, for the various options, an UpdateFC is triggered. This example is for a traffic stream of six back-to-back, 256-byte Posted TLPs, using a x4 Port, where the maximum Posted Header credit is 25 and the maximum Posted Payload credit is 128. A 256-byte Payload requires 16 credits (1 credit per 16 bytes). Therefore, each TLP in this case consumes 1 Header and 16 Payload credits.

Once a high-priority UpdateFC is triggered, if there are sufficient on-chip resources to do so, the running credit deficit is fully restored. For most non-congested applications, it is likely that ample chip resources will exist, to fully restore credit with every UpdateFC. However, if resources are running low, only a portion of the running credit is restored. If the threshold for transmitting an UpdateFC remains crossed, then, as more resources become available, a subsequent DLLP is transmitted until the deficit is satisfied.

Selecting the 100% policy results in a high-priority UpdateFC for every TLP received. By itself, this policy results in 1 DLLP/TLP, without factoring in the ACK policy. The 75% policy triggers 1 DLLP for every 2 TLPs for this traffic load, which results in 0.5 DLLP/TLP without the ACK. The 50% policy results in 0.25 DLLP/TLP, and the 25% policy results in 0.16 DLLP/TLP.

Table 8-9. Example UpdateFC Options

TLP Received	Running Credit Header, Payload Consumed/Total	25% Remains Triggers when 6 Header or 32 Payload Credits Remain	50% Remains Triggers when 12 Header or 64 Payload Credits Remain	75% Remains Triggers when 18 Header or 96 Payload Credits Remain	Less than 100% Remains Update ASAP
TLP0	24/25, 112/128	–	–	–	UpdateFC
TLP1	23/25, 96/128	–	–	UpdateFC	UpdateFC
TLP2	22/25, 80/128	–	–	UpdateFC	UpdateFC
TLP3	21/25, 64/128	–	UpdateFC	UpdateFC	UpdateFC
TLP4	20/25, 48/128	–	UpdateFC	UpdateFC	UpdateFC
TLP5	19/25, 32/128	UpdateFC	UpdateFC	UpdateFC	UpdateFC

8.3.3 Unidirectional DLLP Policies

For unidirectional traffic, the PEX 8624 DLLP policies allow the most-frequent DLLPs, because DLLPs do not interfere with TLPs. (DLLPs flow in the opposite direction of TLPs.)

The PEX 8624 can transmit a DLLP ACK almost immediately upon receiving and verifying a TLP. A faster ACK results in fast Transmitter de-allocation of the TLP, and can therefore allow a shallow TLP Replay buffer. The default values can be overwritten, to increase or decrease the ACK DLLP rate. For unidirectional traffic, a small number, *such as* 1, is recommended.

The number programmed into the **ACK Transmission Latency Limit** register *ACK Transmission Latency Limit* field (offset 1F8h[11:0]) sets the ACK Transmission Latency Timer, to count the number of symbol times after receiving a TLP, before transmitting an ACK.

Similar to the ACK programmability, the PEX 8624 can immediately transmit an UpdateFC after receiving only the TLP Header. By transmitting an UpdateFC earlier, the total credit advertised can be minimized. For large Payloads (*such as* 1,024 and 2,048 bytes), reserve PEX 8624 resources only as necessary. By programming fewer credits and having a fast UpdateFC policy, the system does not run out of credits and the PEX 8624 does not waste Buffer space on reservations that do not arrive. The following are the recommended settings:

- Set the UpdateFC policy for unidirectional traffic to 100%
- Set the credits to be sufficient to allow 3 to 4 TLPs

8.4 Ingress Resources

The PEX 8624 includes two types of on-chip RAM – Header RAM and Payload RAM. Each Station partitions its Header RAM into 256 Header credits and Payload RAM into 2,048 Payload credits. By design, the PEX 8624 reserves 12 Header credits and 32 Payload credits for various operational cases.

The STRAP_STN*x*_PORTCFG*x* inputs configure the quantity of enabled Ports in each Station, and the Link width of each Port. At initialization, the PEX 8624 optimally assigns the credits, based upon the selected Port configuration.

Header RAM stores TLP Headers, meaning that every Header credit advertised reserves one Header RAM location, and every TLP on the PEX 8624 uses one Header RAM location. There are 244 Header RAM entries available, per Station.

Payload RAM stores TLP Payload. Payload credit is in units of 16 bytes. Of the 2,016 user-configurable entries, 4 credits must be allocated for each Posted and Completion Header credit advertised. These credits are used internally, for linking Posted and Completion TLP Payload to their respective Header.

Every Port receives and transmits the following three traffic types (packets):

- Posted (P)
- Non-Posted (NP)
- Completions (Cpl)

All three traffic types need credit, for each Port. The **INCH Threshold** register bit fields (refer to Table 8-13) allocate the credit to be reserved (and advertised) for each Port and traffic type. Once allocated, the credits remain dedicated to each Port and traffic type.

As TLPs arrive, they are stored on the PEX 8624, until an ACK is received from the final destination. Until the ACK is received, each TLP stored consumes credit, and continues to occupy RAM until released. The RAM/credit is released only after the Receiver has acknowledged to the sender the arrival of the TLP, without any errors per ACK/Negative Acknowledge (NAK) policy. The total number of TLPs stored, but not yet forwarded to, and acknowledged by, the next PCI Express device, depends upon congestion and the ACK policy of the next PCI Express device.

There are trade-offs between the number of credits allocated for a particular traffic type and Port combination, perhaps more for one system configuration than another. To alleviate these trade-offs, the PEX 8624 contains an innovative Dynamic Buffering design that allows a programmable-sized portion of the RAM to store any of the three traffic-type TLPs from any Port associated with that Station. The credits that remain after allocating credits for each of the three traffic types, for each Port, become part of a *Dynamic buffer*. The Dynamic buffer is essentially a common pool of credits, and is discussed in detail in Section 8.4.2 and Section 8.4.3.

The PEX 8624 default credit allocation values, which create a sizeable Dynamic buffer for each of the possible Port configurations, are optimal for most applications. Detailed tables of the default initial credit allocation for all three TLP types, and an explanation of the common credit pool, are addressed in the following sections.

8.4.1 Initial Credit Allocation

The PEX 8624 default credit allocation values depend upon the strapped Link width, not the negotiated Link width. The initial credit values that the Initialization Flow Control (InitFC) DLLP advertises on a per-Port basis, which the PEX 8624 transmits after Linkup, are listed in Table 8-10 (in credits) and Table 8-11 (in bytes).

The amount of credit that a Port initially advertises is controlled by the **INCH Threshold** register field Settings (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets A00h through A38h). (Refer to Section 8.4.3.) The default value of these registers changes, depending upon the STRAP_STN*x*_PORTCFG*x* input levels. In some cases, the Dynamic Buffer will allocate one to two additional initial Payload credits out of the common pool. If this occurs, the Port will advertise this additional initial credit.

Table 8-10. Initial Credit Allocation in Credits (*where* 1 Header credit means storage is available for all Header bytes and 1 Payload Credit = 16 bytes)

Port Configuration	Posted Header/Payload	Non-Posted Header/Payload	Completion Header/Payload
Upstream Port			
x8	32/128	22/infinite	32/144
x4	16/128	12/infinite	18/128
Downstream Ports			
x8	46/144	29/infinite	22/128
x4	25/128	16/infinite	12/128

Table 8-11. Initial Credit Allocation in Credits for Header (*where* 1 Header credit means that storage is available for all Header bytes; Payload credits are listed in bytes)

Port Configuration	Posted Header/Payload	Non-Posted Header/Payload	Completion Header/Payload
Upstream Port			
	64/2,048	32/infinite	64/4,096
x8	32/2,048	22/infinite	32/2,304
Downstream Ports			
	88/4,352	55/infinite	32/2,048
x8	46/2,304	29/infinite	22/2,048

8.4.2 Dynamic Buffering

The PEX 8624 default credit values are optimal for most applications, to maintain back-to-back TLP traffic indefinitely, without running out of credit. After any of the initial credit (storage space) is used, more resources are automatically made available from the Dynamic buffer, to maintain the initial credit allotment. These additional resources are not reserved ahead of time. Therefore, they can be used for any of the three TLP types – Posted, Non-Posted, or Completion (P, NP, or Cpl, respectively). Because the TLP type is not pre-specified, these extra resources are termed a *common credit pool*.

When credit is actually replenished depends upon the UpdateFC DLLP policy (refer to Section 8.3.2), which is controlled by Setting the **INCH Threshold** register *UpdateFC High-Priority Threshold* fields (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets A00h through A38h[19:18, 17:16], as appropriate). These thresholds are relative to the initial credits allocated to a Port. Common Pool credits that are allocated to a Port before a high-priority UpdateFC DLLP is sent can be de-allocated if the Port's initial credits are restored before the UpdateFC DLLP is sent.

The common credit pool for Header and Payload credit is as follows:

- **Common Header pool** – What remains after subtracting the advertised Header credits for each of the three TLP types, for each Port in the Station, from the configurable Header RAM space. Figure 8-8 illustrates the way in which the PEX 8624 Header RAM is partitioned (by default) for an upstream x8 Port.
- **Common Payload pool (Common Payload/Completion pool)** – What remains after subtracting the following from the Payload RAM:
  - 4 credits for each Posted and Completion Header Credit advertised, for each Port in the Station
  - Posted (Payload) credits advertised for each Port in the Station
  - Completion credits advertised for each Port in the Station

  Figure 8-9 illustrates the way in which the PEX 8624 Payload (and Completion) RAM is partitioned (by default) for an upstream x8 Port.

Figure 8-8. Upstream x8 Default Configuration of Header RAM (256 Total Credits)

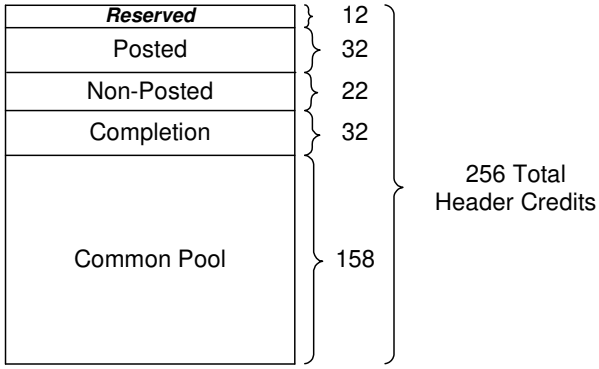
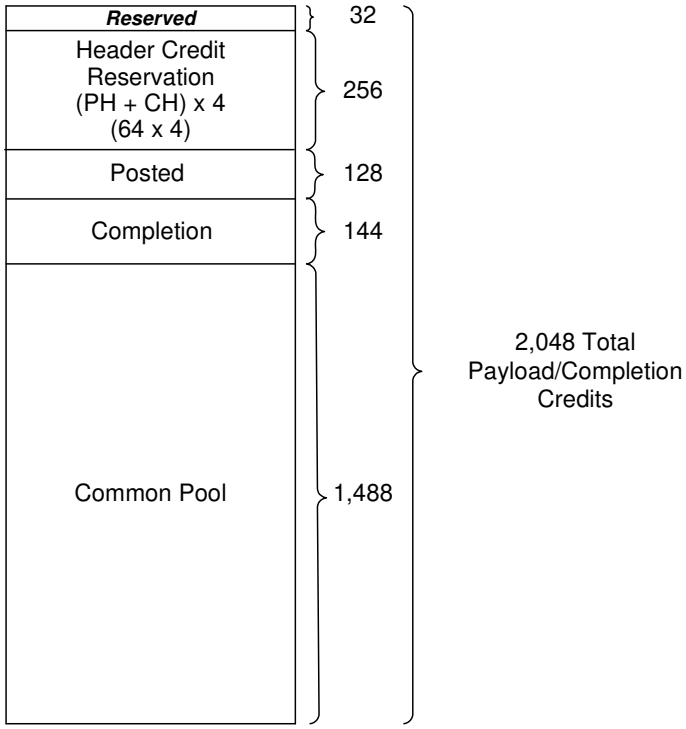


Figure 8-9. Upstream x8 Payload/Completion RAM Default Configuration of 2,048 Credits



A larger common pool allows the most flexibility for handling any possible instantaneous traffic stream, without backpressuring ingress flows. The PEX 8624's initial credit allocation default Settings leave sufficient on-chip RAM to accommodate numerous large TLPs in the common pool, after default values for the initial credits are subtracted. Table 8-12 summarizes the common pool default allotment for each Port configuration (number of Ports/Station).

Table 8-12. Port Configuration Common Pool Default Allotments

Number of Ports/Station	Common Pool Header Credits Upstream/Downstream	Common Pool Payload Credits Upstream/Downstream
1	158/147	1,488/1,472
2	152/138	1,232/1,208

Notes:

1. *Upstream pool values are calculated for a Station that contains the upstream Port, wherein the upstream Port has the greatest width.*
2. *Downstream pool values are calculated for Stations that only have downstream Ports.*
3. *Actual RAM usage for TLP and Header storage and linking is variable.*
4. *The subtraction of 4 credits for each Posted and Completion Header credit advertised, for each Port, is a simplification – the Common Pool credit values can be larger.*

8.4.3 Ingress Credit Handler Threshold Registers (Offsets A00h through A38h)

For each Port, there are three sets of **INCH Threshold** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets A00h through A38h) – Posted, Non-Posted, and Completion. Table 8-13 lists the lower 16 bits for each register. (To view the complete register set, refer to Section 12.16.10, "Device-Specific Registers – Ingress Credit Handler Threshold (Offsets A00h – B7Ch).")

The **INCH Threshold** registers are Station-based and located at the Port offsets, starting with Ports 0, 4, and 8. To select Station 0, 1, or 2, the upper four bits [15:12] of the address are 0000b, 0100b, or 1000b, respectively, while the lower 12 bits select the register.

The Non-Posted credits for Payload are Cleared, which equates to infinite credits. Because Non-Posted TLPs only have a 1-DWord Payload, they will never be longer than 5 DWords. Because the Header RAM is 5 DWords wide, only one Non-Posted Header credit is necessary to store a Non-Posted TLP.

Table 8-13. INCH Threshold Registers (Offsets A00h through A38h), Payload and Header Credit Fields

Ports	Register Offset[a]	Type	Payload		Header	
			Bit(s)	Description	Bit(s)	Description
0, 8	A00h	Posted	8:3	Payload Credit x 8	15:9	Header Credit
	A04h	Non-Posted	8:0	000h (infinite)	15:9	Header Credit
	A08h	Completion	8:3	Payload Credit x 8	15:9	Header Credit
1, 5, 9	A18h	Posted	8:3	Payload Credit x 8	15:9	Header Credit
	A1Ch	Non-Posted	8:0	000h (infinite)	15:9	Header Credit
	A20h	Completion	8:3	Payload Credit x 8	15:9	Header Credit
6	A30h	Posted	8:3	Payload Credit x 8	15:9	Header Credit
	A34h	Non-Posted	8:0	000h (infinite)	15:9	Header Credit
	A38h	Completion	8:3	Payload Credit x 8	15:9	Header Credit

*a. The Station 1, Port 4 register offset is **Software Only**.*

8.4.4 Adjusting Initial Credit Values (Ingress Resources)

The default Initial Credit values listed in Table 8-10 and Table 8-11 can be changed on a per-Station basis; however, to do so, the values must be changed before the initial advertisement by serial EEPROM or I^2C. It is also possible to use software to program the Credit registers over the Link; however, if the Link is up, credit cannot be removed, and values can only be increased. The Credit registers are sticky – a Hot Reset preserves any programmed values, and thereby allows any of the available programming methods to program credits at any time, even after the Link is up, if a Hot Reset is issued afterward to re-run the InitFC sequence.

When changing any credit value, follow the rules outlined in this section; otherwise, the credit can be incorrectly issued and data can be lost.

Credit is partitioned/programmed on a per-Station basis. Per the *PCI Express Base r2.0*, the minimum initial credit must be sufficient to meet the credit requirements of the MPS. To meet this requirement with a 2,048-byte MPS, the minimum credit value assigned to a Port, for both Posted and Completion TLPs, must be 128 credits each (one credit represents 16 bytes of storage).

Additionally, because each TLP may not optimally fill each location in the internal RAM, the Header credit affects Payload credit used to store the Payloads. Therefore, for every Posted or Completion Header credit reserved, 4 credits from the Payload/Completion RAM must also be held in reserve.

The following abbreviations are used in the rules outlined in this section:

- *PH* is the total Posted Header credits advertised or that can be stored
- *NPH* is the total Non-Posted Header credits advertised or that can be stored
- *CH* is the total Completion Header credits advertised or that can be stored
- *MPS* is the Maximum Payload Size
- *Hmax* is the maximum number of Header credits that can be assigned, per Station
- *Pmax* is the maximum number of Payload and Completion credits

The total credit advertised, per Station, must follow these rules:

1. Sum of all Header credits ≤ Hmax = 244.
   Sum of all Header credits = sum (all Ports PH + NPH + CH).
2. Payload and Completion credit must be sufficient for 1 MPS, for each Port.

   Note: *Non-Posted Payload credit is infinite and Read-Only.*
3. Sum of all Payload and Completion credits assigned, per Station,
   is ≤ Pmax = 2,016 ≤ (Advertised Posted Payload + Advertised Completion Payload + (4 x (sum of all Ports PH + CH)))

Programming Example – To satisfy these rules, the following example is presented, using the default values of a Station strapped to have two downstream x4, x4 Ports.

1. From Table 8-10, the sum of all Header credits = 2 x (25 + 16 + 12) = 106, which is ≤ Hmax = 244.
2. For a 2,048-byte MPS, 128 credits must be allocated/advertised for both a Posted and Completion Payload, for each Port. Therefore, for both Ports, this uses 2 x 256 credits, or 512 Payload/ Completion credits.
3. For this case, the Payload/Completion credits used = 512 credits + 4 credits (2 Ports x (25 + 12)/Port) = 808 credits which is ≤ Pmax (2,016).

For this example:

- Common Header Pool = (244 - 106) = 138 Header Credits
- Common Payload/Completion Pool = (2,016 - 808) = 1,208 Payload/Completion Credits

8.4.5 Credit Allocation When Common Pool Is Consumed

A Station's common credit pool is consumed by any Port's Ingress or Egress queue, on a first-come, first-served basis, until the entire common pool is consumed. Once the Station's common pool is completely consumed (and therefore each Port's credit), the PEX 8624 is in a congested state. In the congested state, the PEX 8624 is unable to provide additional credit, to any Port, until credit is released. Credit is released only after the Receiver acknowledges the packet with an ACK. In this state, the **INCH Threshold Station x Port x VC0 Posted** register *Congested Port Weight* field (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets A00h, A18h, and A30h[22:20]) provides a method for users to weight each Port's request for more credit, from the Station's internal credit allocation logic.

In the congested state, the Station's internal credit allocation logic decides which Port will receive the next available credit, by evaluating the following:

- Each Port's *Congested Port Weight* field Setting
- Number of Common Pool credits that Port has already consumed
- Recent history of which Ports have recently received credit

By default, the *Congested Port Weight* field for each Port is Cleared. The default value is called an *effective rate setting*. For the default case, if the Station is configured into two Ports (x4, x4) each Port receives credits based upon on the Port's width. One x4 Port would receive 50% of the credit updates, and the other x4 Port would receive 50% of the remaining credits as they become available.

Table 8-14 defines the *Congested Port Weight* field values. Requests are weighted, based upon the Port's effective Link width, relative to the effective Link widths of the other Stations' Ports. Settings can reduce or increase a Port's effective rate, down to x1 or up to x8, respectively. (*That is*, regardless of the actual Link width, a Link can only be reduced to a x1 effective rate, or increased to a x8 effective rate.) The effective Link Width Request weight is calculated, by multiplying the Port's negotiated Link width (not strapped width) times the *Congested Port Weight* field Setting.

The Station's internal credit allocation logic decides how to allocate the Common Pool credits, as they become available in a congested scenario. Regardless of the Common Pool credit availability, each Port maintains ownership of the credits that were initially allocated to it. Those dedicated credits are replenished to their assigned Port, once an ACK is received from the final destination.

The effective rate setting applies to both the Common Header and Common Payload/Completion pools, for the selected Station and Port. Although the effective rate setting is in the **INCH Threshold Station x Port x VC0 Posted** register, the value applies to credit updates for all three possible traffic types (Posted, Non-Posted, and Completion).

Table 8-14. INCH Threshold Station x Port x VC0 Posted Register *Congested Port Weight* Field (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets A00h, A18h, and A30h[22:20]) Values

***Congested Port Weight* Setting (Bits [22:20])**	**Description**
000b = eff_rate	Request is weighted, based upon the Port's Link width relative to the effective Link widths of the other Stations' Ports.
001b = 2x eff_rate	Increases the weight of a Request by 2x.
010b = 4x eff_rate	Increases the weight of a Request by 4x.
011b = 8x eff_rate	Increases the weight of a Request by 8x.
100b = 0	Port receives no credit out of the common pool, until a decongested state is reached.
101b = eff_rate/2	Decreases the weight of a Request by 2x.
110b = eff_rate/4	Decreases the weight of a Request by 4x.
111b = eff_rate/8	Decreases the weight of a Request by 8x.

8.4.6 INCH Port Pool Registers (Offset 940h)

The **INCH Port Pool Setting for Stations 0, 1, and 2** (**INCH Port Pool)** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 940h) are registers whose original intent was to provide another level of reservation for Common Pool credits. These registers are essentially redundant to what is accomplished by changing the values of the **INCH Threshold** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets A00h through A38h).

Consider the INCH Port Pool registers to be *reserved* and only change the credit Settings, using the INCH Threshold registers. Do not change the INCH Port Pool registers from their default values, unless directed otherwise by PLX Technical Support.

The **INCH Port Pool** registers initial values are provided in sets of two for each Port – Payload pool and Header pool. Table 8-15 lists the bit decode for each Port.

The initial values of the **INCH Port Pool** registers are all Cleared, which means that by default, there is no additional level of reservation. Additionally, the **INCH Threshold** registers default values evenly allocate all available credit, across all enabled Ports.

Table 8-15. INCH Port Pool Setting for Stations 0, 1, and 2 Registers (Offset 940h)[a]

Ports	Payload Pool Bit(s)	Header Pool Bit(s)
0, 8	2:0	6:4
1, 5, 9	10:8	14:12
6	18:16	22:20

*a. The Station 1, Port 4 register offset is **Software Only**.*

8.4.7 Wait for ACK – Avoiding Congestion

Once a TLP arrives, it remains on the PEX 8624 until it is no longer required. The TLP can quickly egress the PEX 8624. However, until an ACK is received, indicating that the TLP was correctly received, each TLP must remain on the PEX 8624 and be ready to be re-sent multiple times. While on the PEX 8624, the TLP continues to use common pool resources.

The *PCI Express Base r2.0* recommends sending an ACK within the approximate time it takes to send 1.5 to 3 MPS TLPs. It does not, however, suggest that smaller TLPs obtain faster ACKs. This data book describes the way in which the PEX 8624 sends an ACK. However, the PEX 8624, has no way of knowing its Link partner's ACK policy.

To minimize the amount of TLPs stored on the PEX 8624 while waiting for an ACK, follow these guidelines:

- Avoid traffic patterns where a great deal of back-to-back TLP bytes travel from a wide Link to a single narrow Link, because the narrow Link can only forward TLPs at a fraction of the ingress rate. *For example*, if a 4-KB MRd is transmitted upstream from a x4 Port and the upstream Port is x8, the upstream Port transmits a 4-KB CPLD to the Requester, two times faster than the Requester can receive the data. If the Requester transmits many of these MRd Requests, large amounts of CPLD data that require storage on the PEX 8624 will quickly accumulate.
- If there are many small TLPs, determine whether the PEX 8624's ACK response time can be reduced, as per the *PCI Express Base r2.0* guidelines.
- Evenly space the TLP pattern, rather than use a burst of many back-to-back TLPs followed by a long stall, to even the distribution and accommodate a fixed ACK Transmission Latency Timer.

8.5 Latency

Latency is the length of time it takes to proceed from one event to another. Latency can be measured in several different ways, but perhaps the most common measurement for a switch is *Start TLP-to-Start TLP (STP-to-STP) latency*. Figure 8-10 and Table 8-16 illustrate an STP-to-STP latency measurement. When the Egress Start TLP symbol is transmitted out of a switch before the Ingress Port End symbol arrives, the transfer is termed *Cut-Thru*. If the Destination Port is not congested, the PEX 8624 always cuts the packet through. The PEX 8624 has the same latency, regardless of whether the traffic is upstream or peer-to-peer.

As expected with the PEX 8624 Cut-Thru architecture, STP-to-STP latency is basically constant for all Payload sizes, from any width to the same width or smaller, as indicated by the shaded-green entries in Table 8-16. A faster Link can receive the Header for decode faster, with a slightly lower latency. For cases in which the egress Port has a higher bandwidth than the ingress Port, then a fraction of the packet:

$$F = (E-I) / E$$

must be stored, before the TLP can be forwarded without running out of data in the middle of transmission.

where

- *F* is the fraction sum
- *E* is egress bandwidth
- *I* is ingress bandwidth

Figure 8-10. Start TLP-to-Start TLP Latency Measurement

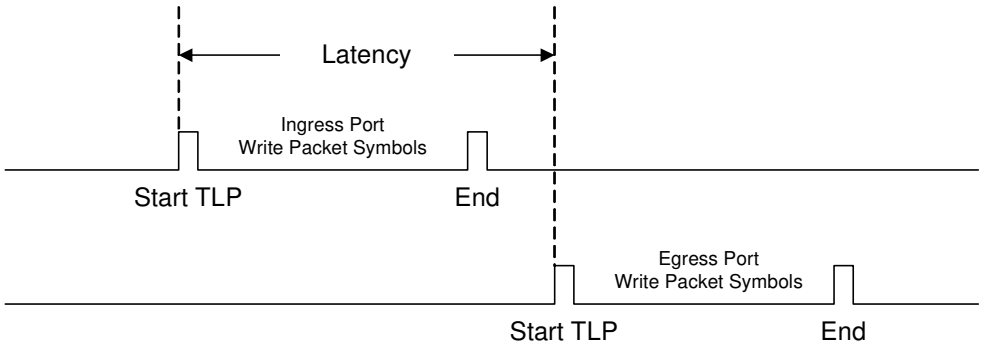


Table 8-16. Sample STP-to-STP Latency

Latency for TLP with a Data Payload of 4/64/256 Bytes (in ns)			
Ingress			
	x8 Gen 2	x4 Gen 2	x1 Gen 1
Egress			
x8 Gen 2	148/157/157	154/183/233	237/479/1,248
x4 Gen 2	151/159/156	154/158/157	238/478/1,246
x1 Gen 1	148/157/158	150/157/158	238/381/381

8.5.1 Host-Centric Latency

Host-centric traffic flows only to or from the Host. Host-centric latency depends upon the number of active streams. If there is only one active stream, or if the total Host bandwidth is greater than or equal to the sum of all traffic streams, the traffic is well-balanced and the latency measurements provided in Table 8-16 apply.

If there is more traffic than an upstream Host can sink, congestion occurs when all the TLPs concurrently attempt to use the limited Host bandwidth. The latencies in that case depend upon the level of traffic congestion. In this case, Host bandwidth is at 100%, but the total downstream bandwidth is more than the Host bandwidth, and latencies continue to increase until the congestion eases.

Another case of increased latency is if the Host serially sends large amounts of Read Completion data to one downstream Port and then another downstream Port. *For example*, if the upstream Port is x8 and the two downstream Ports are both x4, it appears that there should not be a latency build-up, because the bandwidth matches. However, if the Host cannot interleave the destinations, one destination must wait until the Host completes transmitting traffic to the other destination, before it can receive any Read Completion data. In this case, the round-trip Read latency can significantly increase.

For example, suppose that one downstream Port transmits 16, 4-KB MRd Requests upstream. Those Read Requests represent 64 KB of data. If the upstream Port is x8 and the downstream Port is x4, the Read Completions back up into the PEX 8624, perhaps all the way to the Root Complex. Suppose another downstream Port transmits only one, 1-KB MRd Request upstream, shortly after the 16, 4-KB MRds were received by the Root Complex. For many Root Complexes, this one, 1-KB Read Request from the second device must wait for the 16, 4-KB MRd Requests from the first device to complete before being serviced. The PEX 8624 buffer is approximately 10 KB; therefore, the second downstream device must wait for (64-10) 54 KB of Completion data to transmit across a x4 Link before it begins to receive its Read Completions. On a x4 Link, 54 KB takes about 48 µs, which significantly increases the second device's latency. The PEX 8624 contains Read Pacing logic that prevents this type of latency increase that occurs when multiple devices concurrently read data from the Root Complex. (Refer to Section 8.7.)

8.5.2 Peer-to-Peer Latency

If there is no congestion, peer-to-peer latencies match the best-case values listed in Table 8-16. The PEX 8624 has the same latency, regardless of whether the traffic is Host-centric or peer-to-peer. Latency is constant in the non-congested case, no matter the Source Port nor Destination Port, if the Source Port has the same or greater bandwidth than the Destination Port.

The discussion for Host-centric traffic applies to all Ports for peer-to-peer traffic. It is recommended that there be a method outside the scope of this data book, however, for balancing traffic flow for peer-to-peer applications.

8.5.3 Other Latency Measurements

In addition to STP-to-STP latency, there are other latencies to consider. Table 8-17 lists various best-case latencies for several Link widths and speeds. Transmitted DLLPs can be required to wait for a TLP. DLLP policies can prevent sending a DLLP for a time period longer than the best case.

Table 8-17. Miscellaneous Best Case Link Latencies (in ns)

Latency[a]	x8 Gen 2	x4 Gen 2
STP in to UpdateFC SDP[b]	162	163
TLP's END in to ACK SDP	114	120
UpdateFC SDP in to STP	138	138
STP in to UpdateFC SDP	162	163

a. Gen 1 latency values are expected to be the same as, or very close to, Gen 2 latency values.

b. SDP is "Start DLLP".

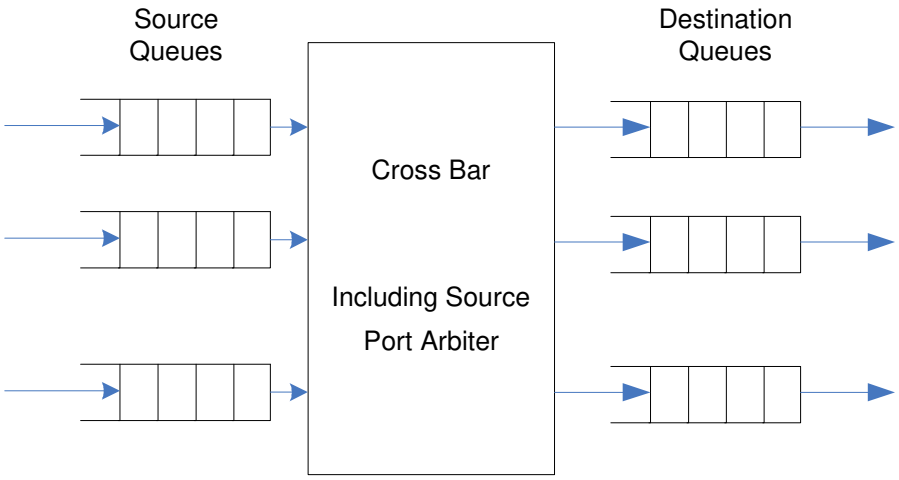
8.6 Queuing Options

On-chip queuing does not exist in balanced bandwidth scenarios, where the total ingress bandwidth is less than or equal to the egress bandwidth. In the common case, where the total ingress bandwidth is greater than the egress bandwidth, queues develop on the PEX 8624. The PEX 8624 provides two alternatives to where to locate such queuing (refer to Figure 8-11):

- **Destination queue** – Associated with a single Destination Port. All the TLPs in a Destination queue will egress out the same Port.
- **Source queue** – Associated with a single ingress Port. All the TLPs in a Source queue come from the same Port.

Each queue is discussed in the sections that follow.

Figure 8-11. On-Chip Queuing



8.6.1 Destination Queuing

Note: *For the queuing examples provided in this section, "Port 1" indicates "first Port," not the Port physically identified as Port 1.*

The default behavior is for all queues to develop at the Destination Port. If TLPs are arriving from four sources to a common Destination Port, the TLPs are scheduled according to First-In, First-Out (FIFO). The crossbar can forward a TLP every 4 ns, to each Destination queue; therefore, it is unlikely that a Source queue can develop or last very long.

A Destination queue develops whenever the *ingress rate* – the sum of all ingress Ports targeting a Destination Port – exceeds the egress rate. A Destination queue might also develop in a credit-starved situation, where there is no credit available to forward TLPs.

For example, if TLPs arriving from four sources all go to a common Destination Port, the TLPs are scheduled, based upon the order in which they arrive at the Destination queue FIFO[a]. If all four flows are equally active, the TLPs naturally interleave as 1,2,3,4,1,2,3,4. If three of the Ports, however, have a head start before the fourth Port turns On, the output can be 1,2,3,1,2,3,1,2,3,1,2,3,1,2,3,4,1,2,3,4. In this case, all the new Port (Port 4) TLPs must wait for the earlier Port 1,2,3 traffic to be transferred before the Port 4 TLPs can be transferred. Therefore, the latency for Port 4 traffic to travel through the PEX 8624 can widely vary, based upon the traffic passing through the switch.

a. Conventional PCI Strong Ordering rules can override the FIFO. Conventional PCI requires Posted TLPs to be able to pass Non-Posted and Completion TLPs, to avoid deadlock.

8.6.2 Source Queuing

Caution: ***Source Queuing and Read Pacing should not be concurrently enabled. The two features are incompatible and doing so can result in Fatal errors.***

Note: *For the queuing examples provided in this section, "Port 1" indicates "first Port," not the Port physically identified as Port 1.*

Source queuing can be enabled for applications that require deterministic bounded latency for a few Ports, while the latency for other Ports is not as important.

Source queuing limits the Destination queue depth. When the Destination queue reaches the maximum depth, any subsequent TLPs targeting that Port are not forwarded, but are queued up in a per-Source Port-based queue. The Source Port queue does not forward TLPs until the Destination queue drops to a programmed threshold, upon which TLP forwarding is re-enabled.

Note: *A Source Port queue that cannot forward to a Destination queue blocks all subsequent TLPs arriving on that same Source Port, although the target Port is a different destination.*

The **Port Egress TLP Threshold** register (offset F10h) controls the minimum and maximum queue depths. Table 8-18 summarizes the register bit Settings. The Port Lower TLP Counter is the quantity of TLPs that the Destination queue must reach after becoming saturated, before re-enabling TLP forwarding. The Port Upper TLP Counter is the number of TLPs that can be queued in the Destination queue.

In the Destination queue example provided in Section 8.6.1, the early arriving Port 1,2,3 TLPs stalled Port 4's TLP for an indeterminate length of time. By programming, with source queuing enabled and a Destination Port Lower TLP Counter programmed to 1 and Port Upper TLP Counter programmed to 3 (TLPs), the worst case is that Port 4 must wait for three TLPs (1,2,3) before getting its first turn. With these Settings, the example TLP output would be 1,2,3,4,1,2,3,4,1,2,3,4. The *turn to be forwarded* refers to a Port arbitration wait, described in Section 8.6.3.

To avoid unnecessary idles on the destination Link, program a Port Lower TLP Counter of 1, and a Port Upper TLP Counter of 2.

Table 8-18. Port Egress TLP Threshold Register Port Lower and Upper TLP Counts (Offset F10h)

Bit(s)	Name	Description
10:0	**Port Lower TLP Counter**	When Source Scheduling is disabled due to the Port Upper TLP Counter (threshold) being exceeded, Source Scheduling is re-enabled when the Port TLP Counter goes below the Port Lower TLP Counter (this threshold). Because the default Setting of this field is 7FFh (2,047), which is greater than the maximum amount of TLPs that can be queued in the PEX 8624, the Source Scheduler is disabled, by default.
26:16	**Port Upper TLP Counter**	When the Port TLP Counter is greater than or equal to this value, the Source Scheduler disables TLP Scheduling to this egress Port. Because the default Setting of this field is 7FFh (2,047), which is greater than the maximum amount of TLPs that can be queued in the PEX 8624, the Source Scheduler is disabled, by default.

Note: *Bits not identified in Table 8-18 are* ***reserved****.*

8.6.3 Port Arbitration

In the crossbar that connects the Source queues to the Destination queues, there is a Port Arbiter for each Destination Port. The Port Arbiter ensures that each Source Port receives a deterministic bandwidth connecting to a Destination Port. Port arbitration uses Device-Specific Weighted Round-Robin (WRR) Port arbitration. Device-Specific WRR arbitration is Round-Robin arbitration, with optionally more weight for a particular Port or Ports.

Each Port Arbiter has a 32-phase Port Arbitration Table, as outlined in the *PCI Express Base r2.0*, and documented in the **Port Arbitration Table Phase *x*** registers (Upstream Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 1A8h through 1B4h). (Refer to the *PCI Express Base r2.0* for further details.)

Port arbitration makes decisions on a per-TLP basis. A Port with more short TLPs will appear to receive less bandwidth, compared to a Port with fewer long TLPs, if both Ports have the same weight and both target a congested Port.

8.6.4 Port Bandwidth Allocation

For applications that need to allocate a fixed bandwidth to each Port, the PEX 8624 can help enforce the relative bandwidth ratio between Ports in a congested scenario.

By combining source queuing, Port arbitration, and initial credit, as well as some knowledge of average Payload size, many combinations of Port bandwidth allocation are possible.

8.7 Read Pacing

Caution: ***Read Pacing and Source Queuing should not be concurrently enabled. The two features are incompatible and doing so can result in Fatal errors.***

Although the Read Pacing feature is supported on all Ports, its registers are implemented on upstream Port 0. If Port 0 is the NT Port, the NT Port Virtual Interface implements the Read Pacing registers. Otherwise, the Read Pacing-related registers are ***reserved***.

PCI Express has a weakness concerning the number of outstanding bytes requested by Reads. It is possible that a single device can overwhelm the system with a reasonable number of large Read Requests, thereby impacting the performance of other connected devices, by filling the ingress transaction queue in the Root Complex.

The Root Complex must handle the transactions in the order in which they are posted. Transactions posted from less aggressive reading devices, which may be more sensitive to latency, suffer performance reductions due to the unfairly weighted path (head of line blocking) in the transaction queue that the large reads represent.

Read Pacing attempts to apply some rules to Memory Read Requests, so that no one Port can overwhelm a system. There are two aspects to the PEX 8624's Read Pacing capability:

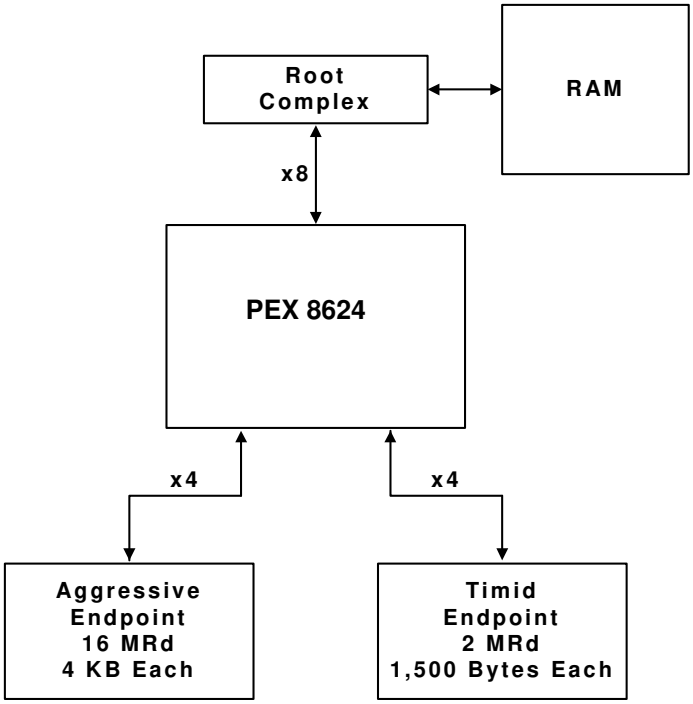
- Read spacing
- Read threshold

The following sections provide examples and further information regarding Read Pacing.

8.7.1 Read Pacing Example

Figure 8-12 illustrates an example of a system that benefits from Read Pacing.

Figure 8-12. Read Pacing Example



In a typical Host-centric application, endpoints have Direct Memory Access (DMA) engines that write to and read from Main memory. A performance bottleneck can occur during the Read to Main memory, through the Root Complex. For the example illustrated in Figure 8-12, the aggressive endpoint sends many large (16, 4-KB) Memory Read Requests, while another endpoint, or Timid Endpoint (TEP), sends only two 1,500-byte Memory Read Requests. The TEP then waits for a response before sending additional Read Requests[a].

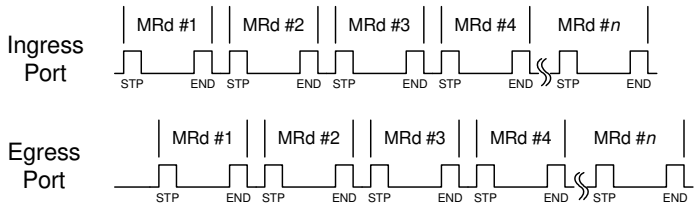
If either endpoint is running by itself, neither sees a problem. However, if both endpoints are concurrently active, the aggressive endpoint dominates the Root Complex Memory Controller. In addition, due to the bandwidth mismatch, Completions can queue up in the PEX 8624, creating too many Completions for the switch to store at one time. As a result, the PEX 8624 backpressures the Root Complex for Completions. The Root Complex can only forward Completions to the PEX 8624 at the aggressive endpoint's rate, which is significantly less than the Root Complex could otherwise handle.

The net impact is not to the aggressive endpoint, because there are a sufficient number of Completions queued up in the PEX 8624 to keep it busy. In fact, the aggressive endpoint experiences better performance with a switch, than connected directly to the Root Complex[b]. Rather, the TEP experiences lower performance results. Its Memory Read Requests wait in line behind multiple aggressive endpoint Requests, and the Root Complex can drain Requests only at the same rate of the PEX 8624, not at the upstream Link's capacity.

Figure 8-13 illustrates how a PCI Express switch, without Read Pacing, forwards Memory Read Requests (MRds).

Read Pacing solves the performance loss seen by the TEP, while improving the aggressive endpoint's performance. The following sections provide examples of the way in which the PEX 8624 functions when Read Pacing is enabled, and Read Spreading is enabled or disabled.

Figure 8-13. Read Pacing Off (Disabled)



a. This is based upon an actual setup in a third-party lab. Fibre Channel endpoints can easily send 16, 4-KB MRd at a time, while Gigabit Ethernet endpoints might send only one or two 1,500-byte endpoints at a time.

b. Without a switch, when the Root Complex has something else to do, the aggressive endpoint loses its data stream. With a switch, the buffering of multiple Completions hides the fact that the Root Complex is multitasking.

8.7.2 Read Spacing (Spreading) Logic

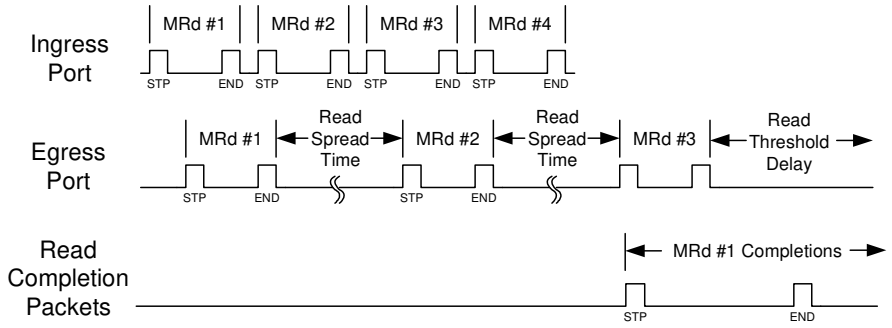
Read Spacing (also referred to as *Read Spreading*) spreads out Read Requests. The PEX 8624 Read Spacing logic looks at the Read Request size and the endpoint's bandwidth, to determine how often to forward subsequent Read Requests. *For example*, Read Requests arriving on a x4 Link can only sink data at a x4 rate. If a x4 endpoint submits multiple Read Requests to a x8 Link, the Read Spacing logic does not forward the subsequent Read Requests until the endpoint has sufficient time to sink a portion of the Completion data from the previous Read Requests.

Initially, a queue of Completions must build up to hide the time that it takes for the data to return. As a result, Reads are forwarded at 2x the endpoint's bandwidth. This 2x rate is maintained until a threshold of outstanding Read data is reached, at which time Reads are forwarded at 1x the endpoint's bandwidth.

Read Pacing must be enabled for Read Spreading to be enabled. *That is*, for a Port to have Read Spreading enabled, the Port's **Read Pacing Control** register *Port x Read Pacing Disable* and *Port x Memory Read Spreading Disable* bits (offset F34h[9, 8, 6, 5, 1, 0 and 25, 24, 22, 21, 17, 16], respectively) must both be Cleared.

Figure 8-14 illustrates the way in which the PEX 8624 forwards Read Requests when the Port's Read Pacing- and Read Spreading-related bits are enabled. (Refer to Section 8.7.5 for additional register/bit information.) The PEX 8624 continues to spread and forward the Read Requests, until the amount of Completion data for which it is waiting exceeds the value programmed in the **Read Pacing Threshold *x*** register(s) for that Link width (Upstream Port 0, or NT Port Virtual Interface (if Port 0 is the NT Port, offsets F38h and F3Ch).

Figure 8-14. Read Pacing On (Enabled) and Read Spreading On (Enabled)

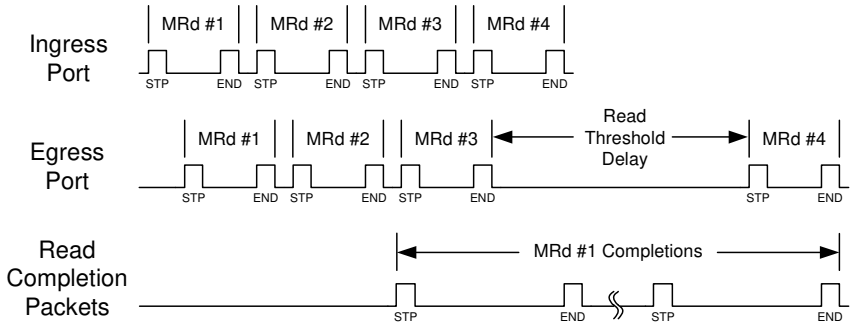


8.7.3 Read Threshold

The Read threshold is the maximum number of outstanding DWords (1 DWord = 4 bytes) that the endpoint Port requested to be read, but were not yet returned as Completion data. The threshold is related to the PEX 8624's buffering capacity – all outstanding Read data ought to be able to be buffered in the switch, to remain out of the way of other Completions for other endpoint's Read Requests.

After a Port reaches its Read threshold, subsequent Read Requests from that Port queue up in the PEX 8624, waiting for Completion data to reduce the outstanding count to below the threshold. If an overabundant number of Read Requests queue in the PEX 8624, no additional Read credit is allocated, which backpressures the Read Requester. Figure 8-15 illustrates the way in which the PEX 8624 forwards Read Requests when its Read Spacing logic is enabled and Read Spreading logic is disabled.

Figure 8-15. Read Pacing On (Enabled) and Read Spreading Off (Disabled)



8.7.4 Read Pacing Benefits

When Read Pacing logic is enabled, the PEX 8624 provides the follow benefits:

- Maximum Read latency that an endpoint may experience can be dramatically reduced.

  By reducing the amount of queued Read Requests, and therefore pending Read Completion data at the Root Complex, new Read Requests from Ports that do not have pending Read Requests can be serviced with a predictable and/or reasonable amount of latency.

- Timid endpoint bandwidth is dramatically increased in busy applications.

  Because queues of pending Read Requests in the Root Complex are limited, and congestion caused by a large amount of Completion data intended for a high-bandwidth, needy Port (or Ports) is avoided, the bandwidth needs of endpoints with smaller bandwidth requirements are met (*that is*, the endpoints are not starved).

- PEX 8624's Read Pacing Threshold logic allows all busy Ports to be equally serviced in congested scenarios, regardless of their individual Read requesting behavior.

  For example, all Ports might simultaneously request data, some aggressively and some timidly. While unable to quickly drain their queued Completions, the Ports' Read Pacing Threshold logic forwards the additional Read Requests to the Root Complex, equally and fairly, while ensuring Completion data is available for each Port, when the Port is ready to accept it.

8.7.5 Enabling Read Pacing and Read Spreading

Read Pacing is disabled, by default. To enable Read Pacing, the Port's **Read Pacing Control** register *Port x Read Pacing Disable* bit (Upstream Port 0, or NT Port Virtual Interface (if Port 0 is the NT Port, offset F34h) must be Cleared. A bit value of 0 enables Read Pacing, whereas a value of 1 (default) disables Read Pacing.

The Port's **Read Pacing Control** register *Port x Memory Read Spreading Disable* bit (Upstream Port 0, or NT Port Virtual Interface (if Port 0 is the NT Port, offset F34h) is used to enable or disable Read Spreading. A value of 1 disables Read Spreading for the corresponding Port. Read Spreading is enabled, by default (value of 0); however, it is overridden by the Port's *Port x Read Pacing Disable* bit, by default.

Both sets of Read Spreading and Pacing Control register bits are represented in Table 8-19. (For complete details, refer to the register offset F34h description provided in Section 12.16.14, "Device-Specific Registers – Read Pacing (Offsets F34h – F3Ch)."). Figure 8-13 through Figure 8-15 illustrate what occurs when the bits are enabled or disabled.

The Read Pacing thresholds are Set, based upon the Source Port's programmed Link width. The **Read Pacing Threshold 1** register controls the threshold values for x8 Link widths, and the **Read Pacing Threshold 2** register controls the threshold values for x4 and x2 Link widths (Upstream Port 0, or NT Port Virtual Interface (if Port 0 is the NT Port, offsets F38h and F3Ch, respectively). The thresholds are in DWords. Narrower Link widths have lower thresholds, because they must buffer smaller quantities.

Table 8-19. Read Pacing Control Register Read Pacing and Memory Read Spreading Disable (Offset F34h)

Bit(s)	Description	Default
9, 8, 6, 5, 1, 0	**Port *x* Read Pacing Disable** Bits [9, 8, 6, 5, 1, 0] correspond to the Read Pacing Disable for Ports 9, 8, 6, 5, 1, and 0, respectively. 0 = Read Pacing is enabled for this Port 1 = Read Pacing is disabled for this Port	3Fh
25, 24, 22, 21, 17, 16	**Port *x* Memory Read Spreading Disable** Bits [25, 24, 22, 21, 17, 16] correspond to the Memory Read Spreading Disable for Ports 9, 8, 6, 5, 1, and 0, respectively. 0 = Memory Read Spreading is enabled for this Port 1 = Memory Read Spreading is disabled for this Port	00h

Note: *Bits not identified in Table 8-19 are* ***Reserved*** *or* ***Factory Test Only****.*

8.8 Using the Dual Cast Feature

8.8.1 Introduction

This section describes the functions and programming of the PEX 8624's Dual Cast feature. A typical system configuration and register programming example is also provided.

Dual Cast allows programs to concurrently write the same data to two different destinations. Whenever Posted Memory Write TLPs entering the PEX 8624 through a designated Port (referred to as the *Dual Cast Source Port*) are addressed to designated memory regions (referred to as *Dual Cast BARs*), the switch automatically generates a copy of the original TLP (referred to as the *Dual Cast Copy TLP*), replacing the original TLP's address with one that is mapped to an egress Port designated as the *Dual Cast Destination Port*.

When an incoming TLP is copied in this manner, both the original TLP and Dual Cast copy TLP are concurrently queued at their respective egress Ports, effectively doubling the PEX 8624's egress rate for the same ingress rate.

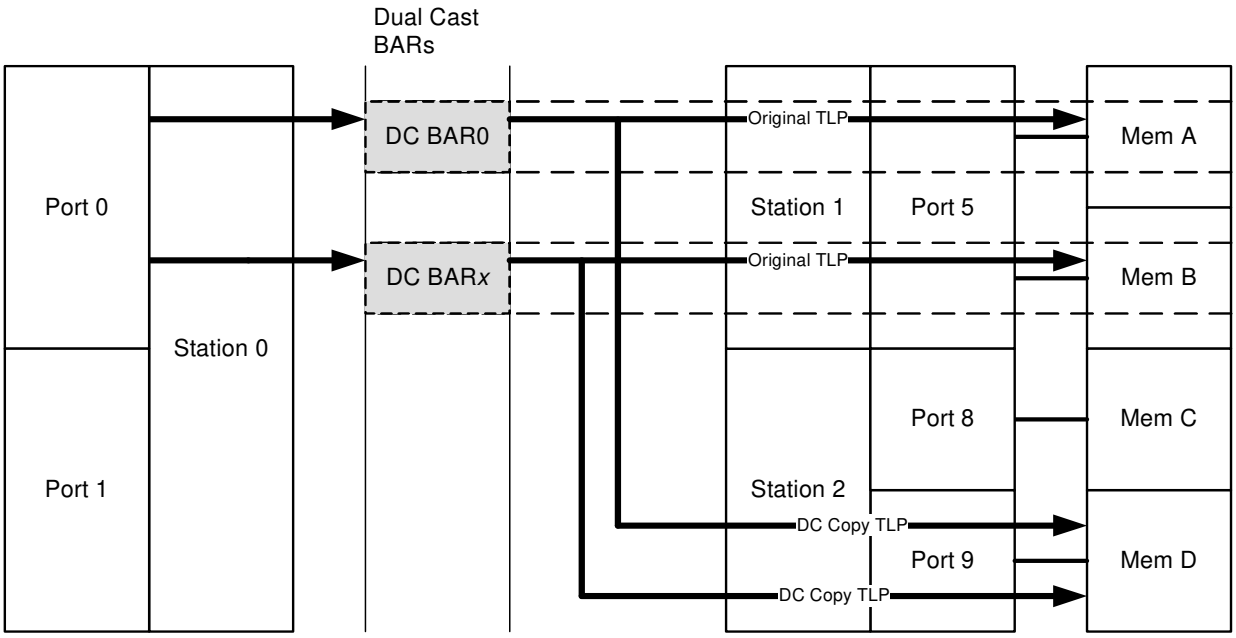
8.8.2 Dual Cast System Model

Figure 8-16 illustrates Dual Cast functions. In this figure, the designated Dual Cast Source Port is Port 0. Only Memory Write TLPs that enter the PEX 8624 through this Port (or alternately, any Port of a designated Station) are subject to Dual Casting. Dual Cast Control registers allow the programmer to define up to eight separate Dual Cast BARs, over which Dual Casting will be applied. If a Memory Write TLP enters the PEX 8624 through the designated Dual Cast Source Station/Port, **and** its Header address falls within an active Dual Cast BAR, then the switch automatically generates a Dual Cast Copy TLP, replacing the original TLP's Header address with a new address mapped to the designated Dual Cast Destination Port, in this case, Port 9.

Dual Cast BARs can be mapped to any egress Port of the PEX 8624. In other words, original Memory Write TLPs that are being copied can exit the PEX 8624 on any egress Port, as they would normally. However, Dual Cast Copy TLPs, regardless of which Dual Cast BAR generates them, must all exit the PEX 8624 through the designated Dual Cast Destination Port.

The Dual Cast Destination Port can also be configured as NT. Refer to Section 8.8.5 for additional programming requirements.

Figure 8-16. Typical Dual-Cast System Model



8.8.3 Dual Cast Control Registers

This section describes each of the Dual Cast Control registers. Eight sets of identical registers describe each of the eight Dual Cast BARs. An additional register specifies the Dual Cast Source and Destination Ports. These registers are described, in detail, in the following sub-sections. For a complete listing of the registers, refer to Section 12.14.9, "Device-Specific Registers – Vendor-Specific Dual Cast Extended Capability (Offsets 448h – 51Ch)." The Dual Cast registers are located in Port 0, and also the NT Port Virtual Interface if Port 0 is the NT Port.

8.8.3.1 Dual Cast Low BAR[0-7], Dual Cast High BAR[0-7]

The 32-bit **Dual Cast Low** and **High BAR*x*** registers in Port 0 (refer to Table 8-20) are used to define the 64-bit physical Base address of each of the Dual Cast BAR address windows, numbered 0 through 7.

Dual Cast Low BAR*x* contains the lower 32-bits of the Base address of Dual Cast BAR window *n*. Only the upper 12 bits [31:20] of this register are used to specify address. Bits [19:0] of this register are not de-coded, and are hardwired with the value 0_000Ch. Thus, Dual Cast BARs are naturally aligned on 1-MB boundaries. Because the 1-MB boundary is also a 4-KB boundary, any Memory Write TLP that falls within the Dual Cast BAR's Address range will be guaranteed never to exceed the top of the Dual Cast BAR*x* range.

Dual Cast High BAR*x* contains the upper 32 bits of the Base address for Dual Cast BAR window *n*. For Base addresses in the lower 4 GB or for all 32-bit systems, this register should be Cleared (default).

Table 8-20. Dual Cast High/Low BAR*x* Register Locations

Base Address Register	Port 0 Register Offset	
	Dual Cast Low[31:0] (Lower 32 Bits)	Dual Cast High[31:0] (Upper 32 Bits)
BAR0	450h	454h
BAR1	468h	46Ch
BAR2	480h	484h
BAR3	498h	49Ch
BAR4	4B0h	4B4h
BAR5	4C8h	4CCh
BAR6	4E0h	4E4h
BAR7	4F8h	4FCh

8.8.3.2 Dual Cast Low BAR[0-7] Translation, Dual Cast High BAR[0-7] Translation

The 32-bit **Dual Cast Low** and **High BAR*x* Translation** registers in Port 0 (refer to Table 8-21) specify the destination address of the Dual Cast Copy TLP for their corresponding Dual Cast BARs. When a Dual Cast Copy TLP is formed, the original TLP's Header Address bits are replaced with corresponding Address bits from these registers.

Restrictions

- Dual Cast BAR Translation addresses must be mapped to the Dual Cast Destination Port, as specified in the **Dual Cast Source Destination Port** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 510h). (Refer to Section 8.8.3.4.) While the original TLPs that are copied can be mapped to any Port of the PEX 8624, copied TLPs from all Dual Cast BARs must be mapped to the Dual Cast Destination Port.
- Dual Cast BAR Translation address plus the Dual Cast BAR window size must never exceed the Address range mapped to the Dual Cast Destination Port.

Table 8-21. Dual Cast High/Low BAR*x* Translation Register Locations

Base Address Register	Port 0 Register Offset	
	Dual Cast Low Translation[31:0] (Lower 32 Bits)	Dual Cast High Translation[31:0] (Upper 32 Bits)
BAR0	458h	45Ch
BAR1	470h	474h
BAR2	488h	48Ch
BAR3	4A0h	4A4h
BAR4	4B8h	4BCh
BAR5	4D0h	4D4h
BAR6	4E8h	4ECh
BAR7	500h	504h

8.8.3.3 Dual Cast Low BAR[0-7] Setup, Dual Cast High BAR[0-7] Setup

The 32-bit **Dual Cast Low** and **High BAR*x* Setup** registers in Port 0 (refer to Table 8-22) form a 64-bit value used to define the Dual Cast BAR window size, which increases in powers of 2 in size, starting from 1 MB.

The Dual Cast BAR window size increases in powers of 2, starting from 1 MB. The address window size is determined by the quantity of Set bits, starting from bit 63 down to bit 20. For each bit that is a value of 1, the Copy TLP's Header Address bit is replaced by the corresponding Address bit in the **Dual Cast Low/High BAR*x* Translation** registers, as illustrated in Figure 8-17.

If bits [63:20] are all Set, the source window size is 1 MB. If bits [63:21] are all Set, and bit 20 is Cleared, the window size is 2 MB. When **Dual Cast High BAR*x* Setup**[31] is Cleared, the corresponding Dual Cast BAR is disabled. Table 8-23 lists example **Dual Cast Low/High BAR*x* Setup** register values and corresponding Dual Cast BAR Address window sizes.

Table 8-22. Dual Cast High/Low BAR*x* Setup Register Locations

Base Address Register	Port 0 Register Offset	
	Dual Cast Low Setup[31:0] (Lower 32 Bits)	Dual Cast High Setup[31:0] (Upper 32 Bits)
BAR0	460h	464h
BAR1	478h	47Ch
BAR2	490h	494h
BAR3	4A8h	4ACh
BAR4	4C0h	4C4h
BAR5	4D8h	4DCh
BAR6	4F0h	4F4h
BAR7	508h	50Ch

Figure 8-17. Dual Cast High/Low BAR*x* Setup Register Example

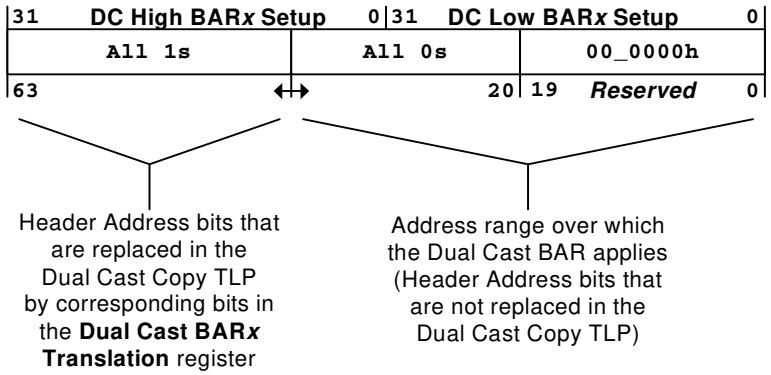


Table 8-23. Dual Cast BAR*x* Setup Register Address Window Sizing Examples

Dual Cast High BAR*x* Setup[31:0]	Dual Cast Low BAR*x* Setup[31:20]	Dual Cast BAR*x* Window Size
0000_0000h	XXXh	Disabled (default)
FFFF_FFFFh	FFFh	1 MB
FFFF_FFFFh	FFEh	2 MB
FFFF_FFFFh	000h	4 GB
FFFF_FFFEh	000h	8 GB

Restrictions

- Dual Cast BAR Address windows must not overlap one another.
- Dual Cast Source Address windows 0 through 7 can be mapped to any Station or Port (including the upstream Port and NT Port); however, only Write TLPs that enter the PEX 8624 through the designated Dual Cast Source Station/Port are subject to Dual Casting. (Refer to Section 8.8.3.4.)
- Both the original forwarded TLP **and** Dual Cast Copy TLP must be acknowledged on their respective egress Ports, before the original incoming TLP can be retired.
- Dual Cast BAR regions can be coded only as 64-bit BARs. For regions under 4 GB, Dual Cast High **BAR*x*** = 0000_0000h.

8.8.3.4 Dual Cast Source Destination Port

The **Dual Cast Source Destination Port** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port; ***Reserved*** (RsvdP) for Dual Cast BAR Limit Lower register, offset 510h) is used to specify the Dual Cast Source Station/Port and Dual Cast Destination Port. Table 8-24 lists the bit definitions for this register. Bits not listed are ***reserved*** (zero).

Table 8-24. Dual Cast Source Destination Port Register Definition (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port; *Reserved* (RsvdP) for Dual Cast BAR Limit Lower register, offset 510h)

Register Bits	Function
1:0	**Dual Cast Source Port #**[a] Valid only when bit 8 (*Dual Cast Source Port Enable*) is Set. Specifies the source (ingress) Port Number upon which Dual Cast BARs are applied. Refer to Table 8-25 for Source Port # to Source Station # mapping.
3:2	**Dual Cast Source Station #** Specifies the source (ingress) Station Number upon which Dual Cast BARs are applied. Refer to Table 8-25 for Source Port # to Source Station # mapping.
7:4	**Dual Cast Destination Port #** Specifies the destination (egress) Port Number to which Dual Cast BAR Translation addresses are mapped, and to which Dual Cast Copy TLPs will be queued.
8	**Dual Cast Source Port Enable** 0 = Dual Cast applies to Write TLPs entering any Port on the Dual Cast Source Station specified in field [3:2] (*Dual Cast Source Station #*). In that case, the field [1:0] (*Dual Cast Source Port #*) value is "Don't Care." 1 = Dual Cast applies only to Write TLPs entering the PEX 8624, by way of the Dual Cast Source Port Number specified in field [1:0].

a. Elsewhere in PEX 8624 documentation, Ports are numbered using 4-bit values 0000b, 0001b, and so forth. In this register, Dual Cast Source Ports are numbered on a per-Station basis. For example, what is referred to as Port 9 elsewhere in the documentation is described in this register as Station 10b, Port 01b.

Table 8-25. Dual Cast Source Destination Port Register – Source Port # and Source Station Field Values, by Port (Offset 510h)

Port	Dual Cast Source Port # (Field [1:0] Value)	Dual Cast Source Station # (Field [3:2] Value)
0	00b	00b
1	01b	00b
5	01b	01b
6	10b	01b
8	00b	10b
9	01b	10b

8.8.4 Dual Cast Programming Example

In this example, we consider a PEX 8624 configured as x8, x8, x8, with Port 0 being the upstream Port (connected to Root Complex), and Ports 5 and 8 configured as Transparent downstream Ports. Port 5 maps to a block of physical memory at Base address AAA0_0000h (32-bit addressing). Port 8 maps to a block of memory at Base address BBB0_0000h.

For this example, the switch must be programmed such that Write TLPs entering Port 0 and addressed to Port 5 (in the range AAA0_0000h to AAAF_FFFFh) are Dual Cast (copied) to the memory that is mapped to Port 8, starting at address BBB0_0000h.

8.8.4.1 Register Programming Steps

1. Program the **Dual Cast BAR0** registers with the Base address of the memory on Port 5.
   Dual Cast Low BAR0[31:0]=AAA0_000Ch ***(Note:** Bits [19:0] are hardwired to 0_0000h.)*
   Dual Cast High BAR0[31:0]=0000_0000h
2. Program the **Dual Cast BAR0 Setup** registers to specify the Dual Cast BAR window size (1 MB).
   Dual Cast Low BAR0 Setup[31:0]=FFF0_0000h ***(Note:** Bits [19:0] are hardwired to 0_0000h.)*
   Dual Cast High BAR0 Setup[31:0]=FFFF_FFFFh
3. Program the **Dual Cast BAR0 Translation** registers with the address of the memory on Port 8.
   Dual Cast Low BAR0 Translation[31:0]=BBB0_0000h ***(Note:** Bits [19:0] are hardwired to 0_0000h.)*
   Dual Cast High BAR0 Translation[31:0]=0000_0000h
4. Program the **Dual Cast Source Destination Port** register bits, as follows:
   Dual Cast Source Destination Port[3:0]=0h (Dual Cast Source Station/Port = 0)
   Dual Cast Source Destination Port[7:4]=8h (Dual Cast Destination Port = 8)
   Dual Cast Source Destination Port[8]=1 (Dual Cast on Station 0, Port 0 only)
   –or–
   Dual Cast Source Destination Port[8]=0 (Dual Cast on Station 0, Ports 0 and 1)

At this point, all Write TLPs entering the PEX 8624 by way of Port 0, having addresses in the range AAA0_0000h to AAAF_FFFFh, will be copied to memory at Base address BBB0_0000h. To verify that Dual Cast is enabled, try Clearing memory at address BBB0_0000h, then write a non-zero pattern to memory at address AAA0_0000h. A read of memory at BBB0_0000h should now show what was written at address AAA0_0000h.

8.8.5 Dual Cast to a Non-Transparent Destination Port

When the Dual Cast Destination Port is configured as Non-Transparent (NT), the Dual Cast Copy TLPs do not use the same Address Translation mechanism as original unicast TLPs that are routed to that Port. Where a unicast TLP uses the Address Translation mechanism in the NT Port (NT BAR), Dual Cast Copy TLPs are sent directly to the NT Port's Egress queue. Therefore, in applications where the Dual Cast Destination Port is the NT Port, the **Dual Cast Low/High BAR*x* Translation** registers must be loaded with the physical Base address of the destination memory in the NT address domain.

8.8.6 Error Reporting of Failed Dual Cast Cycles

If either the PCI address-routed destination device or the device connected to the Dual Cast Destination Port fails to return an ACK for the Dual Casted Memory Write, the standard PCI Express Correctable Errors (Replay Timer Timeout on first transmission attempt, Replay Rollover Status after four failed attempts) are reported.

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Chapter 9 Interrupts

9.1 Interrupt Support

The PEX 8624 supports the PCI Express interrupt model, which uses two mechanisms:

- INT*x* Interrupt Message-type emulation (compatible with the *PCI r3.0*-defined Interrupt signals)
- Message Signaled Interrupt (MSI), when enabled

For Conventional PCI compatibility, the PCI INT*x* emulation mechanism is used to signal interrupts to the System Interrupt Controller. This mechanism is compatible with existing PCI software, provides the same level of service as the corresponding PCI interrupt signaling mechanism, and is independent of System Interrupt Controller specifics. The PCI INT*x* emulation mechanism virtualizes PCI physical Interrupt signals, by using an in-band signaling mechanism, for the assertion and de-assertion of INT*x* interrupt signals.

In addition to PCI INT*x*-compatible interrupt emulation, the PEX 8624 supports the MSI mechanism. The PCI Express MSI mechanism is compatible with the MSI Capability defined in the *PCI r3.0*.

INT*x* and MSIs are mutually exclusive, on a per-Port basis; either can be enabled in a system (depending upon which interrupt type the system software supports), but never concurrently within the same domain. (Refer to the **PCI Command** register *Interrupt Disable* bit, offset 04h[10], and **MSI Capability** register, offset 48h, respectively.) The PEX 8624 does not convert received INT*x* Messages to MSI Messages.

The PEX 8624's external Interrupt output, PEX_INTA#, indicates the assertion and/or de-assertion of the internally generated INT*x* signal:

- **Non-Hot Plug-triggered interrupts** – PEX_INTA# assertion is controlled by the following **ECC Error Check Disable** register bits:
  - *Enable PEX_INTA# Interrupt Output(s) for NT-Virtual Doorbell-Generated Interrupts* bit (NT Port Virtual Interface, or Port 0 if Port 0 is the NT Port, offset 1C8h[7], NT mode only)
  - *Enable PEX_INTA# Interrupt Output(s) for GPIO-Generated Interrupts* bit (offset 1C8h[6])
  - *Enable PEX_INTA# Interrupt Output(s) for Device-Specific Error- and Event-Triggered Interrupts* bit (Port 0 (or if in NT mode, NT Port Virtual Interface, or Port 0 if Port 0 is the NT Port), offset 1C8h[5])

  When any of these bits are Set, Device-Specific errors and events trigger PEX_INTA# assertion; however, PEX_INTA# assertion and INT*x* Message generation are mutually exclusive, on a per-Station basis.
- **Hot Plug or Link State-triggered INT*x* events** – PEX_INTA# assertion is controlled by the **ECC Error Check Disable** register *Enable PEX_INTA# Interrupt Output(s) for Hot Plug or Link State Event-Triggered Interrupts* bit (offset 1C8h[4]). When this bit is Set, Hot Plug or Link State events trigger PEX_INTA# assertion; however, an INT*x* Message is not generated in this case. PEX_INTA# assertion and INT*x* Message generation for Hot Plug or Link State cases are mutually exclusive, on a per-Station basis.

The NT Port Virtual and Link Interfaces can each independently support the interrupt mechanism (INT*x* or MSI) used in their respective domains. (Refer to Section 13.5, "NT Port Interrupts," for details.)

9.1.1 Interrupt Sources or Events

The PEX 8624 internally generated interrupt/Message sources include:

- For Hot Plug-capable Ports
  - Presence Detect Changed (logical OR of PRSNT# (HP_PRSNT_*x*# or I/O Expander PRSNT# input), and SerDes Receiver Detect[a] on Lane(s) associated with that Port)
  - Attention Button Pressed
  - Power Fault Detected
  - MRL Sensor Changed
  - Command Completed
  - Link Bandwidth Management Status
  - Link Autonomous Bandwidth Status
- For non-Hot Plug-capable downstream Ports
  - Presence Detect Changed (SerDes Receiver Detect[a] on Lane(s) associated with that Port)
  - Data Link Layer State Changed
- Device-Specific errors (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, unless noted otherwise):
  - Payload Link List RAM 1-Bit ECC error (offset 1C0h[2:0])
  - Payload Link List RAM 2-Bit ECC error (offset 1C0h[5:3])
  - Ingress Link List RAM 1-Bit ECC error (offset 1C0h[6])
  - Ingress Link List RAM 2-Bit ECC error (offset 1C0h[7])
  - Packet RAM 0 1-Bit ECC error (offset 1C0h[13:8])
  - Packet RAM 0 2-Bit ECC error (offset 1C0h[19:14])
  - Packet RAM 1 1-Bit ECC error (offset 1C0h[25:20])
  - Packet RAM 1 2-Bit ECC error (offset 1C0h[31:26])
  - Egress Completion FIFO Overflow (All Ports, offset 1CCh[0])
  - Destination Queue Linked List RAM 2-Bit ECC error (offset 1CCh[4])
  - Destination Queue Linked List RAM 1-Bit ECC error (offset 1CCh[6])
  - Source Queue Linked List RAM 1-Bit ECC error (offset 1CCh[8])
  - Source Queue Linked List RAM 2-Bit ECC error (offset 1CCh[9])
  - Retry Buffer 1-Bit ECC error (offset 1CCh[10])
  - Retry Buffer 2-Bit ECC error (offset 1CCh[11])
  - Header (TLP ID) RAM 2-Bit ECC error (offset 1CCh[22:20])
  - Header (TLP ID) RAM 1-Bit ECC error (offset 1CCh[26:24])
  - NT-Link Port Correctable error (NT Port Link Interface, offset FC4h)
  - NT-Link Port Uncorrectable error (NT Port Link Interface, offset FB8h)
  - NT-Link Port Data Link Layer State change
  - NT-Link Port received (and consequently dropped) a Fatal or Non-Fatal Error Message
- General-Purpose Input/Output (GPIO) events
- Non-Transparent-Virtual (NT-Virtual) Doorbell events (refer to Section 13.5, "NT Port Interrupts")

*a. The SerDes Receiver Detect mechanism is comprised of the **Physical Layer Receiver Detect Status** register's Receiver Detected on Lane x bits (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 200h[31:16]) or Hot Plug PRSNT# (from external I^2C I/O Expander) input for the Port.*

The PEX 8624 externally generated interrupt/Message sources include INT*x* Messages from downstream devices.

Table 9-1 lists the interrupt sources.

Table 9-1. Interrupt Sources

Event/Error	Description
Hot Plug or Link State events	**Slot Status** register (Downstream Ports, offset 80h): • *Presence Detect Changed* (bit 19 is Set) • *Data Link Layer State Changed* (bit 24 is Set)
PCI Express Hot Plug events	The master control of Hot Plug interrupt is the **Slot Control** register *Hot Plug Interrupt Enable* bit (Transparent downstream Ports, offset 80h[5]). There are six sources of Hot Plug interrupt. Each Hot Plug source has its own *Enable* bit in the **Slot Control** register: • *Attention Button Pressed* (bit 16) • *Power Fault Detected* (bit 17) • *MRL Sensor Changed* (bit 18) • *Presence Detect Changed* (bit 19) • *Command Completed* (bit 20) • *Data Link Layer State Changed* (bit 24) The interrupt status of each Hot Plug source is provided by the Port's **Slot Status** register (offset 80h). ***Note:*** *Presence (Presence Detect State, offset 80h[22], in each Transparent downstream Port) is determined by the logical OR of:* • *SerDes Receiver Detect (**Physical Layer Receiver Detect Status** register Receiver Detected on Lane x bits (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 200h[31:16])), and* • *HP_PRSNT_x# –or–* • *PRSNT# (from external I^2C I/O Expander) input for the Port*
General-Purpose Input Interrupt events	External interrupt from any of the GPIO[19:12] and PEX_PORT_GOOD*x*# signals that are configured as an Interrupt input in the **GPIO 0_9 Direction Control** and **GPIO 10_19 Direction Control** register *Direction Control* bit(s) (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 62Ch and 630h, respectively).

Table 9-1. Interrupt Sources *(Cont.)*

Event/Error	Description
Device-Specific errors	• Egress Completion FIFO Overflow error indicated by the Port's **Error Handler 32-Bit Error Status** register *Completion FIFO Overflow Status* bit (offset 1CCh[0]), if not masked by the Port's **Error Handler 32-Bit Error Mask** register *Completion FIFO Overflow Mask* bit (offset 1D0h[0]). • Device-Specific errors indicated by the **Device-Specific Error Status for Egress ECC Error** register bit(s), if not masked in their corresponding **Device-Specific Error Mask for Egress ECC Error** register bit(s) (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 1C0h[31:0] and 1C4h[31:0], respectively). • Device-Specific errors indicated by the **Error Handler 32-Bit Error Status** register, if not masked in the **Error Handler 32-Bit Error Mask** register (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 1CCh[26:4] and 1D0h[26:4], respectively). • NT Port Link Interface Correctable errors reported by the NT Port Virtual Interface (to the Host of the upstream Port domain), collectively flagged in the **Link Error Status Virtual** register *Link Side Correctable Error Status* bit (NT Port Virtual Interface, offset FE0h[0]), with specific errors indicated in the **Correctable Error Status** register (NT Port Link Interface, offset FC4h), if not masked both globally in the **Link Error Mask Virtual** register *Link Side Correctable Error Mask* bit (NT Port Virtual Interface, offset FE4h[0]), nor individually in the **Correctable Error Mask** register (NT Port Link Interface, offset FC8h). • NT Port Link Interface Uncorrectable errors reported by the NT Port Virtual Interface (to the Host of the upstream Port domain), collectively flagged in the **Link Error Status Virtual** register *Link Side Uncorrectable Error Status* bit (NT Port Virtual Interface, offset FE0h[1]), with specific errors indicated in the **Uncorrectable Error Status** register (NT Port Link Interface, offset FB8h), if not masked both globally in the **Link Error Mask Virtual** register *Link Side Uncorrectable Error Mask* bit (NT Port Virtual Interface, offset FE4h[1]), nor individually in the **Uncorrectable Error Mask** register (NT Port Link Interface, offset FBCh). • NT Port Link Interface State change – Interrupt to the NT Port Virtual Interface Host, if enabled (not masked) by the **Link Error Mask Virtual** register *Link Side DL Active Change Mask* bit (NT Port Virtual Interface, offset FE4h[2]). • Link Side Uncorrectable Error Message Drop interrupt to the NT Port Virtual Interface Host, if enabled (not masked) by the **Link Error Mask Virtual** register *Link Side Uncorrectable Error Message Drop Mask* bit (NT Port Virtual Interface, offset FE4h[3]). This feature supports applications using back-to-back NT Ports, where an Uncorrectable Error Message received (and properly dropped) by the NT Port Link Interface can trigger an interrupt to the NT Port Virtual Interface Host.

Table 9-1. Interrupt Sources *(Cont.)*

Event/Error	Description
NT-Virtual Doorbell events	**NT Virtual Interface IRQ Set/Clear** register (offsets C4Ch[15:0] and/or C50h[15:0]) bit is Set while the corresponding **NT Virtual Interface IRQ Set/Clear** register (offsets C54h[15:0] and/or C58h[15:0]) bit is Cleared.
NT-Link Doorbell events	**NT Link Interface IRQ Set/Clear** register (offsets C5Ch[15:0] and/or C60h[15:0]) bit is Set while the corresponding **NT Link Interface IRQ Set/Clear** register (offsets C64h[15:0] and/or C68h[15:0]) bit is Cleared.
Device-Specific NT Port Link Interface errors and events	• NT Port Link Interface Correctable errors reported by the NT Port Virtual Interface (to the Host of the upstream Port domain), collectively flagged in the **Link Error Status Virtual** register *Link Side Correctable Error Status* bit (NT Port Virtual Interface, offset FE0h[0]), with specific errors indicated in the **Correctable Error Status** register (NT Port Link Interface, offset FC4h), if not masked both globally in the **Link Error Mask Virtual** register *Link Side Correctable Error Mask* bit (NT Port Virtual Interface, offset FE4h[0]), nor individually in the **Correctable Error Mask** register (NT Port Link Interface, offset FC8h). • NT Port Link Interface Uncorrectable errors reported by the NT Port Virtual Interface (to the Host of the upstream Port domain), collectively flagged in the **Link Error Status Virtual** register *Link Side Uncorrectable Error Status* bit (NT Port Virtual Interface, offset FE0h[1]), with specific errors indicated in the **Uncorrectable Error Status** register (NT Port Link Interface, offset FB8h), if not masked both globally in the **Link Error Mask Virtual** register *Link Side Uncorrectable Error Mask* bit (NT Port Virtual Interface, offset FE4h[1]), nor individually in the **Uncorrectable Error Mask** register (NT Port Link Interface, offset FBCh). • NT Port Link Interface State change – Interrupt to the NT Port Virtual Interface Host, if enabled (not masked) by the **Link Error Mask Virtual** register *Link Side DL Active Change Mask* bit (NT Port Virtual Interface, offset FE4h[2]). • Link Side Uncorrectable Error Message Drop interrupt to the NT Port Virtual Interface Host, if enabled (not masked) by the **Link Error Mask Virtual** register *Link Side Uncorrectable Error Message Drop Mask* bit (NT Port Virtual Interface, offset FE4h[3]). This feature supports applications using back-to-back NT Ports, where an Uncorrectable Error Message received (and properly dropped) by the NT Port Link Interface can trigger an interrupt to the NT Port Virtual Interface Host.

9.1.2 Interrupt Handling

The PEX 8624 provides an Interrupt Generation module with each Port. The module reads the Request for interrupts from different sources and generates an MSI or PCI-compatible Assert_INT*x*/ Deassert_INT*x* Interrupt Message. MSIs support a PCI Express edge-triggered interrupt, whereas Assert_INT*x* and Deassert_INT*x* Message transactions emulate PCI level-triggered interrupt signaling. The System Interrupt Controller functions include:

- Sensing Interrupt events
- Signaling the interrupt, by way of the INT*x* mechanism, and Setting the *Interrupt Status* bit
- Signaling the interrupt, by way of the MSI mechanism
- Handling INT*x*-type Interrupt Messages from downstream devices

9.2 INT*x* Emulation Support

The PEX 8624 supports PCI INT*x* emulation, to signal interrupts to the System Interrupt Controller. This mechanism is compatible with existing PCI software. PCI INT*x* emulation virtualizes PCI physical Interrupt signals, by using the in-band signaling mechanism.

PCI **Interrupt** registers (defined in the *PCI r3.0*) are supported. The *PCI r3.0* **PCI Command** register *Interrupt Disable* and **PCI Status** register *Interrupt Status* bits are also supported (offset 04h[10 and 19], respectively).

Although the *PCI Express Base r2.0* provides INTA#, INTB#, INTC#, and INTD# for INT*x* signaling, the PEX 8624 uses only INTA# for internal Interrupt Message generation, because it is a single-function device. However, incoming Messages from downstream devices can be of INTA#, INTB#, INTC#, or INTD# type. Internally generated INTA# Messages from the downstream Port are also re-mapped and collapsed at the upstream Port, according to the downstream Port's Device Number, with its own Device Number and Received Device Number from the downstream device.

When an interrupt is requested, the **PCI Status** register *Interrupt Status* bit is Set. If INT*x* interrupts are enabled (**PCI Command** register *Interrupt Disable* and **MSI Control** register *MSI Enable* bits, offsets 04h[10] and 48h[16], respectively, are both Cleared), an Assert_INT*x* Message is generated and transmitted upstream to indicate the Port interrupt status. For each interrupt event, there is a corresponding *Interrupt Mask* bit; an Interrupt Message can be generated only when the corresponding *Interrupt Mask* bit is Cleared. Software reads and Clears the event and *Interrupt Status* bit after servicing the interrupt.

A Port de-asserts INT*x* or PEX_INTA# interrupts, in response to one or more of the following conditions:

- Port's **PCI Command** register *Interrupt Disable* bit (offset 04h[10]) is Set
- Corresponding *Interrupt Mask* bit is Set
- Upstream Port Link goes down (DL_Down condition), or receives a Hot Reset (unless Hot Reset/ DL_Down Reset is disabled, by Setting the **Debug Control** register *Upstream Port and NT-Link DL_Down Reset Propagation Disable* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1DCh[20]))
- Software Clears the corresponding *Interrupt Status* bit

9.2.1 INT*x*-Type Interrupt Message Re-Mapping and Collapsing

The upstream Port re-maps and collapses the INT*x virtual wires* received at the downstream Port, based upon the downstream Port's Device Number and Received INT*x* Message Requester ID Device Number, and generates a new Interrupt Message, according to the mapping defined in Table 9-2.

Each virtual PCI-to-PCI bridge of a downstream Port specifies the Port Number associated with the INT*x* (Interrupt) Messages received or generated, and forwards the Interrupt Messages upstream.

A downstream Port transmits an Assert_INTA/Deassert_INTA Message to the upstream Port, due to a Hot Plug or PCI Express Hot Plug, Link State, GPIO, or NT Port Doorbell interrupt, and/or Device-Specific error/event.

Internally generated INT*x* Messages always originate as type INTA Messages, because the PEX 8624 is a single-function device. Internally generated Interrupt INTA Messages from downstream Ports are re-mapped at the upstream Port to INTA, INTB, INTC, or INTD Messages, according to the mapping defined in Table 9-2.

INT*x* Messages from downstream devices and from internally generated Interrupt Messages are ORed together to generate INTA, INTB, INTC, or INTD level-sensitive signals, and edge-detection circuitry in the upstream Port generates the Assert_INT*x* and Deassert_INT*x* Messages. The upstream Port then forwards the new Messages upstream, by way of its Link.

Table 9-2. Downstream/Upstream Port INT*x* Interrupt Message Mapping

Device Number	At Downstream Port	By Upstream Port
0, 8	INTA	INTA
	INTB	INTB
	INTC	INTC
	INTD	INTD
1, 5, 9	INTA	INTB
	INTB	INTC
	INTC	INTD
	INTD	INTA
6	INTA	INTC
	INTB	INTD
	INTC	INTA
	INTD	INTB

9.3 MSI Support

One of the interrupt schemes supported by the PEX 8624 is the MSI mechanism, which is required for PCI Express devices. The MSI method uses Memory Write transactions to deliver interrupts. MSIs are edge-triggered interrupts.

Note: *MSIs and INTx are mutually exclusive, on a per-Port basis. The mechanisms that generate these types of interrupts* ***cannot*** *be simultaneously enabled.*

9.3.1 MSI Operation

At configuration time, system software traverses the function Capability list. If a Capability ID of 05h is found, the function implements MSIs. System software reads the **MSI Capability** structure registers, to determine function capabilities.

The **MSI Control** register *Multiple Message Capable* field (offset 48h[19:17]) default value is 010b, which indicates that the PEX 8624 requests up to four MSI Vectors (Address and Data). When the register's *Multiple Message Enable* field (offset 48h[22:20]) is Cleared (default), only one Vector is allocated, and therefore, the PEX 8624 can generate only one Vector for all errors or events. When system software writes a non-zero value to the *Multiple Message Enable* field, multiple-Vector support is enabled (the number of Vectors supported is dependent upon the value). Table 9-3 lists the four supported MSI Vector types.

Table 9-3. Supported MSI Vector Types

Vector Type	Modes	
	Transparent	NT
Power Management, or Hot Plug or Link State events	✔	✔
Device-Specific errors and events	✔	✔
GPIO interrupts	✔	✔
NT Doorbell interrupts		✔

System software initializes the MSI Address registers (offsets 4Ch and 50h) and **MSI Data** register (offset 54h), with a system-specified Vector. After system software enables the MSI function (by Setting the **MSI Control** register *MSI Enable* bit, offset 48h[16]), when an Interrupt event occurs, the Interrupt Generation module generates a DWord Memory Write to the address specified by the **MSI Address** (lower 32 bits of the *Message Address* field) and **MSI Upper Address** (upper 32 bits of the *Message Address* field) register contents (offsets 4Ch and 50h, respectively). The single DWord Payload includes zero (0) for the upper two bytes, and the lower two bytes are taken from the **MSI Data** register. The **MSI Control** register *Multiple Message Enable* field (offset 48h[22:20]) can be programmed to a value of 000b, 001b, or 010b. When programmed to 010b, the lower three bits of Message data are changed to indicate the general type of interrupt event that occurred. (Refer to Table 9-3.)

The number of MSI Vectors generated is dependent upon the quantity enabled, as follows:

- If **one** MSI Vector is enabled (default), all interrupt categories generate the same MSI Vector
- If **two** MSI Vectors are enabled, Device-Specific errors and events generate their own MSI Vector, while all other categories are combined and generate the same Vector
- If **four** MSI Vectors are enabled, each interrupt category generates its own MSI Vector

If a non-masked Interrupt event occurs before system software Sets the *MSI Enable* bit, normally (but unlike Conventional PCI interrupts, which are level-triggered), an MSI packet is sent immediately after software Sets the *MSI Enable* bit, to notify the system of the prior event. Alternatively, MSIs for prior events can be disabled, on a per-Port basis, by Setting the **ECC Error Check Disable** register *Disable Sending MSI if MSI Is Enabled after Interrupt Status Set* bit (offset 1C8h[8]).

When the error or event that caused the interrupt is serviced, the PEX 8624 can generate a new MSI Memory Write as a result of new events. Because an MSI is an edge-triggered event, four bits are provided for masking the events (**MSI Mask** register *Interrupt Mask* bits, offset 58h[3:0]). A new MSI can be generated only after the *Interrupt Mask* bits are serviced. System software should mask these bits when the MSI event is being processed.

The **MSI Control** register *MSI 64-Bit Address Capable* bit (offset 48h[23]) is enabled, by default. If the serial EEPROM or I^2C Clears the bit, the **MSI Capability** structure is reduced by 1 DWord (*that is*, register offsets 54h, 58h, and 5Ch change to 50h, 54h, and 58h, respectively).

9.3.2 MSI Capability Registers

For details, refer to Section 12.8, "MSI Capability Registers (Offsets 48h – 64h)."

9.4 PEX_INTA# Interrupts

PEX_INTA# Interrupt output is enabled when the following conditions exist:

- INT*x* Messages are enabled (**PCI Command** register *Interrupt Disable* bit, offset 04h[10], is Cleared), and MSIs are disabled (**MSI Control** register *MSI Enable* bit, offset 48h[16], is Cleared), and
- PEX_INTA# output is enabled for the following errors and events, when the **ECC Error Check Disable** register bit associated with that error or event is Set:
  - *Enable PEX_INTA# Interrupt Output(s) for NT-Virtual Doorbell-Generated Interrupts* bit (NT Port Virtual Interface, or Port 0 if Port 0 is the NT Port, offset 1C8h[7], NT mode only)
  - *Enable PEX_INTA# Interrupt Output(s) for GPIO-Generated Interrupts* bit (offset 1C8h[6])
  - *Enable PEX_INTA# Interrupt Output(s) for Device-Specific Error- and Event-Triggered Interrupts* bit (Port 0 (or if in NT mode, NT Port Virtual Interface, or Port 0 if Port 0 is the NT Port), offset 1C8h[5])
  - **ECC Error Check Disable** register *Enable PEX_INTA# Interrupt Output(s) for Hot Plug or Link State Event-Triggered Interrupts* bit (offset 1C8h[4])

The three interrupt mechanisms, listed below, are mutually exclusive modes of operation, on a per-Port basis, for all interrupt sources:

- Conventional PCI INT*x* Message generation
- Native MSI transaction generation
- Device-Specific PEX_INTA# assertion

PEX_INTA# assertion (Low) indicates that the PEX 8624 detected one or more of the events and/or errors (if not masked) listed in Table 9-1.

Note: *PEX_INTA# assertion and INTx messaging are mutually exclusive for a given interrupt event. When MSIs are enabled (offset 48h[16], is Set), both PEX_INTA# and INTx are disabled for PEX 8624 internally generated interrupts. The forwarding of external INTx Messages received from a downstream Port to the upstream Port is always enabled.*

9.5 General-Purpose Input/Output

The PEX 8624 contains 20 GPIO balls, in two groups. Default functionality is programmed by the STRAP_TESTMODE[3:0] inputs, and can be selectively changed by software, serial EEPROM, and/or I^2C.

- The first group is comprised of 12 balls – PEX_PORT_GOOD*x*# (enabled Ports only) and GPIO[11, 10, 7, 4:2] indicators – each of which can be used as GPIO or Interrupt inputs
- The second group is comprised of 8 balls – GPIO[19:12] – each of which can be used as GPIO, Interrupt inputs, or Serial Hot Plug PERST# outputs

Table 9-4 lists the registers used for GPIO functionality.

Table 9-4. Registers Used for GPIO Functionality

Register Offset	Register Name
62Ch	**GPIO 0_9 Direction Control**
630h	**GPIO 10_19 Direction Control**
638h	**GPIO 0_19 Input De-Bounce**
63Ch	**GPIO 0_11 Input Data**
640h	**GPIO 12_19 Input Data**
644h	**GPIO 0_11 Output Data**
648h	**GPIO 12_19 Output Data**
64Ch	**GPIO 0_19 Interrupt Polarity**
650h	**GPIO 0_19 Interrupt Status**
654h	**GPIO 0_19 Interrupt Mask**

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Chapter 10 Hot Plug Support

10.1 Introduction

Note: *In this chapter, unless stated otherwise, "Hot Plug Controller" references both the Parallel and Serial Hot Plug Controllers.*

Hot Plug capability allows board insertion and removal from a running system, without adversely affecting the system. Boards are typically inserted or removed to repair faulty boards or re-configure the system without system down time. Hot Plug capability allows systems to isolate faulty boards in the event of a failure.

Each PEX 8624 Transparent downstream Port includes a Hot Plug Controller. Each Station in the PEX 8624 includes one set of 10 Hot Plug signals that can be associated to any single Port within that Station (default association is to Ports 1, 5, and 9, except when a Station is configured as a single x8 Port, default association is to that single Port in the Station, as indicated by the yellow highlighted cells in Table 4-1, "Port Configurations"). If more than one Port per Station requires Hot Plug signals, the additional Ports can use an external I^2C I/O Expander (one 16-pin Maxim MAX7311, NXP PCA9555, or TI PCA9555 per slot, –or–, if a programmed serial EEPROM is present, one 40-pin NXP PCA9698 per two slots), to provide the external signals (11 pins for Hot Plug, 4 pins for Slot ID, and 1 pin as General-Purpose Input/Output (GPIO)).

Hot Plug signals are enabled, configured, and accessed through the **Slot Capability** and **Slot Status and Control** registers (offsets 7Ch and 80h, respectively), in each Port. Also, each Port's **Power Management Hot Plug User Configuration** register (offset 1E0h) provides additional Device-Specific configuration and control, for both Parallel and Serial Hot Plug implementations.

10.2 Hot Plug Features

The following are the PEX 8624 Hot Plug features:

- Hot Plug features are supported on all Transparent downstream Ports.
- Each Station provides one set of Hot Plug signals, for use by one Transparent downstream Port in the Station.
- Additional Hot Plug signals for all other Transparent downstream Ports are implemented with external I^2C I/O Expanders, which alert the PEX 8624 through the SHPC_INT# input, that inputs have toggled, and the PEX 8624 internal Hot Plug Controllers and registers automatically communicate with and control the I/O Expanders, using the PEX 8624 I^2C Master interface (I2C_SCL1 and I2C_SDA1 balls).
- Insertion and removal of PCI Express boards, without removing system power.
- Board Present and Manually operated Retention Latch (MRL) signals are implemented. Presence Detect is accomplished through either an in-band SerDes Receiver Detect mechanism (**Physical Layer Receiver Detect Status** register *Receiver Detected on Lane x* bits (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 200h[31:16])) –or– by using the HP_PRSNT_*x*# inputs.
- Power Indicator and Attention Indicator Output signals are controlled.
- Attention Button is monitored.
- Power Fault detection and Faulty board isolation.
- Power Controller Control bit for controlling downstream device power.
- Generates PME for Hot Plug events in sleeping systems (D3hot Device Power Management (PM) state).
- Electromechanical Interlock Control feature available on Serial Hot Plug-capable Ports.
- Hot Plug interrupts can be sent in-band using INT*x* or MSI Messages, or signaled externally using PEX_INTA#.

10.3 Hot Plug Elements

Table 10-1 summarizes the Hot Plug elements required for PCI Express Hot Plug implementation. For specific platform requirements, refer to the PCI Express Form Factor specifications.

Table 10-1. Required Hot Plug Elements for PCI Express Implementation

Element	Purpose
Attention Button	Used for requesting Hot Plug operations. Implemented on the PEX 8624's Hot Plug-capable Transparent downstream Ports.
Attention Indicator	Implemented on the PEX 8624's Hot Plug-capable Transparent downstream Ports. LED functions: • **Off** – Standard operation. • **On** – Operational Problem at this slot. • **Blinking** – Slot is being identified at user's request. Blinking frequency is 1 Hz. 50% duty cycle.
Power Indicator	Implemented on the PEX 8624's Hot Plug-capable Transparent downstream Ports. LED functions: • **Off** – Slot is powered off. Board insertion or removal is permitted. • **On** – Board insertion or removal is not permitted. • **Blinking** – Slot is in the process of powering up or down. Blinking frequency is 2 Hz. 50% duty cycle.
MRL	Manually-operated Retention Latch, that holds add-in boards in place.
MRL Sensor	Reports the position of a slot's MRL to the Port. A logic Low indicates that the latch is closed.
Electromechanical Interlock	Prevents removal of adapter from slot.

10.4 Hot Plug Signals

10.4.1 Hot Plug Port External Signals

The on-chip signals for Parallel Hot Plug Controller support are defined in Section 3.4.2.1, "Parallel Hot Plug Signals."

The on-chip signals for Serial Hot Plug Controller support are defined in Section 3.4.2.2, "Serial Hot Plug Signals."

In addition to the set of on-chip Serial Hot Plug signals for any one Port per Station, the PEX 8624 supports Serial Hot Plug signals to and from the I^2C I/O Expander, which are used with Serial Hot Plug-capable Transparent downstream Ports. (Refer to Section 10.8.2.) Also, although the I^2C I/O Expander provides a Reset output (Serial Hot Plug PERST#), control through the serial interface is too slow for Reset functionality. As a result, the PEX 8624 provides GPIO signals that can be configured for Serial Hot Plug PERST# functionality, to replace the I/O Expander PERST# output. (Refer to the GPIO[19:12] signal description in Table 3-11, "Device-Specific Signals.")

10.4.2 Hot Plug Output States for Disabled Hot Plug Slots

When a Hot Plug slot is disabled, the Hot Plug Output balls for that Port are in the logic states defined in Table 10-2.

Table 10-2. Hot Plug Outputs for Disabled Hot Plug Slot

Output Signal	Logic	Comments
HP_ATNLED_*x*#	High	Attention LED is turned Off
HP_CLKEN_*x*#	High	Reference Clock is not driven to the slot
HP_PERST_*x*#	Low	Slot remains in reset
HP_PWREN_*x*	Low	Power Controller is turned Off
HP_PWRLED_*x*#	High	Power LED is turned Off

10.5 Hot Plug Registers

All Transparent downstream Ports and Stations include identical sets of Hot Plug registers, and all Hot Plug Ports use the identical register sets, regardless of whether Hot Plug is implemented using the PEX 8624 Hot Plug signals, or Serial Hot Plug signals on the external I^2C I/O Expanders. Therefore, other than initial configuration (typically programmed by serial EEPROM), whether Hot Plug functionality for a Port is implemented using a Parallel Hot Plug Controller or Serial Hot Plug Controller (with external I^2C I/O Expander) is effectively transparent to software.

The PCI Express Hot Plug Configuration, Capability, Command, Status, and Event registers are described in Section 12.9, "PCI Express Capability Registers (Offsets 68h – A0h)."

Device-Specific Hot Plug configuration features are programmable in register offset 1E0h of each Station and Transparent downstream Port.

10.6 Hot Plug Interrupts

Refer to Chapter 9, "Interrupts," for interrupt details.

10.7 Hot Plug Controller Slot Power-Up/Down Sequence

If a Hot Plug-capable Transparent downstream Port is enabled, the Port's Hot Plug Controller can power-up or power-down the slot. This section describes how this process occurs.

10.7.1 Slot Power-Up Sequence

If a Hot Plug-capable Transparent downstream Port is connected to a slot, its associated Hot Plug Controller can power up that slot, with or without an external serial EEPROM. Hot Plug Controller sequencing is determined by the states of the following bits:

- **Slot Capability** register *Power Controller Present* bit (offset 7Ch[1])
- **Slot Capability** register *MRL Sensor Present* bit (offset 7Ch[2])
- **Slot Control** register *Power Controller Control* bit (offset 80h[10])

and the HP_MRL_*x*# input state, if the *MRL Sensor Present* bit is Set. Hot Plug-configurable features are programmable only by the serial EEPROM and/or I^2C.

10.7.1.1 Configuring Slot Power-Up Sequence Features with Serial EEPROM

An external serial EEPROM can be used to configure the Hot Plug Controller and Hot Plug outputs. Features can be changed by using the registers defined in Table 10-3. The Hot Plug Controller outputs remain in the default state described in Table 10-2, before the serial EEPROM image is loaded into the device.

After the serial EEPROM image is loaded, the Hot Plug Controller starts a power-up sequence on each slot that has the **Slot Capability** register *Power Controller Present* bit (offset 7Ch[1]) Set and the **Slot Control** register *Power Controller Control* bit (offset 80h[10]) Cleared.

Table 10-3. Configuring Slot Power-Up Sequence Features with Serial EEPROM

Register Bit	Hot Plug Controller and Hot Plug Output Signal Configurable Features
Power Controller Present (**Slot Capability** register, offset 7Ch[1])	***Reserved*** for the upstream Port and NT Port. The *Power Controller Present* bit enables or disables the Hot Plug Controller on the PEX 8624 Hot Plug-capable Transparent downstream Ports. If the *Power Controller Present* bit is Cleared, the Hot Plug Controller is disabled for that slot and a power-up sequence is not executed. The slot remains in the disabled state, as defined in Table 10-2. If the *Power Controller Present* bit is Set, the Hot Plug Controller powers up the slot when the MRL is closed and the **Slot Control** register *Power Controller Control* bit (offset 80h[10]) is Cleared. Otherwise, if the *MRL Sensor Present* bit is disabled (Cleared), the MRL's position has no effect on powering up the slot.
MRL Sensor Present (**Slot Capability** register, offset 7Ch[2])	***Reserved*** for the upstream Port and NT Port. When enabled (Set), the PEX 8624 senses whether the MRL is open or closed for a slot. If this bit is Set, the MRL should be Low for power-on for that slot. If this bit is Cleared, the MRL position is "Don't Care" for that slot.
Attention Indicator Present (**Slot Capability** register, offset 7Ch[3])	***Reserved*** for the upstream Port and NT Port. When Set, this bit controls whether the HP_ATNLED_*x*# output for the slot drives out Active-Low. Otherwise, this output is not functional on the slot.
Power Indicator Present (**Slot Capability** register, offset 7Ch[4])	***Reserved*** for the upstream Port and NT Port. When Set, this bit controls whether the HP_PWRLED_*x*# output for the slot drives out Active-Low. Otherwise, this output is not functional on the slot.
HPC Tpepv (**Power Management Hot Plug User Configuration** register, offset 1E0h[4:3])	Functionality associated with this field is enabled only on the downstream Ports. This field indicates the delay from when an HP_PWREN_*x* output is asserted High, to when power is valid at a slot. (Refer to Section 10.7.1.2.) 00b = Feature is disabled, and HP_PWR_GOOD_*x* inputs are used for Power Valid 01b = 128 ms 10b = 256 ms 11b = 512 ms
HP_PWR_GOOD_x Active-Low Enable (**Power Management Hot Plug User Configuration** register, offset 1E0h[6])	Functionality associated with this bit is enabled only on the downstream Ports. Controls the HP_PWR_GOOD_*x* input polarity. (Refer to Section 10.7.1.2.) 0 = HP_PWR_GOOD_*x* inputs are Active-High 1 = HP_PWR_GOOD_*x* inputs are Active-Low

10.7.1.2 Slot Power-Up Sequencing When *Power Controller Present* Bit Is Set

By default, the *Power Controller Present*, *MRL Sensor Present*, and *Power Controller Control* (when the MRL is open) bits are Set on a Hot Plug-capable downstream Port. When the serial EEPROM is not present, present but blank, or programmed with default register values, the Hot Plug Controller is initially powered up, the **PCI Express Capability** register *Slot Implemented* bit (offset 68h[24]) is Set, and the PEX 8624 is in the following state:

1. Hot Plug Controller is enabled for Hot Plug-capable Transparent downstream Port.
2. Slots associated with Hot Plug-capable Transparent downstream Ports are enabled to be powered up.
3. Attention LED (HP_ATNLED_*x*#) and Power LED (HP_PWRLED_*x*#) are High on the slot chassis.

Immediately after the PEX 8624 exits Reset (PEX_PERST# input goes High), if the Hot Plug-capable Transparent downstream Port's *MRL Sensor Present* bit is Set (default), the HP_MRL_*x*# input for that slot is sampled. If HP_MRL_*x*# input is enabled and asserted (value of 0), the device Clears the *Power Controller Control* bit, to enable slot power-up. If the *Power Controller Control* bit is not Cleared, either by initially enabling it (default) and asserting HP_MRL_*x*#, or by Clearing both the serial EEPROM *MRL Sensor Present* and *Power Controller Control* register bits, the downstream slot is not powered up and remains in the disabled state, as defined in Table 10-2.

If a slot's *Power Controller Present* bit is Set, and the *Power Controller Control* bit is Cleared (either by initially enabling and asserting HP_MRL_*x*#, or by programming the *MRL Sensor Present* and *Power Controller Control* bits to 0 in the serial EEPROM), the slot starts power-up sequencing with HP_PWREN_*x* and HP_PWRLED_*x*# assertion, following PEX_PERST# input de-assertion and serial EEPROM initialization. The serial EEPROM initialization delay is determined by the following:

- Serial EEPROM clock (EE_SK) frequency, programmable through the **Serial EEPROM Clock Frequency** register *EepFreq[2:0]* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 268h[2:0])
- Number of registers that are programmed to be initialized by the serial EEPROM

The power-up sequence is as follows:

1. The Hot Plug Controller drives HP_PWRLED_*x*# Low, to turn On the Power Indicator, and drives HP_PWREN_*x* High, to turn On the external Power Controller.
2. After HP_PWR_GOOD_*x* input is sampled asserted High or T_{pepv} delay following HP_PWREN_*x* assertion, power to the slot is valid and the Hot Plug Controller drives HP_CLKEN_*x*# Low, to turn On the Reference Clock (PEX_REFCLKn/p) to the slot. The T_{pepv} time delay is specified by programming the **Power Management Hot Plug User Configuration** register *HPC Tpepv* field (offset 1E0h[4:3]) to a non-zero value. Values of 01b, 10b, or 11b program the delay to 128, 256, or 512 ms, respectively. The default value, 00b, disables the feature, and uses the HP_PWR_GOOD_*x* input instead.
3. After the 100-ms T_{pvperl} time delay following HP_CLKEN_*x*# assertion, the Hot Plug Controller de-asserts HP_PERST_*x*# to release slot reset.

   Consideration should be given to the combination of the serial EEPROM clock (EE_SK) frequency (programmable through the **Serial EEPROM Clock Frequency** register *EepFreq[2:0]* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 268h[2:0])), along with the number of registers to be initialized by serial EEPROM, as well as any delay for cascaded resets through multiple devices, and allow sufficient margin for devices to be ready for Host enumeration.

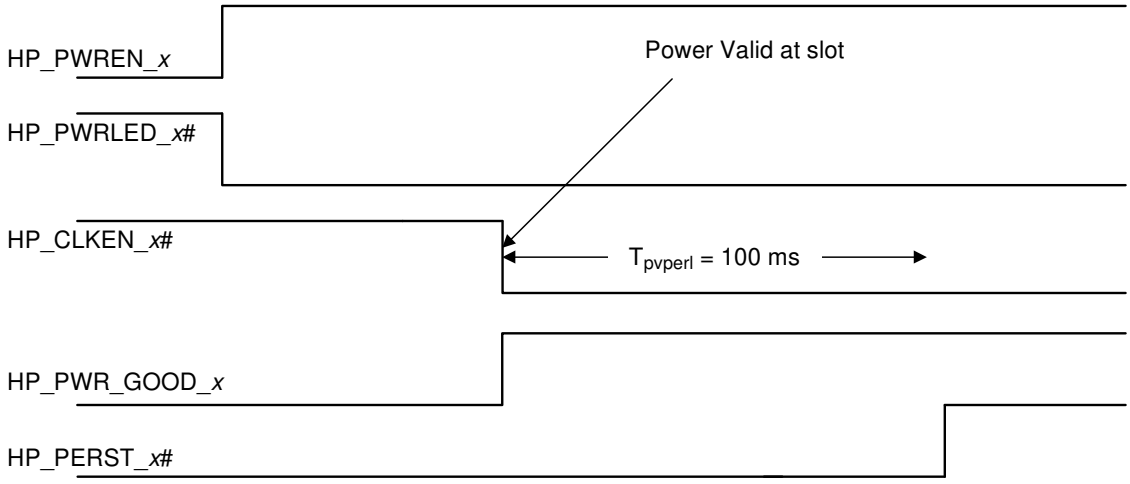
Figure 10-1 illustrates the timing sequence with the *Power Controller Present* bit (offset 7Ch[1]) Set. This timing sequence occurs at system power-up, or when a slot is being powered up by the user, using software control.

If HP_MRL_*x*# is enabled but not asserted to power-up the slot immediately after reset, HP_MRL_*x*# can be asserted at runtime to start the slot power-up sequence, provided that the *MRL Sensor Present* and *Power Controller Present* bits (offset 7Ch[2:1], respectively) are Set (either by default values when the serial EEPROM is not present or blank, or by programming the serial EEPROM to Set these bits), and the *Power Controller Control* bit (offset 80h[10]) is Cleared (either by the programmed serial EEPROM or by software).

Power-up sequencing at runtime is controlled by software Clearing the *Power Controller Control* bit in response to an interrupt caused by HP_MRL_*x*# input assertion (if an MRL Sensor is present, and the **Slot Control** register *Hot Plug Interrupt Enable* and *MRL Sensor Changed Enable* bits (offset 80h[5 and 2], respectively) are Set), and/or by the user pressing the Attention Button, if enabled (**Slot Control** register *Hot Plug Interrupt Enable* and *Attention Button Pressed Enable* bits (offset 80h[5 and 0], respectively) must be Set).

HP_MRL_*x*# and HP_BUTTON_*x*# assertion and de-assertion at runtime are not latched until the 10-ms de-bounce ensures that the state change is stable.

Figure 10-1. Slot Power-Up Timing When *Power Controller Present* Bit Is Set



Note: *HP_PWRLED_x# is not asserted if the serial EEPROM or I^2C Slave interface Clears the Power Indicator Present bit (offset 7Ch[4]).*

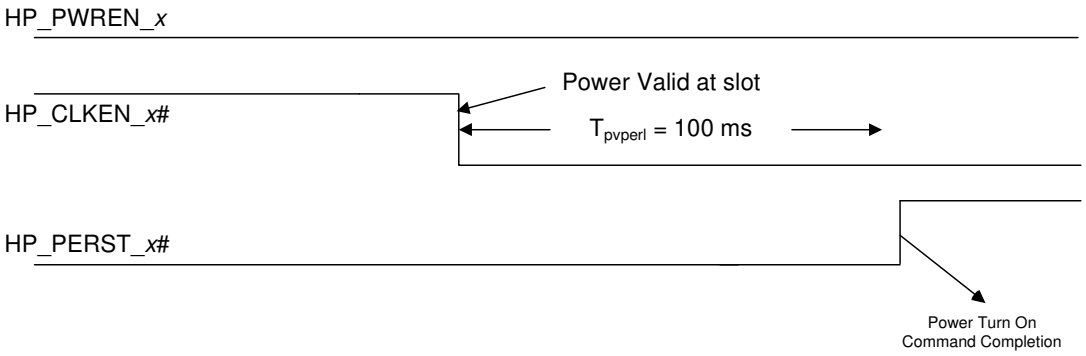
10.7.1.3 HP_PERST_*x*# (Reset) and HP_PWRLED_*x*# Output Power-Up Sequencing When *Power Controller Present* Bit Is Cleared

The HP_PERST_*x*# and HP_PWRLED_*x*# outputs can be used without enabling the Hot Plug Power Controller (HP_PWREN_*x* and HP_CLKEN_*x*# outputs and HP_PWRFLT_*x*# input). *For example*, HP_PERST_*x*# can be used to reset an on-board downstream device.

If the *Power Controller Present* and *Power Controller Control* bits (offsets 7Ch[1] and 80h[10], respectively) are Cleared by the serial EEPROM, HP_PERST_*x*# is de-asserted (High) and HP_PWRLED_*x*# is asserted (Low), after the Root Complex PERST# input is de-asserted, as illustrated in Figure 10-2. However, HP_PWRLED_*x*# is not asserted if the serial EEPROM also Cleared the *Power Indicator Present* bit (offset 7Ch[4]).

If the serial EEPROM is initially blank, causing register default values to be loaded, HP_PERST_*x*# is asserted and HP_PWRLED_*x*# is not asserted unless HP_MRL_*x*# is Low. Therefore, if the HP_PERST_*x*# and/or HP_PWRLED_*x*# outputs are used (and an MRL is ***not*** used), pull HP_MRL_*x*# Low, to allow the outputs to toggle, regardless of whether the serial EEPROM is blank.

Figure 10-2. Hot Plug Outputs When *Power Controller Present* and *Power Controller Control* Bits Are Cleared



Note: *HP_PWRLED_x# is not asserted if the serial EEPROM or I²C Slave interface Clears the Power Indicator Present bit (offset 7Ch[4]).*

10.7.1.4 Disabling Power-Up Hot Plug Output Sequencing

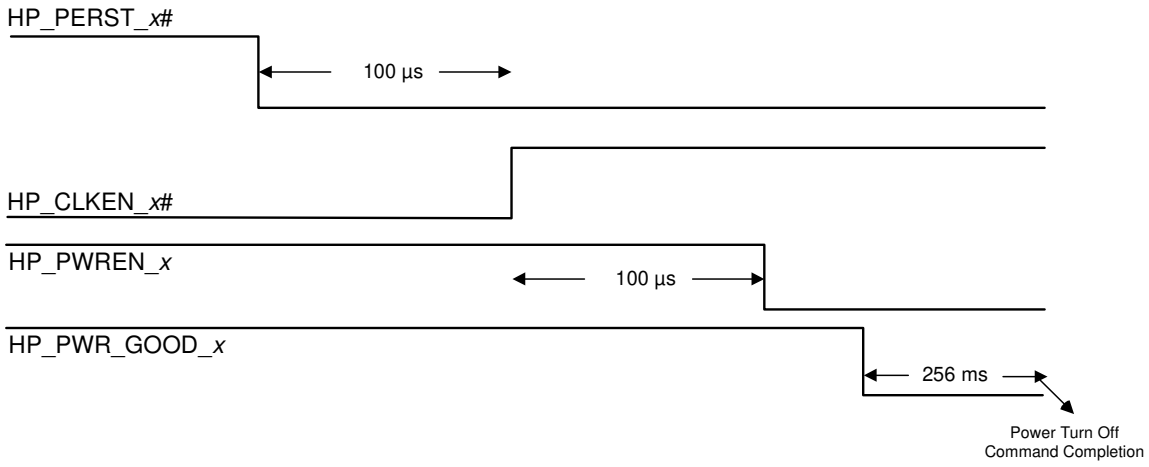
If the *Power Controller Control* bit is Set, after reset using the serial EEPROM, the HP_PWRLED_*x*#, and HP_CLKEN_*x*# outputs remain High, and the HP_PERST_*x*# and HP_PWREN_*x* outputs remain Low. The HP_PWRLED_*x*# and HP_CLKEN_*x*# outputs also remain High if HP_MRL_*x*# is not asserted during the default Hot Plug power-up sequencing described in Section 10.7.1.2.

10.7.2 Slot Power-Down Sequence

Software can power-down slots by Setting the *Power Controller Control* bit (offset 80h[10]). If the *MRL Sensor Present* bit (offset 7Ch[2]) is Set, the Hot Plug Controller automatically powers down the slot if the MRL is open. Figure 10-3 illustrates the following power-down timing sequence for either event:

1. HP_PERST_*x*# to the Port is asserted.
2. HP_CLKEN_*x*# is de-asserted to the slot 100 s after HP_PERST_*x*# is asserted.
3. HP_PWREN_*x* is de-asserted to the slot 100 s after HP_CLKEN_*x*# is de-asserted.

Figure 10-3. Hot Plug Automatic Power-Down Sequence

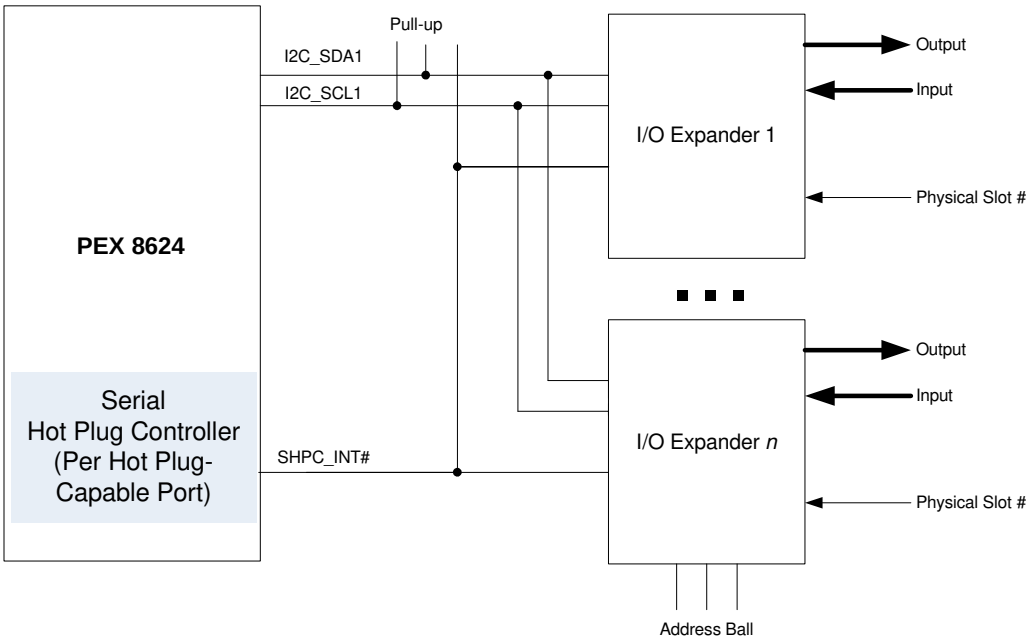


10.8 Serial Hot Plug Controller

Note: *The I²C Master interface is described in this section. The Master capabilities are limited to the Serial Hot Plug Controller.*

Using I/O Expander ICs sitting on an I²C Bus, the PEX 8624 has the option of Hot Plug capability on all its Transparent downstream Ports. Figure 10-4 illustrates the internal Serial Hot Plug Controller interface. The Serial Hot Plug Controller controls the output Ports on the I/O Expanders and retrieves the Port status, *such as* device connect status, Power Fault, and MRL Sensor position, from all I/O Expanders. When there is an input change to an I/O Expander, an INT*x* interrupt from an I/O Expander goes Low and the PEX 8624 reads the I/O Expander. When an I/O Expander output Port requires updating with a new value, the PEX 8624 writes to the I/O Expander through the I²C Bus.

Figure 10-4. Serial Hot Plug Interface Diagram



10.8.1 Hot Plug Operations by way of I²C I/O Expander

When software issues a Slot Power On command, the Serial Hot Plug Controller issues an I²C Write to the I/O Expander, to assert the PWREN output on the I/O Expander, and thereby turn On the power. After the Write is complete, either the HP_PWR_GOOD_*x* input is sampled asserted or the T_{pepv} time has elapsed, the Serial Hot Plug Controller issues another Write to the I/O Expander, to assert its REFCLKEN# output, and thereby turn On the Reference Clock (REFCLK) at the slot.

Note: *The T_{pepv} value is used when the HP_PWR_GOOD_x input is not used, as indicated by the **Power Management Hot Plug User Configuration** register HPC Tpepv field (offset 1E0h[4:3]) not being Cleared (Cleared is the default).*

After the REFCLKEN# output is asserted, the Serial Hot Plug Controller waits 100 ms, then issues another Write, to de-assert the I/O Expander PERST# output to the slot. If there are commands, *such as* Attention or Power LED changes along with the Power Control command, the Serial Hot Plug Controller includes the LED output value change, along with these Writes, to change the LED status. The same procedure applies to other commands, *such as* Port Power Off. After the Serial Hot Plug Controller completes all Write operations, it Sets the *Command Completed* bit. When another command is issued before the current command completes, the results are undefined. With a 100-kHz I²C clock, the time required to complete one Write operation to an I/O Expander is approximately 1 ms.

10.8.2 I²C I/O Expander Parts Selection and Pin Definition

Two types of I²C I/O Expanders can be used for Serial Hot Plug:

- **16-bit device** – For the 16-bit device, the 7-bit I²C address must be 0100_XXXb; a Maxim MAX7311, NXP PCA9555, or TI PCA9555 is recommended. All 16 I/O pins of the devices are used for one Port. A 16-bit device supports one Serial Hot Plug Port.

  For further details, refer to the manufacturer's data sheets for the Maxim MAX7311, NXP PCA9555, or TI PCA9555.
- **40-bit device** – For the 40-bit device, the 7-bit I²C address must be 0100_XXXb; an NXP PCA9698 is recommended. The lower 32 I/O pins are used for two Ports. A 40-bit device supports two Serial Hot Plug Ports.

  For further details, refer to the manufacturer's data sheet for the NXP PCA9698.

The PEX 8624 can support multiple 16- or 40-bit I/O Expanders, but not both types concurrently, to provide Hot Plug services on all Transparent downstream Ports. (Refer to the **Power Management Hot Plug User Configuration** register *40-Pin I/O Expander Enable* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1E0h[17])). The NXP PCA9555 and TI PCA9555 devices have only eight programmable I²C addresses; therefore, the maximum number of Serial Hot Plug-capable Ports with these I/O Expanders is eight. However, the Maxim MAX7311 can have up to 64 programmable Slave addresses; therefore, if using the MAX7311 I/O Expanders, all Transparent downstream Ports can be made Hot Plug-capable.

Table 10-4 defines the external I²C I/O Expander pins, in location order.

Table 10-4. External Hot Plug I²C I/O Expander Pin Definitions, by Location

Signal Name	Direction	Description	Location	
			16-Bit Device	40-Bit Device
PWRLED#	O	**Hot Plug Power LED Output** Same function as HP_PWRLED_[C, B, A]#.	IO0_0 or P00	IO0_0 IO2_0
ATNLED#	O	**Hot Plug Attention LED Output** Same function as HP_ATNLED_[C, B, A]#.	IO0_1 or P01	IO0_1 IO2_1
PWREN	O	**Hot Plug Power Enable Output** Same function as HP_PWREN_[C, B, A].	IO0_2 or P02	IO0_2 IO2_2
REFCLKEN#	O	**Hot Plug Reference Clock Enable Output** Same function as HP_CLKEN_[C, B, A]#.	IO0_3 or P03	IO0_3 IO2_3
PERST#	O	**Hot Plug Reset Output** Same function as HP_PERST_[C, B, A]#.	IO0_4 or P04	IO0_4 IO2_4
INTERLOCK	O	**Electromechanical Interlock Output Control** Used to physically lock the adapter or MRL in place until software releases it. The signal default is 0. The current state of the Electromechanical Interlock is reflected in the **Slot Status** register *Electromechanical Interlock Status* bit (offset 80h[23]). This output can be toggled by writing 1 to the **Slot Control** register *Electromechanical Interlock Control* bit (offset 80h[11]). A Write of 0 has no effect. INTERLOCK is enabled when the **Slot Capability** register *Electromechanical Interlock Present* bit (offset 7Ch[17]) is Set. By default, the bit is Set for Serial Hot Plug-capable Transparent downstream Ports.	IO0_5 or P05	IO0_5 IO2_5
GPIO	I/O	**General-Purpose Input/Output (GPIO)** Configured as input (default) or output by the *HPC GPIO Config* bit (offset 1E0h[18]), with the pin value in the *HPC GPIO Input/Output Value* bit (offset 1E0h[19]).	IO0_6 or P06	IO0_6 IO2_6
SLOT NUMBER[3:0]	I	**Physical Slot Number Bits 7Ch[26:23]** Slot Number value from I/O Expander inputs, which map to the **Slot Capability** register *Physical Slot Number* bits (offset 7Ch[26:23]). The value of the lowest 4 bits of the Physical Slot Number (offset 7Ch[22:19]) are automatically Set equal to the Port Number.	{IO1_2:0, IO0_7} or {P1[2:0], P07}	{IO1_2:0, IO0_7} {IO3_2:0, IO2_7}
PRSNT#	I	**Hot Plug PRSNT2# Input** Same function as HP_PRSNT_[C, B, A]#, but input only.	IO1_3 or P13	IO1_3 IO3_3
MRL#	I	**Hot Plug Manually Operated Retention Latch Sensor Input** Same function as HP_MRL_[C, A]# and HP_MRL_B#.	IO1_4 or P14	IO1_4 IO3_4
BUTTON#	I	**Hot Plug Attention Button Input** Same function as HP_BUTTON_[C, B, A]#.	IO1_5 or P15	IO1_5 IO3_5
PWRFLT#	I	**Hot Plug Power Fault Input** Same function as HP_PWRFLT_[C, B, A]#.	IO1_6 or P16	IO1_6 IO3_6
PWR_GOOD	I	**Hot Plug Power Good Input** Same function as HP_PWR_GOOD_[C, B, A].	IO1_7 or P17	IO1_7 IO3_7

10.8.3 Serial Hot Plug Port Enumeration and Assignment

Each I/O Expander has a 7-bit address; the PEX 8624 scans for sequential I^2C addresses, starting with address 40h.

After PEX_PERST# de-asserts and the serial EEPROM (if present) load completes, the Serial Hot Plug Controller accesses all I^2C addresses to perform the I/O Expander hunt, to determine the presence of external I/O Expander devices. If the Controller receives an Acknowledge Control Packet (ACK) from the I/O Expander, it remembers the presence of an external I/O Expander device, which is assigned to one of the Transparent downstream Ports.

The PEX 8624 has three Stations, for a total of one to two PCI Express Ports per Station. The PEX 8624 has only sufficient signal balls to support one Parallel Hot Plug-capable Port per Station. Each Station (Stations 0, 1, and 2) has a 2-bit Configuration register field that is used to select the Parallel Hot Plug-capable Port (*HP Parallel Port* field (Port 0, 4, or 8, offset 1E0h[14:13]). The default value of this field is 01b for Stations configured with two Ports, which means that Ports 1, 5, and 9 are Parallel Hot Plug-capable. When Station 0 and/or 2 is programmed as x8, the value of this field is 00b, and therefore the first Port in the Station (Port 0 and/or 8) is Parallel Hot Plug-capable. This field can be programmed by serial EEPROM data loading.

To simplify the Serial Hot Plug Port enumeration and assignment, the virtual Serial Hot Plug Port definition is provided as follows, and the mapping between virtual Serial Hot Plug Port and PEX 8624 Ports is provided later.

Table 10-5 defines the virtual Serial Hot Plug Port for a 16-bit device, *such as* a Maxim MAX7311, NXP PCA9555, or TI PCA9555. Table 10-6 defines the virtual Serial Hot Plug Port for a 40-bit device, *such as* an NXP PCA9698.

Table 10-5. Virtual Serial Hot Plug Port Definition for 16-Bit Device

I^2C Slave Address[2:0]	0	1	2	3	4	5	6	7
Virtual Serial Hot Plug Port #	0	1	2	3	4	5	6	7

Table 10-6. Virtual Serial Hot Plug Port Definition for 40-Bit Device

I^2C Slave Address[2:0]	0	0	1	1	2	2	3	3
I/O Pin Range	0-15	16-31	0-15	16-31	0-15	16-31	0-15	16-31
Virtual Serial Hot Plug Port #	0	1	2	3	4	5	6	7

The following four types of Ports are not Serial Hot Plug-capable, and therefore are not assigned a virtual Serial Hot Plug Port Number:

- Disabled Ports, due to Port configuration

  For the Ports residing on Stations 0 and 2, the first Port's Number starts from 0 (*that is*, the first Port of Station 0 is Port 0 and the first Port of Station 2 is Port 8). For the Ports residing on Station 1, the first Port's number starts from 1 (*that is*, the first Port of Station 1 is Port 5). While doing the Serial Hot Plug Port enumeration and assignment, treat Port 4 as enabled. Port 4 can be assigned a virtual Serial Hot Plug Port Number, though it may seem wasted.
- Upstream Port
- NT Port (Station 0 only)
- Parallel Hot Plug-capable Ports (per Port, per Station) (*that is*, Ports that are both Serial and Parallel Hot Plug-capable will be designated as Parallel Hot Plug-capable Ports)

10.9 Hot Plug Board Insertion and Removal Process

Table 10-7 defines the board insertion procedure supported by the PEX 8624. Table 10-8 defines the board removal procedure. Both processes apply to Parallel and Serial Hot Plug-capable Transparent downstream Ports.

Table 10-7. Hot Plug Board Insertion Process

Operator / Action	Hot Plug Controller	Software
A. Places board in slot.	**1.** Sets the *Presence Detect State* bit. **2.** Sets the *Presence Detect Changed* bit. **3.** Generates an Interrupt Message due to Presence Detect Changed event, if enabled.	Clears the *Presence Detect Changed* bit.
	4. Transmits an Interrupt de-assertion Message, if enabled.	
B. Locks MRL.	**5.** Clears the *MRL Sensor State* bit. **6.** Sets the *MRL Sensor Changed* bit. **7.** Generates an Interrupt Message due to MRL Sensor Changed event, if enabled.	Clears the *MRL Sensor Changed* bit.
	8. Transmits an Interrupt de-assertion Message, if enabled.	
C. Presses Attention Button.	**9.** Sets the *Attention Button Pressed* bit. **10.** Generates an Interrupt Message due to Attention Button Pressed event, if enabled.	Clears the *Attention Button Pressed* bit.
	11. Transmits an Interrupt de-assertion Message, if enabled.	Programs the **Slot Control** register *Power Indicator Control* field to 10b, to blink the Power Indicator LED, which indicates that the board is being powered up.

Continued…

Table 10-7. Hot Plug Board Insertion Process *(Cont.)*

Operator / Action	Hot Plug Controller	Software
D. Power Indicator blinks.	**12.** Blinks the Power Indicator LED. **13.** Sets the *Command Completed* bit. **14.** Generates an Interrupt Message due to Power Indicator Blink command Completion, if enabled.	Clears the *Command Completed* bit.
	15. Transmits an Interrupt de-assertion Message, if enabled.	Clears the **Slot Control** register *Power Controller Control* bit, to turn On power to the Port.
	16. Slot is powered up. **17.** After HP_PWR_GOOD_*x* input is sampled asserted High or T_{pepv} delay, Sets the *Command Completed* bit. **18.** Generates an Interrupt Message due to Power Turn On command Completion, if enabled.	Clears the *Command Completed* bit.
	19. Transmits an Interrupt de-assertion Message, if enabled.	Programs the **Slot Control** register *Power Indicator Control* field to 01b, to turn On the Power Indicator LED, which indicates that the slot is fully powered On.
E. Power Indicator On.	**20.** Turns On the Power Indicator LED. **21.** Transmits an Interrupt assertion Message due to Power Indicator Turn On command Completion, if enabled.	Clears the *Command Completed* bit.
	22. Transmits an Interrupt de-assertion Message, if enabled. **23.** After the Data Link Layer is up, Sets the **Slot Status** register *Data Link Layer State Changed* bit (offset 80h[24]), and transmits the corresponding interrupt, if enabled.	Software can now read the **Link Status** register *Data Link Layer Link Active* bit (offset 78h[29]). A value of 1 in this bit indicates that the board is ready to be used. Clears the *Data Link Layer State Changed* bit and interrupt, if enabled.
	24. Transmits an Interrupt de-assertion Message, if enabled.	

Table 10-8. Hot Plug Board Removal Process

Operator / Action	Hot Plug Controller	Software
A. Presses Attention Button.	**1.** Sets the *Attention Button Pressed* bit. **2.** Generates an Interrupt Message due to Attention Button pressed, if enabled.	Clears the *Attention Button Pressed* bit.
	3. Transmits an Interrupt de-assertion Message, if enabled.	Programs the **Slot Control** register *Power Indicator Control* field to 10b, to blink the Power Indicator LED, which indicates that the board is being powered down.
B. Power Indicator blinks.	**4.** Blinks the Power Indicator LED. **5.** Sets the *Command Completed* bit. **6.** Generates an Interrupt Message due to Power Indicator Blink command Completion, if enabled.	Clears the *Command Completed* bit.
	7. Transmits an Interrupt de-assertion Message, if enabled.	Sets the **Slot Control** register *Power Controller Control* bit, to turn Off power to the Port.
C. Power Indicator Off.	**8.** Slot is powered Off. **9.** Sets the *Data Link Layer State Changed* bit, and transmits an interrupt, if enabled. **10.** After a 256-ms delay from HP_PWR_GOOD_*x* sampled de-asserted (if HP_PWR_GOOD_*x* input is enabled through the *HPC Tpepv* field (offset 1E0h[4:3], is Cleared)), Sets the *Command Completed* bit. **11.** Generates an Interrupt Message due to Power Turn Off command Completion, if enabled.	Clears the *Data Link Layer State Changed* bit and interrupt. Clears the *Command Completed* bit. Programs the *Power Indicator Control* field to 11b, to turn Off the Power Indicator LED, which indicates that the slot is fully powered Off and the board can be removed.
D. Power Indicator Off, board ready to be removed.	**12.** Turns Off the Power Indicator LED. **13.** Sets the *Command Completed* bit, due to Power Indicator Off command Completion.	Clears the *Command Completed* bit.
	14. Transmits an Interrupt de-assertion Message, if enabled.	
E. Unlocks MRL.	**15.** Sets the *MRL Sensor State* bit. **16.** Sets the *MRL Sensor Changed* bit. **17.** Generates an Interrupt Message due to MRL Sensor state change, if enabled.	Clears the *MRL Sensor Changed* bit.
	18. Transmits an Interrupt de-assertion Message, if enabled.	
F. Removes board from slot.	**19.** Clears the *Presence Detect State* bit. **20.** Sets the *Presence Detect Changed* bit. **21.** Generates an Interrupt Message due to Presence Detect change, if enabled.	Clears the *Presence Detect Changed* bit.
	22. Transmits an Interrupt de-assertion Message, if enabled.	

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Chapter 11 Power Management

11.1 Overview

The PEX 8624 Power Management (PM) features provide the following services:

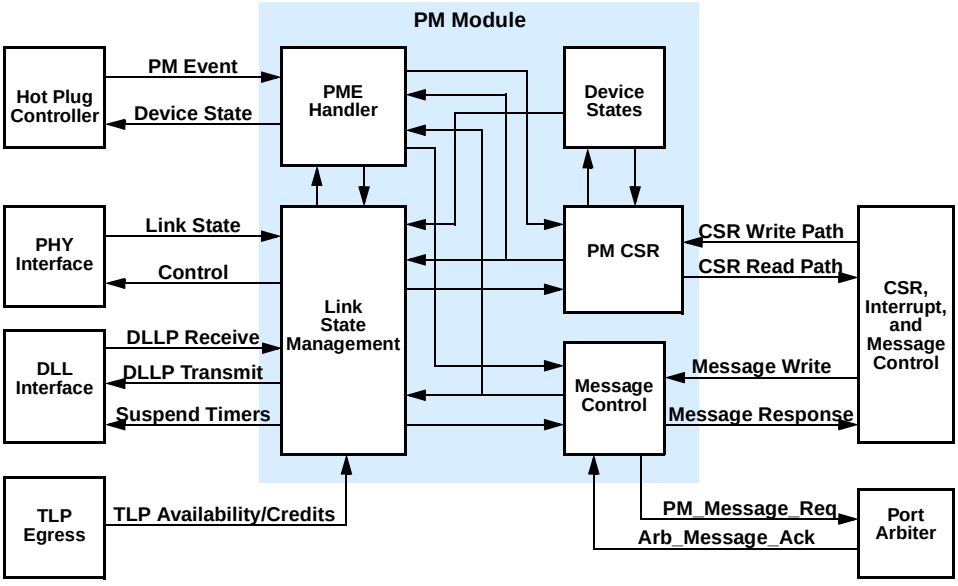
- Mechanisms to identify PM capabilities
- Ability to transition into certain PM states
- Notification of the current PM state of each Port
- Support for the option to wakeup the system upon a specific event

The PEX 8624 supports hardware-autonomous PM and software-driven D-State PM. The switch also supports the L0s and L1 Link PM states in hardware-autonomous Active State Power Management (ASPM), as well as the L1, L2/L3 Ready, and L3 Link PM states in Conventional PCI-compatible PM. D0, D3hot, and D3cold Device PM states are supported in Conventional PCI-compatible PM. Because the PEX 8624 does ***not support*** Vaux, Power Management Event (PME) generation from the D3cold Device PM state is ***not supported***.

The PM module interfaces with a Physical Layer (PHY) electrical sub-block, to transition the Link state into a low-power state, when the module receives a Power State Change Request from a downstream component, or an internal event forces the Link state entry into low-power states in hardware-autonomous ASPM mode. PCI Express Link states are not directly visible to Conventional PCI Bus driver software; however, they are derived from the PM state of the components residing on those Links.

Figure 11-1 provides a functional block diagram of the PEX 8624 PM module.

Figure 11-1. PM Module Functional Block Diagram



Note: *The Hot Plug Controller is available only on Hot Plug-capable Transparent downstream Ports.*

11.2 Power Management Features

- *PCI Express Base r2.0*-compliant
- *PCI Power Mgmt. r1.2*-compliant
- Link Power Management States (*L-States*; also referred to as *Link PM states*)
  - PCI Bus Power Management – L1, L2/L3 Ready, and L3 (Vaux is ***not supported***)
  - Active State Power Management (ASPM) – L0s and L1
- Device Power Management State (*D-States*; also referred to as *Device PM states*)
  - D0 (D0uninitialized and D0active) and D3 (D3hot) support
- Power Management Event (PME) support from D3hot
- PME due to Hot Plug and/or PCI Express Hot Plug events
- Forwards PME_Turn_Off broadcast messages
- Implements Gen 2-specific Control and Status registers, and associated interrupts
- Supports ASPM L0s, ASPM L1, PCI PM L1, and L2/L3 Ready power states in NT mode

11.3 Power Management Capability

11.3.1 Device Power Management States

The PEX 8624 supports the PCI Express PCI-PM D0 and D3hot Device PM states. The D1 and D2 Device PM states, which are optional in the *PCI Express Base r2.0*, are ***not supported*** by the PEX 8624.

The D3hot Device PM state can be entered from the D0 Device PM state, when system software programs the Port's **PCI Power Management Status and Control** register *Power State* field (offset 44h[1:0]) to 11b. The D0uninitialized Device PM state can be entered from the D3hot Device PM state when system software Clears the Port's *Power State* field.

11.3.1.1 D0 Device Power Management State

The D0 Device PM state is divided into two distinct sub-states – *uninitialized* and *active*. When power is initially applied to a PCI Express component, it defaults to the D0uninitialized Device PM state. The component remains in the D0uninitialized Device PM state until the serial EEPROM load and initial Link training completes.

A device enters the D0active Device PM state when system software Sets any combination of the **PCI Command** register *Bus Master Enable*, *Memory Access Enable*, and/or *I/O Access Enable* bits (offset 04h[2, 1, and/or 0], respectively).

11.3.1.2 D3hot Device Power Management State

Once in the D3hot Device PM state, the PEX 8624 can later be transitioned into the D3cold Device PM state, by removing power from its Host component. Functions that are in the D3hot Device PM state can be transitioned, by software, to the D0uninitialized Device PM state. When in the D3hot Device PM state, Hot Plug or Link State operations cause a PME in the PEX 8624.

Only Type 0 Configuration accesses are allowed in the D3hot Device PM state. Memory and I/O transactions result in an Unsupported Request (UR). Completions flowing in either direction are not affected.

Type 1 transactions flowing toward a PEX 8624 Port in the D3hot Device PM state are terminated as URs. Type 0 Configuration transactions complete successfully. When the PEX 8624 upstream Port is programmed to the D3hot Device PM state, the Port initiates Conventional PCI-PM L1 Link PM state entry.

11.3.2 Link Power Management States

PEX 8624 components hold their upstream Link and downstream Links in the L0 Link PM state during standard device operation (Conventional PCI-PM state is in the D0active Device PM state). ASPM defines a mechanism for components in the D0 Device PM state, to reduce Link power by placing their Links into a low-power state and instructing the other end of the Link to do likewise. This allows hardware-autonomous, dynamic Link power reduction beyond what is achievable by software-only-controlled PM. Table 11-1 defines the relationship between a component's Power state and upstream Link. Table 11-2 defines the relationship between Link PM states and power-saving actions.

Conventional PCI PM, and the L1 and L2/L3 Ready Link PM states are controlled by system software programming the PEX 8624 into the D3hot Device PM state, and subsequently causing the Root Complex to broadcast the PME_Turn_Off Message to the downstream hierarchy.

Table 11-1. Relationship between Component Power State and Upstream Link

Downstream Component Device PM State	Permissible Upstream Component Device PM State	Permissible Interconnect Link PM State
D0	D0	L0, L0s, L1 (optional) – ASPM.
D3hot	D0 to D3hot	L1, L2/L3 Ready.
D3cold (no Vaux)	D0 to D3cold	L3 (off). Zero power.

Table 11-2. Relationship between Link PM States and Power-Saving Actions

Link PM State	Power-Saving Actions
Tx L0s	PHY Tx Lanes are in a high-impedance state.
Rx L0s	PHY Rx Lanes in a low-power state.
L1	PHY Tx and Rx Lanes are in a low-power state. Flow Control (FC) timers are suspended.
L2/L3 Ready	PHY Tx and Rx Lanes are in a low-power state. FC timers are suspended.
L3 (D3cold)	Component is fully powered Off.

11.3.3 PCI Express Power Management Support

The PEX 8624 supports PM features required in the *PCI Express Base r2.0*. Table 11-3 lists supported and non-supported features and the register bits/fields used for configuration or activation.

Table 11-3. Supported PCI Express PM Capabilities

Register		Description	Supported	
Offset	Bit(s)		Yes	No
40h	PCI Power Management Capability (All Ports)			
	7:0	**Capability ID** Programmed to 01h, indicating that the Capability structure is the PCI Power Management Capability structure.	✔	
	15:8	**Next Capability Pointer** Default 48h points to the **MSI Capability** structure.	✔	
	18:16	**Version** Default 011b indicates compliance with the *PCI Power Mgmt. r1.2*.	✔	
	19	**PME Clock** Power Management Event (PME) clock. Does not apply to PCI Express. Returns 0.		✔
	21	**Device-Specific Initialization** Default 0 indicates that Device-Specific Initialization is ***not*** required.	✔	
	24:22	**AUX Current** The PEX 8624 does ***not support*** PME generation from the D3cold Device Power Management (PM) state; therefore, the serial EEPROM value for this field should be 000b.		✔
	25	**D1 Support** Default value of 0 indicates that the PEX 8624 does ***not support*** the D1 Device PM state.		✔
	26	**D2 Support** Default value of 0 indicates that the PEX 8624 does ***not support*** the D2 Device PM state.		✔
	31:27	**PME Support** Bits [31, 30, and 27] must be Set, to indicate that the PEX 8624 will forward PME Messages, as required by the *PCI Express Base r2.0*.	✔	

Table 11-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
	PCI Power Management Status and Control (All Ports)			
	1:0	**Power State** Used to determine the Port's current Device PM state, and to program the Port into a new Device PM state. 00b = D0 01b = D1 – ***Not supported*** 10b = D2 – ***Not supported*** 11b = D3hot If software attempts to write an unsupported state to this field, the Write operation completes normally; however, the data is discarded and no state change occurs.	✔	
	3	**No Soft Reset** 1 = Devices transitioning from the D3hot to D0 Device PM state, because of Power State commands, do not perform an internal reset	✔	
	8	**PME Enable** 0 = Disables PME generation by the corresponding PEX 8624 Port[a] 1 = Enables PME generation by the corresponding PEX 8624 Port	✔	
44h	12:9	**Data Select** Initially writable by serial EEPROM and/or I^2C only[b]. This Configuration Space register (CSR) access privilege changes to RW after a Serial EEPROM or I^2C Write occurs to this register. Selects the **Data** and **Data Scale** registers (fields [31:24 and 14:13], respectively). 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated All other encodings are ***reserved***.	✔	
	14:13	**Data Scale** Writable by serial EEPROM and/or I^2C only[b]. Indicates the scaling factor to be used when interpreting the **Data** register value. The value and meaning of this field varies, depending upon which data value is selected by field [12:9] (*Data Select*). There are four internal **Data Scale** registers (one each, per *Data Select* values 0h, 3h, 4h, and 7h), per Port. For other *Data Select* values, the **Data Scale** value returned is 0h.	✔	
	15	**PME Status** 0 = PME is not generated by the corresponding PEX 8624 Port[a] 1 = PME is being generated by the corresponding PEX 8624 Port	✔	

a. Because the PEX 8624 does not consume auxiliary power, this bit is not sticky, and is always Cleared at power-on reset.

*b. With no serial EEPROM nor previous I^2C programming, Reads return 00h for the **Data** and **Data Scale** registers (for all Data Selects).*

Table 11-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
44h		**PCI Power Management Control/Status Bridge Extensions (All Ports)**		
	22	**B2/B3 Support** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.		✔
	23	**Bus Power/Clock Control Enable** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.		✔
		PCI Power Management Data (All Ports)		
	31:24	**Data** Writable by serial EEPROM and/or I^2C only[b]. There are four supported *Data Select* values (0h, 3h, 4h, and 7h), per Port. For other *Data Select* values, the **Data Scale** value returned is 0h. Selected by field [12:9] (*Data Select*).	✔	
6Ch		**Device Capability (All Ports)**		
	8:6	**Endpoint L0s Acceptable Latency** Because the PEX 8624 is a switch and not an endpoint, the PEX 8624 does ***not support*** this feature. 000b = Disables the capability		✔
	11:9	**Endpoint L1 Acceptable Latency** Because the PEX 8624 is a switch and not an endpoint, the PEX 8624 does ***not support*** this feature. 000b = Disables the capability		✔
	25:18	**Captured Slot Power Limit Value (Upstream Port and NT Port)** For the PEX 8624 upstream Port, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [27:26] (*Captured Slot Power Limit Scale*). Do not change for downstream Ports.	✔	
	27:26	**Captured Slot Power Limit Scale (Upstream Port and NT Port)** For the PEX 8624 upstream Port, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [25:18] (*Captured Slot Power Limit Value*). 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001 Do not change for downstream Ports.	✔	

a. Because the PEX 8624 does not consume auxiliary power, this bit is not sticky, and is always Cleared at power-on reset.

*b. With no serial EEPROM nor previous I^2C programming, Reads return 00h for the **Data** and **Data Scale** registers (for all Data Selects).*

Table 11-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
70h		**Device Control (All Ports)**		
	10	**AUX Power PM Enable**		✔
		Device Status (All Ports)		
	20	**AUX Power Detected**		✔
74h		**Link Capability (All Ports)**		
	11:10	**Active State Power Management (ASPM) Support** Active State Link PM support. Indicates the level of ASPM supported by the Port. 01b = L0s Link PM state entry is supported 11b = L0s and L1 Link PM states are supported All other encodings are ***reserved***.	✔	
	14:12	**L0s Exit Latency** Indicates the L0s Link PM state exit latency for the given PCI Express Link. Value depends upon the **Physical Layer Command and Status** register *N_FTS Value* field (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 220h[15:8]) value and Link speed. Exit latency is calculated, as follows: • **2.5 GHz** – Multiply *N_FTS Value* x 4 (4 symbol times in 1 N_FTS) x 4 ns (1 symbol time at 2.5 GT/s) • **5.0 GHz** – Multiply *N_FTS Value* x 4 (4 symbol times in 1 N_FTS) x 2 ns (1 symbol time at 5.0 GT/s) 100b = Corresponding PEX 8624 Port L0s Link PM state Exit Latency is 512 ns to less than 1 s at 5.0 GT/s 101b = Corresponding PEX 8624 Port L0s Link PM state Exit Latency is 1 s to less than 2 s at 2.5 GT/s	✔	
	17:15	**L1 Exit Latency** Indicates the L1 Link PM state exit latency for the given PCI Express Link. Value depends upon the Link speed. 001b = Corresponding PEX 8624 Port L1 Link PM state Exit Latency is 1 s to less than 2 s at 5.0 GT/s 010b = Corresponding PEX 8624 Port L1 Link PM state Exit Latency is 2 s to less than 4 s at 2.5 GT/s	✔	
	18	**Clock Power Management Capable**	✔	

Table 11-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
78h		**Link Control (All Ports)**		
	1:0	**Active State Power Management (ASPM)** 00b = Disable[c] 01b = Enables only L0s Link PM state Entry 10b = Enables only L1 Link PM state Entry 11b = Enables both L0s and L1 Link PM state Entries	✔	
	8	**Clock Power Management Enable** The PEX 8624 does ***not support*** removal of the Reference Clock in the L1 and L2/L3 Ready Link PM states.		✔
7Ch		**Slot Capability (Only Downstream Ports; Upstream Port Always Reads 0)**		
	0	**Attention Button Present** ***Reserved*** for the upstream Port and NT Port. 0 = Attention Button is not implemented. 1 = Attention Button is implemented on the slot chassis of the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port. Set if the Port is Parallel or Serial Hot Plug-capable.	✔	
	1	**Power Controller Present** ***Reserved*** for the upstream Port and NT Port. Enables or disables the Hot Plug Controller on the PEX 8624 Hot Plug-capable Transparent downstream Ports. Set if the Port is Parallel or Serial Hot Plug-capable. 0 = Power Controller is not implemented. The Hot Plug Controller is disabled for that slot and a power-up sequence is not executed. The slot remains in the disabled state. 1 = Power Controller is implemented for the slot of the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port. Hot Plug Controller powers up the slot when the Manually operated Retention Latch (MRL) is closed and the **Slot Control** register *Power Controller Control* bit (offset 80h[10]) is Cleared. Otherwise, if bit 2 (*MRL Sensor Present*) is disabled (Cleared), the MRL's position has no effect on powering up the slot.	✔	
	2	**MRL Sensor Present** ***Reserved*** for the upstream Port and NT Port. Set if the Port is Parallel or Serial Hot Plug-capable. 0 = MRL Sensor is not implemented. MRL position is "Don't Care" for that slot. 1 = MRL Sensor is implemented on the slot chassis of the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port. The PEX 8624 senses whether the MRL is open or closed for a slot. MRL should be Low for power-on for that slot.	✔	
	3	**Attention Indicator Present** ***Reserved*** for the upstream Port and NT Port. Set if the Port is Parallel or Serial Hot Plug-capable. 0 = Attention Indicator is not implemented. HP_ATNLED_*x*# output is not functional on the slot. 1 = Attention Indicator is implemented on the slot chassis of the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port. Controls whether the HP_ATNLED_*x*# output for the slot drives out Active-Low.	✔	

c. The Port Receiver must be capable of entering the L0s Link PM state, regardless of whether the state is disabled.

Table 11-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
7Ch		**Slot Capability (Only Downstream Ports; Upstream Port Always Reads 0) *(Cont.)***		
	4	**Power Indicator Present** ***Reserved*** for the upstream Port and NT Port. Set if the Port is Parallel or Serial Hot Plug-capable. 0 = Power Indicator is not implemented. HP_PWRLED_*x*# output is not functional on the slot. 1 = Power Indicator is implemented on the slot chassis of the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port. Controls whether the HP_PWRLED_*x*# output for the slot drives out Active-Low.	✔	
	5	**Hot Plug Surprise** ***Reserved*** for the upstream Port and NT Port. 0 = No device in the corresponding PEX 8624 downstream Port slot is removed from the system without prior notification 1 = Device in the corresponding PEX 8624 downstream Port slot can be removed from the system without prior notification	✔	
	6	**Hot Plug Capable** ***Reserved*** for the upstream Port and NT Port. 0 = Corresponding PEX 8624 downstream Port slot is not capable of supporting Hot Plug operations. 1 = Corresponding PEX 8624 downstream Port slot is capable of supporting Hot Plug operations. Set if the Port is Parallel or Serial Hot Plug-capable.	✔	
	14:7	**Slot Power Limit Value** ***Reserved*** for the upstream Port. The maximum power supplied by the corresponding PEX 8624 downstream slot is determined by multiplying the value in this field (expressed in decimal; 25d = 19h) by the value specified in the *Slot Power Limit Scale* field. This field must be implemented if the **PCI Express Capability** register *Slot Implemented* bit (offset 68h[24]) is Set (default). Serial EEPROM and/or I^2C Writes to this register or a DLL Up event causes the downstream Port to send the Set_Slot_Power_Limit Message to the device connected to it, so as to convey the Limit value to the downstream device's upstream Port **Device Capability** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields.	✔	
	16:15	**Slot Power Limit Scale** ***Reserved*** for the upstream Port. The maximum power supplied by the corresponding PEX 8624 downstream slot is determined by multiplying the value in this field by the value specified in the *Slot Power Limit Value* field. This field must be implemented if the **PCI Express Capability** register *Slot Implemented* bit (offset 68h[24]) is Set (default). Serial EEPROM and/or I^2C Writes to this register or a DLL Up event causes the downstream Port to send the Set_Slot_Power_Limit Message to the device connected to it, so as to convey the Limit value to the downstream device's upstream Port **Device Capability** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	✔	

Table 11-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
80h	**Slot Control (Only Downstream Ports; Upstream Port Always Reads 0)**			
	1	**Power Fault Detector Enable** ***Reserved*** for the upstream Port and NT Port. 0 = Function is disabled 1 = Enables software notification with an interrupt if the Port is in the D0 Device PM state (**PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], is Cleared), or with a PME Message if the Port is in the D3hot Device PM state (offset 44h[1:0], are both Set), for a Power Fault Detected event on the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port.	✔	
	9:8	**Power Indicator Control** ***Reserved*** for the upstream Port and NT Port. Controls the Power Indicator on the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port slot. Reads return the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port Power Indicator's current state. Writing a non-zero value triggers a Command Completed event (even if the value written is the same as the existing value). Writing 00b preserves the current value and does not trigger a Command Completed event. 00b = ***Reserved*** – Writes are ignored 01b = Turns On indicator to constant On state 10b = Causes indicator to blink 11b = Turns Off indicator	✔	
	10	**Power Controller Control** ***Reserved*** for the upstream Port and NT Port. Controls the Power Controller on the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port slot. 0 = Turns On the Power Controller; requires some delay to be effective 1 = Turns Off the Power Controller	✔	
	Slot Status (Only Downstream Ports; Upstream Port Always Reads 0)			
	17	**Power Fault Detected** ***Reserved*** for the upstream Port and NT Port. 1 = Power Controller of the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port slot detected a Power Fault at the slot	✔	

Table 11-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
138h	**Power Budget Extended Capability Header (Only Upstream Port, and also NT Port Link Interface; *Reserved* (RsvdP) for All Other Ports)**			
	15:0	**PCI Express Extended Capability ID** Program to 0004h, as required by the *PCI Express Base r2.0*.	✔	
	19:16	**Capability Version** Program to 1h, as required by the *PCI Express Base r2.0*.	✔	
	31:20	**Next Capability Offset** Program to 148h, which addresses the **Virtual Channel Extended Capability** structure.	✔	
13Ch	**Data Select (Only Upstream Port, and also NT Port Link Interface; *Reserved* (RsvdP) for All Other Ports)**			
	7:0	**Data Select** Indexes the Power Budget data reported, by way of eight upstream Port/NT Port Link Interface **Power Budget Data** registers, and selects the DWord of Power Budget data that appears in each **Power Budget Data** register. Index values start at 0, to select the first DWord of Power Budget data; subsequent DWords of Power Budget data are selected by increasing index values 1 to 7.	✔	

Table 11-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
140h		**Power Budget Data (Only Upstream Port, and also NT Port Link Interface; *Reserved* (RsvdP) for All Other Ports)**		
	7:0	**Base Power** Eight registers per upstream Port/NT Port Link Interface. Specifies (in Watts) the base power value in the operating condition. This value must be multiplied by the field [9:8] (*Data Scale*) contents, to produce the actual power consumption value.	✔	
	9:8	**Data Scale** Specifies the scale to apply to the Base Power value. The device power consumption is determined by multiplying the field [7:0] (*Base Power*) contents with the value corresponding to the encoding returned by this field. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	✔	
	12:10	**PM Sub-State** 000b = Power Management sub-state of the operating condition being described	✔	
	14:13	**PM State** Power Management state of the operating condition being described. 00b = D0 Device PM state 11b = D3 Device PM state All other encodings are ***reserved***.	✔	
	17:15	**Type** Type of operating condition being described. 000b = PME Auxiliary 001b = Auxiliary 010b = Idle 011b = Sustained 111b = Maximum All other encodings are ***reserved***.	✔	
	20:18	**Power Rail** Power Rail of the operating condition being described. 000b = Power 12V 001b = Power 3.3V 010b = Power 1.8V 111b = Thermal All other encodings are ***reserved***.	✔	
		Note: *Eight registers, per upstream Port/NT Port Link Interface, can be programmed through the serial EEPROM or I^2C. Each non-zero register value describes the power usage for a different operating condition. Each configuration is selected by writing to the* ***Data Select*** *register Data Select field (Upstream Port/NT Port Link Interface, offset 13Ch[7:0]).*		

Table 11-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
144h	**Power Budget Capability (Only Upstream Port, and also NT Port Link Interface; *Reserved* (RsvdP) for All Other Ports)**			
	0	**System Allocated** 1 = Power budget for the device is included within the system power budget	✔	
1E0h	**Power Management Hot Plug User Configuration (All Ports except NT Port Virtual Interface, and also NT Port Link Interface)**			
	0	**L0s Entry Idle Counter** Traffic Idle time to meet, to enter the L0s Link PM state. 0 = Idle condition must last 1 s 1 = Idle condition must last 4 s	✔	
	2	**HPC PME Turn-Off Enable** Functionality associated with this bit is enabled only on the downstream Ports. 1 = PME Turn-Off Message is transmitted before the Port is turned Off on a downstream Port	✔	
	4:3	**HPC T_{pepv}** Functionality associated with this field is enabled only on the downstream Ports. Hot Plug Port time from Power Enable to Power Valid. Controls the delay from when an HP_PWREN_*x* output is asserted High, to when power is valid at a slot. (Refer to Section 10.7.1.2, "Slot Power-Up Sequencing When Power Controller Present Bit Is Set," for details.) 00b = Feature is disabled, and HP_PWR_GOOD_*x* input is used for Power Valid 01b = 128 ms 10b = 256 ms 11b = 512 ms	✔	
	6	**HP_PWR_GOOD_x Active-Low Enable** Functionality associated with this bit is enabled only on the downstream Ports. Controls the HP_PWR_GOOD_*x* input polarity. (Refer to Section 10.7.1.2, "Slot Power-Up Sequencing When Power Controller Present Bit Is Set," for details.) 0 = HP_PWR_GOOD_*x* is Active-High 1 = HP_PWR_GOOD_*x* is Active-Low	✔	
	10	**L0s Entry Disable** 0 = Enables entry into the L0s Link PM state on a Port when the L0s idle conditions are met 1 = Disables entry into the L0s Link PM state on a Port when the L0s idle conditions are met	✔	

11.4 Power Management Tracking

Note: *NT Port Link Interface entry and exit to ASPM and Conventional PCI PM-compatible power states do not depend upon the Transparent upstream nor downstream Port power states or traffic. They are solely dependent upon the NT Port Link Interface's traffic conditions.*

Upstream Port logic tracks the Link status of each downstream and upstream Port Link, to derive the following conditions:

- Upstream Port enters the L0s Link PM state when all enabled downstream Receivers are in the L0s Link PM state or deeper, or in a Link Down state.
- Upstream Port enters the active L1 Link PM state, only when all downstream Ports are in the active L1 Link PM state or deeper, or the Link is down.
- When a downstream Port is in the active L1 Link PM state and an ASPM L1 Link PM state exit is occurring in the downstream Port, the upstream Port exits the L1 Link PM state.
- When the upstream Port is in the active L1 Link PM state and an active L1 Link PM state exit is occurring, due to Receiver Electrical Idle exit, the downstream Port exits the L1 Link PM state.
- When a PME_TO_Ack Message is received only on all active (not in Link Down) downstream Ports, a PME_TO_Ack Message is issued toward the upstream Port. The NT Port Virtual Interface is marked as being in the *DL_Down* state.
- When all downstream Ports are in the L2/L3 Ready Link PM or Link Down state, the upstream Port transmits PM_ENTER_L23 Data Link Layer Packets (DLLPs) toward the Root Complex.

11.5 Power Management Event Handler

PM_PME Messages are Posted Transaction Layer Packets (TLPs) that inform the PM software which agent within the PCI Express hierarchy has requested a PM-state change. PM_PME Messages are always routed toward the Root Complex.

PCI Express components are permitted to wake the system from any supported PM state, through the request of a PME.

When a PEX 8624 Transparent downstream Port is in the D3hot Device PM state, the following Hot Plug and/or PCI Express Hot Plug events cause the **PCI Power Management Status and Control** register *PME Status* bit (offset 44h[15]) to be Set:

- For Hot Plug-capable Ports
  - Presence Detect Changed (logical OR of PRSNT# (HP_PRSNT_***x***# or I/O Expander PRSNT# input), and SerDes Receiver Detect[a] on Lane(s) associated with that Port)
  - Attention Button Pressed
  - Power Fault Detected
  - MRL Sensor Changed
  - Command Completed
- For non-Hot Plug-capable downstream Ports
  - Presence Detect Changed (SerDes Receiver Detect[a] on Lane(s) associated with that Port)
  - Data Link Layer State Changed

This causes the downstream Port to generate a PM_PME Message, if the **PCI Power Management Status and Control** register *PME Enable* bit (offset 44h[8]) is Set.

*a. The SerDes Receiver Detect mechanism is comprised of the **Physical Layer Receiver Detect Status** register's Receiver Detected on Lane x bits (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 200h[31:16]) or Hot Plug PRSNT# (from external I^2C I/O Expander) input for the Port.*

Chapter 12 Transparent Port Registers

12.1 Introduction

This chapter defines the PEX 8624 Transparent Port registers. Each PEX 8624 Port has its own Configuration, Capability, Control, and Status register space. The register mapping is the same for each Port. (Refer to Table 12-1.) This chapter also presents the PEX 8624 programmable registers and the order in which they appear in the register map. Register descriptions, when applicable, include details regarding their use and meaning in the upstream Port and downstream Ports. (Refer to Table 12-4.) Other registers are defined in:

- Chapter 14, "NT Port Virtual Interface Registers – NT Mode Only"
- Chapter 15, "NT Port Link Interface Registers – NT Mode Only"

Note: *For Chip- and Station-specific registers (those that exist only in Port 0), if Port 0 is the NT Port, then those registers exist only in the NT Port Virtual Interface.*

All PEX 8624 registers can be accessed by Configuration or Memory Requests.

For further details regarding register names and descriptions, refer to the following specifications:

- *PCI r3.0*
- *PCI Power Mgmt. r1.2*
- *PCI-to-PCI Bridge r1.2*
- *PCI Express Base r2.0*
- *I^2C Bus v2.1*

12.2 Type 1 Port Register Map

Table 12-1 defines the Transparent mode Type 1 Port register mapping.

Table 12-1. Type 1 Port Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI-Compatible Type 1 Configuration Header Registers (Offsets 00h – 3Ch)		Capability Pointer (40h)	00h … 34h … 3Ch
	Next Capability Pointer (48h)	Capability ID (01h)	40h
PCI Power Management Capability Registers (Offsets 40h – 44h)			44h
	Next Capability Pointer (68h)	Capability ID (05h)	48h
MSI Capability Registers (Offsets 48h – 64h)			… 64h
	Next Capability Pointer (A4h)	Capability ID (10h)	68h
PCI Express Capability Registers (Offsets 68h – A0h)			… A0h
	Next Capability Pointer (00h)	SSID/SSVID Capability ID (0Dh)	A4h
Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)			… FCh
Next Capability Offset (FB4h)	1h	PCI Express Extended Capability ID (0003h)	100h
Device Serial Number Extended Capability Registers (Offsets 100h – 134h)			… 134h
Next Capability Offset (148h)	1h	PCI Express Extended Capability ID (0004h)	138h
Power Budget Extended Capability Registers (Offsets 138h – 144h)			… 144h
Next Capability Offset (448h, 950h, or 520h)	1h	PCI Express Extended Capability ID (0002h)	148h
Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)			… 1BCh

Table 12-1. Type 1 Port Register Map *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Device-Specific Registers (Offsets 1C0h – 51Ch)		1C0h …
Next Capability Offset (950h or 520h)	1h PCI Express Extended Capability ID (000Bh)	448h
Device-Specific Registers (Offsets 1C0h – 51Ch)		… 51Ch
Next Capability Offset (950h)	1h PCI Express Extended Capability ID (000Dh)	520h
ACS Extended Capability Registers (Offsets 520h – 528h)		… 528h
Factory Test Only/Reserved		52Ch – 548h
Device-Specific Registers (Offsets 54Ch – F8Ch)		54Ch …
Next Capability Offset 2 (000h)	1h PCI Express Extended Capability ID 2 (000Bh)	950h
Device-Specific Registers (Offsets 54Ch – F8Ch)		… F8Ch
Reserved		F90h – FB0h
Next Capability Offset (138h or 148h)	1h PCI Express Extended Capability ID (0001h)	FB4h
Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)		… FDCh
Reserved		FE0h – FFCh

Table 12-2 lists registers that are generally individual registers that support all Ports (changing the register value in one Port changes the same register in all Ports), except for the NT Port Link Interface, which has its own registers (not duplicated in other Ports). Additional exceptions are also listed.

Table 12-2. Singular Registers Shared by Multiple Ports

Register Offset	Register Name	Comment
00h	Vendor ID and Device ID	
08h	PCI Class Code and Revision ID	NT Port Virtual Interface has its own register.
34h	Capability Pointer	
A4h	Subsystem Capability	NT Port Virtual Interface has its own register.
A8h	Subsystem Vendor ID and Subsystem ID	
100h	Device Serial Number Extended Capability Header	
104h	Serial Number (Lower DW)	
108h	Serial Number (Upper DW)	
520h	ACS Extended Capability Header	
950h	Vendor-Specific Extended Capability 2	NT Port Virtual Interface has its own register.
954h	Vendor-Specific Header 2	
958h	Hardwired Vendor ID and Hardwired Device ID	Shared by all Ports, including the NT Port Link Interface.
95Ch	Hardwired Revision ID	Shared by all Ports, including the NT Port Link Interface.

12.3 Port Register Configuration and Map

The PEX 8624 Port registers are configured similarly – not all the same. Port 0 of Station 0, Port 4 of Station 1, and Port 8 of Station 2 include more Device-Specific registers than the other Ports. Port 0 also contains registers that are used to set up and control the PEX 8624, as well as a serial EEPROM interface and I^2C Slave interface logic and control. The Port registers contain setup and control information specific to the Station and its associated Port. Table 12-3 defines the Port register configuration and map.

Notes: *For Chip- and Station-specific registers (those that exist only in Port 0), if Port 0 is the NT Port, then those registers exist only in the NT Port Virtual Interface.*

The six PEX 8624 Ports that connect to PCI Express Transmitters and Receivers are Ports 0, 1, 5, 6, 8, and 9, and each Port has its own set of registers. An additional set of Port 4 registers is visible to software, although the Port is not connected to external signals. The Port 4 registers include:

- *Other Device-Specific registers.*
- *"Station" registers, that control all Ports in Station 1 (Ports 5 and 6), and are identical to the Port 0 registers that control all Ports in Station 0 (Ports 0 and 1) and Port 8 registers that control all Ports in Station 2 (Ports 8 and 9). The Station registers include Physical Layer registers, Device-Specific Error registers, and internal mapping (CAM) registers.*

Table 12-3. Port Register Configuration and Map

Register Types	Station 0, Port 0	Station 1, Port 4 Station 2, Port 8	Station 0, Port 1 Station 1, Ports 5 and 6 Station 2, Port 9
PCI-Compatible Type 1 Configuration Header Registers (Offsets 00h – 3Ch)	00h – 3Ch	00h – 3Ch	00h – 3Ch
PCI Power Management Capability Registers (Offsets 40h – 44h)	40h – 44h	40h – 44h	40h – 44h
MSI Capability Registers (Offsets 48h – 64h)	48h – 64h	48h – 64h	48h – 64h
PCI Express Capability Registers (Offsets 68h – A0h)	68h – A0h	68h – A0h	68h – A0h
Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)	A4h – FCh	A4h – FCh	A4h – FCh
Device Serial Number Extended Capability Registers (Offsets 100h – 134h)	100h – 134h	100h – 134h	100h – 134h
Power Budget Extended Capability Registers (Offsets 138h – 144h)	Upstream Port, 138h – 144h		
Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)	148h – 1BCh	148h – 1BCh	148h – 1BCh
Port Arbitration Table Registers (Offsets 1A8h – 1BCh)	Upstream Port 0, 1A8h – 1BCh		
Device-Specific Registers (Offsets 1C0h – 51Ch)			
Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)	1C0h – 1FCh	1C0h, 1C4h, 1CCh – 1D0h, 1E0h – 1ECh, 1F8h, 1FCh	1E0h – 1ECh, 1F8h, 1FCh
Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)	200h – 25Ch	200h – 25Ch	
Device-Specific Registers – Serial EEPROM (Offsets 260h – 26Ch)	260h – 26Ch		

Table 12-3. Port Register Configuration and Map *(Cont.)*

Register Types	Station 0, Port 0	Station 1, Port 4 Station 2, Port 8	Station 0, Port 1 Station 1, Ports 5 and 6 Station 2, Port 9
Device-Specific Registers – Physical Layer (Offsets 270h – 28Ch)	270h – 28Ch		
Device-Specific Registers – I2C Slave Interface (Offsets 290h – 2C4h)	290h – 2C4h		
Device-Specific Registers – Bus Number CAM (Offsets 2C8h – 304h)	2C8h – 304h	2C8h – 304h	
Device-Specific Registers – I/O CAM (Offsets 308h – 344h)	308h – 344h	308h – 344h	
Device-Specific Registers – Address-Mapping CAM (Offsets 348h – 444h)	348h – 444h	348h – 444h	
Device-Specific Registers – Vendor-Specific Dual Cast Extended Capability (Offsets 448h – 51Ch)	448h – 51Ch		
ACS Extended Capability Registers (Offsets 520h – 528h)	520h – 528h	520h – 528h	520h – 528h
Device-Specific Registers (Offsets 54Ch – F8Ch)			
Device-Specific Registers – Port Configuration (Offsets 574h – 628h)	574h – 628h		
Device-Specific Registers – General-Purpose Input/Output (Offsets 62Ch – 65Ch)	62Ch – 65Ch		
Device-Specific Registers – Ingress Control and Port Enable (Offsets 660h – 67Ch)	660h – 67Ch	660h – 67Ch	
Device-Specific Registers – IOCAM Base and Limit Upper 16 Bits (Offsets 680h – 6BCh)	680h – 6BCh	680h – 6BCh	
Device-Specific Registers – Base Address Shadow (Offsets 6C0h – 73Ch)	6C0h – 73Ch	6C0h – 73Ch	
Device-Specific Registers – Virtual Channel Resource Control Shadow (Offsets 740h – 83Ch)	740h – 83Ch	740h – 83Ch	
Device-Specific Registers – Ingress Credit Handler Port Pool (Offsets 940h – 94Ch)	940h – 94Ch	940h – 94Ch	
Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)	950h – 95Ch	950h – 95Ch	950h – 95Ch
Device-Specific Registers – ACS Extended Capability (Offsets 980h – 9FCh)	980h – 9FCh	980h – 9FCh	
Device-Specific Registers – Ingress Credit Handler Threshold (Offsets A00h – B7Ch)	A00h – B7Ch	A00h – B7Ch	
Device-Specific Registers – SerDes Support (Offsets B80h – BFCh)	B80h – BFCh	B80h – BFCh	
Device-Specific Registers – Port Configuration Header (Offsets E00h – E3Ch)	E00h – E3Ch	E00h – E3Ch	
Device-Specific Registers – Source Queue Weight and Soft Error (Offsets F00h – F30h)	F00h – F30h	F00h – F30h	F10h

Table 12-3. Port Register Configuration and Map *(Cont.)*

Register Types	Station 0, Port 0	Station 1, Port 4 Station 2, Port 8	Station 0, Port 1 Station 1, Ports 5 and 6 Station 2, Port 9
Device-Specific Registers – Read Pacing (Offsets F34h – F3Ch)	Upstream Port 0, F34h – F3Ch		
Device-Specific Registers – Error Reporting (Offsets F40h – F4Ch)	F40h – F4Ch	F40h – F4Ch	
Device-Specific Registers – ARI Capability (Offsets F50h – F8Ch)	F50h – F8Ch	F50h – F8Ch	
Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)	FB4h – FDCh	FB4h – FDCh	FB4h – FDCh

12.4 Register Access

Each PEX 8624 Port implements a 4-KB Configuration Space. The lower 256 bytes (offsets 00h through FFh) comprise the PCI-compatible Configuration Space, and the upper 960 Dwords (offsets 100h through FFFh) comprise the PCI Express Extended Configuration Space. The PEX 8624 supports five mechanisms for accessing the Transparent Mode registers:

- PCI r3.0-Compatible Configuration Mechanism
- PCI Express Enhanced Configuration Access Mechanism
- Device-Specific Memory-Mapped Configuration Mechanism
- I^2C Slave Interface (refer to Chapter 7, "I2C Slave Interface Operation")
- Serial Peripheral Interface (SPI) Bus (refer to Chapter 6, "Serial EEPROM Controller")

The sideband register mechanisms (serial EEPROM and/or I^2C) can modify Read-Only (RO) register values.

Each Port captures the Bus Number and Device Number on every Type 0 Configuration Write, as required by the *PCI r3.0*. Therefore, following a Fundamental Reset, software must initially perform a Configuration Write to each Port (using either the PCI r3.0-Compatible Configuration Mechanism or PCI Express Enhanced Configuration Access Mechanism), to allow each Port to capture its designated Bus Number and Device Number. The initial access to each Port, *for example*, could be a Configuration Write Request to a RO register, such as the **Device ID** / **Vendor ID** register (offset 00h).

12.4.1 *PCI r3.0*-Compatible Configuration Mechanism

The *PCI r3.0*-Compatible Configuration mechanism provides standard access to the PEX 8624 Ports' first 256 bytes (the bytes at offsets 00h through FFh) of the PCI Express Configuration Space. The mechanism uses PCI Type 0 and Type 1 Configuration transactions to access the PEX 8624 Configuration registers. Each Port can convert a Type 1 Configuration Request (destined to a downstream Port or device) to a Type 0 Configuration Request (targeting the next downstream Port or device), as described below.

The PEX 8624 decodes all Type 1 Configuration accesses received on its upstream Port, when any of the following conditions exist:

- If the Bus Number in the Configuration access is not within the upstream Port's Secondary Bus Number and Subordinate Bus Number range, the PEX 8624 upstream Port responds with an Unsupported Request (UR).
- Specified Bus Number in the Configuration access is the PEX 8624 internal virtual PCI Bus Number, the PEX 8624 automatically converts the Type 1 Configuration access into the appropriate Type 0 Configuration access for the specified device.
  - If the specified device corresponds to the PCI-to-PCI bridge in one of the PEX 8624 downstream Ports, the PEX 8624 processes the Read or Write Request to the specified downstream Port register specified in the original Type 1 Configuration access.
  - If the specified Device Number does not correspond to any of the PEX 8624 downstream Port Device Numbers, the PEX 8624 responds with a UR.

- If the specified Bus Number in the Type 1 Configuration access is not the PEX 8624 internal virtual PCI Bus Number, but is the number of one of the PEX 8624 downstream Port secondary/ subordinate buses, the PEX 8624 passes the Configuration access on to the PCI Express Link attached to that PEX 8624 downstream Port.
- If the specified Bus Number is the downstream Port Secondary Bus Number, and the specified Device Number is 0, the PEX 8624 converts the Type 1 Configuration access to a Type 0 Configuration access before passing it on.
  - If the specified Device Number is not 0, the downstream Port drops the Transaction Layer Packet (TLP) and generates a UR.
- If the specified Bus Number is not the downstream Port Secondary Bus Number, the PEX 8624 passes along the Type 1 Configuration access, without change.

Because the mechanism is limited to the first 256 bytes of the PCI Express Configuration Space of the PEX 8624 Ports, the PCI Express Enhanced Configuration Access Mechanism or Device-Specific Memory-Mapped Configuration Mechanism must be used to access beyond Byte FFh. The PCI Express Enhanced Configuration Access mechanism can access the registers in the PCI-compatible region, as well as those in the PCI Express Extended Configuration Space.

12.4.2 PCI Express Enhanced Configuration Access Mechanism

The PCI Express Enhanced Configuration Access mechanism is implemented on all PCI Express PCs and on systems that do not implement a processor-specific firmware interface to the Configuration Space. The mechanism provides a Memory-Mapped Address space in the Root Complex, through which the Root Complex translates a Memory access into one or more Configuration Requests. Device drivers normally use an application programming interface (API) provided by the Operating System (OS), to use this mechanism.

The PCI Express Enhanced Configuration Access mechanism can be used to access all PEX 8624 registers.

12.4.3 Device-Specific Memory-Mapped Configuration Mechanism

The Device-Specific Memory-Mapped Configuration mechanism provides a method to access the Configuration registers of all Ports in a single 128-KB Memory map, as listed in Table 12-4. The registers of each Port are contained within a 4-KB range. The PEX 8624 supports up to six simultaneously active Ports.

This mechanism follows the *PCI Express Base r2.0* Configuration Request Routing rules, which do not allow the propagation of Configuration Requests from downstream-to-upstream nor peer-to-peer. By default, if any PEX 8624 downstream Port receives a Memory Request from a downstream device targeting the PEX 8624 Configuration registers, the Port:

- Responds to a Memory Read Request with a UR
- By default:
  - Silently discards a Memory Write Request (in compliance with the *PCI Express Base r2.0*) –or–
  - If the Port's **ECC Error Check Disable** register *Software Force Non-Posted Request* bit (offset 1C8h[3]) is Set, the Port responds with a UR

In Memory Requests that target PEX 8624 registers, the Payload Length indicated within the Memory Request Header must be 1 DWord. Lengths greater than 1 DWord result in a Completer Abort error.

To use this mechanism, program the upstream Port Type 1 Configuration Space **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively), which are typically enumerated at boot time by BIOS or the OS software. After the PEX 8624 upstream Port BARs are enumerated, Port 0 registers can be accessed with Memory Reads from and Writes to the first 4 KB (0000h to 0FFFh), Port 1 registers can be accessed with Memory Reads from and Writes to the second 4 KB (1000h to 1FFFh), and so forth. (Refer to Table 12-4.) Within each of these 4-KB windows, individual registers are located at the DWord offsets indicated in Table 12-1.

If upstream Port **BAR0** and **BAR1** are enumerated by serial EEPROM, rather than by BIOS/OS, the serial EEPROM must be programmed to also load the same values to the **BAR0** and **BAR1 Shadow** registers in each Station.

Note: *The Shadow registers provide another option. After **BAR0** and **BAR1** are programmed, it is possible to overwrite the "shadowed" location (using the serial EEPROM, I^2C Slave interface, or software) to set up non-tree hierarchies, in which each Station can have different Memory windows. If doing this, it is recommended to match the upstream Station Shadow register with the BARs.*

Table 12-4. Register Offsets from Upstream Port BAR0/1 Base Address

Port Number	Internal Register 4-KB Memory Space Range	Location Range
Port 0	0000h to 0FFFh	0 to 4 KB
Port 1	1000h to 1FFFh	4 to 8 KB
Port 4[a]	4000h to 4FFFh	16 to 20 KB
Port 5	5000h to 5FFFh	20 to 24 KB
Port 6	6000h to 6FFFh	24 to 28 KB
Port 8	8000h to 8FFFh	32 to 36 KB
Port 9	9000h to 9FFFh	36 to 40 KB

*a. Port 4 is **Software Only**.*

12.5 Register Descriptions

The remainder of this chapter details the PEX 8624 registers, including:

- Bit/field names
- Description of register functions for the PEX 8624 upstream Port and downstream Ports
- Type (*such as* RW or HwInit; refer to Table 12-5 for Type descriptions)
- Whether the power-on/reset value can be modified, by way of the PEX 8624 serial EEPROM and/or I^2C Initialization feature
- Default power-on/reset value

Table 12-5. Register Types, Grouped by User Accessibility

Type	Description
HwInit	**Hardware-Initialized** Refers to the PEX 8624 Hardware-Initialization mechanism or PEX 8624 Serial EEPROM or I^2C register Initialization features. RO after initialization and can only be reset with a Fundamental Reset. HwInit register bits are not modified by a Soft Reset.
RO	**Read-Only** Read-Only and cannot be altered by software. Permitted to be initialized by the PEX 8624 Hardware-Initialization mechanism or PEX 8624 serial EEPROM and/or I^2C register Initialization features.
ROS	**Read-Only, Sticky** Same as RO, except that bits are neither initialized nor modified by a Soft Reset.
RsvdP	***Reserved* and Preserved** ***Reserved*** for future RW implementations. Registers are RO and must return 0 when read. Software must preserve value read for Writes to bits.
RsvdZ	***Reserved* and Zero** ***Reserved*** for future RW1C implementations. Registers are RO and must return 0 when read. Software must use 0 for Writes to bits.
RW	**Read-Write** Read/Write and permitted to be Set or Cleared by software to the needed state.
RW1C	**Write 1 to Clear Status (Transparent mode)** Indicates status when read. A status bit Set by the system (to indicate status) is Cleared by writing 1 to that bit. Writing 0 has no effect. **Read-Write, Clear Interrupt (NT mode, Doorbell interrupts)** Indicates that a value of 1 Clears the interrupt.
RW1CS	**Write 1 to Clear, Sticky** Same as RW1C, except that bits are neither initialized nor modified by a Soft Reset.
RW1S	**Read-Write, Set Interrupt (NT mode, Doorbell interrupts)** Indicates that a value of 1 Sets the interrupt.
RWS	**Read-Write, Sticky** Same as RW, except that bits are Set or Cleared by software to the needed state. Bits are neither initialized nor modified by a Soft Reset.
RZ	**Software Read Zero** Software Read always returns 0; however, software is allowed to write this register.

12.6 PCI-Compatible Type 1 Configuration Header Registers (Offsets 00h – 3Ch)

This section details the PCI-Compatible Type 1 Configuration Header registers. Table 12-6 defines the register map.

Table 12-6. PCI-Compatible Type 1 Configuration Header Register Map (All Ports)[a]

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device ID		Vendor ID		00h
PCI Status		PCI Command		04h
PCI Class Code			PCI Revision ID	08h
PCI BIST ***(Not Supported)***	PCI Header Type	Master Latency Timer ***(Not Supported)***	Cache Line Size	0Ch
Base Address 0				10h
Base Address 1				14h
Secondary Latency Timer ***(Not Supported)***	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	18h
Secondary Status	***Not Supported/Reserved***	I/O Limit	I/O Base	1Ch
Memory Limit		Memory Base		20h
Prefetchable Memory Limit		Prefetchable Memory Base		24h
Prefetchable Memory Upper Base Address				28h
Prefetchable Memory Upper Limit Address				2Ch
I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits		30h
Reserved			Capability Pointer (40h)	34h
Expansion ROM Base Address ***(Reserved)***				38h
Not Supported/Reserved	Bridge Control	PCI Interrupt Pin	PCI Interrupt Line	3Ch

a. Some registers are available to all Ports; others are available only to Transparent Ports. Refer to the individual registers for details.

Register 12-1. 00h PCI Configuration ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**Vendor ID** Identifies the device manufacturer. Defaults to the PCI-SIG-issued Vendor ID of PLX (10B5h), if not overwritten by serial EEPROM and/or I^2C.	RO	Yes	10B5h
31:16	**Device ID** Identifies the particular device. Defaults to the PLX part number for the PEX 8624, if not overwritten by serial EEPROM and/or I^2C.	RO	Yes	8624h

Register 12-2. 04h PCI Command/Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	PCI Command			
0	**I/O Access Enable** 0 = PEX 8624 ignores I/O Space accesses on the corresponding Port's primary interface 1 = PEX 8624 responds to I/O Space accesses on the corresponding Port's primary interface	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8624 ignores Memory Space accesses on the corresponding Port's primary interface 1 = PEX 8624 responds to Memory Space accesses on the corresponding Port's primary interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8624 Memory and I/O Request forwarding upstream. Neither affect Message (including INT*x* Interrupt Messages) forwarding nor Completions traveling upstream or downstream. 0 = PEX 8624 handles Memory and I/O Requests received on the corresponding Port downstream/secondary interface as Unsupported Requests (URs); for Non-Posted Requests, the PEX 8624 returns a Completion with UR Completion status. Because MSI Messages are in-band Memory Writes, disables MSI Messages as well. 1 = PEX 8624 forwards Memory and I/O Requests upstream.	RW	Yes	0
3	**Special Cycle Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	0
4	**Memory Write and Invalidate Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	0
5	**VGA Palette Snoop** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	0
6	**Parity Error Response Enable** Controls bit 24 (*Master Data Parity Error Detected*).	RW	Yes	0
7	**IDSEL Stepping/Wait Cycle Control** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	0

Register 12-2. 04h PCI Command/Status (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
8	**SERR# Enable** Controls bit 30 (*Signaled System Error*). 1 = Enables reporting of Fatal and Non-Fatal errors detected by the device to the Root Complex, and, enables primary interface forwarding of ERR_FATAL and ERR_NONFATAL Messages from downstream Ports and devices when the Port's **Bridge Control** register *SERR# Enable* bit (offset 3Ch[17]) is Set	RW	Yes	0
9	**Fast Back-to-Back Transactions Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	0
10	**Interrupt Disable** 0 = Corresponding PEX 8624 Port is enabled to generate INT*x* Interrupt Messages and assert PEX_INTA# output 1 = Corresponding PEX 8624 Port is prevented from generating INT*x* Interrupt Messages and asserting PEX_INTA# output	RW	Yes	0
15:11	***Reserved***	RsvdP	No	00h

Register 12-2. 04h PCI Command/Status (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	PCI Status			
18:16	***Reserved***	RsvdP	No	000b
19	**Interrupt Status** 0 = No INT*x* Interrupt Message is pending 1 = INT*x* Interrupt Message is pending internally to the corresponding PEX 8624 Port –or– PEX_INTA# (if enabled) is asserted	RO	No	0
20	**Capability List** Capability function is supported. Set, as required by the *PCI Express Base r2.0*.	RO	Yes	1
21	**66 MHz Capable** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	0
22	***Reserved***	RsvdP	No	0
23	**Fast Back-to-Back Transactions Capable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	0
24	**Master Data Parity Error Detected** If bit 6 (*Parity Error Response Enable*) is Set, the corresponding PEX 8624 Port Sets this bit when the Port: • Forwards the poisoned TLP Write Request from the secondary to the primary interface, –or– • Receives a Completion marked as poisoned on the primary interface If the *Parity Error Response Enable* bit is Cleared, the PEX 8624 never Sets this bit. This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	**DEVSEL# Timing** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	00b
27	**Signaled Target Abort** The upstream Port Sets this bit if one of the following conditions exist: • Upstream Port receives a Memory Request targeting a PEX 8624 register, and the Payload Length (indicated within the Memory Request Header) is greater than 1 DWord • Upstream Port receives a Memory Request targeting a PEX 8624 register address within a non-existent Port • Transparent downstream Port Sets this bit if it detects an Access Control Services (ACS) violation This error is reported by the **Uncorrectable Error Status** register *Completer Abort Status* bit (offset FB8h[15]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0

Register 12-2. 04h PCI Command/Status (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
28	**Received Target Abort** Cleared; never Set.	RsvdP	No	0
29	**Received Master Abort** Cleared; never Set.	RsvdP	No	0
30	**Signaled System Error** If bit 8 (*SERR# Enable*) is Set, the corresponding PEX 8624 Port Sets this bit when it transmits or forwards an ERR_FATAL or ERR_NONFATAL Message upstream. This error is natively reported by the **Device Status** register *Fatal Error Detected* and *Non-Fatal Error Detected* bits (offset 70h[18:17], respectively), which are mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
31	**Detected Parity Error** 1 = Corresponding Port receives a Poisoned TLP on its primary side, regardless of the bit 6 (*Parity Error Response Enable*) state This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0

Register 12-3. 08h PCI Class Code and Revision ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
PCI Revision ID				
7:0	**Revision ID** Unless overwritten by the serial EEPROM, returns the Silicon Revision (AAh, ABh, or BBh), the PLX-assigned Revision ID for this version of the PEX 8624. The PEX 8624 Serial EEPROM register Initialization capability is used to replace the PLX Revision ID with another Revision ID.	RO	Yes	AAh, ABh, or BBh
PCI Class Code				**060400h**
15:8	**Register-Level Programming Interface** The PEX 8624 Ports support the *PCI-to-PCI Bridge r1.2* requirements, but not subtractive decoding, on their upstream interface.	RO	Yes	00h
23:16	**Sub-Class Code** PCI-to-PCI bridge.	RO	Yes	04h
31:24	**Base Class Code** Bridge device.	RO	Yes	06h

Register 12-4. 0Ch Miscellaneous Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Cache Line Size				
7:0	**Cache Line Size** System Cache Line Size. Implemented as a RW field for Conventional PCI compatibility purposes and does not impact PEX 8624 functionality.	RW	Yes	00h
Master Latency Timer				
15:8	**Master Latency Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	00h
PCI Header Type				
22:16	**Configuration Layout Type** The corresponding PEX 8624 Port Configuration Space Header adheres to the Type 1 PCI-to-PCI Bridge Configuration Space layout defined by the *PCI-to-PCI Bridge r1.2*.	RO	No	01h
23	**Multi-Function Device** 0 = Single-function device 1 = Indicates multiple (up to eight) functions (logical devices), each containing its own, individually addressable Configuration Space, 256 DWords in size	RO	No	0
PCI BIST				
31:24	**PCI BIST** ***Not supported*** Built-In Self-Test (BIST) Pass or Fail.	RsvdP	No	00h

Register 12-5. 10h Base Address 0 (Only Upstream Port; *Reserved* (RsvdP) for Downstream Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
0	**Memory Space Indicator** 0 = Base Address register maps the PEX 8624 Configuration registers into Memory space ***Note:*** *The upstream Port is hardwired to 0.*	Upstream	RO	No	0
	Reserved	Downstream	RsvdP	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	Upstream	RO	Yes	00b
	Reserved	Downstream	RsvdP	No	00b
3	**Prefetchable** 0 = Base Address register maps the PEX 8624 Configuration registers into Non-Prefetchable Memory space ***Note:*** *The upstream Port is hardwired to 0.*	Upstream	RO	Yes	0
	Reserved	Downstream	RsvdP	No	0
16:4	***Reserved***		RsvdP	No	0-0h
31:17	**Base Address 0** Base Address (**BAR0**) for the Device-Specific Memory-Mapped Configuration mechanism.	Upstream	RW	Yes	0-0h
	Reserved	Downstream	RsvdP	No	0-0h

Register 12-6. 14h Base Address 1 (Only Upstream Port; *Reserved* (RsvdP) for Downstream Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
31:0	**Base Address 1** For 64-bit addressing, Base Address 1 (**BAR1**) extends Base Address 0 (**BAR0**) to provide the upper 32 Address bits when the **Base Address 0** register *Memory Map Type* field (Upstream Port, offset 10h[2:1]) is programmed to 10b.	Upstream	RW	Yes	0000_0000h
	RO when the **Base Address 0** register is not enabled as a 64-bit BAR (*Memory Map Type* field (Upstream Port, offset 10h[2:1]) is not programmed to 10b).		RO	Yes	0000_0000h
	Reserved	Downstream	RsvdP	No	0000_0000h

Register 12-7. 18h Bus Number (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Primary Bus Number** Primary Bus Number of this PCI-to-PCI bridge. Records the Bus Number of the PCI Bus segment to which the primary interface of this Port is connected. Set by Configuration software.	RW	Yes	00h
15:8	**Secondary Bus Number** Secondary Bus Number of this PCI-to-PCI bridge. Records the Bus Number of the PCI Bus segment that is the secondary interface of this Port. Set by Configuration software.	RW	Yes	00h
23:16	**Subordinate Bus Number** Subordinate Bus Number of this PCI-to-PCI bridge. Records the Bus Number of the highest numbered PCI Bus segment that is subordinate to this Port. Set by Configuration software.	RW	Yes	00h
31:24	**Secondary Latency Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	00h

Register 12-8. 1Ch Secondary Status, I/O Limit, and I/O Base (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *If ISA Addressing mode is enabled (**PCI Command** register I/O Access Enable bit, offset 04h[0], is Set), the PEX 8624 Port forwards I/O transactions from its primary interface to its secondary interface (downstream) if an I/O address is within the range defined by the **I/O Base** and **I/O Limit** registers when the Base is less than or equal to the Limit.* *Conversely, the PEX 8624 Port forwards I/O transactions from its secondary interface to its primary interface (upstream) if an I/O address is outside this Address range. If the PEX 8624 Port does not implement an I/O Address range, the Port forwards all I/O transactions on its secondary interface upstream, to its primary interface.*				
I/O Base				
3:0	**I/O Base Addressing Capability** 1h = 32-bit I/O Address decoding is supported All other encodings are ***reserved***.	RO	Yes	1h
7:4	**I/O_BAR[15:12]** I/O Base Address[15:12]. The PEX 8624 Ports use their **I/O Base** and **I/O Limit** registers to determine the address range of I/O transactions to forward from one interface to the other. I/O Base Address[15:12] bits specify the corresponding PEX 8624 Port I/O Base Address[15:12]. The PEX 8624 assumes I/O Base Address[11:0]=000h. For 16-bit I/O addressing, the PEX 8624 assumes Address[31:16]=0000h. For 32-bit addressing, the PEX 8624 decodes Address[31:0], and uses the **I/O Upper Base and Limit Address** register *I/O Base Upper 16 Bits* and *I/O Limit Upper 16 Bits* fields (offset 30h[15:0 and 31:16], respectively).	RW	Yes	Fh
I/O Limit				
11:8	**I/O Limit Addressing Capability** 1h = 32-bit I/O Address decoding is supported All other encodings are ***reserved***.	RO	Yes	1h
15:12	**I/O_Limit[15:12]** I/O Limit Address[15:12]. The PEX 8624 Ports use their **I/O Base** and **I/O Limit** registers to determine the Address range of I/O transactions to forward from one interface to the other. I/O Limit Address[15:12] bits specify the corresponding PEX 8624 Port I/O Limit Address[15:12]. The PEX 8624 assumes Address bits [11:0] of the I/O Limit Address are FFFh. For 16-bit I/O addressing, the PEX 8624 decodes Address bits [15:0] and assumes Address bits [31:16] of the I/O Limit Address are 0000h. For 32-bit addressing, the PEX 8624 decodes Address bits [31:0], and uses the **I/O Upper Base and Limit Address** register *I/O Base Upper 16 Bits* and *I/O Limit Upper 16 Bits* fields (offset 30h[15:0 and 31:16], respectively). If the I/O Limit Address is less than the I/O Base Address, the PEX 8624 does not forward I/O transactions from the corresponding Port primary/upstream bus to its secondary/downstream bus. However, the PEX 8624 forwards all I/O transactions from the secondary bus of the corresponding Port to its primary bus.	RW	Yes	0h

Register 12-8. 1Ch Secondary Status, I/O Limit, and I/O Base (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	Secondary Status			
20:16	***Reserved***	RsvdP	No	0-0h
21	**66 MHz Capable** ***Not supported*** 0 = Not enabled, because PCI Express does ***not support*** 66 MHz	RsvdP	No	0
22	***Reserved***	RsvdP	No	0
23	**Fast Back-to-Back Transactions Capable** ***Reserved*** Not enabled, because PCI Express does ***not support*** this function.	RsvdP	No	0
24	**Master Data Parity Error** If the **Bridge Control** register *Parity Error Response Enable* bit (offset 3Ch[16]) is Set, the corresponding PEX 8624 Port Sets this bit when transmitting or receiving a TLP on its downstream side, and when either of the following two conditions occur: • Port receives Completion marked poisoned • Port forwards poisoned TLP Write Request If the *Parity Error Response Enable* bit is Cleared, the PEX 8624 never Sets this bit. These errors are reported by the Port's **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), and mirrored to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	**DEVSEL# Timing** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	00b
27	**Signaled Target Abort** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
28	**Received Target Abort** Cleared, as required by the *PCI Express Base r2.0*, because the PEX 8624 never initiates a Request itself.	RsvdP	No	0
29	**Received Master Abort** Cleared, as required by the *PCI Express Base r2.0*, because the PEX 8624 never initiates a Request itself.	RsvdP	No	0
30	**Received System Error** 1 = Downstream Port receives an ERR_FATAL or ERR_NONFATAL Message on its secondary interface from a downstream device	RW1C	Yes	0
31	**Detected Parity Error** Set by a downstream Port when receiving a poisoned TLP from a downstream device, regardless of the **Bridge Control** register *Parity Error Response Enable* bit (offset 3Ch[16]) state.	RW1C	Yes	0

Register 12-9. 20h Memory Base and Limit (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The PEX 8624 Port forwards Memory transactions from its primary interface to its secondary interface (downstream) if a Memory address is within the range defined by the* ***Memory Base*** *and* ***Memory Limit*** *registers (when the Base is less than or equal to the Limit).* *Conversely, the PEX 8624 Port forwards Memory transactions from its secondary interface to its primary interface (upstream) if a Memory address is outside this Address range (provided that the address is not within the range defined by the* ***Prefetchable Memory Base*** *(offsets 28h + 24h[15:0]) and* ***Prefetchable Memory Limit*** *(offsets 2Ch + 24h[31:16]) registers).*			
Memory Base				
3:0	***Reserved***	RsvdP	No	0h
15:4	**MEM_BAR[31:20]** Memory Base Address[31:20]. Specifies the corresponding PEX 8624 Port Non-Prefetchable Memory Base Address[31:20]. The PEX 8624 assumes Memory Base Address[19:0]=0_0000h.	RW	Yes	FFFh
Memory Limit				
19:16	***Reserved***	RsvdP	No	0h
31:20	**MEM_Limit[31:20]** Memory Limit Address[31:20]. Specifies the corresponding PEX 8624 Port Non-Prefetchable Memory Limit Address[31:20]. The PEX 8624 assumes Memory Limit Address[19:0]=F_FFFFh.	RW	Yes	000h

Register 12-10. 24h Prefetchable Memory Base and Limit (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: *The PEX 8624 Port forwards Memory transactions from its primary interface to its secondary interface (downstream) if a Memory address is within the range defined by the* ***Prefetchable Memory Base*** *(offsets 28h + 24h[15:0]) and* ***Prefetchable Memory Limit*** *(offsets 2Ch + 24h[31:16]) registers (when the Base is less than or equal to the Limit).* *Conversely, the PEX 8624 Port forwards Memory transactions from its secondary interface to its primary interface (upstream) if a Memory address is outside this Address range (provided that the address is not within the range defined by the* ***Memory Base*** *and* ***Memory Limit*** *registers (offset 20h)).*				
Prefetchable Memory Base				
0	**Prefetchable Memory Base Capability** 0 = Corresponding PEX 8624 Port supports 32-bit Prefetchable Memory Addressing 1 = Corresponding PEX 8624 Port defaults to 64-bit Prefetchable Memory Addressing support, as required by the *PCI Express Base r2.0* ***Note:*** *If the application needs 32-bit only Prefetchable space, the serial EEPROM or I^2C must Clear both this bit and bit 16 (Prefetchable Memory Limit Capability).*	RO	Yes	1
3:1	***Reserved***	RsvdP	No	000b
15:4	**PMEM_BAR[31:20]** Prefetchable Memory Base Address[31:20]. Specifies the corresponding PEX 8624 Port Prefetchable Memory Base Address[31:20]. The PEX 8624 assumes Prefetchable Memory Base Address[19:0]=0_0000h.	RW	Yes	FFFh
Prefetchable Memory Limit				
16	**Prefetchable Memory Limit Capability** 0 = Corresponding PEX 8624 Port supports 32-bit Prefetchable Memory Addressing 1 = Corresponding PEX 8624 Port defaults to 64-bit Prefetchable Memory Addressing support, as required by the *PCI Express Base r2.0*	RO	Yes	1
19:17	***Reserved***	RsvdP	No	000b
31:20	**PMEM_Limit[31:20]** Prefetchable Memory Limit Address[31:20]. Specifies the corresponding PEX 8624 Port Prefetchable Memory Limit Address[31:20]. The PEX 8624 assumes Prefetchable Memory Limit Address[19:0]=F_FFFFh.	RW	Yes	000h

Register 12-11. 28h Prefetchable Memory Upper Base Address (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
31:0	**PBUP[63:32]** Prefetchable Memory Base Address[63:32]. The PEX 8624 uses this register for Prefetchable Memory Upper Base Address[63:32]. When the **Prefetchable Memory Base** register *Prefetchable Memory Base Capability* field indicates 32-bit addressing, this register is RO and returns 0000_0000h.	Offset 24h[0]=1	RW	Yes	0000_0000h
		Offset 24h[0]=0	RO	No	0000_0000h

Register 12-12. 2Ch Prefetchable Memory Upper Limit Address (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
31:0	**PLIMUP[63:32]** Prefetchable Memory Limit Address[63:32]. The PEX 8624 uses this register for Prefetchable Memory Upper Limit Address[63:32]. When the **Prefetchable Memory Limit** register *Prefetchable Memory Limit Capability* field indicates 32-bit addressing, this register is RO and returns 0000_0000h. ***Note:*** *The serial EEPROM must not write a non-zero value into this register when the RO attribute is Set for this register.*	Offset 24h[16]=1	RW	Yes	0000_0000h
		Offset 24h[16]=0	RO	No	0000_0000h

Register 12-13. 30h I/O Upper Base and Limit Address (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
15:0	**I/O Base Upper 16 Bits** The PEX 8624 uses this register for I/O Base Address[31:16]. When the **I/O Base** register *I/O Base Addressing Capability* field indicates 16-bit addressing, this register is RO and returns 0000h.	Offset 1Ch[3:0]=1h	RW	Yes	0000h
		Offset 1Ch[3:0]=0h	RO	No	0000h
31:16	**I/O Limit Upper 16 Bits** The PEX 8624 uses this register for I/O Limit Address[31:16]. When the **I/O Limit** register *I/O Limit Addressing Capability* field indicates 16-bit addressing, this register is RO and returns 0000h. ***Note:*** *The serial EEPROM must not write a non-zero value into this register when the RO attribute is Set for this register.*	Offset 1Ch[11:8]=1h	RW	Yes	0000h
		Offset 1Ch[11:8]=0h	RO	No	0000h

Register 12-14. 34h Capability Pointer (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Capability Pointer** Default 40h points to the **PCI Power Management Capability** structure.	RO	Yes	40h
31:8	***Reserved***	RsvdP	No	0000_00h

Register 12-15. 38h Expansion ROM Base Address (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Expansion ROM Base Address** ***Reserved***	RsvdP	No	0000_0000h

Register 12-16. 3Ch Bridge Control and PCI Interrupt Signal (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	PCI Interrupt Signal			
7:0	**PCI Interrupt Line** Interrupt line routing value. The PEX 8624 does ***not*** use this register; however, the register is included for operating system and device driver use.	RW	Yes	00h
15:8	**PCI Interrupt Pin** Identifies the Conventional PCI Interrupt Message(s) that the device (or device function) uses. Only value 00h or 01h is allowed in the PEX 8624. 00h = Indicates that the device does not use Conventional PCI Interrupt Message(s) 01h, 02h, 03h, and 04h = Maps to Conventional PCI Interrupt Messages for INTA#, INTB#, INTC#, and INTD#, respectively	RO	Yes	01h
	Bridge Control			
16	**Parity Error Response Enable** Controls the response to Poisoned TLPs. 0 = Disables the **Secondary Status** register *Master Data Parity Error* bit (offset 1Ch[24]) 1 = Enables the **Secondary Status** register *Master Data Parity Error* bit (offset 1Ch[24])	RW	Yes	0
17	**SERR# Enable** Controls forwarding of ERR_COR, ERR_FATAL, and ERR_NONFATAL from the secondary interface to the primary interface. When Set, and the **PCI Command** register *SERR# Enable* bit (offset 04h[8]) is also Set, enables the **PCI Status** register *Signaled System Error* bit (offset 04h[30]).	RW	Yes	0
18	**ISA Enable** Modifies the PEX 8624's response to ISA I/O addresses enabled by the **I/O Base** and **I/O Limit** registers (offset 1Ch[7:0 and 15:8], respectively) and located in the first 64 KB of the PCI I/O Address space (0000_0000h to 0000_FFFFh). The default state of this bit after reset is 0. 0 = If ISA Addressing mode is enabled (**PCI Command** register *I/O Access Enable* bit, offset 04h[0], is Set), the PEX 8624 Port forwards I/O Requests within the Address range defined by the **I/O Base** and **I/O Limit** registers. 1 = PEX 8624 blocks forwarding from the primary to secondary interface, of I/O transactions addressing the last 768 bytes in each 1-KB block of the Port's I/O Address range. In the opposite direction (secondary to primary), if I/O Addressing mode is enabled, the PEX 8624 Port forwards I/O transactions that address the last 768 bytes in each 1-KB block of the Port's I/O Address range. ***Note:*** *Refer also to the **Ingress Control** register Disable VGA BIOS Memory Access Decoding bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 660h[28]).*	RW	Yes	0

Register 12-16. 3Ch Bridge Control and PCI Interrupt Signal (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
19	**VGA Enable** Modifies the bridge response to VGA-compatible addresses. When Set, the bridge positively decodes and forwards the following addresses on the primary interface to the secondary interface (and, conversely, blocks forwarding of these addresses from the secondary interface to the primary interface): • Memory addresses within the range 000A_0000h to 000B_FFFFh • I/O addresses in the first 64 KB of the I/O Address space (AD[31:16] is 0000h), where AD[9:0] is within the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – AD[15:10] is not decoded) Additionally, when Set, forwarding of these addresses is independent of the: • Memory and I/O Address ranges defined by the bridge **I/O Base**, **I/O Limit**, **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers • Bit 18 (*ISA Enable*) or **PCI Command** register *VGA Palette Snoop* bit (offset 04h[5]) Settings VGA address forwarding is qualified by the **PCI Command** register *Memory Access Enable* and *I/O Access Enable* bits (offset 04h[1:0], respectively). The default state of this bit after reset must be 0. 0 = Do not forward VGA-compatible Memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined Memory and I/O Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (when the *I/O Access Enable* and *Memory Access Enable* bits are Set), independent of the Memory and I/O Address ranges and independent of the *ISA Enable* bit ***Notes:*** *When Set in an egress Port, the Port is configured as a non-Cut-Thru path. (Refer to Section 2.1.3.2, "Cut-Thru Mode," for further details.)* *Refer also to the **Ingress Control** register Disable VGA BIOS Memory Access Decoding bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 660h[28]).* ***Conventional PCI VGA support** – To avoid potential I/O address conflicts, if the VGA Enable bit is Set in the upstream Port and a downstream Port, Set the **PCI Command** register I/O Access Enable bit (offset 04h[0]) in the remaining downstream Ports, unless those downstream Ports are configured to use default 32-bit address decoding and their I/O Address range is programmed above 1_0000h.*	RW	Yes	0

Register 12-16. 3Ch Bridge Control and PCI Interrupt Signal (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
20	**VGA 16-Bit Decode Enable** Used only when bit 19 (*VGA Enable*) or the **PCI Command** register *VGA Palette Snoop* bit (offset 04h[5]) is also Set, enabling VGA I/O decoding and forwarding by the bridge. Status after reset is 0. Enables system configuration software to select between 10- and 16-bit I/O address decoding, for VGA I/O register accesses forwarded from the primary interface to the secondary interface. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses ***Note:*** *Refer also to the **Ingress Control** register Disable VGA BIOS Memory Access Decoding bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 660h[28]).*	RW	Yes	0
21	**Master Abort Mode** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
22	**Secondary Bus Reset** 1 = Causes a Hot Reset on the corresponding PEX 8624 Port downstream Link	RW	Yes	0
23	**Fast Back-to-Back Transactions Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
24	**Primary Discard Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
25	**Secondary Discard Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
26	**Discard Timer Status** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
27	**Discard Timer SERR# Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
31:28	***Reserved***	RsvdP	No	0h

12.7 PCI Power Management Capability Registers (Offsets 40h – 44h)

This section details the PCI Power Management Capability registers. Table 12-7 defines the register map.

Table 12-7. PCI Power Management Capability Register Map (All Ports)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Power Management Capability		Next Capability Pointer (48h)	Capability ID (01h)	40h
PCI Power Management Data	PCI Power Management Control/Status Bridge Extensions ***(Reserved)***	PCI Power Management Status and Control		44h

Register 12-17. 40h PCI Power Management Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Capability ID** Programmed to 01h, indicating that the Capability structure is the **PCI Power Management Capability** structure.	RO	Yes	01h
15:8	**Next Capability Pointer** Default 48h points to the **MSI Capability** structure.	RO	Yes	48h
18:16	**Version** Default 011b indicates compliance with the *PCI Power Mgmt. r1.2.*	RO	Yes	011b
19	**PME Clock** Power Management Event (PME) clock. Does not apply to PCI Express. Returns 0.	RsvdP	No	0
20	***Reserved***	RsvdP	No	0
21	**Device-Specific Initialization** Default 0 indicates that Device-Specific Initialization is ***not*** required.	RO	Yes	0
24:22	**AUX Current** The PEX 8624 does ***not support*** PME generation from the D3cold Device Power Management (PM) state; therefore, the serial EEPROM value for this field should be 000b.	RO	Yes	000b
25	**D1 Support** ***Not supported*** Default value of 0 indicates that the PEX 8624 does ***not support*** the D1 Device PM state.	RsvdP	No	0
26	**D2 Support** ***Not supported*** Default value of 0 indicates that the PEX 8624 does ***not support*** the D2 Device PM state.	RsvdP	No	0
31:27	**PME Support** Bits [31, 30, and 27] must be Set, to indicate that the PEX 8624 will forward PME Messages, as required by the *PCI Express Base r2.0*.	RO	Yes	19h

Register 12-18. 44h PCI Power Management Status and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
PCI Power Management Status and Control				
1:0	**Power State** Used to determine the Port's current Device PM state, and to program the Port into a new Device PM state. 00b = D0 01b = D1 – ***Not supported*** 10b = D2 – ***Not supported*** 11b = D3hot If software attempts to write an unsupported state to this field, the Write operation completes normally; however, the data is discarded and no state change occurs.	RW	Yes	00b
2	***Reserved***	RsvdP	No	0
3	**No Soft Reset** 1 = Devices transitioning from the D3hot to D0 Device PM state, because of Power State commands, do not perform an internal reset	RO	Yes	1
7:4	***Reserved***	RsvdP	No	0h
8	**PME Enable** 0 = Disables PME generation by the corresponding PEX 8624 Port[a] 1 = Enables PME generation by the corresponding PEX 8624 Port	RWS	No	0
12:9	**Data Select** Initially writable by serial EEPROM and/or I²C only[b]. This Configuration Space register (CSR) access privilege changes to RW after a Serial EEPROM or I²C Write occurs to this register. Selects the **Data** and **Data Scale** registers (fields [31:24 and 14:13], respectively). 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated All other encodings are ***reserved***.	RO	Yes	0h
14:13	**Data Scale** Writable by serial EEPROM and/or I²C only[b]. Indicates the scaling factor to be used when interpreting the **Data** register value. The value and meaning of this field varies, depending upon which data value is selected by field [12:9] (*Data Select*). There are four internal **Data Scale** registers (one each, per *Data Select* values 0h, 3h, 4h, and 7h), per Port. For other *Data Select* values, the **Data Scale** value returned is 0h.	RO	Yes	00b
15	**PME Status** 0 = PME is not generated by the corresponding PEX 8624 Port[a] 1 = PME is being generated by the corresponding PEX 8624 Port	RW1CS	No	0

Register 12-18. 44h PCI Power Management Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
PCI Power Management Control/Status Bridge Extensions				
21:16	***Reserved***	RsvdP	No	0-0h
22	**B2/B3 Support** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
23	**Bus Power/Clock Control Enable** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
PCI Power Management Data				
31:24	**Data** Writable by serial EEPROM and/or I^2C only[b]. There are four supported *Data Select* values (0h, 3h, 4h, and 7h), per Port. For other *Data Select* values, the **Data Scale** value returned is 0h. Selected by field [12:9] (*Data Select*).	RO	Yes	00h

a. Because the PEX 8624 does not consume auxiliary power, this bit is not sticky, and is always Cleared at power-on reset.

*b. With no serial EEPROM nor previous I^2C programming, Reads return 00h for the **Data** and **Data Scale** registers (for all Data Selects).*

12.8 MSI Capability Registers (Offsets 48h – 64h)

This section details the Message Signaled Interrupt (MSI) Capability registers. Table 12-8 defines the register map.

Table 12-8. MSI Capability Register Map (All Ports)[a]

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
MSI Control		Next Capability Pointer (68h)	Capability ID (05h)	48h
MSI Address				4Ch
MSI Upper Address				50h
Reserved		MSI Data		54h
MSI Mask				58h
MSI Status				5Ch
Reserved				60h – 64h

*a. Offsets 54h, 58h, and 5Ch change to 50h, 54h, and 58h, respectively, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.*

Register 12-19. 48h MSI Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
MSI Capability Header				
7:0	**Capability ID** Programmed to 05h, as required by the *PCI r3.0.*	RO	Yes	05h
15:8	**Next Capability Pointer** Programmed to 68h, to point to the **PCI Express Capability** structure.	RO	Yes	68h
MSI Control				
16	**MSI Enable** 0 = MSIs for the corresponding Port are disabled 1 = MSIs for the corresponding Port are enabled, and INT*x* Interrupt Messages and PEX_INTA# output assertion are disabled	RW	Yes	0
19:17	**Multiple Message Capable** 000b = PEX 8624 Port can request only one Vector 001b = PEX 8624 Port can request two Vectors 010b = PEX 8624 Port can request four Vectors 010b through 111b = PEX 8624 Port can request four Vectors	RO	Yes	010b
22:20	**Multiple Message Enable** 000b = PEX 8624 Port is allocated one Vector, by default 001b = PEX 8624 Port is allocated two Vectors 010b through 111b = PEX 8624 Port is allocated four Vectors ***Note:*** *This field should not be programmed with a value larger than that of field [19:17] (Multiple Message Capable). If the value of this field is larger than that of field [19:17], the Multiple Message Capable value takes effect.*	RW	Yes	000b
23	**MSI 64-Bit Address Capable** 0 = PEX 8624 is capable of generating MSI 32-bit addresses (**MSI Address** register, offset 4Ch, is the Message address) 1 = PEX 8624 is capable of generating MSI 64-bit addresses (**MSI Address** register, offset 4Ch, is the lower 32 bits of the Message address, and **MSI Upper Address** register, offset 50h, is the upper 32 bits of the Message address)	RO	Yes	1
24	**Per Vector Masking Capable** 0 = PEX 8624 does not have Per Vector Masking capability 1 = PEX 8624 has Per Vector Masking capability	RO	Yes	1
31:25	***Reserved***	RsvdP	No	0-0h

Register 12-20. 4Ch MSI Address (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
1:0	***Reserved***	RsvdP	No	00b
31:2	**Message Address** ***Note:*** *Refer to register offset 50h for MSI Upper Address, if offset 48h[23] is Set (default).*	RW	Yes	0-0h

Register 12-21. 50h MSI Upper Address (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Message Upper Address** This register is valid/used only when the **MSI Control** register *MSI 64-Bit Address Capable* bit (offset 48h[23]) is Set. MSI Write transaction upper address[63:32]. ***Note:*** *Refer to register offset 4Ch for MSI Address.*	RW	Yes	0000_0000h

Register 12-22. 54h MSI Data (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The offset for this register changes from 54h, to 50h, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.*				
15:0	**Message Data** MSI Write transaction TLP payload.	RW	Yes	0000h
31:16	***Reserved***	RsvdP	No	0000h

Register 12-23. 58h MSI Mask (All Ports)

Bit(s)	Description		Ports	Type	Serial EEPROM and I²C	Default
The interrupt sources in a PEX 8624 Port are grouped into four main categories – Power Management/Hot Plug or Link State events, Device-Specific errors and events, and GPIO-generated interrupts, and NT-Virtual Doorbell-generated interrupts. The number of allocated MSI Vectors is determined by the **MSI Control** register *Multiple Message Capable* and *Multiple Message Enable* fields (offset 48h[19:17 and 22:20], respectively). When the number of MSI Vectors that can be requested is: • **Four** – Device-Specific errors and events, Power Management/Hot Plug or Link State events, and GPIO events each generate their own MSI Vector. • **Two** – Device-Specific errors and events generate their own MSI Vector, while all other categories are combined and generate the same Vector. • **One** – All interrupt categories generate the same MSI Vector. NT-Virtual Doorbell interrupts are generated only on the NT Port. The Type is the same, regardless of whether it is for a Transparent or NT Port. ***Note:*** *The offset for this register changes from 58h, to 54h, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.* *The bits in this register can be used to mask their respective **MSI Status** register bits (offset 5Ch).*						
0	**MSI Mask for Hot Plug or Link State Events** MSI mask for Power Management event- or Hot Plug or Link State event-generated interrupts.	Offset 48h[22:20] ≥010b	All Ports	RW	Yes	0
	MSI Mask for Shared Interrupt Sources MSI mask for all interrupt sources when the **MSI Control** register *Multiple Message Enable* field indicates that the Host has allocated one or two Vectors.	Offset 48h[22:20] ≤001b	All Ports	RW	Yes	0
1	**MSI Mask for Device-Specific Errors and Events** MSI mask for Device-Specific error- and event-generated interrupts. ***Note:*** *For further details, refer to Section 9.1.1, "Interrupt Sources or Events."*					
	Enables MSIs for the RAM ECC errors defined in the **Device-Specific Error Status for Egress ECC Error**, **Device-Specific Error Mask for Egress ECC Error**, **Error Handler 32-Bit Error Status**, and **Error Handler 32-Bit Error Mask** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, unless noted otherwise, offsets 1C0h, 1C4h, 1CCh, and 1D0h, respectively).	Offset 48h[22:20] ≥001b	Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, unless noted otherwise	RW	Yes	0
	Also enables MSIs for the NT-Link Port events defined in the **Link Error Status Virtual** and **Link Error Mask Virtual** registers (NT Port Virtual Interface, offsets FE0h and FE4h, respectively).	Offset 48h[22:20] ≥001b	Port 0, NT Port Virtual Interface	RW	Yes	0
	Reserved	Offset 48h[22:20] =000b	–	RsvdP	No	0

Register 12-23. 58h MSI Mask (All Ports) *(Cont.)*

Bit(s)	Description		Ports	Type	Serial EEPROM and I^2C	Default
2	**MSI Mask for GPIO-Generated Interrupts**	Offset 48h[22:20] ≥010b	Port 0	RW	Yes	0
	Reserved	Offset 48h[22:20] ≤001b	–	RsvdP	No	0
3	**MSI Mask for NT-Virtual Doorbell-Generated Interrupts** ***This bit is valid only in NT mode.*** Refer to the NT Port registers located at offsets C4Ch through C58h.	Offset 48h[22:20] ≥010b	Port 0, NT Port Virtual Interface	RW	Yes	0
	Reserved	Offset 48h[22:20] ≤001b	–	RsvdP	No	0
31:4	***Reserved***			RsvdP	No	0000_000h

Register 12-24. 5Ch MSI Status (All Ports)

Bit(s)	Description		Ports	Type	Serial EEPROM and I^2C	Default
The interrupt sources in a PEX 8624 Port are grouped into four categories – Power Management/Hot Plug or Link State events, Device-Specific errors and events, GPIO-generated interrupts, and NT-Virtual Doorbell-generated interrupts. The number of allocated MSI Vectors is determined by the **MSI Control** register *Multiple Message Capable* and *Multiple Message Enable* fields (offset 48h[19:17 and 22:20], respectively). When the number of MSI Vectors that can be requested is: • **Four** – Device-Specific errors and events, Power Management/Hot Plug or Link State events, and GPIO events each generate their own MSI Vector. • **Two** – Device-Specific errors and events generate their own MSI Vector, while all other categories are combined and generate the same Vector. • **One** – All interrupt categories generate the same MSI Vector. NT-Virtual Doorbell interrupts are generated only on the NT Port. The Type is the same, regardless of whether it is for a Transparent or NT Port. ***Note:*** *The offset for this register changes from 5Ch, to 58h, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.* *The bits in this register can be masked by their respective **MSI Mask** register bits (offset 58h).*						
0	**MSI Pending Status for Hot Plug or Link State Events** MSI pending status for Power Management event- or Hot Plug or Link State event-generated interrupts.	Offset 48h[22:20] ≥010b	All Ports	RO	No	0
	MSI Pending Status for Shared Interrupt Sources MSI pending status for all interrupt sources when the **MSI Control** register *Multiple Message Enable* field indicates that the Host has allocated one or two Vectors.	Offset 48h[22:20] ≤001b	All Ports	RO	No	0

Register 12-24. 5Ch MSI Status (All Ports) *(Cont.)*

Bit(s)	Description		Ports	Type	Serial EEPROM and I²C	Default
1	**MSI Pending Status for Device-Specific Errors and Events** MSI pending status for Device-Specific error- and event-generated interrupts. ***Note:*** *For further details, refer to Section 9.1.1, "Interrupt Sources or Events."*					
	Reports status of enabled MSIs for the RAM ECC errors defined in the **Device-Specific Error Status for Egress ECC Error**, **Device-Specific Error Mask for Egress ECC Error**, **Error Handler 32-Bit Error Status**, and **Error Handler 32-Bit Error Mask** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, unless noted otherwise, offsets 1C0h, 1C4h, 1CCh, and 1D0h, respectively).	Offset 48h[22:20] ≥001b	Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, unless noted otherwise	RO	No	0
	Also reports status of enabled MSIs for the NT-Link Port events defined in the **Link Error Status Virtual** and **Link Error Mask Virtual** registers (NT Port Virtual Interface, offsets FE0h and FE4h, respectively).	Offset 48h[22:20] ≥001b	Port 0, NT Port Virtual Interface	RO	No	0
	Reserved	Offset 48h[22:20] =000b	–	RsvdP	No	0
2	**MSI Pending Status for GPIO-Generated Interrupts**	Offset 48h[22:20] ≥010b	Port 0	RO	No	0
	Reserved	Offset 48h[22:20] ≤001b	–	RsvdP	No	0
3	**MSI Pending Status for NT-Virtual Doorbell-Generated Interrupts** ***This bit is valid only in NT mode.*** Refer to the NT Port registers located at offsets C4Ch through C58h.	Offset 48h[22:20] ≥010b	Port 0, NT Port Virtual Interface	RO	No	0
	Reserved	Offset 48h[22:20] ≤001b	–	RsvdP	No	0
31:4	***Reserved***			RsvdP	No	0000_000h

12.9 PCI Express Capability Registers (Offsets 68h – A0h)

This section details the PCI Express Capability registers. Hot Plug Capability, Command, Status, and Events are included in these registers. Table 12-9 defines the register map.

Table 12-9. PCI Express Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Express Capability		Next Capability Pointer (A4h)	Capability ID (10h)	68h
Device Capability				6Ch
Device Status		***Not Supported/Reserved***	Device Control	70h
Link Capability				74h
Link Status		Link Control		78h
Reserved (Upstream) Slot Capability (Downstream)				7Ch
Reserved (Upstream)				80h
Slot Status (Downstream)		Slot Control (Downstream)		
Reserved				84h – 88h
Device Capability 2				8Ch
Device Status 2 ***(Reserved)***		Device Control 2		90h
Reserved				94h
Link Status 2		Link Control 2		98h
Reserved				9Ch – A0h

Register 12-25. 68h PCI Express Capability List and Capability (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
PCI Express Capability List					
7:0	**Capability ID** Programmed to 10h, as required by the *PCI Express Base r2.0.*		RO	Yes	10h
15:8	**Next Capability Pointer** Programmed to A4h, to point to the **Subsystem Capability** structure.		RO	Yes	A4h
PCI Express Capability					
19:16	**Capability Version** The PEX 8624 Ports program this field to 2h, as required by the *PCI Express Base r2.0.*		RO	Yes	2h
23:20	**Device/Port Type** Set at reset, as required by the *PCI Express Base r2.0.*	Upstream	RO	Yes	5h
		Downstream	RO	Yes	6h
24	**Slot Implemented** 0 = Disables or connects to the upstream Port	Upstream	RsvdP	No	0
	0 = Disables or connects to an integrated component 1 = Indicates that the downstream Port connects to a slot, as opposed to being connected to an integrated component or being disabled ***Note:*** *The PEX 8624 serial EEPROM register Initialization capability and/or I^2C can be used to Clear this bit, indicating that the corresponding PEX 8624 downstream Port connects to an integrated component or is disabled.*	Downstream	RO	Yes	1
29:25	**Interrupt Message Number** The serial EEPROM writes 00_000b, because the Base Message and MSI Messages are the same.		RO	Yes	00_000b
31:30	***Reserved***		RsvdP	No	00b

Register 12-26. 6Ch Device Capability (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
2:0	**Maximum Payload Size Supported** The Maximum Payload Size for each Port is 2,048 bytes. 000b = PEX 8624 Port supports a 128-byte maximum payload 001b = PEX 8624 Port supports a 256-byte maximum payload 010b = PEX 8624 Port supports a 512-byte maximum payload 011b = PEX 8624 Port supports a 1,024-byte maximum payload 100b = PEX 8624 Port supports a 2,048-byte maximum payload No other encodings are supported.		HwInit	Yes	100b
4:3	**Phantom Functions Supported** ***Not supported***		RO	Yes	00b
5	**Extended Tag Field Supported** 0 = Maximum *Tag* field is 5 bits 1 = Maximum *Tag* field is 8 bits		RO	Yes	0
8:6	**Endpoint L0s Acceptable Latency** ***Not supported*** Because the PEX 8624 is a switch and not an endpoint, the PEX 8624 does ***not support*** this feature. 000b = Disables the capability		RO	Yes	000b
11:9	**Endpoint L1 Acceptable Latency** ***Not supported*** Because the PEX 8624 is a switch and not an endpoint, the PEX 8624 does ***not support*** this feature. 000b = Disables the capability		RO	Yes	000b
14:12	***Reserved***, as required by the *PCI Express Base r2.0*.		RsvdP	No	000b
15	**Role-Based Error Reporting**		RO	Yes	1
17:16	***Reserved***		RsvdP	No	00b
25:18	**Captured Slot Power Limit Value** For the PEX 8624 upstream Port, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [27:26] (*Captured Slot Power Limit Scale*).	Upstream	RO	Yes	00h
	Not valid	Downstream	RsvdP	No	00h
27:26	**Captured Slot Power Limit Scale** For the PEX 8624 upstream Port, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [25:18] (*Captured Slot Power Limit Value*). 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001	Upstream	RO	Yes	00b
	Not valid	Downstream	RsvdP	No	00b
31:28	***Reserved***		RsvdP	No	0h

Register 12-27. 70h Device Status and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Device Control				
0	**Correctable Error Reporting Enable** 0 = Disables 1 = Enables the corresponding PEX 8624 Port to report Correctable errors	RW	Yes	0
1	**Non-Fatal Error Reporting Enable** 0 = Disables 1 = Enables the corresponding PEX 8624 Port to report Non-Fatal errors	RW	Yes	0
2	**Fatal Error Reporting Enable** 0 = Disables 1 = Enables the corresponding PEX 8624 Port to report Fatal errors	RW	Yes	0
3	**Unsupported Request Reporting Enable** 0 = Disables 1 = Enables the corresponding PEX 8624 Port to report UR errors	RW	Yes	0
4	**Enable Relaxed Ordering** ***Not supported***	RsvdP	No	0
7:5	**Maximum Payload Size** Software can change this field to configure the PEX 8624 Ports to support other Payload Sizes; however, software cannot change this field to a value larger than that indicated by the **Device Capability** register *Maximum Payload Size Supported* field (offset 6Ch[2:0]). 000b = PEX 8624 Port supports a 128-byte maximum payload 001b = PEX 8624 Port supports a 256-byte maximum payload 010b = PEX 8624 Port supports a 512-byte maximum payload 011b = PEX 8624 Port supports a 1,024-byte maximum payload 100b = PEX 8624 Port supports a 2,048-byte maximum payload No other encodings are supported.	RW	Yes	000b
8	**Extended Tag Field Enable** ***Not supported***	RsvdP	No	0
9	**Phantom Functions Enable** ***Not supported***	RsvdP	No	0
10	**AUX Power PM Enable** ***Not supported***	RsvdP	No	0
11	**Enable No Snoop** ***Not supported***	RsvdP	No	0
14:12	**Max Read Request Size** ***Not supported***	RsvdP	No	000b
15	***Reserved*** Hardwired to 0, as required by the *PCI Express Base r2.0*.	RsvdP	No	0

Register 12-27. 70h Device Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	Device Status			
16	**Correctable Error Detected** Set when the corresponding Port detects a Correctable error, regardless of the bit 0 (*Correctable Error Reporting Enable*) state. 0 = Corresponding PEX 8624 Port did not detect a Correctable error 1 = Corresponding PEX 8624 Port detected a Correctable error	RW1C	Yes	0
17	**Non-Fatal Error Detected** Set when the corresponding Port detects a Non-Fatal error, regardless of the bit 1 (*Non-Fatal Error Reporting Enable*) state. 0 = Corresponding PEX 8624 Port did not detect a Non-Fatal error 1 = Corresponding PEX 8624 Port detected a Non-Fatal error	RW1C	Yes	0
18	**Fatal Error Detected** Set when the corresponding Port detects a Fatal error, regardless of the bit 2 (*Fatal Error Reporting Enable*) state. 0 = Corresponding PEX 8624 Port did not detect a Fatal error 1 = Corresponding PEX 8624 Port detected a Fatal error	RW1C	Yes	0
19	**Unsupported Request Detected** Set when the corresponding Port detects a UR, regardless of the bit 3 (*Unsupported Request Reporting Enable*) state. 0 = Corresponding PEX 8624 Port did not detect a UR 1 = Corresponding PEX 8624 Port detected a UR	RW1C	Yes	0
20	**AUX Power Detected** ***Not supported***	RsvdP	No	0
21	**Transactions Pending** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 12-28. 74h Link Capability (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Note: *The Port configuration (including Link width) for each Station is provided in Table 12-10. Yellow-highlighted table cells indicate the default Hot Plug Port for each configuration.*					
3:0	**Supported Link Speeds** Indicates the Port's supported Link speed. 0001b = 2.5 GT/s Link speed is supported 0010b = 5.0 GT/s and 2.5 GT/s Link speeds are supported All other encodings are ***reserved***.		RO	Yes	0010b (STRAP_RESERVED17#=H) 0001b (STRAP_RESERVED17#=L)
9:4	**Maximum Link Width** The PEX 8624 maximum Link width is x8 = 00_1000b. Actual maximum Link width is Set by the STRAP_STN*x*_PORTCFG*x* inputs. 00_0000b = ***Reserved*** 00_0001b = x1 00_0010b = x2 00_0100b = x4 00_1000b = x8 All other encodings are ***not supported***.		ROS	No	Set by STRAP_STN*x*_PORTCFG*x* input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station x* bits (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[5:0])
11:10	**Active State Power Management (ASPM) Support** Active State Link PM support. Indicates the level of ASPM supported by the Port. 01b = L0s Link PM state entry is supported 11b = L0s and L1 Link PM states are supported All other encodings are ***reserved***.		RO	Yes	11b

Register 12-28. 74h Link Capability (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
14:12	**L0s Exit Latency** Indicates the L0s Link PM state exit latency for the given PCI Express Link. Value depends upon the **Physical Layer Command and Status** register *N_FTS Value* field (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 220h[15:8]) value and Link speed. Exit latency is calculated, as follows: • **2.5 GHz** – Multiply *N_FTS Value* x 4 (4 symbol times in 1 N_FTS) x 4 ns (1 symbol time at 2.5 GT/s) • **5.0 GHz** – Multiply *N_FTS Value* x 4 (4 symbol times in 1 N_FTS) x 2 ns (1 symbol time at 5.0 GT/s) 100b = Corresponding PEX 8624 Port L0s Link PM state Exit Latency is 512 ns to less than 1 s at 5.0 GT/s 101b = Corresponding PEX 8624 Port L0s Link PM state Exit Latency is 1 s to less than 2 s at 2.5 GT/s All other encodings are ***reserved***.		RO	No	100b (5.0 GT/s) 101b (2.5 GT/s)
17:15	**L1 Exit Latency** Indicates the L1 Link PM state exit latency for the given PCI Express Link. Value depends upon the Link speed. 001b = Corresponding PEX 8624 Port L1 Link PM state Exit Latency is 1 s to less than 2 s at 5.0 GT/s 010b = Corresponding PEX 8624 Port L1 Link PM state Exit Latency is 2 s to less than 4 s at 2.5 GT/s All other encodings are ***reserved***.		RO	Yes	001b (5.0 GT/s) 010b (2.5 GT/s)
18	**Clock Power Management Capable**		RO	Yes	0
19	***Reserved*** Must be hardwired to 0, for the upstream Port and components that do not support this optional capability.	Upstream	RsvdP	No	0
	Surprise Down Error Reporting Capable Must be Set if the component supports the optional capability of detecting and reporting a Surprise Down error condition. If this bit is Cleared, the **Uncorrectable Error Status** register *Surprise Down Error Status* bit (offset FB8h[5]) is disabled. ***Note:*** *If this bit is Set and later Cleared at runtime (such as by I²C), it must be Cleared while the Link is up; otherwise, if the Link is down when this bit is Cleared, a subsequent Surprise Down error event is not masked.*	Downstream	RO	Yes	1

Register 12-28. 74h Link Capability (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	Data Link Layer Link Active Reporting Capable Valid for downstream Ports only.	Downstream	RO	Yes	1
21	***Reserved*** Hardwired to 0, as required by the *PCI Express Base r2.0*.	Upstream	RsvdP	No	0
	Link Bandwidth Notification Capability 1 = Indicates support for the Link Bandwidth Notification status and interrupt mechanisms	Downstream	RO	Yes	1
23:22	***Reserved***		RsvdP	No	00b
31:24	**Port Number** The Port Number is defined by input Strapping options. (Refer to Table 12-10.) Station 0, STRAP_STN0_PORTCFG1 – Ports 0, 1 Station 1, STRAP_STN1_PORTCFG0 – Ports 5, 6 Station 2, STRAP_STN2_PORTCFG1 – Ports 8, 9		ROS	No	Set by STRAP_STN*x*_PORTCFG*x* input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station x* bits (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[5:0])

Table 12-10. Port Configurations

Port Configuration Strapping STRAP_STN0_PORTCFG1, STRAP_RESERVED4	Port Configuration Register Value Port 0, Offset 574h[23:20, 1:0]	Station 0 Link Width/Port		
		Port 0	Port 1	–
0, 0	0h, 00b	x4	x4	
1, 0	0h, 10b	x8		
Port Configuration Strapping **STRAP_RESERVED7, STRAP_STN1_PORTCFG0**	**Port Configuration Register Value** **Port 0, Offset 574h[27:24, 3:2]**	**Station 1 Link Width/Port**		
		Port 4	**Port 5**	**Port 6**
1, 0	0h, 10b	***Software Only***	x8	
1, 1	0h, 11b	***Software Only***	x4	x4
Port Configuration Strapping **STRAP_STN2_PORTCFG1, STRAP_RESERVED8**	**Port Configuration Register Value** **Port 0, Offset 574h[31:28, 5:4]**	**Station 1 Link Width/Port**		
		Port 8	**Port 9**	**–**
0, 0	0h, 00b	x4	x4	
1, 0	0h, 10b	x8		

Register 12-29. 78h Link Status and Control (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
	Link Control				
1:0	**Active State Power Management (ASPM)** 00b = Disable[a] 01b = Enables only L0s Link PM state Entry 10b = Enables only L1 Link PM state Entry 11b = Enables both L0s and L1 Link PM state Entries		RW	Yes	00b
2	***Reserved***		RsvdP	No	0
3	**Read Request Return Parameter Control** Read Request Return Parameter "R" control. Read Completion Boundary (RCB). Cleared, as required by the *PCI Express Base r2.0.*		RO	Yes	0
4	***Not valid***	Upstream	RsvdP	No	0
	Link Disable 1 = Places the Link on the corresponding PEX 8624 downstream Port to the Disabled Link Training state	Downstream	RW	Yes	0
5	***Not valid*** Always read as 0.	Upstream	RsvdP	No	0
	Retrain Link For PEX 8624 Ports, always returns 0 when read; however, software is allowed to write this register. Writing 1 to this bit causes the corresponding PEX 8624 downstream Port to initiate retraining of its PCI Express Link.	Downstream	RZ	Yes	0
6	**Common Clock Configuration** 0 = Port and the device at the other end of the Port's PCI Express Link use an asynchronous Reference Clock source 1 = Port and the device at the other end of the Port's PCI Express Link use a common (synchronous) Reference Clock source (constant phase relationship)		RW	Yes	0
7	**Extended Sync** 1 = Causes the Port to transmit: • 4,096 FTS Ordered-Sets in the L0s Link PM state, • Followed by a single SKIP Ordered-Set prior to entering the L0 Link PM state, • Finally, transmission of 1,024 TS1 Ordered-Sets in the *Recovery* state.		RW	Yes	0

Register 12-29. 78h Link Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
8	**Clock Power Management Enable** ***Reserved*** Read and Writable only when the **Link Capability** register *Clock Power Management Capable* bit is Set. The PEX 8624 does ***not support*** removal of the Reference Clock in the L1 and L2/L3 Ready Link PM states.		RsvdP	No	0
9	**Hardware-Autonomous Width Disable** ***Reserved***		RsvdP	No	0
10	***Reserved***	Upstream	RsvdP	No	0
	Link Bandwidth Management Interrupt Enable 0 = Disables interrupt generation 1 = Enables generation of an interrupt, to indicate that the **Link Status** register *Link Bandwidth Management Status* bit (offset 78h[30]) has been Set	Downstream	RW	Yes	0
11	***Reserved***	Upstream	RsvdP	No	0
	Link Autonomous Bandwidth Interrupt Enable 0 = Disables interrupt generation 1 = Enables generation of an interrupt, to indicate that the **Link Status** register *Link Autonomous Bandwidth Status* bit (offset 78h[31]) has been Set	Downstream	RW	Yes	0
15:12	***Reserved***		RsvdP	No	0h
	Link Status				
19:16	**Current Link Speed** Indicates the negotiated Link speed of the Port's PCI Express Link. 0001b = 2.5 GT/s Link speed 0010b = 5.0 GT/s Link speed All other encodings are ***reserved***. The value in this field is undefined when the Link is not up.		RO	No	0001b
25:20	**Negotiated Link Width** Dependent upon the physical Port configuration. Link width is determined by the negotiated value with the attached Lane/Port. 00_0000b = Link is down (default) 00_0001b = x1 or Port is in the *DL_Down* state 00_0010b = x2 00_0100b = x4 00_1000b = x8 All other encodings are ***not supported***.		RO	No	00_0000b
26	***Reserved***		RsvdP	No	0
27	***Reserved***	Upstream	RsvdP	No	0
	Link Training 1 = Indicates that the corresponding PEX 8624 downstream Port requested Link training, and the Link training is in-progress or about to start	Downstream	RO	No	0

Register 12-29. 78h Link Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
28	**Slot Clock Configuration** 0 = Indicates that the PEX 8624 uses an independent clock 1 = Indicates that the PEX 8624 uses the same physical Reference Clock that the platform provides on the connector		HwInit	Yes	0
29	***Reserved***	Upstream	RsvdP	No	0
	Data Link Layer Link Active When Set, and the **Link Capability** register *Data Link Layer Link Active Reporting Capable* bit (offset 74h[20]) is also Set, indicates the following: • Data Link Layer (DLL) is in the *DL_Active* state • Link is operational • Flow Control (FC) Initialization has successfully completed	Downstream	RO	Yes	0
30	***Reserved***	Upstream	RsvdP	No	0
	Link Bandwidth Management Status Set by hardware to indicate that either of the following has occurred, without the Port transitioning through DL_Down status: • Link retraining has completed following a Write of 1 to the **Link Control** register *Retrain Link* bit (offset 78h[5]) • Hardware has changed Link speed or width, to attempt to correct unreliable Link operation, either through a Link Training and Status State Machine (LTSSM) timeout or higher-level process	Downstream	RW1C	Yes	0
31	***Reserved***	Upstream	RsvdP	No	0
	Link Autonomous Bandwidth Status Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation.	Downstream	RW1C	Yes	0

a. The Port Receiver must be capable of entering the L0s Link PM state, regardless of whether the state is disabled.

Register 12-30. 7Ch Slot Capability (Only Downstream Ports; Upstream Port Always Reads 0)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Notes: *For bits [6, 4:0], the default values are shown to be 1 for downstream Ports, which is true only if the Port is Parallel or Serial Hot Plug-capable; otherwise, the default value is 0. This also applies to bit 17 for Serial Hot Plug Ports. Serial Hot Plug-capable means that the PEX 8624 has detected that an I/O Expander is present.* *Stations 0, 1, and 2 each support one* ***Parallel*** *Hot Plug Controller, which uses the set of on-chip Hot Plug I/O signals designated with suffixes A, B, and C, respectively. The Transparent downstream Port to which the Hot Plug signals are assigned is designated in the HP Parallel Port field (Port 0, 4, or 8, offset 1E0h[14:13]). All other Transparent downstream Ports support a* ***Serial*** *Hot Plug Controller, which uses signals on an external I^2C I/O Expander, for Hot Plug signaling.*					
	Reserved	Upstream	RsvdP	No	0
0	**Attention Button Present** 0 = Attention Button is not implemented. 1 = Attention Button is implemented on the slot chassis of the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port. Set if the Port is Parallel or Serial Hot Plug-capable.	Downstream	RO	Yes	1
	Reserved	Upstream	RsvdP	No	0
1	**Power Controller Present** Enables or disables the Hot Plug Controller on the PEX 8624 Hot Plug-capable Transparent downstream Ports. Set if the Port is Parallel or Serial Hot Plug-capable. 0 = Power Controller is not implemented. The Hot Plug Controller is disabled for that slot and a power-up sequence is not executed. The slot remains in the disabled state. 1 = Power Controller is implemented for the slot of the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port. The Hot Plug Controller powers up the slot when the Manually operated Retention Latch (MRL) is closed and the **Slot Control** register *Power Controller Control* bit (offset 80h[10]) is Cleared. Otherwise, if bit 2 (*MRL Sensor Present*) is disabled (Cleared), the MRL's position has no effect on powering up the slot.	Downstream	RO	Yes	1

Register 12-30. 7Ch Slot Capability
(Only Downstream Ports; Upstream Port Always Reads 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
	Reserved	Upstream	RsvdP	No	0
2	**MRL Sensor Present** Set if the Port is Parallel or Serial Hot Plug-capable. 0 = MRL Sensor is not implemented. MRL position is "Don't Care" for that slot. 1 = MRL Sensor is implemented on the slot chassis of the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port. The PEX 8624 senses whether the MRL is open or closed for a slot. MRL should be Low for power-on for that slot.	Downstream	RO	Yes	1
	Reserved	Upstream	RsvdP	No	0
3	**Attention Indicator Present** Set if the Port is Parallel or Serial Hot Plug-capable. 0 = Attention Indicator is not implemented. HP_ATNLED_*x*# output is not functional on the slot. 1 = Attention Indicator is implemented on the slot chassis of the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port. Controls whether the HP_ATNLED_*x*# output for the slot drives out Active-Low.	Downstream	RO	Yes	1
	Reserved	Upstream	RsvdP	No	0
4	**Power Indicator Present** Set if the Port is Parallel or Serial Hot Plug-capable. 0 = Power Indicator is not implemented. HP_PWRLED_*x*# output is not functional on the slot. 1 = Power Indicator is implemented on the slot chassis of the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port. Controls whether the HP_PWRLED_*x*# output for the slot drives out Active-Low.	Downstream	RO	Yes	1
	Reserved	Upstream	RsvdP	No	0
5	**Hot Plug Surprise** 0 = No device in the corresponding PEX 8624 downstream Port slot is removed from the system without prior notification 1 = Device in the corresponding PEX 8624 downstream Port slot can be removed from the system without prior notification	Downstream	RO	Yes	0

Register 12-30. 7Ch Slot Capability
(Only Downstream Ports; Upstream Port Always Reads 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
6	***Reserved***	Upstream	RsvdP	No	0
	Hot Plug Capable 0 = Corresponding PEX 8624 downstream Port slot is not capable of supporting Hot Plug operations. 1 = Corresponding PEX 8624 downstream Port slot is capable of supporting Hot Plug operations. Set if the Port is Parallel or Serial Hot Plug-capable.	Downstream	RO	Yes	1
14:7	***Reserved***	Upstream	RsvdP	No	00h
	Slot Power Limit Value The maximum power supplied by the corresponding PEX 8624 downstream slot is determined by multiplying the value in this field (expressed in decimal; 25d = 19h) by the *Slot Power Limit Scale* field value. This field must be implemented if the **PCI Express Capability** register *Slot Implemented* bit (offset 68h[24]) is Set (default). Serial EEPROM and/or I²C Writes to this register or a DLL Up event causes the downstream Port to send the Set_Slot_Power_Limit Message to the device connected to it, so as to convey the Limit value to the downstream device's upstream Port **Device Capability** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields.	Downstream	RO	Yes	19h
16:15	***Reserved***	Upstream	RsvdP	No	00b
	Slot Power Limit Scale The maximum power supplied by the corresponding PEX 8624 downstream slot is determined by multiplying the value in this field by the *Slot Power Limit Value* field value. This field must be implemented if the **PCI Express Capability** register *Slot Implemented* bit (offset 68h[24]) is Set (default). Serial EEPROM and/or I²C Writes to this register or a DLL Up event causes the downstream Port to send the Set_Slot_Power_Limit Message to the device connected to it, so as to convey the Limit value to the downstream device's upstream Port **Device Capability** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	Downstream	RO	Yes	00b

Register 12-30. 7Ch Slot Capability
(Only Downstream Ports; Upstream Port Always Reads 0) *(Cont.)*

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Ports</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td></td><td>Reserved</td><td>Upstream; Downstream non-Serial Hot Plug-enabled</td><td>RsvdZ</td><td>No</td><td>0</td></tr>
<tr><td>17</td><td>Electromechanical Interlock Present
This bit is valid for Serial Hot Plug Ports that have an I/O Expander; this bit is not valid for Parallel Hot Plug Ports.
0 = Electromechanical Interlock is not implemented on the chassis for this slot
1 = Electromechanical Interlock is implemented on the chassis for this slot</td><td>Downstream Serial Hot Plug-enabled</td><td>RO</td><td>Yes</td><td>1</td></tr>
<tr><td>18</td><td>No Command Completed Support
Reserved</td><td></td><td>RsvdP</td><td>No</td><td>0</td></tr>
<tr><td rowspan="6">31:19</td><td>Reserved</td><td>Upstream</td><td>RsvdP</td><td>No</td><td>0-0h</td></tr>
<tr><td rowspan="5">Physical Slot Number
Indicates the physical Slot Number attached to this Port.
If the PCI Express Capability register Slot Implemented bit (offset 68h[24]) is Set (default), this field must be hardware-initialized to a value that assigns a Slot Number that is unique within the chassis, regardless of the form factor associated with the slot. Must be initialized to 0h for Ports connected to devices that are integrated on the system board. Bit usage depends upon whether the Port is Serial Hot Plug-capable.
Serial Hot Plug-Capable Downstream Ports
Bit(s) — Description/Function
22:19 — Port Numbers 0, 1, 5, 6, 8, and 9
26:23 — Loaded from I/O Expander
31:27 — Reserved
Non-Serial Hot Plug-Capable Downstream Ports
Bit(s) — Description/Function
22:19 — Port Numbers 0, 1, 5, 6, 8, and 9
25:23 — Value of I2C_ADDR[2:0] (same as the lower three bits of the I2C Configuration register Slave Address field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 294h[2:0]))
31:26 — Reserved</td><td>Downstream</td><td>RO</td><td>Yes</td><td>0-0h</td></tr>
</table>

Register 12-31. 80h Slot Status and Control (Only Downstream Ports; Upstream Port Always Reads 0)

Bit(s)	Description		Ports	Type	Serial EEPROM and I²C	Default
Slot Control						
Note: *To change the values of the MRL Sensor Changed Enable (bit 2), Power Fault Detector Enable (bit 1), and/or Attention Button Pressed Enable (bit 0) bits, the corresponding bit(s) in the* ***Slot Capability*** *register (offset 7Ch[2:0], respectively) must be Set first.*						
0	***Reserved***		Upstream	RsvdP	No	0
	Attention Button Pressed Enable 0 = Function is disabled 1 = Enables software notification with an interrupt if the Port is in the D0 Device PM state (**PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], is Cleared), or with a PME Message if the Port is in the D3hot Device PM state (offset 44h[1:0], are both Set), for an Attention Button Pressed event on the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port	Offset 7Ch[0]=0	Downstream	RO	No	0
		Offset 7Ch[0]=1	Downstream	RW	Yes	0
1	***Reserved***		Upstream	RsvdP	No	0
	Power Fault Detector Enable 0 = Function is disabled 1 = Enables software notification with an interrupt if the Port is in the D0 Device PM state (**PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], is Cleared), or with a PME Message if the Port is in the D3hot Device PM state (offset 44h[1:0], are both Set), for a Power Fault Detected event on the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port	Offset 7Ch[1]=0	Downstream	RO	No	0
		Offset 7Ch[1]=1	Downstream	RW	Yes	0

Register 12-31. 80h Slot Status and Control
(Only Downstream Ports; Upstream Port Always Reads 0) *(Cont.)*

Bit(s)	Description		Ports	Type	Serial EEPROM and I²C	Default
2	***Reserved***		Upstream	RsvdP	No	0
	MRL Sensor Changed Enable 0 = Function is disabled 1 = Enables software notification with an interrupt if the Port is in the D0 Device PM state (**PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], is Cleared), or with a PME Message if the Port is in the D3hot Device PM state (offset 44h[1:0], are both Set), for an MRL Sensor Changed event on the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port	Offset 7Ch[2]=0	Downstream	RO	No	0
		Offset 7Ch[2]=1	Downstream	RW	Yes	0
3	***Not valid***		Upstream	RsvdP	No	0
	Presence Detect Changed Enable A Presence Detect Changed event is triggered by either the SerDes Receiver Detect (**Physical Layer Receiver Detect Status** register *Receiver Detected on Lane x* bits (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 200h[31:16])) on the corresponding PEX 8624 downstream Port, or by HP_PRSNT_*x*# input or external I/O Expander PRSNT# input on the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port. 0 = Function is disabled 1 = Enables software notification with an interrupt if the Port is in the D0 Device PM state (**PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], is Cleared), or with a PME Message if the Port is in the D3hot Device PM state (offset 44h[1:0], are both Set), for a Presence Detect Changed event on the corresponding PEX 8624 downstream Port		Downstream	RW	Yes	0

Register 12-31. 80h Slot Status and Control
(Only Downstream Ports; Upstream Port Always Reads 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
4	***Reserved***	Upstream	RsvdP	No	0
	Command Completed Interrupt Enable 0 = Function is disabled 1 = Enables software notification with an interrupt when a command is completed by the Hot Plug Controller on the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port	Downstream	RW	Yes	0
5	***Reserved***	Upstream	RsvdP	No	0
	Hot Plug Interrupt Enable 0 = Function is disabled 1 = Enables an interrupt on enabled Hot Plug/Link State events for the corresponding PEX 8624 downstream Port	Downstream	RW	Yes	0
7:6	***Reserved***	Upstream	RsvdP	No	00b
	Attention Indicator Control Controls the Attention Indicator on the corresponding PEX 8624 downstream Port slot. Reads return the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port Attention Indicator's current state. Writing a non-zero value triggers a Command Completed event (even if the value written is the same as the existing value). Writing 00b preserves the current value and does not trigger a Command Completed event. 00b = ***Reserved*** – Writes are ignored 01b = Turns On indicator to constant On state 10b = Causes indicator to blink 11b = Turns Off indicator	Downstream	RW	Yes	11b

Register 12-31. 80h Slot Status and Control (Only Downstream Ports; Upstream Port Always Reads 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
9:8	***Reserved***	Upstream	RsvdP	No	00b
	Power Indicator Control Controls the Power Indicator on the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port slot. Reads return the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port Power Indicator's current state. Writing a non-zero value triggers a Command Completed event (even if the value written is the same as the existing value). Writing 00b preserves the current value and does not trigger a Command Completed event. 00b = ***Reserved*** – Writes are ignored 01b = Turns On indicator to constant On state 10b = Causes indicator to blink 11b = Turns Off indicator	Downstream	RW	Yes	11b (MRL open) 01b (MRL closed)
10	***Reserved***	Upstream	RsvdP	No	0
	Power Controller Control Controls the Power Controller on the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port slot. 0 = Turns On the Power Controller; requires some delay to be effective 1 = Turns Off the Power Controller	Downstream	RW	Yes	1 (MRL open) 0 (MRL closed)
11	***Reserved***	Upstream; Downstream non-Serial Hot Plug-enabled	RsvdP	No	0
	Electromechanical Interlock Control This bit is valid for Serial Hot Plug Ports that have an I/O Expander; this bit is ***not*** valid for Parallel Hot Plug Ports. If an Electromechanical Interlock is implemented, writing 1 to this bit causes the state of the interlock to toggle. A Write of 0 to this bit has no effect. A Read of this bit always returns 0.	Downstream Serial Hot Plug-enabled	RW	Yes	0
12	***Not valid***	Upstream	RsvdP	No	0
	Data Link Layer State Changed Enable Enables software notification with an interrupt if the Port is in the D0 Device PM state (**PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], is Cleared), or with a PME Message if the Port is in the D3hot Device PM state (offset 44h[1:0], are both Set), when the **Link Status** register *Data Link Layer Link Active* bit (offset 78h[29]) is changed.	Downstream	RW	Yes	0
15:13	***Reserved***		RsvdP	No	000b

Register 12-31. 80h Slot Status and Control (Only Downstream Ports; Upstream Port Always Reads 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Slot Status					
16	***Reserved***	Upstream	RsvdP	No	0
	Attention Button Pressed 1 = Attention Button of the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port slot was pressed	Downstream	RW1C	Yes	0
17	***Reserved***	Upstream	RsvdP	No	0
	Power Fault Detected 1 = Power Controller of the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port slot detected a Power Fault at the slot	Downstream	RW1C	Yes	0
18	***Reserved***	Upstream	RsvdP	No	0
	MRL Sensor Changed 1 = MRL Sensor state change was detected on the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port slot	Downstream	RW1C	Yes	0
19	***Reserved***	Upstream	RsvdP	No	0
	Presence Detect Changed A Presence Detect Changed event is triggered by either the SerDes Receiver Detect on the corresponding PEX 8624 downstream Port (**Physical Layer Receiver Detect Status** register *Receiver Detected on Lane x* bits (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 200h[31:16])), or by HP_PRSNT_*x*# or PRSNT# input (from external I^2C I/O Expander) on the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port. Write 1 to Clear. 1 = Value reported in bit 22 (*Presence Detect State*) changed	Downstream	RW1C	Yes	0

Register 12-31. 80h Slot Status and Control (Only Downstream Ports; Upstream Port Always Reads 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	Command Completed 1 = Hot Plug Controller on the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port slot completed an issued command to: • *Attention Indicator Control* (field [7:6]) • *Power Indicator Control* (field [9:8]) • *Power Controller Control* (bit 10) • *Electromechanical Interlock Control* (bit 11) (Serial Hot Plug-enabled Ports only)	Downstream	RW1C	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	MRL Sensor State Reveals the corresponding PEX 8624 Hot Plug-capable Transparent downstream Port MRL Sensor's current state. 0 = MRL Sensor is closed 1 = MRL Sensor is open	Downstream	RO	No	0
22	***Not valid***	Upstream	RsvdP	No	0
	Presence Detect State For downstream Ports that implement slots, indicates the presence of an adapter in the slot, reflected by the logical OR of the corresponding downstream Port's SerDes Receiver Detect, and, if present, the Port's HP_PRSNT_*x*# input (de-bounced) or the PRSNT# input on the external I/O Expander for the Serial Hot Plug-enabled Port. Hardwired to 1 when the **PCI Express Capability** register *Slot Implemented* bit (offset 68h[24]) value is 0. 0 = Slot is empty, or device is not present 1 = Slot is occupied, or device is present	Downstream, Offset 68h[24]=1	RO	No	0
		Downstream, Offset 68h[24]=0	RO	No	1
23	***Reserved***	Upstream; Downstream non-Serial Hot Plug-enabled	RsvdP	No	0
	Electromechanical Interlock Status This bit is valid for Serial Hot Plug Ports that have an I/O Expander; this bit is ***not*** valid for Parallel Hot Plug Ports. When an Electromechanical Interlock is implemented, indicates the Electromechanical Interlock's current status. 0 = Electromechanical Interlock is disengaged 1 = Electromechanical Interlock is engaged	Downstream Serial Hot Plug-enabled	RW1C	Yes	0

Register 12-31. 80h Slot Status and Control (Only Downstream Ports; Upstream Port Always Reads 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
24	***Not valid***	Upstream	RsvdP	No	0
	Data Link Layer State Changed In response to a Data Link Layer State Changed event, software must read the **Link Status** register *Data Link Layer Link Active* bit (offset 78h[29]), to determine whether the Link is active before initiating Configuration Requests to the device. 1 = Value reported in the **Link Status** register *Data Link Layer Link Active* bit changed	Downstream	RW1C	Yes	0
31:25	***Reserved***		RsvdZ	No	0-0h

Register 12-32. 8Ch Device Capability 2 (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
4:0	***Reserved***		RsvdP	No	0-0h
5	***Reserved***	Upstream	RsvdP	No	0
	ARI Forwarding Supported 0 = Alternative Routing-ID Interpretation (ARI) forwarding is not supported 1 = ARI forwarding is supported	Downstream	RO	Yes	1
31:6	***Reserved***		RsvdP	No	0-0h

Register 12-33. 90h Device Status and Control 2 (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Device Control 2					
4:0	***Reserved***		RsvdP	No	0-0h
5	***Reserved***	Upstream	RsvdP	No	0
	ARI Forwarding Enable 0 = Disabled 1 = Enabled; Downstream Port disables its traditional Device Number field from being forced to 0 when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to extended functions in an ARI device immediately below the Port	Downstream	RW	Yes	0
15:6	***Reserved***		RsvdP	No	0-0h
Device Status 2					
31:16	***Reserved***		RsvdP	No	0000h

Register 12-34. 98h Link Status and Control 2 (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Link Control 2					
3:0	**Target Link Speed** 0001b = 2.5 GT/s Link speed supported 0010b = 5.0 GT/s Link speed supported All other encodings are ***reserved***.		RWS	Yes	0010b
4	**Enter Compliance**		RWS	Yes	0
5	**Hardware Autonomous Speed Disable** ***Reserved*** Initial transition to the highest supported common Link speed is not blocked by this bit.		RsvdP	No	0
6	***Not valid***	Upstream	RsvdP	Yes	0
	Selectable De-Emphasis Selects the standard de-emphasis level when the Link is operating at 5.0 GT/s. When the Link is operating at 2.5 GT/s, the Setting of this bit has no effect (de-emphasis at 2.5 GT/s is -3.5 dB). 0 = -6 dB 1 = -3.5 dB	Downstream	HwInit	Yes	0 (5.0 GT/s) 1 (2.5 GT/s)
9:7	**Transmit Margin** Intended for debug and compliance testing only.		RWS	Yes	000b
10	**Enter Modified Compliance** Intended for debug and compliance testing only.		RWS	Yes	0
11	**Compliance SOS** 1 = LTSSM must periodically send SKIP Ordered-Sets between sequences when sending the Compliance Pattern or Modified Compliance Pattern		RWS	Yes	0
12	**Compliance De-Emphasis** Sets the de-emphasis level in the *Polling.Compliance* state, if the entry occurred due to bit 4 (*Enter Compliance*) being Set.		RWS	Yes	0
15:13	***Reserved***		RsvdP	No	000b
Link Status 2					
16	**Current De-Emphasis Level** Reflects the de-emphasis level. 0 = -6 dB (Link is operating at 5.0 GT/s) 1 = -3.5 dB		RO	Yes	0 (5.0 GT/s) 1 (2.5 GT/s)
31:17	***Reserved***		RsvdP	No	0-0h

12.10 Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)

This section details the Subsystem ID and Subsystem Vendor ID Capability registers. Table 12-11 defines the register map.

Table 12-11. Subsystem ID and Subsystem Vendor ID Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved	Next Capability Pointer (00h) / SSID/SSVID Capability ID (0Dh)	A4h
Subsystem ID	Subsystem Vendor ID	A8h
Reserved		ACh – FCh

Register 12-35. A4h Subsystem Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**SSID/SSVID Capability ID** SSID/SSVID registers for the PCI-to-PCI bridge. Program to 0Dh, as required by the *PCI-to-PCI Bridge r1.2*.	RO	Yes	0Dh
15:8	**Next Capability Pointer** 00h = This capability is the last capability in the PEX 8624 Port's Capabilities list The PEX 8624 Port Extended Capabilities list starts at offset 100h.	RO	Yes	00h
31:16	***Reserved***	RsvdP	No	0000h

Register 12-36. A8h Subsystem ID and Subsystem Vendor ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**Subsystem Vendor ID** The Vendor ID (offset 00h[15:0]) identifies the manufacturer of the PEX 8624, and the Subsystem Vendor ID optionally identifies the board or system vendor. As with the Vendor ID value, the Subsystem Vendor ID value must be a valid PCI-SIG-assigned Vendor ID.	RO	Yes	10B5h
31:16	**Subsystem ID** The Device ID (offset 00h[31:16]) identifies the PEX 8624, and optionally the Subsystem ID in combination with the Subsystem Vendor ID, uniquely identifies the board or system. The *Subsystem ID* value is chosen or assigned only by the "owner" of the valid Vendor ID value used for the Subsystem Vendor ID. If the board or system vendor is not a PCI-SIG member, PLX can assign, free of charge, a unique *Subsystem ID* value, in which case the Subsystem Vendor ID remains the PLX default value, 10B5h. The *Subsystem Vendor ID* and *Subsystem ID* values are usually identical for all PEX 8624 Ports.	RO	Yes	8624h

12.11 Device Serial Number Extended Capability Registers (Offsets 100h – 134h)

This section details the Device Serial Number Extended Capability registers. Table 12-12 defines the register map.

Table 12-12. Device Serial Number Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (FB4h)	Capability Version (1h)	PCI Express Extended Capability ID (0003h)	100h
Serial Number (Lower DW)		104h
Serial Number (Upper DW)		108h
Reserved	10Ch –	134h

Register 12-37. 100h Device Serial Number Extended Capability Header (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**PCI Express Extended Capability ID** Programmed to 0003h, as required by the *PCI Express Base r2.0*.	RO	Yes	0003h
19:16	**Capability Version** Programmed to 1h, as required by the *PCI Express Base r2.0*.	RO	Yes	1h
31:20	**Next Capability Offset** Programmed to FB4h, which addresses the **Advanced Error Reporting Extended Capability** structure.	RO	Yes	FB4h

Register 12-38. 104h Serial Number (Lower DW) (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**PCI Express Device Serial Number (1st DW)** Lower half of a 64-bit register. Value programmed by Serial EEPROM register initialization. Per the *PCI Express Base r2.0*, all switch Ports must contain the same value; therefore, one physical register is shared by all PEX 8624 Ports. (Refer to Table 12-2.) The Serial Number registers contain the IEEE-defined 64-bit Extended Unique Identifier (EUI-64™). The lower 24 bits are the Company ID value assigned by the IEEE registration authority, and the upper 40 bits are the Extension ID assigned by the identified Company.	RO	Yes	B5DF_0E00h

Register 12-39. 108h Serial Number (Upper DW) (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**PCI Express Device Serial Number (2nd DW)** Upper half of a 64-bit register. Value programmed by Serial EEPROM register initialization. Per the *PCI Express Base r2.0*, all switch Ports must contain the same value; therefore, one physical register is shared by all PEX 8624 Ports. (Refer to Table 12-2.) The Serial Number registers contain the IEEE-defined 64-bit Extended Unique Identifier (EUI-64™). The lower 24 bits are the Company ID value assigned by the IEEE registration authority, and the upper 40 bits are the Extension ID assigned by the identified Company.	RO	Yes	AA_8600_10h

12.12 Power Budget Extended Capability Registers (Offsets 138h – 144h)

This section details the Power Budget Extended Capability registers. These registers work differently than the others, especially with respect to serial EEPROM Reads and Writes. *For example*, when writing to Index 5 of the upstream Port/NT Port Link Interface **Power Budget Data** register (offset 140h), write 5 into the upstream Port/NT Port Link Interface **Data Select** register *Data Select* field (offset 13Ch[7:0]), then write the value into the upstream Port/NT Port Link Interface **Power Budget Data** register. Table 12-13 defines the register map.

Table 12-13. Power Budget Extended Capability Register Map (Only Upstream Port, and also NT Port Link Interface; *Reserved* (RsvdP) for All Other Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (148h) / Capability Version (1h)	PCI Express Extended Capability ID (0004h)	138h
Reserved	Data Select	13Ch
Power Budget Data		140h
Power Budget Capability		144h

Register 12-40. 138h Power Budget Extended Capability Header (Only Upstream Port, and also NT Port Link Interface; *Reserved* (RsvdP) for All Other Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
15:0	**PCI Express Extended Capability ID** Programmed to 0004h, as required by the *PCI Express Base r2.0.*	Upstream	RO	Yes	0004h
	Reserved	Downstream	RsvdP	No	0000h
19:16	**Capability Version** Programmed to 1h, as required by the *PCI Express Base r2.0.*	Upstream	RO	Yes	1h
	Reserved	Downstream	RsvdP	No	0h
31:20	**Next Capability Offset** Programmed to 148h, which addresses the **Virtual Channel Extended Capability** structure.	Upstream	RO	Yes	148h
	Reserved	Downstream	RsvdP	No	000h

Register 12-41. 13Ch Data Select (Only Upstream Port, and also NT Port Link Interface; *Reserved* (RsvdP) for All Other Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
7:0	**Data Select** Indexes the Power Budget data reported, by way of eight upstream Port/NT Port Link Interface **Power Budget Data** registers, per Port, and selects the DWord of Power Budget data that appears in each **Power Budget Data** register. Index values start at 0, to select the first DWord of Power Budget data; subsequent DWords of Power Budget data are selected by increasing index values 1 to 7.	Upstream	RW	Yes	00h
	Reserved	Downstream	RsvdP	No	00h
31:8	***Reserved***		RsvdP	No	0-0h

Register 12-42. 140h Power Budget Data (Only Upstream Port, and also NT Port Link Interface; *Reserved* (RsvdP) for All Other Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Note: *Eight registers, per upstream Port/NT Port Link Interface, can be programmed, through the serial EEPROM or I²C. Each non-zero register value describes the power usage for a different operating condition. Each configuration is selected by writing to the **Data Select** register Data Select field (Upstream Port/NT Port Link Interface, offset 13Ch[7:0]).*					
7:0	**Base Power** Eight registers per upstream Port/NT Port Link Interface. Specifies (in Watts) the base power value in the operating condition. This value must be multiplied by the field [9:8] (*Data Scale*) contents, to produce the actual power consumption value.	Upstream	RO	Yes	00h
	Reserved	Downstream	RsvdP	No	00h
9:8	**Data Scale** Specifies the scale to apply to the Base Power value. The device power consumption is determined by multiplying the field [7:0] (*Base Power*) contents with the value corresponding to the encoding returned by this field. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	Upstream	RO	Yes	00b
	Reserved	Downstream	RsvdP	No	00b
12:10	**PM Sub-State** 000b = Power Management sub-state of the operating condition being described	Upstream	RO	Yes	000b
	Reserved	Downstream	RsvdP	No	000b

Register 12-42. 140h Power Budget Data (Only Upstream Port, and also NT Port Link Interface; *Reserved* (RsvdP) for All Other Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
14:13	**PM State** Power Management state of the operating condition being described. 00b = D0 Device PM state 11b = D3 Device PM state All other encodings are ***reserved***.	Upstream	RO	Yes	00b
	Reserved	Downstream	RsvdP	No	00b
17:15	**Type** Type of operating condition being described. 000b = PME Auxiliary 001b = Auxiliary 010b = Idle 011b = Sustained 111b = Maximum All other encodings are ***reserved***.	Upstream	RO	Yes	000b
	Reserved	Downstream	RsvdP	No	000b
20:18	**Power Rail** Power Rail of the operating condition being described. 000b = Power 12V 001b = Power 3.3V 010b = Power 1.8V 111b = Thermal All other encodings are ***reserved***.	Upstream	RO	Yes	000b
	Reserved	Downstream	RsvdP	No	000b
31:21	***Reserved***		RsvdP	No	0-0h

Register 12-43. 144h Power Budget Capability (Only Upstream Port, and also NT Port Link Interface; *Reserved* (RsvdP) for All Other Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
0	**System Allocated** 1 = Power budget for the device is included within the system power budget	Upstream	HwInit	Yes	1
	Reserved	Downstream	RsvdP	No	0
31:1	***Reserved***		RsvdP	No	0-0h

12.13 Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)

This section details the Virtual Channel Extended Capability registers, which are duplicated for each Port. Table 12-14 defines the register map for one Port.

Table 12-14. Virtual Channel Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (448h, 950h, or 520h)	Capability Version (1h) / PCI Express Extended Capability ID (0002h)	148h
Port VC Capability 1		14Ch
Port VC Capability 2		150h
Port VC Status ***(Reserved)***	Port VC Control	154h
VC0 Resource Capability		158h
VC0 Resource Control		15Ch
VC0 Resource Status	***Reserved***	160h
Reserved		164h – 1A4h
Port Arbitration Table Registers (Offsets 1A8h – 1BCh)		1A8h … 1BCh

Register 12-44. 148h Virtual Channel Extended Capability Header (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
15:0	**PCI Express Extended Capability ID** Programmed to 0002h, as required by the *PCI Express Base r2.0*.		RO	No	0002h
19:16	**Capability Version** Programmed to 1h, as required by the *PCI Express Base r2.0*.		RO	No	1h
31:20	**Next Capability Offset** Next extended capability is the **Vendor-Specific Extended Capability** structure, offset 448h.	Port 0 is a Transparent Port	RO	No	448h
	Next extended capability is the **Vendor-Specific Extended Capability 2** structure, offset 950h.	Upstream, if not Port 0	RO	No	950h
	Next extended capability is the **ACS Extended Capability** structure, offset 520h.	Downstream, except Port 0	RO	No	520h

Register 12-45. 14Ch Port VC Capability 1 (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
0	**Extended VC Counter** 0 = PEX 8624 Port supports only one Virtual Channel, VC0 1 = ***Reserved***		RO	No	0
3:1	***Reserved***		RsvdP	No	000b
4	**Low-Priority Extended VC Counter** For Strict Priority arbitration, indicates the number of extended Virtual Channels (VCs) (those in addition to VC0) that belong to the Low-Priority VC group for this PEX 8624 Port. 0 = For this PEX 8624 Port, only VC0 belongs to the Low-Priority VC group 1 = ***Reserved***, because the PEX 8624 supports only one VC		RO	No	0
7:5	***Reserved***		RsvdP	No	000b
9:8	**Reference Clock** Cleared.		RsvdP	No	00b
11:10	**Port Arbitration Table Entry Size** 00b = Port Arbitration Table entry size is 1 bit 10b = Port Arbitration Table entry size is 4 bits ***Note:*** *This field is valid only on upstream Port 0, and* ***reserved*** *on all other Ports.*	Upstream Port 0 (refer to Note)	RO	Yes	10b
	Reserved	All other Ports	RsvdP	No	00b
31:12	***Reserved***		RsvdP	No	0000_0h

Register 12-46. 150h Port VC Capability 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**VC Arbitration Capability** 0 = Indicates that the Round-Robin (Hardware-Fixed) Arbitration scheme is not supported 1 = ***Reserved***, because the PEX 8624 supports only one VC (**Port VC Capability 2** register *Low-Priority Extended VC Counter* bit, offset 14Ch[4], is Cleared)	RO	No	0
31:1	***Reserved***	RsvdP	No	0-0h

Register 12-47. 154h Port VC Status and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Port VC Control				
0	**Load VC Arbitration Table** Writing 1 updates the VC Arbitration Table for the corresponding PEX 8624 Port. Reads always return 0.	RsvdP	No	0
3:1	**VC Arbitration Select** Selects the VC arbitration type for the corresponding PEX 8624 Port, as per the supported arbitration type indicated by the **Port VC Capability 2** register *VC Arbitration Capability* field (offset 150h[0]) value. 000b = Bit 0; Round-Robin (Hardware-Fixed) arbitration scheme All other encodings are ***reserved***.	RW	Yes	000b
15:4	***Reserved***	RsvdP	No	000h
Port VC Status				
16	**VC Arbitration Table Status** ***Reserved***	RsvdP	No	0
31:17	***Reserved***	RsvdP	No	0-0h

Register 12-48. 158h VC0 Resource Capability (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
1:0	**Port Arbitration Capability** Bit 0 = 1 – Non-configurable Round-Robin (Hardware-Fixed) arbitration Bit 1 = 1 – Weighted Round-Robin (WRR) arbitration with 32 Phases ***Note:*** *This field's value is 10b for upstream Port 0, and 01b for all other Ports.*	Upstream Port 0 (refer to Note)	RO	No	10b
		All other Ports	RO	No	01b
14:2	***Reserved***		RsvdP	No	0-0h
15	**Reject Snoop Transactions** Not a PCI Express switch feature; therefore, Cleared.		RsvdP	No	0
22:16	**Maximum Time Slots** Cleared.		RsvdP	No	000_0000b
23	***Reserved***		RsvdP	No	0
31:24	**Port Arbitration Table Offset** Offset of the Port Arbitration Table, as the number of DQWords from the Base address of the **Virtual Channel Extended Capability** structure. (Refer to Section 12.13.1 for further details.) 00h = Port Arbitration Table is not present 06h = Port Arbitration Table is located at register offset 1A8h (148h + 6 x 4 DWords) ***Note:*** *This field is valid only on upstream Port 0, and **reserved** on all other Ports.*	Upstream Port 0 (refer to Note)	RO	No	06h
	Reserved	All other Ports	RsvdP	No	00h

Register 12-49. 15Ch VC0 Resource Control (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
0	**TC/VC Map** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped to VC0. Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.		RO	No	1
7:1			RW	Yes	7Fh
15:8	***Reserved***		RsvdP	No	00h
16	**Load Port Arbitration Table** Software writes this bit, to load the updated WRR Port Arbitration Table value to the internal logic. Software Read always returns 0.		RW	Yes	0
19:17	**Port Arbitration Select** Selects the Port Arbitration type for the corresponding PEX 8624 Port. Indicates the bit number in the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[1:0]) that corresponds to the arbitration type. 0 = Round-Robin (Hardware-Fixed) arbitration scheme 1 = Weighted Round-Robin with 32 Phases ***Note:*** *This field's value is 001b for upstream Port 0, and 000b for all other Ports.*	Upstream Port 0 (refer to Note)	RW	Yes	001b
		All other Ports	RW	Yes	000b
23:20	***Reserved***		RsvdP	No	0h
24	**VC ID** Defines the corresponding PEX 8624 Port VC0 ID code. Cleared, because VC0 is the only/default VC.		RO	No	0
30:25	***Reserved***		RsvdP	No	0-0h
31	**VC Enable** 0 = Not allowed 1 = Enables the corresponding PEX 8624 Port VC0		RO	No	1

Register 12-50. 160h VC0 Resource Status (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
15:0	***Reserved***		RsvdP	No	0000h
16	**Port Arbitration Table Status** 0 = Hardware has finished loading values stored in the Port Arbitration Table, after software Sets the **VC0 Resource Control** register *Load Port Arbitration Table* bit (offset 15Ch[16]) 1 = Port Arbitration Table entry was written to by software ***Note:*** *This bit is valid only on Port 0, and* ***reserved*** *on all other Ports.*	Upstream Port 0 (refer to Note)	RO	No	0
	Reserved	All other Ports	RsvdP	No	0
17	**VC0 Negotiation Pending** 0 = Port's VC0 negotiation is complete 1 = Port's VC0 initialization is not complete		RO	Yes	1
31:18	***Reserved***		RsvdP	No	0-0h

12.13.1 Port Arbitration Table Registers (Offsets 1A8h – 1BCh)

This section details the Port Arbitration Table registers. Port Arbitration Table phases are used to determine Port weighting during "Weighted Round-Robin with 32 Phases" Port arbitration.

These registers are implemented as follows. If Port 0 is the NT Port, the NT Port Virtual Interface implements this register. Otherwise, Port 0 implements this register.

Table 12-15 defines the register map. The numbers along the top of the register map table indicate the 4-bit fields of each 32-bit register. There are 32 phases.

Note: ***The Port Arbitration Table is used only when Weighted Round-Robin with 32-phase Port Arbitration is selected, by way of the VC0 Resource Control register Port Arbitration Select field (offset 15Ch[19:17]=001b).***

Table 12-15. Port Arbitration Table Register Map (Only Upstream Port 0, or NT Port Virtual Interface (if Port 0 is the NT Port); *Reserved* (RsvdP) for All Other Ports)

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	
Phase 7	Phase 6	Phase 5	Phase 4	Phase 3	Phase 2	Phase 1	Phase 0	1A8h
Phase 15	Phase 14	Phase 13	Phase 12	Phase 11	Phase 10	Phase 9	Phase 8	1ACh
Phase 23	Phase 22	Phase 21	Phase 20	Phase 19	Phase 18	Phase 17	Phase 16	1B0h
Phase 31	Phase 30	Phase 29	Phase 28	Phase 27	Phase 26	Phase 25	Phase 24	1B4h
Reserved							1B8h –	1BCh

Register 12-51. 1A8h Port Arbitration Table Phases 0 to 7 (Only Upstream Port 0, or NT Port Virtual Interface (if Port 0 is the NT Port); *Reserved* (RsvdP) for All Other Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Note: *If Port 0 is the NT Port, the NT Port Virtual Interface implements this register. Otherwise, Port 0 implements this register.*					
3:0	**Port Arbitration Table Phase 0**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
7:4	**Port Arbitration Table Phase 1**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
11:8	**Port Arbitration Table Phase 2**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
15:12	**Port Arbitration Table Phase 3**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
19:16	**Port Arbitration Table Phase 4**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
23:20	**Port Arbitration Table Phase 5**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
27:24	**Port Arbitration Table Phase 6**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
31:28	**Port Arbitration Table Phase 7**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h

Register 12-52. 1ACh Port Arbitration Table Phases 8 to 15 (Only Upstream Port 0, or NT Port Virtual Interface (if Port 0 is the NT Port); *Reserved* (RsvdP) for All Other Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Note: *If Port 0 is the NT Port, the NT Port Virtual Interface implements this register. Otherwise, Port 0 implements this register.*					
3:0	**Port Arbitration Table Phase 8**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
7:4	**Port Arbitration Table Phase 9**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
11:8	**Port Arbitration Table Phase 10**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
15:12	**Port Arbitration Table Phase 11**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
19:16	**Port Arbitration Table Phase 12**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
23:20	**Port Arbitration Table Phase 13**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
27:24	**Port Arbitration Table Phase 14**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
31:28	**Port Arbitration Table Phase 15**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h

Register 12-53. 1B0h Port Arbitration Table Phases 16 to 23 (Only Upstream Port 0, or NT Port Virtual Interface (if Port 0 is the NT Port); *Reserved* (RsvdP) for All Other Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Note: *If Port 0 is the NT Port, the NT Port Virtual Interface implements this register. Otherwise, Port 0 implements this register.*					
3:0	**Port Arbitration Table Phase 16**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
7:4	**Port Arbitration Table Phase 17**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
11:8	**Port Arbitration Table Phase 18**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
15:12	**Port Arbitration Table Phase 19**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
19:16	**Port Arbitration Table Phase 20**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
23:20	**Port Arbitration Table Phase 21**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
27:24	**Port Arbitration Table Phase 22**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
31:28	**Port Arbitration Table Phase 23**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h

Register 12-54. 1B4h Port Arbitration Table Phases 24 to 31 (Only Upstream Port 0, or NT Port Virtual Interface (if Port 0 is the NT Port); *Reserved* (RsvdP) for All Other Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Note: *If Port 0 is the NT Port, the NT Port Virtual Interface implements this register. Otherwise, Port 0 implements this register.*					
3:0	**Port Arbitration Table Phase 24**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
7:4	**Port Arbitration Table Phase 25**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
11:8	**Port Arbitration Table Phase 26**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
15:12	**Port Arbitration Table Phase 27**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
19:16	**Port Arbitration Table Phase 28**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
23:20	**Port Arbitration Table Phase 29**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
27:24	**Port Arbitration Table Phase 30**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
31:28	**Port Arbitration Table Phase 31**	Upstream Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h

12.14 Device-Specific Registers (Offsets 1C0h – 51Ch)

This section details the Device-Specific registers located at offsets 1C0h through 51Ch. Device-Specific registers are unique to the PEX 8624 and not referenced in the *PCI Express Base r2.0*. Table 12-16 defines the register map.

Other Device-Specific registers are detailed in Section 12.16, "Device-Specific Registers (Offsets 54Ch – F8Ch)."

Note: It is recommended that these registers not be changed from their default values.

Table 12-16. Device-Specific Register Map (Offsets 1C0h – 51Ch)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)		1C0h … 1FCh
Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)		200h … 25Ch
Device-Specific Registers – Serial EEPROM (Offsets 260h – 26Ch)		260h … 26Ch
Device-Specific Registers – Physical Layer (Offsets 270h – 28Ch)		270h … 28Ch
Device-Specific Registers – I2C Slave Interface (Offsets 290h – 2C4h)		290h … 2C4h
Device-Specific Registers – Bus Number CAM (Offsets 2C8h – 304h)		2C8h … 304h
Device-Specific Registers – I/O CAM (Offsets 308h – 344h)		308h … 344h
Device-Specific Registers – Address-Mapping CAM (Offsets 348h – 444h)		348h … 444h
Next Capability Offset (950h or 520h)	1h	PCI Express Extended Capability ID (000Bh)	448h
Device-Specific Registers – Vendor-Specific Dual Cast Extended Capability (Offsets 448h – 51Ch)		… 51Ch

12.14.1 Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)

This section details the Device-Specific Error Checking and Debug registers. Table 12-17 defines the register map.

Table 12-17. Device-Specific Error Checking and Debug Register Map (Ports[a])

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device-Specific Error Status for Egress ECC Error				1C0h
Device-Specific Error Mask for Egress ECC Error				1C4h
ECC Error Check Disable				1C8h
Error Handler 32-Bit Error Status				1CCh
Error Handler 32-Bit Error Mask				1D0h
Factory Test Only				1D4h
Clock Enable				1D8h
Debug Control		***Factory Test Only/Reserved***		1DCh
Power Management Hot Plug User Configuration				1E0h
Factory Test Only				1E4h
Bad TLP Counter				1E8h
Bad DLLP Counter				1ECh
Reserved				1F0h
Station 0/1 Lane Status				1F4h
ACK Transmission Latency Limit				1F8h
Factory Test Only				1FCh

a. Certain registers are Port-specific, others are Station-specific or Chip-specific; all are device-specific.

Register 12-55. 1C0h Device-Specific Error Status for Egress ECC Error (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
ECC is checked by the egress Port, and any ECC error is reported by the egress Station (containing the egress Port), when that Port reads the Packet data from the ingress Station RAM. *For example*, when Port 4 receives a packet, the data is stored in Station 1 RAM; then, if the egress Port is in Station 0 and an ECC error is detected when the Port reads the Station 1 RAM, the error is flagged in the Port 0 register bit that reflects Station 1 error status. ***Note:*** *The bits in this register can be masked by their respective* ***Device-Specific Error Mask for Egress ECC Error*** *register bits (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1C4h).*				
0	**Station 0 Payload Link List RAM Instance 0 1-Bit Soft Error Status** 0 = No 1-bit Soft error is detected 1 = 1-bit Soft error is detected	RW1CS	Yes	0
1	**Station 1 Payload Link List RAM Instance 0 1-Bit Soft Error Status** 0 = No 1-bit Soft error is detected 1 = 1-bit Soft error is detected	RW1CS	Yes	0
2	**Station 2 Payload Link List RAM Instance 0 1-Bit Soft Error Status** 0 = No 1-bit Soft error is detected 1 = 1-bit Soft error is detected	RW1CS	Yes	0
3	**Station 0 Payload Link List RAM Instance 0 Read Detected 2-Bit Soft Error Status** 0 = No 2-bit Soft error is detected 1 = Read detected a 2-bit Soft error	RW1CS	Yes	0
4	**Station 1 Payload Link List RAM Instance 0 Read Detected 2-Bit Soft Error Status** 0 = No 2-bit Soft error is detected 1 = Read detected a 2-bit Soft error	RW1CS	Yes	0
5	**Station 2 Payload Link List RAM Instance 0 Read Detected 2-Bit Soft Error Status** 0 = No 2-bit Soft error is detected 1 = Read detected a 2-bit Soft error	RW1CS	Yes	0
6	**Ingress Link List RAM Read Detected 1-Bit ECC Error Status** 0 = No 1-bit ECC error is detected 1 = Read detected a 1-Bit ECC error	RW1CS	Yes	0
7	**Ingress Link List RAM Read Detected 2-Bit ECC Error Status** 0 = No 2-bit ECC error is detected 1 = Read detected a 2-Bit ECC error	RW1CS	Yes	0

Register 12-55. 1C0h Device-Specific Error Status for Egress ECC Error (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
8	**Station 0 Packet RAM 0 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status** 0 = No 1-Bit Soft Error Tracking Counter overflow is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0
9	**Station 1 Packet RAM 0 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status** 0 = No 1-Bit Soft Error Tracking Counter overflow is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0
10	**Station 2 Packet RAM 0 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status** 0 = No 1-Bit Soft Error Tracking Counter overflow is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0
11	**Station 0 Packet RAM 0 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status** 0 = No 1-Bit Soft Error Tracking Counter overflow is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0
12	**Station 1 Packet RAM 0 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status** 0 = No 1-Bit Soft Error Tracking Counter overflow is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0
13	**Station 2 Packet RAM 0 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status** 0 = No 1-Bit Soft Error Tracking Counter overflow is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0
14	**Station 0 Packet RAM 0 Instance 0 Read Detected 2-Bit Soft Error Status** 0 = No 2-Bit Soft error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0
15	**Station 1 Packet RAM 0 Instance 0 Read Detected 2-Bit Soft Error Status** 0 = No 2-Bit Soft error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0

Register 12-55. 1C0h Device-Specific Error Status for Egress ECC Error (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
16	**Station 2 Packet RAM 0 Instance 0 Read Detected 2-Bit Soft Error Status** 0 = No 2-Bit Soft error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0
17	**Station 0 Packet RAM 0 Instance 1 Read Detected 2-Bit Soft Error Status** 0 = No 2-Bit Soft error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0
18	**Station 1 Packet RAM 0 Instance 1 Read Detected 2-Bit Soft Error Status** 0 = No 2-Bit Soft error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0
19	**Station 2 Packet RAM 0 Instance 1 Read Detected 2-Bit Soft Error Status** 0 = No 2-Bit Soft error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0
20	**Station 0 Packet RAM 1 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status** 0 = No 1-Bit Soft Error Tracking Counter overflow is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0
21	**Station 1 Packet RAM 1 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status** 0 = No 1-Bit Soft Error Tracking Counter overflow is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0
22	**Station 2 Packet RAM 1 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status** 0 = No 1-Bit Soft Error Tracking Counter overflow is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0
23	**Station 0 Packet RAM 1 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status** 0 = No 1-Bit Soft Error Tracking Counter overflow is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0

Register 12-55. 1C0h Device-Specific Error Status for Egress ECC Error (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
24	**Station 1 Packet RAM 1 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status** 0 = No 1-Bit Soft Error Tracking Counter overflow is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0
25	**Station 2 Packet RAM 1 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status** 0 = No 1-Bit Soft Error Tracking Counter overflow is detected 1 = 1-Bit Soft Error Tracking Counter overflow is detected	RW1CS	Yes	0
26	**Station 0 Packet RAM 1 Instance 0 Read Detected 2-Bit Soft Error Status** 0 = No 2-Bit Soft error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0
27	**Station 1 Packet RAM 1 Instance 0 Read Detected 2-Bit Soft Error Status** 0 = No 2-Bit Soft error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0
28	**Station 2 Packet RAM 1 Instance 0 Read Detected 2-Bit Soft Error Status** 0 = No 2-Bit Soft error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0
29	**Station 0 Packet RAM 1 Instance 1 Read Detected 2-Bit Soft Error Status** 0 = No 2-Bit Soft error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0
30	**Station 1 Packet RAM 1 Instance 1 Read Detected 2-Bit Soft Error Status** 0 = No 2-Bit Soft error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0
31	**Station 2 Packet RAM 1 Instance 1 Read Detected 2-Bit Soft Error Status** 0 = No 2-Bit Soft error is detected 1 = Read detected a 2-Bit Soft error	RW1CS	Yes	0

Register 12-56. 1C4h Device-Specific Error Mask for Egress ECC Error (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Notes: *The bits in this register can be used to mask their respective* ***Device-Specific Error Status for Egress ECC Error*** *register bits (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1C0h).* *Bits for Station 0 are valid only in the Port 0 register, bits for Station 1 are valid only in the Port 4 register, and bits for Station 2 are valid only in the Port 8 register. When Port 0 is the NT Port, only those bits for Station 0 are valid in the NT Port Virtual Interface register.*				
0	**Station 0 Payload Link List RAM Instance 0 1-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Station 0 Payload Link List RAM Instance 0 1-Bit Soft Error Status* bit is masked/disabled	RWS	Yes	1
1	**Station 1 Payload Link List RAM Instance 0 1-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Station 1 Payload Link List RAM Instance 0 1-Bit Soft Error Status* bit is masked/disabled	RWS	Yes	1
2	**Station 2 Payload Link List RAM Instance 0 1-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Station 2 Payload Link List RAM Instance 0 1-Bit Soft Error Status* bit is masked/disabled	RWS	Yes	1
3	**Station 0 Payload Link List RAM Instance 0 Read Detected 2-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Station 0 Payload Link List RAM Instance 0 Read Detected 2-Bit Soft Error Status* bit is masked/disabled	RWS	Yes	1
4	**Station 1 Payload Link List RAM Instance 0 Read Detected 2-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Station 1 Payload Link List RAM Instance 0 Read Detected 2-Bit Soft Error Status* bit is masked/disabled	RWS	Yes	1
5	**Station 2 Payload Link List RAM Instance 0 Read Detected 2-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Station 2 Payload Link List RAM Instance 0 Read Detected 2-Bit Soft Error Status* bit is masked/disabled	RWS	Yes	1
6	**Ingress Link List RAM Read Detected 1-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Ingress Link List RAM Read Detected 1-Bit ECC Error Status* bit is masked/disabled	RWS	Yes	1
7	**Ingress Link List RAM Read Detected 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Ingress Link List RAM Read Detected 2-Bit ECC Error Status* bit is masked/disabled	RWS	Yes	1

Register 12-56. 1C4h Device-Specific Error Mask for Egress ECC Error (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
8	**Station 0 Packet RAM 0 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Mask** 0 = No effect on reporting activity 1 = *Station 0 Packet RAM 0 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status* bit is masked/disabled	RWS	Yes	1
9	**Station 1 Packet RAM 0 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Mask** 0 = No effect on reporting activity 1 = *Station 1 Packet RAM 0 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status* bit is masked/disabled	RWS	Yes	1
10	**Station 2 Packet RAM 0 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Mask** 0 = No effect on reporting activity 1 = *Station 2 Packet RAM 0 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status* bit is masked/disabled	RWS	Yes	1
11	**Station 0 Packet RAM 0 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Mask** 0 = No effect on reporting activity 1 = *Station 0 Packet RAM 0 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status* bit is masked/disabled	RWS	Yes	1
12	**Station 1 Packet RAM 0 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Mask** 0 = No effect on reporting activity 1 = *Station 1 Packet RAM 0 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status* bit is masked/disabled	RWS	Yes	1
13	**Station 2 Packet RAM 0 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Mask** 0 = No effect on reporting activity 1 = *Station 2 Packet RAM 0 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status* bit is masked/disabled	RWS	Yes	1
14	**Station 0 Packet RAM 0 Instance 0 Read Detected 2-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Station 0 Packet RAM 0 Instance 0 Read Detected 2-Bit Soft Error Status* bit is masked/disabled	RWS	Yes	1
15	**Station 1 Packet RAM 0 Instance 0 Read Detected 2-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Station 1 Packet RAM 0 Instance 0 Read Detected 2-Bit Soft Error Status* bit is masked/disabled	RWS	Yes	1

Register 12-56. 1C4h Device-Specific Error Mask for Egress ECC Error (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
16	**Station 2 Packet RAM 0 Instance 0 Read Detected 2-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Station 2 Packet RAM 0 Instance 0 Read Detected 2-Bit Soft Error Status* bit is masked/disabled	RWS	Yes	1
17	**Station 0 Packet RAM 0 Instance 1 Read Detected 2-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Station 0 Packet RAM 0 Instance 1 Read Detected 2-Bit Soft Error Status* bit is masked/disabled	RWS	Yes	1
18	**Station 1 Packet RAM 0 Instance 1 Read Detected 2-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Station 1 Packet RAM 0 Instance 1 Read Detected 2-Bit Soft Error Status* bit is masked/disabled	RWS	Yes	1
19	**Station 2 Packet RAM 0 Instance 1 Read Detected 2-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Station 2 Packet RAM 0 Instance 1 Read Detected 2-Bit Soft Error Status* bit is masked/disabled	RWS	Yes	1
20	**Station 0 Packet RAM 1 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Mask** 0 = No effect on reporting activity 1 = *Station 0 Packet RAM 1 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status* bit is masked/disabled	RWS	Yes	1
21	**Station 1 Packet RAM 1 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Mask** 0 = No effect on reporting activity 1 = *Station 1 Packet RAM 1 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status* bit is masked/disabled	RWS	Yes	1
22	**Station 2 Packet RAM 1 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Mask** 0 = No effect on reporting activity 1 = *Station 2 Packet RAM 1 Instance 0 1-Bit Soft Error Tracking Counter Overflow Detected Status* bit is masked/disabled	RWS	Yes	1
23	**Station 0 Packet RAM 1 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Mask** 0 = No effect on reporting activity 1 = *Station 0 Packet RAM 1 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status* bit is masked/disabled	RWS	Yes	1

Register 12-56. 1C4h Device-Specific Error Mask for Egress ECC Error (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
24	**Station 1 Packet RAM 1 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Mask** 0 = No effect on reporting activity 1 = *Station 1 Packet RAM 1 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status* bit is masked/disabled	RWS	Yes	1
25	**Station 2 Packet RAM 1 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Mask** 0 = No effect on reporting activity 1 = *Station 2 Packet RAM 1 Instance 1 1-Bit Soft Error Tracking Counter Overflow Detected Status* bit is masked/disabled	RWS	Yes	1
26	**Station 0 Packet RAM 1 Instance 0 Read Detected 2-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Station 0 Packet RAM 1 Instance 0 Read Detected 2-Bit Soft Error Status* bit is masked/disabled	RWS	Yes	1
27	**Station 1 Packet RAM 1 Instance 0 Read Detected 2-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Station 1 Packet RAM 1 Instance 0 Read Detected 2-Bit Soft Error Status* bit is masked/disabled	RWS	Yes	1
28	**Station 2 Packet RAM 1 Instance 0 Read Detected 2-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Station 2 Packet RAM 1 Instance 0 Read Detected 2-Bit Soft Error Status* bit is masked/disabled	RWS	Yes	1
29	**Station 0 Packet RAM 1 Instance 1 Read Detected 2-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Station 0 Packet RAM 1 Instance 1 Read Detected 2-Bit Soft Error Status* bit is masked/disabled	RWS	Yes	1
30	**Station 1 Packet RAM 1 Instance 1 Read Detected 2-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Station 1 Packet RAM 1 Instance 1 Read Detected 2-Bit Soft Error Status* bit is masked/disabled	RWS	Yes	1
31	**Station 2 Packet RAM 1 Instance 1 Read Detected 2-Bit Soft Error Mask** 0 = No effect on reporting activity 1 = *Station 2 Packet RAM 1 Instance 1 Read Detected 2-Bit Soft Error Status* bit is masked/disabled	RWS	Yes	1

Register 12-57. 1C8h ECC Error Check Disable (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
0	**ECC 1-Bit Error Check Disable** 0 = RAM 1-Bit Soft Error Check enabled 1 = Disables RAM 1-Bit Soft Error Check	0	RWS	Yes	0
1	**ECC 2-Bit Error Check Disable** 0 = RAM 2-Bit Soft Error Check enabled 1 = Disables RAM 2-Bit Soft Error Check	0	RWS	Yes	0
2	**Software Force Error Enable** 1 = **Correctable Error Status** and **Uncorrectable Error Status** registers (offsets FC4h and FB8h, respectively) change from RW1CS to RW		RWS	Yes	0
3	**Software Force Non-Posted Request** Used to select software-forced errors to be associated with Posted or Non-Posted TLPs, because some errors are handled differently, depending upon the TLP type (Posted or Non-Posted). 0 = Handle software-forced errors as if the errors are associated with Posted TLPs 1 = Enables handling of errors associated with Posted TLPs as if those errors are associated with Non-Posted TLPs		RWS	Yes	0
4	**Enable PEX_INTA# Interrupt Output(s) for Hot Plug or Link State Event-Triggered Interrupts** 0 = Hot Plug or Link State Event Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = Hot Plug or Link State Event Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)		RWS	Yes	0
5	**Enable PEX_INTA# Interrupt Output(s) for Device-Specific Error- and Event-Triggered Interrupts** ***Note:*** *For further details, refer to Section 9.1.1, "Interrupt Sources or Events."*				
	Enables PEX_INTA# or INT*x* interrupt signaling for the RAM ECC errors defined in the **Device-Specific Error Status for Egress ECC Error**, **Device-Specific Error Mask for Egress ECC Error**, **Error Handler 32-Bit Error Status**, and **Error Handler 32-Bit Error Mask** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, unless noted otherwise, offsets 1C0h, 1C4h, 1CCh, and 1D0h, respectively). 0 = Device-Specific Error and Event Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = Device-Specific Error and Event Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)	0	RWS	Yes	0
	Also enables PEX_INTA# or INT*x* interrupt signaling for the errors defined in the **Link Error Status Virtual** and **Link Error Mask Virtual** registers (NT Port Virtual Interface, offsets FE0h and FE4h, respectively). 0 = Device-Specific Error and Event Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = Device-Specific Error and Event Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)	NT Port Virtual Interface, or Port 0 if Port 0 is the NT Port	RWS	Yes	0
	Reserved	Otherwise	RsvdP	No	0

Register 12-57. 1C8h ECC Error Check Disable (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
6	**Enable PEX_INTA# Interrupt Output(s) for GPIO-Generated Interrupts** 0 = General-Purpose Input/Output (GPIO) Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = GPIO Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)		RWS	Yes	0
7	**Enable PEX_INTA# Interrupt Output(s) for NT-Virtual Doorbell-Generated Interrupts** ***This bit is valid only in NT mode.*** Enables either PEX_INTA# or INT*x* Messages for NT-Virtual Doorbell interrupts (NT Port Virtual Interface, offsets C4Ch through C58h). 0 = NT-Virtual Doorbell Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = NT-Virtual Doorbell Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)	NT Port Virtual Interface, or Port 0 if Port 0 is the NT Port	RWS	Yes	0
	Reserved	Otherwise	RsvdP	No	0
8	**Disable Sending MSI if MSI Is Enabled after Interrupt Status Set** 0 = Does not disable sending an MSI, if MSIs are enabled after an *Interrupt Status* bit is Set 1 = Disables sending an MSI, if MSIs are enabled after an *Interrupt Status* bit is Set ***Note:*** *This bit must remain Cleared, for compliance to specifications governing the MSI Capability.*		RWS	Yes	0
31:9	***Reserved***		RsvdP	No	0-0h

Register 12-58. 1CCh Error Handler 32-Bit Error Status (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Notes: *All errors in this register generate MSI/INTx interrupts, if enabled.* *The bits in this register can be masked by their respective* ***Error Handler 32-Bit Error Mask*** *register bits (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1D0h, with the exception of bit 0, which is in all Ports).* *Bits for Station 0 are valid only in the Port 0 register, bits for Station 1 are valid only in the Port 4 register, and bits for Station 2 are valid only in the Port 8 register. When Port 0 is the NT Port, only those bits for Station 0 are valid in the NT Port Virtual Interface register.*					
0	**Completion FIFO Overflow Status** 0 = No overflow is detected 1 = Completion FIFO Overflow is detected when a 4-deep Completion FIFO for ingress, or a 1-deep Completion FIFO for egress, overflows	All	RW1CS	Yes	0
1	***Reserved***		RsvdP	No	0
2	***Factory Test Only***		RW1CS	No	0
3	***Reserved***		RsvdP	No	0
4	**Destination Queue Link List RAM 2-Bit Error** 0 = No error is detected 1 = Destination Queue Link List RAM 2-bit error is detected		RW1CS	Yes	0
5	***Reserved***		RsvdP	No	0
6	**Destination Queue Link List RAM 1-Bit Error Counter Overflow** 0 = No error is detected 1 = Destination Queue Link List RAM 1-bit error is detected		RW1CS	Yes	0
7	***Reserved***		RsvdP	No	0
8	**Source Queue Link List RAM 1-Bit Error Counter Overflow** 0 = No error is detected 1 = Source Queue Link List RAM 1-bit error is detected		RW1CS	Yes	0
9	**Source Queue Link List RAM 2-Bit Error** 0 = No error is detected 1 = Source Queue Link List RAM 2-bit error is detected		RW1CS	Yes	0
10	**32 Entry Retry Buffer 1-Bit Error Counter Overflow** 0 = No error is detected 1 = Retry Buffer 1-bit error is detected		RW1CS	Yes	0
11	**32 Entry Retry Buffer 2-Bit ECC Error** 0 = No error is detected 1 = Retry Buffer 2-bit error is detected		RW1CS	Yes	0

Register 12-58. 1CCh Error Handler 32-Bit Error Status (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
19:12	***Reserved***		RsvdP	No	0-0h
20	**TLP ID RAM 2-Bit ECC Error for Station 0** 0 = No error is detected 1 = TLP ID RAM 2-bit ECC error is detected		RW1CS	Yes	0
21	**TLP ID RAM 2-Bit ECC Error for Station 1** 0 = No error is detected 1 = TLP ID RAM 2-bit ECC error is detected		RW1CS	Yes	0
22	**TLP ID RAM 2-Bit ECC Error for Station 2** 0 = No error is detected 1 = TLP ID RAM 2-bit ECC error is detected		RW1CS	Yes	0
23	***Reserved***		RsvdP	No	0
24	**TLP ID RAM 1-Bit ECC Error Counter Overflow for Station 0** 0 = No error is detected 1 = TLP ID RAM 1-bit ECC Error Counter overflow is detected		RW1CS	Yes	0
25	**TLP ID RAM 1-Bit ECC Error Counter Overflow for Station 1** 0 = No error is detected 1 = TLP ID RAM 1-bit ECC Error Counter overflow is detected		RW1CS	Yes	0
26	**TLP ID RAM 1-Bit ECC Error Counter Overflow for Station 2** 0 = No error is detected 1 = TLP ID RAM 1-bit ECC Error Counter overflow is detected		RW1CS	Yes	0
31:27	***Reserved***		RsvdP	No	0-0h

Register 12-59. 1D0h Error Handler 32-Bit Error Mask (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Notes: *Error logging is enabled in this register, by default.* *The bits in this register can be used to mask their respective* ***Error Handler 32-Bit Error Status*** *register bits (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1CCh, with the exception of bit 0, which is in all Ports).* *Bits for Station 0 are valid only in the Port 0 register, bits for Station 1 are valid only in the Port 4 register, and bits for Station 2 are valid only in the Port 8 register. When Port 0 is the NT Port, only those bits for Station 0 are valid in the NT Port Virtual Interface register.*					
0	**Completion FIFO Overflow Mask** 0 = If enabled, error generates MSI/INT*x* interrupt 1 = *Completion FIFO Overflow Status* bit is masked/disabled	All	RWS	Yes	1
1	***Reserved***		RsvdP	No	0
2	***Factory Test Only***		RWS	Yes	1
3	***Reserved***		RsvdP	No	0
4	**Destination Queue Link List RAM 2-Bit Error Mask** 0 = No effect on reporting activity 1 = *Destination Queue Link List RAM 2-Bit Error* bit is masked/disabled		RWS	Yes	1
5	***Reserved***		RsvdP	No	0
6	**Destination Queue Link List RAM 1-Bit Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *Destination Queue Link List RAM 1-Bit Error Counter Overflow* bit is masked/disabled		RWS	Yes	1
7	***Reserved***		RsvdP	No	0
8	**Source Queue Link List RAM 1-Bit Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *Source Queue Link List RAM 1-Bit Error Counter Overflow* bit is masked/disabled		RWS	Yes	1
9	**Source Queue Link List RAM 2-Bit Error Mask** 0 = No effect on reporting activity 1 = *Source Queue Link List RAM 2-Bit Error* bit is masked/disabled		RWS	Yes	1
10	**32 Entry Retry Buffer 1-Bit Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *32 Entry Retry Buffer 1-Bit Error Counter Overflow* bit is masked/disabled		RWS	Yes	1
11	**32 Entry Retry Buffer 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *32 Entry Retry Buffer 2-Bit ECC Error* bit is masked/disabled		RWS	Yes	1

Register 12-59. 1D0h Error Handler 32-Bit Error Mask (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
19:12	***Reserved***		RsvdP	No	0-0h
20	**TLP ID RAM 2-Bit ECC Error Mask for Station 0** 0 = No effect on reporting activity 1 = *TLP ID RAM 2-Bit ECC Error for Station 0* bit is masked/ disabled		RWS	Yes	1
21	**TLP ID RAM 2-Bit ECC Error Mask for Station 1** 0 = No effect on reporting activity 1 = *TLP ID RAM 2-Bit ECC Error for Station 1* bit is masked/ disabled		RWS	Yes	1
22	**TLP ID RAM 2-Bit ECC Error Mask for Station 2** 0 = No effect on reporting activity 1 = *TLP ID RAM 2-Bit ECC Error for Station 2* bit is masked/ disabled		RWS	Yes	1
23	***Reserved***		RsvdP	No	0
24	**TLP ID RAM 1-Bit ECC Error Counter Overflow Mask for Station 0** 0 = No effect on reporting activity 1 = *TLP ID RAM 1-Bit ECC Error Counter Overflow for Station 0* bit is masked/disabled		RWS	Yes	1
25	**TLP ID RAM 1-Bit ECC Error Counter Overflow Mask for Station 1** 0 = No effect on reporting activity 1 = *TLP ID RAM 1-Bit ECC Error Counter Overflow for Station 1* bit is masked/disabled		RWS	Yes	1
26	**TLP ID RAM 1-Bit ECC Error Counter Overflow Mask for Station 2** 0 = No effect on reporting activity 1 = *TLP ID RAM 1-Bit ECC Error Counter Overflow for Station 2* bit is masked/disabled		RWS	Yes	1
31:27	***Reserved***		RsvdP	No	0-0h

Register 12-60. 1D8h Clock Enable (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Ports and Stations are automatically enabled, according to the Port configuration defined by the STRAP_STN*x*_PORTCFG*x* inputs, which can be overridden by programming the **Port Configuration** register *Port Configuration for Station x* bits (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[5:0]). An enabled Port can be selectively disabled, however, by Clearing the Port's *Port x Clock Enable* bit in this register. Port 0 must always remain enabled, and Ports 4 and 8 (containing Station registers) must remain enabled, if other Ports in the respective Stations are enabled.				
0	**Port 0 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	1
1	**Port 1 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	Set by STRAP_STN0_PORTCFG1 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 0* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[1:0])
3:2	***Factory Test Only***	RsvdP	No	00b
4	**Port 4 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	1
5	**Port 5 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	Set by STRAP_STN1_PORTCFG0 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 1* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[3:2])
6	**Port 6 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	Set by STRAP_STN1_PORTCFG0 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 1* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[3:2])
7	***Factory Test Only***	RsvdP	No	0
8	**Port 8 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	Set by STRAP_STN2_PORTCFG1 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 2* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[5:4])
9	**Port 9 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	Set by STRAP_STN2_PORTCFG1 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 2* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[5:4])
11:10	***Factory Test Only***	RsvdP	No	00b

Register 12-60. 1D8h Clock Enable (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
12	**Station 1 Root Clock Enable**	RWS	Yes	1
13	**Station 2 Root Clock Enable**	RWS	Yes	Set by STRAP_STN2_PORTCFG1 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 2* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[5:4])
31:14	***Reserved***	RsvdP	No	0-0h

Register 12-61. 1DCh Debug Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default	
				Transparent Mode (STRAP_NT_ENABLE#=H)	NT Mode (STRAP_NT_ENABLE#=L)
Note: *If this register is programmed by the serial EEPROM, it must be programmed twice by the first two serial EEPROM entries, at locations 4h through 9h, and Ah through Fh, as listed in Table 6-1, "Serial EEPROM Data." The first entry must Set* ***Factory Test Only*** *bit 7, to enable Writes to certain fields within the register, and the second entry must Clear bit 7;* ***all other bit values must be identical in both entries****. If Port 0 is the NT Port, this register is loaded from the NT Port Virtual Interface register offset 1DCh location in the serial EEPROM.*					
3:0	***Factory Test Only***	RO	No	Fh	
6:4	***Reserved***	RsvdP	No	000b	
7	***Factory Test Only***	RWS	Yes	0	
11:8	**Upstream Port ID** Upstream Port Number – Reads the external Strap value on the STRAP_UPSTRM_PORTSEL[3:0] balls, at Reset de-assertion. When bit 15 (*Hardware/Software Configuration Mode Control*) is Cleared, software is not allowed to change this value.	RO	Yes	Set by STRAP_UPSTRM_PORTSEL[3:0] input levels or by serial EEPROM, or by I²C followed by a Soft Reset	
	When bit 15 (*Hardware/Software Configuration Mode Control*) is Set, Upstream Port Number can be Set by software. 0h = Port 0 (recommended) 1h = Port 1 4h = Port 4 5h = Port 5 6h = Port 6 8h = Port 8 9h = Port 9 All other encodings are ***reserved***.	RW[a]	Yes		

Register 12-61. 1DCh Debug Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default	
				Transparent Mode (STRAP_NT_ENABLE#=H)	NT Mode (STRAP_NT_ENABLE#=L)
13:12	**Interrupt Fencing Mode Select** **Mode 1 (Default)** **1.** When the PEX 8624 receives a packet with a Fatal error (Malformed, DLL Protocol error) from an external device, the switch logs the Header on the corresponding Port, sends a Fatal Error Message to the Host, then asserts FATAL_ERR#. **2.** When the PEX 8624 detects an internal Fatal error (ECC failure, Credit Overflow, Receiver Overflow, Surprise Link Down), the switch sends a Fatal Interrupt Message to the Host and asserts FATAL_ERR#. In certain situations, delivery of the interrupt is not guaranteed; however, the signal is always asserted upon a Fatal event. **Mode 2 (Generate Internal Reset)** Upon Fatal error (internal or external) detection, an internal Chip Level reset is asserted (equivalent to an In-Band Reset from the upstream Port). No Error Messages are generated, and no attempt is made to block packets in transit. **Mode 3 (Block All Packet Transmission)** Upon Fatal error (internal or external) detection, the Port logs the error in the **Uncorrectable Error Status** register (offset FB8h), then asserts FATAL_ERR#. This Fatal error detection blocks all the Ports from sending out TLPs. No Error Messages are generated. If a packet is already in transmission, an EDB is inserted to cancel the packet. **Mode 4 (Block All Packet Transmission and Create Surprise Down)** In addition to the Mode 3 actions, the PEX 8624 forces the upstream Link to go down, thus causing a Surprise Down event on the Link, so that the Host is notified. 00b = Mode 1 (default) 01b = Mode 2 – Generate Internal Reset 10b = Mode 3 – Block All Packet Transmission 11b = Mode 4 – Block All Packet Transmission and Create Surprise Down	RWS	Yes	00b	

Register 12-61. 1DCh Debug Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default	
				Transparent Mode (STRAP_NT_ENABLE#=H)	NT Mode (STRAP_NT_ENABLE#=L)
14	***Factory Test Only***	RWS	Yes	0	
15	**Hardware/Software Configuration Mode Control** Allows software to configure which Port is the upstream Port, as well as which Port is the NT Port. 0 = Upstream Port and NT Port selection by the STRAP_UPSTRM_PORTSEL[3:0] and STRAP_NT_UPSTRM_PORTSEL[1:0] inputs, respectively, which can be overridden by the serial EEPROM and/or I²C configuration mechanism. Cannot be changed by in-band software during runtime. 1 = In-band software can change which Port is configured to be the upstream Port and NT Port, by writing new values to fields [11:8 and 25:24] (*Upstream Port ID* and *NT Port Number*, respectively), followed by issuance of a Hot Reset to the upstream Port. Bit 20 (*Upstream Port and NT-Link DL_Down Reset Propagation Disable*) must be Cleared.	RWS	Yes	0	
16	**Upstream Hot Reset Control** 0 = Reset all logic, except Sticky bits and Device-Specific registers 1 = Reset only the Configuration Space registers of all Ports defined by the *PCI Express Base r2.0* ***Note:*** *Only a Fundamental Reset serial EEPROM load affects this bit.*	RWS	Yes	0	1
17	**Disable Serial EEPROM Load on Hot Reset** 0 = Enables serial EEPROM load upon upstream Port or NT Port Link Interface Hot Reset or *DL_Down* state 1 = Disables serial EEPROM load upon upstream Port or NT Port Link Interface Hot Reset or *DL_Down* state	RWS	Yes	0	
18	**NT Mode Enable** Used only in NT mode. NT mode (Intelligent Adapter) is enabled by the STRAP_NT_ENABLE# input, which is overridden by the value of this bit if this register is programmed by the serial EEPROM upon Fundamental Reset. Software, serial EEPROM load upon upstream Port or NT Port Link Interface Hot Reset or *DL_Down* state, and/or I²C are not allowed to change this value. 0 = NT mode is disabled (STRAP_NT_ENABLE#=H) 1 = NT mode is enabled (STRAP_NT_ENABLE#=L)	HwInit	Yes (Serial EEPROM only)	Set by STRAP_NT_ENABLE# input level or by serial EEPROM	
19	***Reserved***	RsvdP	No	0	

Register 12-61. 1DCh Debug Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default	
				Transparent Mode (STRAP_NT_ENABLE#=H)	NT Mode (STRAP_NT_ENABLE#=L)
20	**Upstream Port and NT-Link DL_Down Reset Propagation Disable** Setting this bit: • Enables the upstream Port to ignore a Hot Reset training sequence, • Blocks the PEX 8624 from manifesting an internal reset due to a DL_Down event, and • Prevents the downstream Ports from issuing a Hot Reset to downstream devices when a Hot Reset or DL_Down event occurs on the upstream Link If NT mode is enabled, Setting this bit additionally: • Enables the NT-Link Port to ignore a Hot Reset training sequence, and • Blocks the PEX 8624 NT Port Link Interface from manifesting an internal reset due to a DL_Down event on the NT Port Link	RWS	Yes	0	
21	**Cut-Thru Enable** 0 = Disables Cut-Thru support 1 = Enables Cut-Thru support	RWS	Yes	1	
22	***Reserved***	RsvdP	No	0	
23	***Factory Test Only***	RWS	Yes	0	
25:24	**NT Port Number** Used only in NT mode. When bit 18 (*NT Mode Enable*) is Set, and bit 15 (*Hardware/Software Configuration Mode Control*) is Cleared, the NT Port Number is Set by the STRAP_NT_UPSTRM_PORTSEL[1:0] Strapping inputs. This field is "Don't Care" for Transparent mode. Software is not allowed to change this value. ***Note:*** *Only Station 0 Ports can be selected as the upstream NT Port.*	HwInit	Yes	Set by STRAP_NT_UPSTRM_PORTSEL[1:0] input levels or by serial EEPROM, or by I²C followed by a Soft Reset	
	Used only in NT mode. When bits [18 and 15] (*NT Mode Enable* and *Hardware/Software Configuration Mode Control*, respectively) are both Set, the NT Port Number selected by this field is Set by software, using the values defined below. All other encodings are ***reserved***. 00b = Port 0 01b = Port 1 ***Note:*** *Only Station 0 Ports can be selected as the upstream NT Port.*	R/W[a]	Yes		
27:26	***Reserved***	RsvdP	No	00b	

Register 12-61. 1DCh Debug Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default	
				Transparent Mode (STRAP_NT_ENABLE#=H)	NT Mode (STRAP_NT_ENABLE#=L)
28	**Virtual Interface Access Enable** Used only in NT mode. When the serial EEPROM is not present, the default value is 1; otherwise, the default value is 0. 0 = Retries Type 0 Configuration TLP received on the NT Port Virtual Interface 1 = Accepts Type 0 Configuration TLP on the NT Port Virtual Interface ***Notes:*** *This bit does not affect the PEX 8624 in Transparent mode, nor does it affect other transaction types.* *Set this bit to enable Configuration access to the NT Port Virtual Interface.*	RW	Yes	1	
29	**Link Interface Access Enable** Used only in NT mode. 0 = Retries Type 0 Configuration Request received on the NT Port Link Interface 1 = Accepts Type 0 Configuration Request on the NT Port Link Interface ***Notes:*** *This bit does not affect the PEX 8624 in Transparent mode.* *Set this bit to enable Configuration access to the NT Port Link Interface.*	RW	Yes	0	

Register 12-61. 1DCh Debug Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default	
				Transparent Mode (STRAP_NT_ENABLE#=H)	NT Mode (STRAP_NT_ENABLE#=L)
30	**Inhibit EEPROM NT-Link Load on Hot Reset** Used only in NT mode. Inhibits serial EEPROM load of NT Port Link Interface registers when any one of the following conditions exist: • **Upstream Port Hot Reset** – Bits [17:16] (*Disable Serial EEPROM Load on Hot Reset* and *Upstream Hot Reset Control*, respectively) are Cleared • **Upstream Port *DL_Down* state** – Bits [20, 17:16] (*Upstream Port and NT-Link DL_Down Reset Propagation Disable*, *Disable Serial EEPROM Load on Hot Reset*, and *Upstream Hot Reset Control*, respectively) are Cleared • **NT Port Link Interface Hot Reset or *DL_Down* state** – Bit 17 (*Disable Serial EEPROM Load on Hot Reset*) is Cleared Refer also to Section 6.9, "Serial EEPROM Loading of NT Port Link Interface Registers," for further details.	RW	Yes	0	1
31	**Load Only EEPROM NT-Link on Hot Reset** Used only in NT mode. Load only serial EEPROM NT Port Link Interface register entries when any one of the following conditions exist: • **Upstream Port Hot Reset** – Bits [17:16] (*Disable Serial EEPROM Load on Hot Reset* and *Upstream Hot Reset Control*, respectively) are Cleared • **Upstream Port *DL_Down* state** – Bits [20, 17:16] (*Upstream Port and NT-Link DL_Down Reset Propagation Disable*, *Disable Serial EEPROM Load on Hot Reset*, and *Upstream Hot Reset Control*, respectively) are Cleared • **NT Port Link Interface Hot Reset or *DL_Down* state** – Bit 17 (*Disable Serial EEPROM Load on Hot Reset*) is Cleared Refer also to Section 6.9, "Serial EEPROM Loading of NT Port Link Interface Registers," for further details.	RW	Yes	0	1

a. Although these bits are RW, do not change by software.

Register 12-62. 1E0h Power Management Hot Plug User Configuration (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
0	**L0s Entry Idle Counter** Traffic Idle time to meet, to enter the L0s Link PM state. 0 = Idle condition must last 1 s 1 = Idle condition must last 4 s		RW	Yes	0
1	***Factory Test Only***		RW	Yes	0
2	***Not enabled*** Functionality associated with this bit is enabled only on the downstream Ports.	Upstream	RW	Yes	0
	HPC PME Turn-Off Enable 1 = PME Turn-Off Message is transmitted before the Port is turned Off on a downstream Port	Downstream	RW	Yes	0
4:3	***Not enabled*** Functionality associated with this field is enabled only on the downstream Ports.	Upstream	RW	Yes	00b
	HPC T_{pepv} Hot Plug Port time from Power Enable to Power Valid. Indicates the delay from when an HP_PWREN_*x* output is asserted High, to when power is valid at a slot. (Refer to Section 10.7.1.2, "Slot Power-Up Sequencing When Power Controller Present Bit Is Set," for details.) 00b = Feature is disabled, and HP_PWR_GOOD_*x* inputs are used for Power Valid 01b = 128 ms 10b = 256 ms 11b = 512 ms	Downstream	RW	Yes	00b
5	***Factory Test Only***		RW	Yes	0
6	***Not enabled*** Functionality associated with this bit is enabled only on the downstream Ports.	Upstream	RW	Yes (Serial EEPROM only)	0
	HP_PWR_GOOD_*x* Active-Low Enable Controls the HP_PWR_GOOD_*x* input polarity. (Refer to Section 10.7.1.2, "Slot Power-Up Sequencing When Power Controller Present Bit Is Set," for details.) 0 = HP_PWR_GOOD_*x* inputs are Active-High 1 = HP_PWR_GOOD_*x* inputs are Active-Low	Downstream	RW	Yes (Serial EEPROM only)	0
7	***Factory Test Only***		RW	Yes	0

Register 12-62. 1E0h Power Management Hot Plug User Configuration (All Ports) *(Cont.)*

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Ports</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td>8</td><td>DLLP Timeout Link Retrain Disable
Disable Link retraining when no Data Link Layer Packets (DLLPs) are received for more than 256 s.
0 = Enables Link retraining when no DLLPs are received for more than 256 s (default)
1 = DLLP Timeout is disabled</td><td></td><td>RW</td><td>Yes</td><td>0</td></tr>
<tr><td>9</td><td>Factory Test Only</td><td></td><td>RW</td><td>Yes</td><td>0</td></tr>
<tr><td>10</td><td>L0s Entry Disable
0 = Enables entry into the L0s Link PM state on a Port when the L0s idle conditions are met
1 = Disables entry into the L0s Link PM state on a Port when the L0s idle conditions are met</td><td></td><td>RW</td><td>Yes</td><td>0</td></tr>
<tr><td>12:11</td><td>Factory Test Only</td><td></td><td>RW</td><td>Yes</td><td>00b</td></tr>
<tr><td>14:13</td><td>HP Parallel Port
Indicates which Port in a Station is a Parallel Hot Plug Port. Defaults to Ports 1, 5, and 9. In x8 mode, the PEX 8624 Stations default to using Ports 0 and 8 as Hot Plug Ports (unless disabled by serial EEPROM). A Station Parallel Hot Plug Port is determined by the Port 0 Setting of that Station register (that is, Port 0, 4, or 8). Other Ports' values are unused.
<table>
<tr><th>Value</th><th>Port 0
Station 0</th><th>Port 4
Station 1</th><th>Port 8
Station 2</th></tr>
<tr><td>00b</td><td>Port 0</td><td>Reserved</td><td>Port 8</td></tr>
<tr><td>01b</td><td>Port 1</td><td>Port 5</td><td>Port 9</td></tr>
<tr><td>10b</td><td>Reserved</td><td>Port 6</td><td>Reserved</td></tr>
<tr><td>11b</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
</table></td><td>0, 4, 8</td><td>RO</td><td>Yes</td><td>01b</td></tr>
<tr><td>15</td><td>HPC GPIO Write in Progress
Indicates that the last Write operation to an I/O Expander GPIO x Output Data register (offsets 644h and 648h) is still in-progress.</td><td></td><td>RO</td><td>No</td><td>0</td></tr>
</table>

Register 12-62. 1E0h Power Management Hot Plug User Configuration (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
16	**HPC Serial Expansion Controller Disable** Valid only for Port 0. All other Ports' values are unused. 0 = Enables Serial Hot Plug capability on all Ports 1 = Disables Serial Hot Plug capability on all Ports	0	RW	Yes	0
17	**40-Pin I/O Expander Enable** 0 = Enables 16-pin I/O Expanders for all downstream Ports that implement Serial Hot Plug 1 = Enables 40-pin I/O Expanders for all downstream Ports that implement Serial Hot Plug ***Note:*** *Value of 1 can be enabled only by serial EEPROM (that is, it cannot be enabled by software nor by I²C).*	0/ NT Port Virtual Interface if Port 0 is the NT Port	RW	Yes (See Note)	0
18	**HPC GPIO Config** Programs the GPIO direction for one GPIO. 0 = Input 1 = Output; register is RW		RW	Yes	0
19	**HPC GPIO Input/Output Value** If the external I²C I/O Expander GPIO pin is programmed as input (*HPC GPIO Config*, bit 18 = 0), this bit reflects the logic value of the voltage on that Input pin. If the external I²C I/O Expander GPIO pin is programmed as output (*HPC GPIO Config*, bit 18 = 1), the value written to this bit is written to the external GPIO pin through the I²C Slave interface.		RW	Yes	0
20	**HPC I/O Reload** 1 = Parallel Hot Plug Controller/Serial Hot Plug Controller (I²C I/O Expander) Output pin values are re-loaded from field [26:21] (*HPC Output Reload Value*). After the action is complete, this bit is self-Clearing.		RW	Yes	0
26:21	**HPC Output Reload Value** When bit 20 (*HPC I/O Reload*) is Set, values from this field are re-loaded to the Hot Plug Controller outputs associated with the Port. Bit 21 = HP_PWRLED_*x*# or I/O Expander PWRLED# Bit 22 = HP_ATNLED_*x*# or I/O Expander ATNLED# Bit 23 = HP_PWREN_*x* or I/O Expander PWREN Bit 24 = HP_CLKEN_*x*# or I/O Expander REFCLKEN# Bit 25 = HP_PERST_*x*# or I/O Expander PERST# Bit 26 = I/O Expander INTERLOCK		RW	Yes	0-0h
31:27	***Factory Test Only***		RW	Yes	0-0h

Register 12-63. 1E8h Bad TLP Counter (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Bad TLP Counter** Counts the number of TLPs received with bad Link Cyclic Redundancy Check (LCRC), or number of TLPs with a Sequence Number Mismatch error. The Counter saturates at FFFF_FFFFh and does not roll over to 0000_0000h.	RWS	Yes	0000_0000h

Register 12-64. 1ECh Bad DLLP Counter (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Bad DLLP Counter** Counts the number of DLLPs received with bad LCRC, or number of DLLPs with a Sequence Number Mismatch error. The Counter saturates at FFFF_FFFFh and does not roll over to 0000_0000h.	RWS	Yes	0000_0000h

Register 12-65. 1F4h Station 0/1 Lane Status
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**Lane 0 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
1	**Lane 1 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
2	**Lane 2 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
3	**Lane 3 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
4	**Lane 4 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
5	**Lane 5 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
6	**Lane 6 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
7	**Lane 7 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
23:8	***Factory Test Only***	RsvdP	No	0000h
24	**Lane 24 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
25	**Lane 25 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
26	**Lane 26 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
27	**Lane 27 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1

Register 12-65. 1F4h Station 0/1 Lane Status (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
28	**Lane 28 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
29	**Lane 29 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
30	**Lane 30 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
31	**Lane 31 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1

Register 12-66. 1F8h ACK Transmission Latency Limit (All Ports)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td colspan="5">The value of this register should be valid after Link negotiation.</td></tr>
<tr><td>11:0</td><td>ACK Transmission Latency Limit
Acknowledge Control Packet (ACK) Transmission Latency Limit.
The value of this field changes, based upon the Current Link Speed (offset 78h[19:16]), Negotiated Link Width (offset 78h[25:20]), and Maximum Payload Size (offset 70h[7:5]).
<table>
<tr><th>Maximum Payload Size</th><th>x4 Gen 2 (Symbol Times)</th><th>x8 Gen 2 (Symbol Times)</th></tr>
<tr><td>128B</td><td>124</td><td>118</td></tr>
<tr><td>256B</td><td>169</td><td>158</td></tr>
<tr><td>512B</td><td>205</td><td>137</td></tr>
</table></td><td>RWS</td><td>Yes</td><td>Set by STRAP_STNx_PORT CFGx input levels</td></tr>
<tr><td>15:12</td><td>Reserved</td><td>RsvdP</td><td>No</td><td>0h</td></tr>
<tr><td>23:16</td><td>Upper 8 Bits of the Replay Timer Limit
If the serial EEPROM is not present, the value of this register changes based upon the negotiated Link width after the Link is up.
The value in this register is a multiplier of the default internal timer values that are compliant to the PCI Express Base r2.0. These bits should normally remain the default value, 00h.</td><td>RWS</td><td>Yes</td><td>00h</td></tr>
<tr><td>30:24</td><td>Reserved</td><td>RsvdP</td><td>No</td><td>0-0h</td></tr>
<tr><td>31</td><td>ACK Transmission Latency Timer Status
Indicates the written status of field [11:0] (ACK Transmission Latency Limit). After the register is written, either by software and/or serial EEPROM, this bit is Set, and Cleared only by a Fundamental Reset.</td><td>RO</td><td>No</td><td>0</td></tr>
</table>

12.14.2 Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)

This section details the Device-Specific PHY registers located at offsets 200h through 25Ch. Table 12-18 defines the register map.

Table 12-19 defines the relationship between the SerDes Support registers' Port 0, 4, or 8 parameters and SerDes modules and Lanes, when all Ports are enabled. SerDes modules and Lanes marked "***Factory Test Only***" are associated with bits that are RsvdP and not serial EEPROM nor I^2C writable.

Other Device-Specific PHY registers are detailed in Section 12.14.4, "Device-Specific Registers – Physical Layer (Offsets 270h – 28Ch)."

Table 12-18. Device-Specific Physical Layer Register Map (Offsets 200h – 25Ch)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Physical Layer Receiver Detect Status	Physical Layer Electrical Idle for Compliance Mask	200h
Physical Layer Receiver Not Detected Mask	Physical Layer Electrical Idle Detect Mask	204h
Factory Test Only		208h – 20Ch
Physical Layer User Test Pattern, Bytes 0 through 3		210h
Physical Layer User Test Pattern, Bytes 4 through 7		214h
Physical Layer User Test Pattern, Bytes 8 through 11		218h
Physical Layer User Test Pattern, Bytes 12 through 15		21Ch
Physical Layer Command and Status		220h
Reserved		224h
Physical Layer Test		228h
Factory Test Only		22Ch
Reserved	Physical Layer Port Command	230h
Port Control	SKIP Ordered-Set Interval	234h
SerDes Quad 0 Diagnostic Data		238h
SerDes Quad 1 Diagnostic Data		23Ch
SerDes Quad 2 Diagnostic Data		240h
SerDes Quad 3 Diagnostic Data		244h
Factory Test Only	Port Receiver Error Counter	248h
Factory Test Only	Target Link Width	24Ch
Reserved		250h
Physical Layer Additional Status		254h
PRBS Control/Status		258h
Reserved		25Ch

Notes: *In this section, the term "SerDes quad" or "quad" refers to assembling SerDes modules into groups of four contiguous Lanes for testing purposes.*

The six PEX 8624 Ports that connect to PCI Express Transmitters and Receivers are Ports 0, 1, 5, 6, 8, and 9, and each Port has its own set of registers. An additional set of Port 4 registers is visible to software, although the Port is not connected to external signals. The Port 4 registers include:

- *Other Device-Specific registers.*
- *"Station" registers, that control all Ports in Station 1 (Ports 5 and 6), and are identical to the corresponding Port 0 registers that control all Ports in Station 0 (Ports 0 and 1) and Port 8 registers that control all Ports in Station 2 (Ports 8 and 9). The Station registers include Physical Layer registers, Device-Specific Error registers, and internal mapping (CAM) registers.*

Table 12-19. Port/Physical Lane/SerDes Module/Station/SerDes Quad Relationship, when All Ports Are Enabled, for Offsets 200h through 25Ch

Physical Lanes and SerDes Modules, by Port						SerDes Quad
Station 0, Port 0		Station 1, Port 4		Station 2, Port 8		
Port	Physical Lanes and SerDes Modules	Port	Physical Lanes and SerDes Modules	Port	Physical Lanes and SerDes Modules	
0	0-3	–	***Factory Test Only***	8	32-35	0
1	4-7	–	***Factory Test Only***	9	36-39	1
–	***Factory Test Only***	5	24-27	–	***Factory Test Only***	2
–	***Factory Test Only***	6	28-31	–	***Factory Test Only***	3

Register 12-67. 200h Physical Layer Receiver Detect Status and Electrical Idle for Compliance Mask (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register is used for specifying the pre-determined number of Lanes that detected a Receiver during an LTSSM *Detect* state, but never detected an exit from Electrical Idle. Because the PEX 8624 has multiple Port configurations, a Mask register is used, rather than specifying a number. When multiple bits are Set, and they correspond to Lanes that belong to the same Port, any of those specified Lanes can cause entry into the LTSSM *Polling.Compliance* state. ***Note:*** *Refer to Table 12-20 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules and Lanes.* ***Factory Test Only*** *bits are RsvdP and not serial EEPROM nor I^2C writable.*				
Physical Layer Electrical Idle for Compliance Mask				
This register allows masking that specifies which Lanes must never exit Electrical Idle, for entry to the LTSSM *Polling.Compliance* state to occur.				
0	**Electrical Idle on SerDes 0 or 32 Causes Entry to Compliance State** 0 = The LTSSM *Polling.Compliance* state cannot be entered due to the Electrical Idle condition 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
1	**Electrical Idle on SerDes 1 or 33 Causes Entry to Compliance State** 0 = The LTSSM *Polling.Compliance* state cannot be entered due to the Electrical Idle condition 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
2	**Electrical Idle on SerDes 2 or 34 Causes Entry to Compliance State** 0 = The LTSSM *Polling.Compliance* state cannot be entered due to the Electrical Idle condition 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
3	**Electrical Idle on SerDes 3 or 35 Causes Entry to Compliance State** 0 = The LTSSM *Polling.Compliance* state cannot be entered due to the Electrical Idle condition 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1

Register 12-67. 200h Physical Layer Receiver Detect Status and Electrical Idle for Compliance Mask (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**Electrical Idle on SerDes 4 or 36 Causes Entry to Compliance State** 0 = The LTSSM *Polling.Compliance* state cannot be entered due to the Electrical Idle condition 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
5	**Electrical Idle on SerDes 5 or 37 Causes Entry to Compliance State** 0 = The LTSSM *Polling.Compliance* state cannot be entered due to the Electrical Idle condition 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
6	**Electrical Idle on SerDes 6 or 38 Causes Entry to Compliance State** 0 = The LTSSM *Polling.Compliance* state cannot be entered due to the Electrical Idle condition 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
7	**Electrical Idle on SerDes 7 or 39 Causes Entry to Compliance State** 0 = The LTSSM *Polling.Compliance* state cannot be entered due to the Electrical Idle condition 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1

Register 12-67. 200h Physical Layer Receiver Detect Status and Electrical Idle for Compliance Mask (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**Electrical Idle on SerDes 24 Causes Entry to Compliance State** 0 = The LTSSM *Polling.Compliance* state cannot be entered due to the Electrical Idle condition 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
9	**Electrical Idle on SerDes 25 Causes Entry to Compliance State** 0 = The LTSSM *Polling.Compliance* state cannot be entered due to the Electrical Idle condition 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
10	**Electrical Idle on SerDes 26 Causes Entry to Compliance State** 0 = The LTSSM *Polling.Compliance* state cannot be entered due to the Electrical Idle condition 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
11	**Electrical Idle on SerDes 27 Causes Entry to Compliance State** 0 = The LTSSM *Polling.Compliance* state cannot be entered due to the Electrical Idle condition 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1

Register 12-67. 200h Physical Layer Receiver Detect Status and Electrical Idle for Compliance Mask (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
12	**Electrical Idle on SerDes 28 Causes Entry to Compliance State** 0 = The LTSSM *Polling.Compliance* state cannot be entered due to the Electrical Idle condition 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
13	**Electrical Idle on SerDes 29 Causes Entry to Compliance State** 0 = The LTSSM *Polling.Compliance* state cannot be entered due to the Electrical Idle condition 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
14	**Electrical Idle on SerDes 30 Causes Entry to Compliance State** 0 = The LTSSM *Polling.Compliance* state cannot be entered due to the Electrical Idle condition 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
15	**Electrical Idle on SerDes 31 Causes Entry to Compliance State** 0 = The LTSSM *Polling.Compliance* state cannot be entered due to the Electrical Idle condition 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1

Register 12-67. 200h Physical Layer Receiver Detect Status and Electrical Idle for Compliance Mask (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Physical Layer Receiver Detect Status				
This register returns the Receiver's LTSSM *Detect* state status for all Lanes within the Station.				
16	**Receiver Detected on Lane 0 or 32** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
17	**Receiver Detected on Lane 1 or 33** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
18	**Receiver Detected on Lane 2 or 34** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
19	**Receiver Detected on Lane 3 or 35** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
20	**Receiver Detected on Lane 4 or 36** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
21	**Receiver Detected on Lane 5 or 37** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
22	**Receiver Detected on Lane 6 or 38** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
23	**Receiver Detected on Lane 7 or 39** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
24	**Receiver Detected on Lane 24** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
25	**Receiver Detected on Lane 25** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
26	**Receiver Detected on Lane 26** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
27	**Receiver Detected on Lane 27** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
28	**Receiver Detected on Lane 28** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
29	**Receiver Detected on Lane 29** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
30	**Receiver Detected on Lane 30** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
31	**Receiver Detected on Lane 31** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes

Table 12-20. SerDes Module and Lane Control Relationship, by Station and Port, for Register Offsets 200h and 204h

Bit(s)	Station 0, Port 0 SerDes Module and Physical Lane	Station 1, Port 4 SerDes Module and Physical Lane	Station 2, Port 8 SerDes Module and Physical Lane
0	0	***Factory Test Only***	32
1	1	***Factory Test Only***	33
2	2	***Factory Test Only***	34
3	3	***Factory Test Only***	35
4	4	***Factory Test Only***	36
5	5	***Factory Test Only***	37
6	6	***Factory Test Only***	38
7	7	***Factory Test Only***	39
8	***Factory Test Only***	24	***Factory Test Only***
9	***Factory Test Only***	25	***Factory Test Only***
10	***Factory Test Only***	26	***Factory Test Only***
11	***Factory Test Only***	27	***Factory Test Only***
12	***Factory Test Only***	28	***Factory Test Only***
13	***Factory Test Only***	29	***Factory Test Only***
14	***Factory Test Only***	30	***Factory Test Only***
15	***Factory Test Only***	31	***Factory Test Only***
16	0	***Factory Test Only***	32
17	1	***Factory Test Only***	33
18	2	***Factory Test Only***	34
19	3	***Factory Test Only***	35
20	4	***Factory Test Only***	36
21	5	***Factory Test Only***	37
22	6	***Factory Test Only***	38
23	7	***Factory Test Only***	39
24	***Factory Test Only***	24	***Factory Test Only***
25	***Factory Test Only***	25	***Factory Test Only***
26	***Factory Test Only***	26	***Factory Test Only***
27	***Factory Test Only***	27	***Factory Test Only***
28	***Factory Test Only***	28	***Factory Test Only***
29	***Factory Test Only***	29	***Factory Test Only***
30	***Factory Test Only***	30	***Factory Test Only***
31	***Factory Test Only***	31	***Factory Test Only***

Register 12-68. 204h Electrical Idle Detect/Receiver Detect Mask (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register is used to mask Electrical Idle Detect and Receiver functions for debug purposes. It can also be used to mask SerDes problems with these circuits. Masking Electrical Idle Detect will not affect the inferred Electrical Idle detection. ***Notes: Use this register with caution.*** *Refer to Table 12-20 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules and Lanes.* ***Factory Test Only** bits are RsvdP and not serial EEPROM nor I^2C writable.*				
Physical Layer Electrical Idle Detect Mask				
0	**SerDes 0 or 32 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station. The Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.	RWS	Yes	0
1	**SerDes 1 or 33 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station. The Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.	RWS	Yes	0
2	**SerDes 2 or 34 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station. The Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.	RWS	Yes	0
3	**SerDes 3 or 35 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station. The Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.	RWS	Yes	0
4	**SerDes 4 or 36 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station. The Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.	RWS	Yes	0
5	**SerDes 5 or 37 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station. The Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.	RWS	Yes	0
6	**SerDes 6 or 38 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station. The Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.	RWS	Yes	0
7	**SerDes 7 or 39 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station. The Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.	RWS	Yes	0

Register 12-68. 204h Electrical Idle Detect/Receiver Detect Mask (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**SerDes 24 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station. The Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.	RWS	Yes	0
9	**SerDes 25 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station. The Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.	RWS	Yes	0
10	**SerDes 26 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station. The Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.	RWS	Yes	0
11	**SerDes 27 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station. The Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.	RWS	Yes	0
12	**SerDes 28 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station. The Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.	RWS	Yes	0
13	**SerDes 29 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station. The Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.	RWS	Yes	0
14	**SerDes 30 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station. The Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.	RWS	Yes	0
15	**SerDes 31 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station. The Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.	RWS	Yes	0

Register 12-68. 204h Electrical Idle Detect/Receiver Detect Mask (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Physical Layer Receiver Not Detected Mask				
16	**SerDes 0 or 32 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes Lanes, by Station. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
17	**SerDes 1 or 33 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes Lanes, by Station. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
18	**SerDes 2 or 34 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes Lanes, by Station. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
19	**SerDes 3 or 35 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes Lanes, by Station. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
20	**SerDes 4 or 36 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes Lanes, by Station. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
21	**SerDes 5 or 37 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes Lanes, by Station. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
22	**SerDes 6 or 38 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes Lanes, by Station. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
23	**SerDes 7 or 39 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes Lanes, by Station. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0

Register 12-68. 204h Electrical Idle Detect/Receiver Detect Mask (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
24	**SerDes 24 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes Lanes, by Station. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
25	**SerDes 25 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes Lanes, by Station. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
26	**SerDes 26 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes Lanes, by Station. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
27	**SerDes 27 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes Lanes, by Station. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
28	**SerDes 28 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes Lanes, by Station. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
29	**SerDes 29 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes Lanes, by Station. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
30	**SerDes 30 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes Lanes, by Station. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
31	**SerDes 31 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes Lanes, by Station. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0

Register 12-69. 210h Physical Layer User Test Pattern, Bytes 0 through 3 (Only Ports 0, 4, and 8 (Port 0 is for Station 0 Ports, Port 4 is for Station 1 Ports, Port 8 is for Station 2 Ports), and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
UTP Bytes 0 through 3. Used for Digital Far-End Loopback testing. ***Note:*** *A 16-byte test pattern can be written to register offsets 210h through 21Ch. When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 16.2.3, "Digital Loopback Master Mode," for further details.) Every byte of the UTP can be a control or data character. Illegal control characters can be specified.*				
7:0	Byte 0 of the UTP. This is the first byte transferred.	RW	Yes	00h
15:8	Byte 1 of the UTP.	RW	Yes	00h
23:16	Byte 2 of the UTP.	RW	Yes	00h
31:24	Byte 3 of the UTP.	RW	Yes	00h

Register 12-70. 214h Physical Layer User Test Pattern, Bytes 4 through 7 (Only Ports 0, 4, and 8 (Port 0 is for Station 0 Ports, Port 4 is for Station 1 Ports, Port 8 is for Station 2 Ports), and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
UTP Bytes 4 through 7. Used for Digital Far-End Loopback testing. ***Note:*** *A 16-byte test pattern can be written to register offsets 210h through 21Ch. When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 16.2.3, "Digital Loopback Master Mode," for further details.) Every byte of the UTP can be a control or data character. Illegal control characters can be specified.*				
7:0	Byte 4 of the UTP. This is the fifth byte transferred.	RW	Yes	00h
15:8	Byte 5 of the UTP.	RW	Yes	00h
23:16	Byte 6 of the UTP.	RW	Yes	00h
31:24	Byte 7 of the UTP.	RW	Yes	00h

Register 12-71. 218h Physical Layer User Test Pattern, Bytes 8 through 11 (Only Ports 0, 4, and 8 (Port 0 is for Station 0 Ports, Port 4 is for Station 1 Ports, Port 8 is for Station 2 Ports), and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
UTP Bytes 8 through 11. Used for Digital Far-End Loopback testing. ***Note:*** *A 16-byte test pattern can be written to register offsets 210h through 21Ch. When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 16.2.3, "Digital Loopback Master Mode," for further details.) Every byte of the UTP can be a control or data character. Illegal control characters can be specified.*				
7:0	Byte 8 of the UTP. This is the ninth byte transferred.	RW	Yes	00h
15:8	Byte 9 of the UTP.	RW	Yes	00h
23:16	Byte 10 of the UTP.	RW	Yes	00h
31:24	Byte 11 of the UTP.	RW	Yes	00h

Register 12-72. 21Ch Physical Layer User Test Pattern, Bytes 12 through 15 (Only Ports 0, 4, and 8 (Port 0 is for Station 0 Ports, Port 4 is for Station 1 Ports, Port 8 is for Station 2 Ports), and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
UTP Bytes 12 through 15. Used for Digital Far-End Loopback testing. ***Note:*** *A 16-byte test pattern can be written to register offsets 210h through 21Ch. When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 16.2.3, "Digital Loopback Master Mode," for further details.) Every byte of the UTP can be a control or data character. Illegal control characters can be specified.*				
7:0	Byte 12 of the UTP. This is the thirteenth byte transferred.	RW	Yes	00h
15:8	Byte 13 of the UTP.	RW	Yes	00h
23:16	Byte 14 of the UTP.	RW	Yes	00h
31:24	Byte 15 of the UTP.	RW	Yes	00h

Register 12-73. 220h Physical Layer Command and Status (Only Ports 0, 4, and 8 (Port 0 is for Station 0 Ports, Port 4 is for Station 1 Ports, Port 8 is for Station 2 Ports), and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides various Command and Status bits for PHY operation.				
2:0	**Number of Ports Available in the Station** Returns the quantity of enabled Ports that this Station contains, based upon the selected Port configuration.	RO	No	Set by STRAP_STN*x*_PORTCFG*x* input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station x* bits (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[5:0])
3	**Upstream Cross-Link Enable** 0 = Disables upstream cross-link, upstream Port cannot be connected to another upstream Port 1 = Enables upstream cross-link, upstream Port can be connected to another upstream Port	RWS	Yes	1
4	**Downstream Cross-Link Enable** 0 = Disables downstream cross-link, downstream Ports cannot be connected to other downstream Ports 1 = Enables downstream cross-link, downstream Ports can be connected to other downstream Ports	RWS	Yes	1
5	**Lane Reversal Disable** 0 = Enables Lane reversal on all Ports 1 = Disables Lane reversal on all Ports	RWS	Yes	0
6	***Reserved***	RsvdP	No	0
7	**Elastic Buffer Low-Latency Mode Disable** 0 = Enables Elastic Buffer Low-Latency mode. 1 = Disables Elastic Buffer Low-Latency mode. Latency through the Elastic buffer is increased from 4 symbol times, to 7 symbol times, on all Lanes.	RWS	Yes	0

Register 12-73. 220h Physical Layer Command and Status (Only Ports 0, 4, and 8 (Port 0 is for Station 0 Ports, Port 4 is for Station 1 Ports, Port 8 is for Station 2 Ports), and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:8	**N_FTS Value** Number of Fast Training Sets (N_FTS) value to transmit (in Training Sets).	RWS	Yes	64h
31:16	**User Test Pattern Control/Data** The UTP generators send out a set of 16 bytes of User Programmable data. A k-code bit can be Set for each byte. Bit 16 corresponds to Byte 0 of the User Test Pattern. … Bit 31 corresponds to Byte 15 of the User Test Pattern. 0 = Corresponding byte of the User Test Pattern is transmitted as a Data character 1 = Corresponding byte of the User Test Pattern is transmitted as a Control character ***Note: Use caution when Setting bits in this field, because UTP logic does not check the validity of Control characters.***	RWS	Yes	0000h

Register 12-74. 228h Physical Layer Test (Only Ports 0, 4, and 8 (Port 0 is for Station 0 Ports, Port 4 is for Station 1 Ports, Port 8 is for Station 2 Ports), and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides controls to enable the various PHY test modes. ***Notes:*** *For bits that reference SerDes modules, refer to Table 12-19 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules. SerDes modules and Lanes marked "**Factory Test Only**" are associated with bits that are RsvdP and not serial EEPROM nor I^2C writable.*				
0	**Port 0, 4, or 8 Timer Test Mode Enable** 0 = Normal PHY Timer parameters are used 1 = Millisecond scale timers in the Port's LTSSM are reduced to microsecond scale	RW	Yes	0
1	**Port 1, 5, or 9 Timer Test Mode Enable** 0 = Normal PHY Timer parameters are used 1 = Millisecond scale timers in the Port's LTSSM are reduced to microsecond scale	RW	Yes	0
2	**Port 6 Timer Test Mode Enable** 0 = Normal PHY Timer parameters are used 1 = Millisecond scale timers in the Port's LTSSM are reduced to microsecond scale	RW	Yes	0
3	***Factory Test Only***	RsvdP	No	0
4	**Skip Timer Test Mode Enable** 0 = Disables Skip Timer Test mode. 1 = Enables Skip Timer Test mode. SKIP Ordered-Sets are transmitted every 256 symbol times, on all Ports, regardless of the **SKIP Ordered-Set Interval** register *SKIP Ordered-Set Interval* field (offset 234h[11:0]) value.	RW	Yes	0
5	**TCB Capture Disable** 0 = Training Control Bit (TCB) Capture is enabled 1 = Disables TCB Capture	RWS	Yes	0
6	**Analog Loopback Enable** 0 = PEX 8624 enters Digital Loopback Slave mode if an external device sends at least two consecutive TS1 Ordered-Sets that have the *Loopback* bit exclusively Set in the TS1 Training Control symbol. The PEX 8624 then loops back data through the Elastic buffer, 8b/10b decoder, and 8b/10b encoder. 1 = PEX 8624 enters Analog Loopback Slave mode if an external device sends at least two consecutive TS1 Ordered-Sets that have the *Loopback* bit exclusively Set in the TS1 Training Control symbol. The PEX 8624 then loops back the symbol stream from the 10-bit Receive interface (before the Elastic buffer) to the 10-bit Transmit interface.	RWS	Yes	0
7	***Factory Test Only***	RsvdP	No	0
15:8	***Factory Test Only***	RW	Yes	00h

Register 12-74. 228h Physical Layer Test (Only Ports 0, 4, and 8 (Port 0 is for Station 0 Ports, Port 4 is for Station 1 Ports, Port 8 is for Station 2 Ports), and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
16	**SerDes Quad 0 PRBS Enable** 0 = Disables PRBS sequence generation/checking on SerDes[0-3]/[32-35], by Station. 1 = Enables PRBS sequence generation/checking on SerDes[0-3]/[32-35], by Station. The corresponding SerDes quad will transmit the PRBS 7 data pattern. ***Notes: Bits [19:16 and 31:28] (SerDes Quad x PRBS Enable and User Test Pattern Enable, respectively) are mutually exclusive functions and must not be enabled together for the same SerDes quad. In each Station register (Ports 0, 4, and 8), the logical result of bits [19:16] ANDed with bits [31:28] must be 0000b.*** ***PRBS transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the corresponding Port's Port Control register Port x Quiet bit (Ports 0, 4, and 8, offset 234h[22:20]) is Set.***	RW	Yes	0
17	**SerDes Quad 1 PRBS Enable** 0 = Disables PRBS sequence generation/checking on SerDes[4-7]/[36-39], by Station. 1 = Enables PRBS sequence generation/checking on SerDes[4-7]/[36-39], by Station. The corresponding SerDes quad will transmit the PRBS 7 data pattern. ***Notes: Bits [19:16 and 31:28] (SerDes Quad x PRBS Enable and User Test Pattern Enable, respectively) are mutually exclusive functions and must not be enabled together for the same SerDes quad. In each Station register (Ports 0, 4, and 8), the logical result of bits [19:16] ANDed with bits [31:28] must be 0000b.*** ***PRBS transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the corresponding Port's Port Control register Port x Quiet bit (Ports 0, 4, and 8, offset 234h[22:20]) is Set.***	RW	Yes	0

Register 12-74. 228h Physical Layer Test (Only Ports 0, 4, and 8 (Port 0 is for Station 0 Ports, Port 4 is for Station 1 Ports, Port 8 is for Station 2 Ports), and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
18	**SerDes Quad 2 PRBS Enable** The Port 0 bit is ***Factory Test Only***. 0 = Disables PRBS sequence generation/checking on SerDes[24-27], by Station. 1 = Enables PRBS sequence generation/checking on SerDes[24-27], by Station. The corresponding SerDes quad will transmit the PRBS 7 data pattern. ***Notes: Bits [19:16 and 31:28] (SerDes Quad x PRBS Enable and User Test Pattern Enable, respectively) are mutually exclusive functions and must not be enabled together for the same SerDes quad. In each Station register (Ports 0, 4, and 8), the logical result of bits [19:16] ANDed with bits [31:28] must be 0000b.*** ***PRBS transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the corresponding Port's Port Control register Port x Quiet bit (Ports 0, 4, and 8, offset 234h[22:20]) is Set.***	RW	Yes	0
19	**SerDes Quad 3 PRBS Enable** The Port 0 bit is ***Factory Test Only***. 0 = Disables PRBS sequence generation/checking on SerDes[28-31], by Station. 1 = Enables PRBS sequence generation/checking on SerDes[28-31], by Station. The corresponding SerDes quad will transmit the PRBS 7 data pattern. ***Notes: Bits [19:16 and 31:28] (SerDes Quad x PRBS Enable and User Test Pattern Enable, respectively) are mutually exclusive functions and must not be enabled together for the same SerDes quad. In each Station register (Ports 0, 4, and 8), the logical result of bits [19:16] ANDed with bits [31:28] must be 0000b.*** ***PRBS transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the corresponding Port's Port Control register Port x Quiet bit (Ports 0, 4, and 8, offset 234h[22:20]) is Set.***	RW	Yes	0

Register 12-74. 228h Physical Layer Test (Only Ports 0, 4, and 8 (Port 0 is for Station 0 Ports, Port 4 is for Station 1 Ports, Port 8 is for Station 2 Ports), and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
20	**SerDes Quad 0 Serial Loopback Path Enable** Serial *Loopback* Path enable for Lanes[0-3]/[32-35], by Station. 1 = Corresponding SerDes quad enables the Serial *Loopback* (Master) path, regardless of the LTSSM state	RW	Yes	0
21	**SerDes Quad 1 Serial Loopback Path Enable** Serial *Loopback* Path enable for SerDes[4-7]/[36-39], by Station. 1 = Corresponding SerDes quad enables the Serial *Loopback* (Master) path, regardless of the LTSSM state	RW	Yes	0
22	**SerDes Quad 2 Serial Loopback Path Enable** Serial *Loopback* Path enable for SerDes[24-27], by Station. The Port 0 bit is ***Factory Test Only***. 1 = Corresponding SerDes quad enables the Serial *Loopback* (Master) path, regardless of the LTSSM state	RW	Yes	0
23	**SerDes Quad 3 Serial Loopback Path Enable** Serial *Loopback* Path enable for SerDes[28-31], by Station. The Port 0 bit is ***Factory Test Only***. 1 = Corresponding SerDes quad enables the Serial *Loopback* (Master) path, regardless of the LTSSM state	RW	Yes	0
24	**SerDes Quad 0 Parallel Loopback Path Enable** Parallel *Loopback* Path enable for SerDes[0-3]/[32-35], by Station. 1 = SerDes Quad 0 enables the Parallel *Loopback* (Slave) path, regardless of the LTSSM state. If bit 4 (*Skip Timer Test Mode Enable*) is Set, the *Loopback* path is located before the Elastic buffer. Otherwise, the *Loopback* path is located after the 8b/10b decoder.	RW	Yes	0
25	**SerDes Quad 1 Parallel Loopback Path Enable** Parallel *Loopback* Path enable for SerDes[4-7]/[36-39], by Station. 1 = SerDes Quad 1 enables the Parallel *Loopback* (Slave) path, regardless of the LTSSM state. If bit 4 (*Skip Timer Test Mode Enable*) is Set, the *Loopback* path is located before the Elastic buffer. Otherwise, the *Loopback* path is located after the 8b/10b decoder.	RW	Yes	0
26	**SerDes Quad 2 Parallel Loopback Path Enable** Parallel *Loopback* Path enable for SerDes[24-27], by Station. The Port 0 bit is ***Factory Test Only***. 1 = SerDes Quad 2 enables the Parallel *Loopback* (Slave) path, regardless of the LTSSM state. If bit 4 (*Skip Timer Test Mode Enable*) is Set, the *Loopback* path is located before the Elastic buffer. Otherwise, the *Loopback* path is located after the 8b/10b decoder.	RW	Yes	0
27	**SerDes Quad 3 Parallel Loopback Path Enable** Parallel *Loopback* Path enable for SerDes[28-31], by Station. The Port 0 bit is ***Factory Test Only***. 1 = SerDes Quad 3 enables the Parallel *Loopback* (Slave) path, regardless of the LTSSM state. If bit 4 (*Skip Timer Test Mode Enable*) is Set, the *Loopback* path is located before the Elastic buffer. Otherwise, the *Loopback* path is located after the 8b/10b decoder.	RW	Yes	0

Register 12-74. 228h Physical Layer Test (Only Ports 0, 4, and 8 (Port 0 is for Station 0 Ports, Port 4 is for Station 1 Ports, Port 8 is for Station 2 Ports), and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
28	**SerDes Quad 0 User Test Pattern Enable** User Test Pattern enable for SerDes[0-3]/[32-35], by Station. 0 = Disables transmission of the 128-bit test pattern 1 = Enables transmission of the 128-bit test pattern (**Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 210h through 21Ch)) on SerDes[0-3]/[32-35] in Digital Far-End Loopback Master mode ***Notes: Bits [31:28 and 19:16] (SerDes Quad x User Test Pattern Enable and PRBS Enable, respectively) are mutually exclusive functions and must not be enabled together for the same SerDes quad. In each Station register (Ports 0, 4, and 8), the logical result of bits [31:28] ANDed with bits [19:16] must be 0000b.*** ***UTP transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the corresponding Port's Port Control register Port x Quiet bit (Ports 0, 4, and 8, offset 234h[22:20]) is Set.***	RW	Yes	0
29	**SerDes Quad 1 User Test Pattern Enable** User Test Pattern enable for SerDes[4-7]/[36-39], by Station. 0 = Disables transmission of the 128-bit test pattern 1 = Enables transmission of the 128-bit test pattern (**Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 210h through 21Ch)) on SerDes[4-7]/[36-39] in Digital Far-End Loopback Master mode ***Notes: Bits [31:28 and 19:16] (SerDes Quad x User Test Pattern Enable and PRBS Enable, respectively) are mutually exclusive functions and must not be enabled together for the same SerDes quad. In each Station register (Ports 0, 4, and 8), the logical result of bits [31:28] ANDed with bits [19:16] must be 0000b.*** ***UTP transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the corresponding Port's Port Control register Port x Quiet bit (Ports 0, 4, and 8, offset 234h[22:20]) is Set.***	RW	Yes	0

Register 12-74. 228h Physical Layer Test (Only Ports 0, 4, and 8 (Port 0 is for Station 0 Ports, Port 4 is for Station 1 Ports, Port 8 is for Station 2 Ports), and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
30	**SerDes Quad 2 User Test Pattern Enable** User Test Pattern enable for SerDes[24-27], by Station. The Port 0 bit is ***Factory Test Only***. 0 = Disables transmission of the 128-bit test pattern 1 = Enables transmission of the 128-bit test pattern (**Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 210h through 21Ch)) on SerDes[24-27] in Digital Far-End Loopback Master mode ***Notes: Bits [31:28 and 19:16] (SerDes Quad x User Test Pattern Enable and PRBS Enable, respectively) are mutually exclusive functions and must not be enabled together for the same SerDes quad. In each Station register (Ports 0, 4, and 8), the logical result of bits [31:28] ANDed with bits [19:16] must be 0000b.*** ***UTP transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the corresponding Port's Port Control register Port x Quiet bit (Ports 0, 4, and 8, offset 234h[22:20]) is Set.***	RW	Yes	0
31	**SerDes Quad 3 User Test Pattern Enable** User Test Pattern enable for SerDes[28-31], by Station. The Port 0 bit is ***Factory Test Only***. 0 = Disables transmission of the 128-bit test pattern 1 = Enables transmission of the 128-bit test pattern (**Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 210h through 21Ch)) on SerDes[28-31] in Digital Far-End Loopback Master mode ***Notes: Bits [31:28 and 19:16] (SerDes Quad x User Test Pattern Enable and PRBS Enable, respectively) are mutually exclusive functions and must not be enabled together for the same SerDes quad. In each Station register (Ports 0, 4, and 8), the logical result of bits [31:28] ANDed with bits [19:16] must be 0000b.*** ***UTP transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the corresponding Port's Port Control register Port x Quiet bit (Ports 0, 4, and 8, offset 234h[22:20]) is Set.***	RW	Yes	0

Register 12-75. 230h Physical Layer Port Command (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides the Loopback, Scrambler Disable, and Compliance Receive commands, and Ready as Loopback Master status, for each Port. ***Note:*** *The Port bit controls individual Ports within each Station, as defined in Table 12-21.* ***Factory Test Only*** *bits are RsvdP and not serial EEPROM nor I^2C writable.*				
0	**Port 0, 4, or 8 Loopback Command** The Port 4 bit is ***Factory Test Only***. 0 = Port 0 or 8 is not enabled to go to the *Loopback* Master state. 1 = Port 0 or 8 attempts to enter the *Loopback* state as a Loopback Master. If this bit is Set before the *Configuration* state is reached, the *Configuration.Linkwidth.Start* to *Loopback* path is used. If this bit is Set later, the *Recovery.Idle* to *Loopback* path is used.	RW	Yes	0
1	**Port 0, 4, or 8 Scrambler Disable Command** The Port 4 bit is ***Factory Test Only***. When Set, unconditionally disables the data scramblers on the corresponding Port's Lanes, and causes the *Disable Scrambling* Training Control Bit to be Set in the transmitted Training Sets. There is one bit for each Port in the associated Station. If a serial EEPROM load Sets this bit, the scrambler is disabled in a *Configuration.Complete* state. If software Sets this bit when the Link is in the Up state, hardware immediately disables its scrambler without executing the Link Training protocol. The upstream/downstream device scrambler will not be disabled. 0 = Port 0 or 8 scrambler is enabled 1 = Port 0 or 8 scrambler is disabled	RW	Yes	0
2	**Port 0, 4, or 8 Compliance Receive Command** The Port 4 bit is ***Factory Test Only***. 0 = When the Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is de-asserted 1 = When the Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered Sets is asserted	RW	Yes	0
3	**Port 0, 4, or 8 Ready as Loopback Master** Link Training and Status State Machine (LTSSM) established Loopback as a Master for the corresponding PEX 8624 Port. The Port 4 bit is ***Factory Test Only***. 0 = Port 0 or 8 is not in Loopback Master mode. 1 = Indicates that Port 0 or 8 has successfully transitioned to the *Loopback.Active* state as a Loopback Master. The LTSSM remains in this state, until bit 0 (*Port 0, 4, or 8 Loopback Command*) is Cleared. This bit is Cleared when the PEX 8624 exits the *Loopback.Active* state.	RO	No	0

Register 12-75. 230h Physical Layer Port Command (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**Port 1, 5, or 9 Loopback Command** 0 = Port 1, 5, or 9 is not enabled to go to the *Loopback* Master state. 1 = Port 1, 5, or 9 attempts to enter the *Loopback* state as a Loopback Master. If this bit is Set before the *Configuration* state is reached, the *Configuration.Linkwidth.Start* to *Loopback* path is used. If this bit is Set later, the *Recovery.Idle* to *Loopback* path is used.	RW	Yes	0
5	**Port 1, 5, or 9 Scrambler Disable Command** When Set, unconditionally disables the data scramblers on the corresponding Port's Lanes, and causes the *Disable Scrambling* Training Control Bit to be Set in the transmitted Training Sets. There is one bit for each Port in the associated Station. If a serial EEPROM load Sets this bit, the scrambler is disabled in a *Configuration.Complete* state. If software Sets this bit when the Link is in the Up state, hardware immediately disables its scrambler without executing the Link Training protocol. The upstream/downstream device scrambler will not be disabled. 0 = Port 1, 5, or 9 scrambler is enabled 1 = Port 1, 5, or 9 scrambler is disabled	RW	Yes	0
6	**Port 1, 5, or 9 Compliance Receive Command** 0 = When the Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is de-asserted 1 = When the Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered Sets is asserted	RW	Yes	0
7	**Port 1, 5, or 9 Ready as Loopback Master** LTSSM established Loopback as a Master for the corresponding PEX 8624 Port. 0 = Port 1, 5, or 9 is not in Loopback Master mode. 1 = Indicates that Port 1, 5, or 9 has successfully transitioned to the *Loopback.Active* state as a Loopback Master. The LTSSM remains in this state, until bit 4 (*Port 1, 5, or 9 Loopback Command*) is Cleared. This bit is Cleared when the PEX 8624 exits the *Loopback.Active* state.	RO	No	0

Register 12-75. 230h Physical Layer Port Command (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**Port 6 Loopback Command** 0 = Port 6 is not enabled to go to the *Loopback* Master state. 1 = Port 6 attempts to enter the *Loopback* state as a Loopback Master. If this bit is Set before the *Configuration* state is reached, the *Configuration.Linkwidth.Start* to *Loopback* path is used. If this bit is Set later, the *Recovery.Idle* to *Loopback* path is used.	RW	Yes	0
9	**Port 6 Scrambler Disable Command** When Set, unconditionally disables the data scramblers on the corresponding Port's Lanes, and causes the *Disable Scrambling* Training Control Bit to be Set in the transmitted Training Sets. There is one bit for each Port in the associated Station. If a serial EEPROM load Sets this bit, the scrambler is disabled in a *Configuration.Complete* state. If software Sets this bit when the Link is in the Up state, hardware immediately disables its scrambler without executing the Link Training protocol. The upstream/downstream device scrambler will not be disabled. 0 = Port 6 scrambler is enabled 1 = Port 6 scrambler is disabled	RW	Yes	0
10	**Port 6 Compliance Receive Command** 0 = When the Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is de-asserted 1 = When the Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered Sets is asserted	RW	Yes	0
11	**Port 6 Ready as Loopback Master** LTSSM established Loopback as a Master for the corresponding PEX 8624 Port. 0 = Port 6 is not in Loopback Master mode. 1 = Indicates that Port 6 has successfully transitioned to the *Loopback.Active* state as a Loopback Master. The LTSSM remains in this state, until bit 8 (*Port 6 Loopback Command*) is Cleared. This bit is Cleared when the PEX 8624 exits the *Loopback.Active* state.	RO	No	0
15:12	***Factory Test Only***	RsvdP	No	0h
31:16	***Reserved***	RsvdP	No	0000h

Table 12-21. Port Bit to Port Control Relationship, by Station, for Register Offset 230h

Bit(s)	Station 0 Port 0 Bit Controls Port	Station 1 Port 4 Bit Controls Port	Station 2 Port 8 Bit Controls Port
3:0	0	***Factory Test Only***	8
7:4	1	5	9
11:8	***Factory Test Only***	6	***Factory Test Only***

Register 12-76. 234h SKIP Ordered-Set Interval and Port Control (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
SKIP Ordered-Set Interval				
This register is used to adjust the distance between SKIP Ordered-Sets.				
11:0	**SKIP Ordered-Set Interval** Specifies the SKIP Ordered-Set interval (in symbol times). When a value of 000h is written, SKIP Ordered-Set transmission is disabled. 000h = SKIP Ordered-Set transmission is disabled 49Ch = Minimum interval (1,180 symbol times) 602h = Maximum interval (1,538 symbol times) ***Note:*** *A high value (such as FFFh) can cause the Link to fail.*	RWS	Yes	49Ch
15:12	***Reserved***	RsvdP	No	0h

Register 12-76. 234h SKIP Ordered-Set Interval and Port Control (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Port Control				
This register is used to disable or enable the LTSSM within individual Ports. The Port Control bits are intended to be used in lieu of placing the Port into the *Loopback.Active* state as a Loopback Master. These bits enable the test patterns to be transmitted, with or without a device attached at the far end. The recommended usage is as follows: **1.** Set the Port's *Disable Port x* and *Port x Quiet* bits (bits [18:16 and 22:20], respectively). • Setting the Port's *Disable Port x* bit forces the Port into the *Detect.Quiet* state. If no device is attached, it is not necessary to Set the Port's *Disable Port x* bit. • If 5.0 GT/s is needed, also Set the Port's *Test Pattern x Rate* bit (bits [27:24]). **2.** If Set, Clear the Port's *Disable Port x* bit. **3.** Load the UTP registers and enable UTP transmission, or just enable PRBS transmission. ***Note:*** *The Port bit controls individual Ports within each Station, as defined in Table 12-22.* ***Factory Test Only*** *bits are RsvdP and not serial EEPROM nor I²C writable.*				
16	**Disable Port 0, 4, or 8** When Set, unconditionally disables the corresponding Port. This is different from the Link Training and Status State Machine (LTSSM) *Disabled* state, in that the Port does not attempt to enter this state. If the Port is idle, it ceases attempting to detect a Receiver. If the Port is up, it immediately returns to the *Detect.Quiet* state and remains there. No Electrical Idle Ordered-Set (EIOS) is sent, which could force any connected device to the *Recovery* state, and then to the LTSSM *Detect* state. The Port remains disabled until its *Disable Port x* bit is Cleared. While the Port is disabled, the SerDes that belong to the disabled Port are placed into the L1 Link PM state. The Port 4 bit is ***Factory Test Only***. ***Note:*** *Because Port 4 is configured, but not used, Set Port 4, bit 16.* 0 = Enables Link Training operation on the corresponding Port 1 = LTSSM remains in the *Detect.Quiet* state on the corresponding Port if it is currently in, or returns to, that state	RWS	Yes	0
17	**Disable Port 1, 5, or 9** When Set, unconditionally disables the corresponding Port. This is different from the LTSSM *Disabled* state, in that the Port does not attempt to enter this state. If the Port is idle, it ceases attempting to detect a Receiver. If the Port is up, it immediately returns to the *Detect.Quiet* state and remains there. No Electrical Idle Ordered-Set is sent, which could force any connected device to the *Recovery* state, and then to the LTSSM *Detect* state. The Port remains disabled until its *Disable Port x* bit is Cleared. While the Port is disabled, the SerDes that belong to the disabled Port are placed into the L1 Link PM state. 0 = Enables Link Training operation on the corresponding Port 1 = LTSSM remains in the *Detect.Quiet* state on the corresponding Port if it is currently in, or returns to, that state	RWS	Yes	0

Register 12-76. 234h SKIP Ordered-Set Interval and Port Control (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
18	**Disable Port 6** When Set, unconditionally disables the corresponding Port. This is different from the LTSSM *Disabled* state, in that the Port does not attempt to enter this state. If the Port is idle, it ceases attempting to detect a Receiver. If the Port is up, it immediately returns to the *Detect.Quiet* state and remains there. No Electrical Idle Ordered-Set is sent, which could force any connected device to the *Recovery* state, and then to the LTSSM *Detect* state. The Port remains disabled until its *Disable Port x* bit is Cleared. While the Port is disabled, the SerDes that belong to the disabled Port are placed into the L1 Link PM state. 0 = Enables Link Training operation on the corresponding Port 1 = LTSSM remains in the *Detect.Quiet* state on the corresponding Port if it is currently in, or returns to, that state	RWS	Yes	0
19	***Factory Test Only***	RsvdP	No	0
20	**Port 0, 4, or 8 Quiet** Unlike bit 16 (*Disable Port 0, 4, or 8*), this bit does not force the LTSSM into the *Detect.Quiet* state. Once in the *Detect.Quiet* state, Receiver termination is enabled and the Transmitters are placed in the L0 Link PM state. This Port can now transmit test patterns (PRBS or UTP), with or without an attached device and without being in the *Loopback.Active* state. The Port 4 bit is ***Factory Test Only***. 0 = No effect on the LTSSM. 1 = Port 0, 4, or 8 remains in the *Detect.Quiet* state once it returns there. This bit does not make the LTSSM exit its current state. Receiver termination remains active, and the Transmitters are placed into the L0 Link PM state (ready to transmit data) when the *Detect.Quiet* state is reached. ***Note:*** *Use this bit when it is necessary to transmit some data pattern, without first entering the Loopback.Active state as a Loopback Master.*	RWS	Yes	0
21	**Port 1, 5, or 9 Quiet** Unlike bit 17 (*Disable Port 1, 5, or 9*), this bit does not force the LTSSM into the *Detect.Quiet* state. Once in the *Detect.Quiet* state, Receiver termination is enabled and the Transmitters are placed in the L0 Link PM state. This Port can now transmit test patterns (PRBS or UTP), with or without an attached device and without being in the *Loopback.Active* state. 0 = No effect on the LTSSM. 1 = Port 1, 5, or 9 remains in the *Detect.Quiet* state once it returns there. This bit does not make the LTSSM exit its current state. Receiver termination remains active, and the Transmitters are placed into the L0 Link PM state (ready to transmit data) when the *Detect.Quiet* state is reached. ***Note:*** *Use this bit when it is necessary to transmit some data pattern, without first entering the Loopback.Active state as a Loopback Master.*	RWS	Yes	0

Register 12-76. 234h SKIP Ordered-Set Interval and Port Control (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
22	**Port 6 Quiet** Unlike bit 18 (*Disable Port 6*), this bit does not force the LTSSM into the *Detect.Quiet* state. Once in the *Detect.Quiet* state, Receiver termination is enabled and the Transmitters are placed in the L0 Link PM state. This Port can now transmit test patterns (PRBS or UTP), with or without an attached device and without being in the *Loopback.Active* state. 0 = No effect on the LTSSM. 1 = Port 6 remains in the *Detect.Quiet* state once it returns there. This bit does not make the LTSSM exit its current state. Receiver termination remains active, and the Transmitters are placed into the L0 Link PM state (ready to transmit data) when the *Detect.Quiet* state is reached. ***Note:*** *Use this bit when it is necessary to transmit some data pattern, without first entering the Loopback.Active state as a Loopback Master.*	RWS	Yes	0
23	***Factory Test Only***	RsvdP	No	0
27:24	**Test Pattern *x* Rate** The corresponding Port transmits the selected test pattern (PRBS or UTP), at 5.0 GT/s, if the Port's *Port x Quiet* bit (bits [22:20]), is also Set. Bit 24 controls Test Pattern 0. Bit 25 controls Test Pattern 4. Bit 26 controls Test Pattern 8. Bit 27 controls Test Pattern 12.	RWS	Yes	0h
31:28	***Reserved***	RsvdP	No	0h

Table 12-22. Port Bit to Port Control Relationship, by Station, for Register Offset 234h

Bit(s)	Station 0 Port 0 Bit Controls Port	Station 1 Port 4 Bit Controls Port	Station 2 Port 8 Bit Controls Port
16	0	***Factory Test Only***	8
17	1	5	9
18	***Factory Test Only***	6	***Factory Test Only***
20	0	***Factory Test Only***	8
21	1	5	9
22	***Factory Test Only***	6	***Factory Test Only***
27:24	0	4	8

Register 12-77. 238h SerDes Quad 0 Diagnostic Data (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
There are four **SerDes Quad *x* Diagnostic Data** (Diagnostic Data) registers, one for each SerDes quad, at offsets 238h through 244h, in each Station. The contents of the Diagnostic Data registers reflect the performance of the SerDes that are selected by the registers' *SerDes Diagnostic Data Select* bits (field [25:24]). *For example*, if offset 23Ch[25:24] is programmed to 01b, then the information in that Diagnostic Data register is for SerDes 1 of Quad 1 of that Station (SerDes 5 or 37 in Stations 0 and 2, respectively; the Station 1 bits for that particular SerDes quad and SerDes are ***Factory Test Only***). This register is used to retrieve Diagnostic Test results for SerDes[0-3]/[32-35]. ***Note:*** *Refer to Table 12-23 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules and Lanes. SerDes modules and Lanes marked "**Factory Test Only**" are associated with bits that are RsvdP and not serial EEPROM nor I^2C writable.*				
7:0	**UTP Expected Data** When User Test Pattern (UTP) is enabled, if an error is detected in the received UTP data, this field returns the expected data.	RO	No	00h
15:8	**UTP Actual Data** When UTP is enabled, if an error is detected in the received UTP data, this field returns the actual data that was received.	RO	No	00h
23:16	**UTP/PRBS Error Counter** Receiver Detected flags. Returns the number of errors detected by the UTP (bit 30 is Cleared) or PRBS (bit 30 is Set) Data Checkers. The Error Counter saturates at 255, and is Cleared when UTP/PRBS is disabled. **UTP Mode** To Clear the Counter, disable UTP mode by Clearing the **Physical Layer Test** register *SerDes Quad 0 User Test Pattern Enable* bit (offset 228h[28]). **PRBS Mode** To Clear the Counter, disable PRBS mode by Clearing the **Physical Layer Test** register *SerDes Quad 0 PRBS Enable* bit (offset 228h[16]).	RO	No	00h
25:24	**SerDes Diagnostic Data Select** Used to select the SerDes (SerDes[0-3]/[32-35]) to which the diagnostic data in this SerDes quad pertains. Status selection code for the fields representing RO bits [23:0] of this register. The binary code represents a status selection for one of the SerDes Quad 0 Lanes. The test results for physical device Lanes [0-3]/[32-35] are selected with corresponding binary codes from 0-3. ***Note:*** *To obtain diagnostic data on all SerDes in the quad, run a test, then cycle these bits.*	RW	Yes	00b
29:26	***Reserved***	RO	No	0h
30	**PRBS Counter/-UTP Counter** 0 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the UTP Error Counter (diagnostic data is from the UTP Data Checkers) 1 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the PRBS Error Counter (diagnostic data is from the PRBS Data Checkers)	RO	No	0
31	***Reserved***	RsvdP	No	0

Register 12-78. 23Ch SerDes Quad 1 Diagnostic Data (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
There are four **SerDes Quad *x* Diagnostic Data** (Diagnostic Data) registers, one for each SerDes quad, at offsets 238h through 244h, in each Station. The contents of the Diagnostic Data registers reflect the performance of the SerDes that are selected by the registers' *SerDes Diagnostic Data Select* bits (field [25:24]). *For example*, if field [25:24] of this register is programmed to 01b, then the information in that Diagnostic Data register is for SerDes 1 of Quad 1 of that Station (SerDes 5 or 37 in Stations 0 and 2, respectively; the Station 1 bits for that particular SerDes quad and SerDes are ***Factory Test Only***). This register is used to retrieve Diagnostic Test results for SerDes[4-7]/[36-39]. ***Note:*** *Refer to Table 12-23 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules and Lanes. SerDes modules and Lanes marked "**Factory Test Only**" are associated with bits that are RsvdP and not serial EEPROM nor I^2C writable.*				
7:0	**UTP Expected Data** When User Test Pattern (UTP) is enabled, if an error is detected in the Received UTP data, this field returns the expected data.	RO	No	00h
15:8	**UTP Actual Data** When UTP is enabled, if an error is detected in the Received UTP data, this field returns the actual data that was received.	RO	No	00h
23:16	**UTP/PRBS Error Counter** Receiver Detected flags. Returns the number of errors detected by the UTP (bit 30 is Cleared) or PRBS (bit 30 is Set) Data Checkers. The Error Counter saturates at 255, and is Cleared when UTP/PRBS is disabled. **UTP Mode** To Clear the Counter, disable UTP mode by Clearing the **Physical Layer Test** register *SerDes Quad 1 User Test Pattern Enable* bit (offset 228h[29]). **PRBS Mode** To Clear the Counter, disable PRBS mode by Clearing the **Physical Layer Test** register *SerDes Quad 1 PRBS Enable* bit (offset 228h[17]).	RO	No	00h
25:24	**SerDes Diagnostic Data Select** Used to select the SerDes (SerDes[4-7]/[36-39]) to which the diagnostic data in this SerDes quad pertains. Status selection code for the fields representing RO bits [23:0] of this register. The binary code represents a status selection for one of the SerDes Quad 1 Lanes. The test results for physical device Lanes [4-7]/[36-39] are selected with corresponding binary codes from 0-3. ***Note:*** *To obtain diagnostic data on all SerDes in the quad, run a test, then cycle these bits.*	RW	Yes	00b
29:26	***Reserved***	RO	No	0h
30	**PRBS Counter/-UTP Counter** 0 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the UTP Error Counter (diagnostic data is from the UTP Data Checkers) 1 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the PRBS Error Counter (diagnostic data is from the PRBS Data Checkers)	RO	No	0
31	***Reserved***	RsvdP	No	0

Register 12-79. 240h SerDes Quad 2 Diagnostic Data (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
There are four **SerDes Quad *x* Diagnostic Data** (Diagnostic Data) registers, one for each SerDes quad, at offsets 238h through 244h, in each Station. The contents of the Diagnostic Data registers reflect the performance of the SerDes that are selected by the registers' *SerDes Diagnostic Data Select* bits (field [25:24]). *For example*, if offset 23Ch[25:24] is programmed to 01b, then the information in that Diagnostic Data register is for SerDes 1 of Quad 1 of that Station (SerDes 5 or 37 in Stations 0 and 2, respectively; the Station 1 bits for that particular SerDes quad and SerDes are ***Factory Test Only***). This register is used to retrieve Diagnostic Test results for SerDes[24-27]. ***Note:*** *Refer to Table 12-23 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules and Lanes. SerDes modules and Lanes marked "**Factory Test Only**" are associated with bits that are RsvdP and not serial EEPROM nor I^2C writable.*				
7:0	**UTP Expected Data** When User Test Pattern (UTP) is enabled, if an error is detected in the Received UTP data, this field returns the expected data.	RO	No	00h
15:8	**UTP Actual Data** When UTP is enabled, if an error is detected in the Received UTP data, this field returns the actual data that was received.	RO	No	00h
23:16	**UTP/PRBS Error Counter** Receiver Detected flags. Returns the number of errors detected by the UTP (bit 30 is Cleared) or PRBS (bit 30 is Set) Data Checkers. The Error Counter saturates at 255, and is Cleared when UTP/PRBS is disabled. **UTP Mode** To Clear the Counter, disable UTP mode by Clearing the **Physical Layer Test** register *SerDes Quad 2 User Test Pattern Enable* bit (offset 228h[30]). **PRBS Mode** To Clear the Counter, disable PRBS mode by Clearing the **Physical Layer Test** register *SerDes Quad 2 PRBS Enable* bit (offset 228h[18]).	RO	No	00h
25:24	**SerDes Diagnostic Data Select** Used to select the SerDes (SerDes[24-27]) to which the diagnostic data in this SerDes quad pertains. Status selection code for the fields representing RO bits [23:0] of this register. The binary code represents a status selection for one of the SerDes Quad 2 Lanes. The test results for physical device Lanes [24-27] are selected with corresponding binary codes from 0-3. ***Note:*** *To obtain diagnostic data on all SerDes in the quad, run a test, then cycle these bits.*	RW	Yes	00b
29:26	***Reserved***	RO	No	0h
30	**PRBS Counter/-UTP Counter** 0 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the UTP Error Counter (diagnostic data is from the UTP Data Checkers) 1 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the PRBS Error Counter (diagnostic data is from the PRBS Data Checkers)	RO	No	0
31	***Reserved***	RsvdP	No	0

Register 12-80. 244h SerDes Quad 3 Diagnostic Data (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
There are four **SerDes Quad *x* Diagnostic Data** (Diagnostic Data) registers, one for each SerDes quad, at offsets 238h through 244h, in each Station. The contents of the Diagnostic Data registers reflect the performance of the SerDes that are selected by the registers' *SerDes Diagnostic Data Select* bits (field [25:24]). *For example*, if offset 23Ch[25:24] is programmed to 01b, then the information in that Diagnostic Data register is for SerDes 1 of Quad 1 of that Station (SerDes 5 or 37 in Stations 0 and 2, respectively; the Station 1 bits for that particular SerDes quad and SerDes are ***Factory Test Only***). This register is used to retrieve Diagnostic Test results for SerDes[28-31]. ***Note:*** *Refer to Table 12-23 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules and Lanes. SerDes modules and Lanes marked "**Factory Test Only**" are associated with bits that are RsvdP and not serial EEPROM nor I²C writable.*				
7:0	**UTP Expected Data** When User Test Pattern (UTP) is enabled, if an error is detected in the Received UTP data, this field returns the expected data.	RO	No	00h
15:8	**UTP Actual Data** When UTP is enabled, if an error is detected in the Received UTP data, this field returns the actual data that was received.	RO	No	00h
23:16	**UTP/PRBS Error Counter** Receiver Detected flags. Returns the number of errors detected by the UTP (bit 30 is Cleared) or PRBS (bit 30 is Set) Data Checkers. The Error Counter saturates at 255, and is Cleared when UTP/PRBS is disabled. **UTP Mode** To Clear the Counter, disable UTP mode by Clearing the **Physical Layer Test** register *SerDes Quad 3 User Test Pattern Enable* bit (offset 228h[31]). **PRBS Mode** To Clear the Counter, disable PRBS mode by Clearing the **Physical Layer Test** register *SerDes Quad 3 PRBS Enable* bit (offset 228h[19]).	RO	No	00h
25:24	**SerDes Diagnostic Data Select** Used to select the SerDes (SerDes[28-31]) to which the diagnostic data in this SerDes quad pertains. Status selection code for the fields representing RO bits [23:0] of this register. The binary code represents a status selection for one of the SerDes Quad 3 Lanes. The test results for physical device Lanes [28-31] are selected with corresponding binary codes from 0-3. ***Note:*** *To obtain diagnostic data on all SerDes in the quad, run a test, then cycle these bits.*	RW	Yes	00b
29:26	***Reserved***	RO	No	0h
30	**PRBS Counter/-UTP Counter** 0 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the UTP Error Counter (diagnostic data is from the UTP Data Checkers) 1 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the PRBS Error Counter (diagnostic data is from the PRBS Data Checkers)	RO	No	0
31	***Reserved***	RsvdP	No	0

Table 12-23. Port/SerDes Module/Station/SerDes Quad Relationship, when All Ports Are Enabled, for Register Offsets 238h through 244h

Port 0, 4, or 8 Register Offset	SerDes Quad	SerDes Modules and Physical Lanes by Port					
		Station 0, Port 0		Station 1, Port 4		Station 2, Port 8	
		Port	SerDes Modules and Physical Lanes	Port	SerDes Modules and Physical Lanes	Port	SerDes Modules and Physical Lanes
238h	0	0	0-3	–	***Factory Test Only***	8	32-35
23Ch	1	1	4-7	–	***Factory Test Only***	9	36-39
240h	2	–	***Factory Test Only***	5	24-27	–	***Factory Test Only***
244h	3	–	***Factory Test Only***	6	28-31	–	***Factory Test Only***

Register 12-81. 248h Port Receiver Error Counter (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: *The Port bit controls individual Ports within each Station, as defined in Table 12-24.* ***Factory Test Only*** *bits are RsvdP and not serial EEPROM nor I^2C writable.*				
7:0	**Port 0, 4, or 8 Receiver Error Counter** When read, returns the number of Receiver errors detected by the corresponding Port. The Error Counter saturates at 255. The Counter is Cleared with any Write to the corresponding byte in this register; otherwise, this field is RO. The Port 4 bit is ***Factory Test Only***.	RW1C	No	00h
15:8	**Port 1, 5, or 9 Receiver Error Counter** When read, returns the number of Receiver errors detected by the corresponding Port. The Error Counter saturates at 255. The Counter is Cleared with any Write to the corresponding byte in this register; otherwise, this field is RO.	RW1C	No	00h
23:16	**Port 6 Receiver Error Counter** When read, returns the number of Receiver errors detected by the corresponding Port. The Error Counter saturates at 255. The Counter is Cleared with any Write to the corresponding byte in this register; otherwise, this field is RO.	RW1C	No	00h
31:24	***Factory Test Only***	RsvdP	No	00h

Table 12-24. Port Bit to Port Control Relationship, by Station, for Register Offset 248h

Bit(s)	Station 0 Port 0 Bit Controls Port	Station 1 Port 4 Bit Controls Port	Station 2 Port 8 Bit Controls Port
7:0	0	***Factory Test Only***	8
15:8	1	5	9
23:16	***Factory Test Only***	6	***Factory Test Only***

Register 12-82. 24Ch Target Link Width (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
This register provides the capability to allow software to cause Link retraining to a wider or narrower width than the current width, *such as* to conserve power when maximum bandwidth is not required. Devices advertise such support, by transmitting the appropriate value for the Data Rate Identifier symbol within TS2 Ordered-Sets. If the *Port x Upconfigure Capability Received* bit is Set (indicating that during the previous Link training, the Port received Upconfigure Capability notification from the connected device), software can cause the Port to either upconfigure the Link to a previously negotiated Link width, or downconfigure the Link to a narrower width, by writing the needed Target Link Width value to this register, followed by Setting the Port's **Link Control** register *Retrain Link* bit (offset 78h[5]). ***Note:*** *The Port bit controls individual Ports within each Station, as defined in Table 12-25.* ***Factory Test Only*** *bits are RsvdP and not serial EEPROM nor I²C writable.*				
4:0	**Port 0, 4, or 8 Target Link Width** The Port 4 bit is ***Factory Test Only***. The initial value of this field is the Port's Negotiated Link Width (offset 78h[25:20]).	RW	No	Set by STRAP_STN*x*_PORTCFG*x* input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station x* bits (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[5:0])
6:5	***Reserved***	RsvdP	No	00b
7	**Port 0, 4, or 8 Upconfigure Capability Received** The Port 4 bit is ***Factory Test Only***. Set during Link training, if the Port received an Upconfigure Capability notification from the connected device.	RO	No	0
11:8	**Port 1, 5, or 9 Target Link Width** The initial value of this field is the Port's Negotiated Link Width (offset 78h[25:20]).	RW	No	Set by STRAP_STN*x*_PORTCFG*x* input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station x* bits (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[5:0])
14:12	***Reserved***	RsvdP	No	000b
15	**Port 1, 5, or 9 Upconfigure Capability Received** Set during Link training, if the Port received an Upconfigure Capability notification from the connected device.	RO	No	0

Register 12-82. 24Ch Target Link Width (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
18:16	**Port 6 Target Link Width** The initial value of this field is the Port's Negotiated Link Width (offset 78h[25:20]).	RW	No	Set by STRAP_STN1_PORTCFG0 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station x* bits (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[5:0])
22:19	***Reserved***	RsvdP	No	0h
23	**Port 6 Upconfigure Capability Received** Set during Link training, if the Port received an Upconfigure Capability notification from the connected device.	RO	No	0
31:24	***Factory Test Only***	RsvdP	No	00h

Table 12-25. Port Bit to Port Control Relationship, by Station, for Register Offset 24Ch

Bit(s)	Station 0 Port 0 Bit Controls Port	Station 1 Port 4 Bit Controls Port	Station 2 Port 8 Bit Controls Port
7:0	0	***Factory Test Only***	8
15:8	1	5	9
23:16	***Factory Test Only***	6	***Factory Test Only***

Register 12-83. 254h Physical Layer Additional Status (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The Port bit controls individual Ports within each Station, as defined in Table 12-26.* ***Factory Test Only*** *bits are RsvdP and not serial EEPROM nor I²C writable.*				
0	**Port 0, 4, or 8 Loopback Master Entry Failed** The Port 4 bit is ***Factory Test Only***. 1 = Indicates that the corresponding Port failed to enter the *Loopback* state as a Loopback Master, and abandoned the attempt by returning the LTSSM to the *Detect* state ***Note:*** *If this bit and the Port 0, 4, or 8 Ready as Loopback Master (offset 230h[3]) are both Set, the Loopback state was entered after the initial failure from the Configuration state.*	RW1C	Yes	0
1	**Port 1, 5, or 9 Loopback Master Entry Failed** 1 = Indicates that the corresponding Port failed to enter the *Loopback* state as a Loopback Master, and abandoned the attempt by returning the LTSSM to the *Detect* state ***Note:*** *If this bit and the Port 1, 5, or 9 Ready as Loopback Master (offset 230h[7]) are both Set, the Loopback state was entered after the initial failure from the Configuration state.*	RW1C	Yes	0
2	**Port 6 Loopback Master Entry Failed** 1 = Indicates that the corresponding Port failed to enter the *Loopback* state as a Loopback Master, and abandoned the attempt by returning the LTSSM to the *Detect* state ***Note:*** *If this bit and the Port 6 Ready as Loopback Master (offset 230h[11]) are both Set, the Loopback state was entered after the initial failure from the Configuration state.*	RW1C	Yes	0
3	***Factory Test Only***	RsvdP	No	0
15:4	***Reserved***	RsvdP	No	000h
16	**Port 0, 4, or 8 External Loopback Enable** The Port 4 bit is ***Factory Test Only***. 1 = Allows the corresponding PEX 8624 Port to reach Link Up status, when receiving its own Training Sets during Link training. It is necessary to Set this bit when a Port's Receivers are directly connected, externally, to its Transmitters.	RW	Yes	0
17	**Port 1, 5, or 9 External Loopback Enable** 1 = Allows the corresponding PEX 8624 Port to reach Link Up status, when receiving its own Training Sets during Link training. It is necessary to Set this bit when a Port's Receivers are directly connected, externally, to its Transmitters.	RW	Yes	0
18	**Port 6 External Loopback Enable** 1 = Allows the corresponding PEX 8624 Port to reach Link Up status, when receiving its own Training Sets during Link training. It is necessary to Set this bit when a Port's Receivers are directly connected, externally, to its Transmitters.	RW	Yes	0
19	***Factory Test Only***	RsvdP	No	0
31:20	***Reserved***	RsvdP	No	000h

Table 12-26. Port Bit to Port Control Relationship, by Station, for Register Offset 254h

Bit(s)	Station 0 Port 0 Bit Controls Port	Station 1 Port 4 Bit Controls Port	Station 2 Port 8 Bit Controls Port
0	0	***Factory Test Only***	8
1	1	5	9
2	***Factory Test Only***	6	***Factory Test Only***
16	0	***Factory Test Only***	8
17	1	5	9
18	***Factory Test Only***	6	***Factory Test Only***

Register 12-84. 258h PRBS Control/Status (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
This register provides Control and Status of the PRBS Generator/Checker logic. ***Note:*** *Refer to Table 12-27 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules and Lanes.* ***Factory Test Only*** *bits are RsvdP and not serial EEPROM nor I²C writable.*				
0	**PRBS Pattern Sync Status Device Lane 0 or 32** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
1	**PRBS Pattern Sync Status Device Lane 1 or 33** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
2	**PRBS Pattern Sync Status Device Lane 2 or 34** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
3	**PRBS Pattern Sync Status Device Lane 3 or 35** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0

Register 12-84. 258h PRBS Control/Status (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**PRBS Pattern Sync Status Device Lane 4 or 36** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
5	**PRBS Pattern Sync Status Device Lane 5 or 37** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
6	**PRBS Pattern Sync Status Device Lane 6 or 38** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
7	**PRBS Pattern Sync Status Device Lane 7 or 39** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
8	**PRBS Pattern Sync Status Device Lane 24** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
9	**PRBS Pattern Sync Status Device Lane 25** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
10	**PRBS Pattern Sync Status Device Lane 26** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
11	**PRBS Pattern Sync Status Device Lane 27** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0

Register 12-84. 258h PRBS Control/Status (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
12	**PRBS Pattern Sync Status Device Lane 28** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
13	**PRBS Pattern Sync Status Device Lane 29** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
14	**PRBS Pattern Sync Status Device Lane 30** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
15	**PRBS Pattern Sync Status Device Lane 31** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
16	**PRBS Pattern Invert Enable** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Causes the PRBS pattern generator, when enabled, to output the one's complement of the PRBS7 sequence	RW	Yes	0
31:17	***Reserved***	RsvdP	No	0-0h

Table 12-27. SerDes Module and Lane Control Relationship, by Station and Port, for Register Offset 258h

Bit(s)	Station 0, Port 0 SerDes Module and Physical Lane	Station 1, Port 4 SerDes Module and Physical Lane	Station 2, Port 8 SerDes Module and Physical Lane
0	0	***Factory Test Only***	32
1	1	***Factory Test Only***	33
2	2	***Factory Test Only***	34
3	3	***Factory Test Only***	35
4	4	***Factory Test Only***	36
5	5	***Factory Test Only***	37
6	6	***Factory Test Only***	38
7	7	***Factory Test Only***	39
8	***Factory Test Only***	24	***Factory Test Only***
9	***Factory Test Only***	25	***Factory Test Only***
10	***Factory Test Only***	26	***Factory Test Only***
11	***Factory Test Only***	27	***Factory Test Only***
12	***Factory Test Only***	28	***Factory Test Only***
13	***Factory Test Only***	29	***Factory Test Only***
14	***Factory Test Only***	30	***Factory Test Only***
15	***Factory Test Only***	31	***Factory Test Only***

12.14.3 Device-Specific Registers – Serial EEPROM (Offsets 260h – 26Ch)

This section details the Device-Specific Serial EEPROM registers. Table 12-28 defines the register map.

Table 12-28. Device-Specific Serial EEPROM Register Map (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Status Data from Serial EEPROM	Serial EEPROM Status	Serial EEPROM Control	260h
Serial EEPROM Buffer			264h
Serial EEPROM Clock Frequency			268h
Expansion ROM Base Address	***Reserved***	Serial EEPROM 3rd Address Byte	26Ch

Register 12-85. 260h Serial EEPROM Status and Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Serial EEPROM Control				
12:0	**EepBlkAddr** Serial EEPROM Block Address for 32 KB.	RW	Yes	000h
15:13	**EepCmd[2:0]** Commands to the Serial EEPROM Controller. 000b = ***Reserved*** 001b = Data from bits [31:24] (**Status Data from Serial EEPROM** register) is written to the serial EEPROM's internal **Status** register 010b = Write four bytes of data from the EepBuf into the memory location pointed to by field [12:0] (*EepBlkAddr*) 011b = Read four bytes of data from the memory location pointed to by field [12:0] (*EepBlkAddr*) into the EepBuf 100b = Reset Write Enable latch 101b = Data from the serial EEPROM's internal **Status** register is written to bits [31:24] (**Status Data from Serial EEPROM** register) 110b = Set Write Enable latch 111b = ***Reserved*** ***Note:*** *For value of 001b, only bits [31, 27:26] can be written into the serial EEPROM's internal* ***Status*** *register.*	RW	Yes	000b

Register 12-85. 260h Serial EEPROM Status and Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Serial EEPROM Status				
17:16	**EepPrsnt[1:0]** Serial EEPROM Present status. 00b = Not present 01b = Serial EEPROM is present – validation signature verified 10b = ***Reserved*** 11b = Serial EEPROM is present – validation signature not verified	RO	No	00b
18	**EepCmdStatus** Serial EEPROM Command status. 0 = Serial EEPROM Command is complete 1 = Serial EEPROM Command is not complete	RO	No	0
19	***Reserved***	RsvdP	No	0
20	**EepBlkAddr Upper Bit** Serial EEPROM Block Address upper bit 13. Extends the serial EEPROM to 64 KB.	RW	Yes	0
21	**EepAddrWidth Override** 0 = Field [23:22] (*EepAddrWidth*) is RO 1 = Field [23:22] (*EepAddrWidth*) is software-writable	RW	Yes	0
23:22	**EepAddrWidth** Serial EEPROM Address width. If the addressing width cannot be determined, 00b is returned. A non-zero value is reported only if the validation signature (5Ah) is successfully read from the first serial EEPROM location. This field is usually RO; however, it is RW if bit 21 (*EepAddrWidth Override*) is Set. 00b = Undetermined 01b = 1 byte 10b = 2 bytes 11b = 3 bytes	RO/RW	No	00b

Register 12-85. 260h Serial EEPROM Status and Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td colspan="5">Status Data from Serial EEPROM[a]</td></tr>
<tr><td>24</td><td>EepRdy
Serial EEPROM RDY#.
0 = Serial EEPROM is ready to transmit data
1 = Write cycle is in-progress</td><td>RW</td><td>Yes</td><td>0</td></tr>
<tr><td>25</td><td>EepWen
Serial EEPROM Write enable.
0 = Serial EEPROM Write is disabled
1 = Serial EEPROM Write is enabled</td><td>RW</td><td>Yes</td><td>0</td></tr>
<tr><td>27:26</td><td>EepBp[1:0]
Serial EEPROM Block-Write Protect bits. Block Protection options protect the top ¼, top ½, or the entire serial EEPROM. PEX 8624 Configuration data is stored in the lower addresses; therefore, when using Block Protection, the entire serial EEPROM should be protected with BP[1:0] programmed to 11b.
<table>
<tr><th rowspan="2">BP[1:0]</th><th rowspan="2">Level</th><th colspan="4">Array Addresses Protected</th></tr>
<tr><th>8-KB Device</th><th>16-KB Device</th><th>32-KB Device</th><th>64-KB Device</th></tr>
<tr><td>00b</td><td>0</td><td>None</td><td>None</td><td>None</td><td>None</td></tr>
<tr><td>01b</td><td>1 (top ¼)</td><td>1800h – 1FFFh</td><td>3000h – 3FFFh</td><td>6000h – 7FFFh</td><td>–</td></tr>
<tr><td>10b</td><td>2 (top ½)</td><td>1000h – 1FFFh</td><td>2000h – 3FFFh</td><td>4000h – 7FFFh</td><td>–</td></tr>
<tr><td>11b</td><td>3 (All)</td><td>0000h – 1FFFh</td><td>0000h – 3FFFh</td><td>0000h – 7FFFh</td><td>–</td></tr>
</table></td><td>RW</td><td>Yes</td><td>00b</td></tr>
</table>

Register 12-85. 260h Serial EEPROM Status and Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
30:28	**EepWrStatus** Serial EEPROM Write status. Value is 000b when the serial EEPROM is not in an internal Write cycle. ***Note:*** *The definition of this field varies among serial EEPROM manufacturers. Reads of the serial EEPROM's internal* ***Status*** *register can return 000b or 111b, depending upon the serial EEPROM that is used.*	RO	No	000b
31	**EepWpen** Serial EEPROM Write Protect enable. Overrides the internal serial EEPROM Write Protect WP# input and enables/disables Writes to the **Serial EEPROM Status** register (bits [23:16] of this register): • When WP#=H or this bit is Cleared, and bit 25 (*EepWen*) is Set, the **Serial EEPROM Status** register is writable • When WP#=L and this bit is Set, or bit 25 (*EepWen*) is Cleared, the **Serial EEPROM Status** register is write-protected ***Notes:*** *If the internal serial EEPROM Write Protect WP# input is Low, after software Sets the EepWen bit to write-protect the* ***Serial EEPROM Status*** *register, the EepWen value cannot be Cleared, nor can the EepBp[1:0] field be Cleared to disable Block Protection, until the WP# input is High.* *This bit is* ***not*** *implemented in certain serial EEPROMs. Refer to the serial EEPROM manufacturer's data sheet.*	RW	Yes	0

a. Within the serial EEPROM's internal ***Status*** *register, only bits [31, 27:26] can be written.*

Register 12-86. 264h Serial EEPROM Buffer (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**EepBuf** Serial EEPROM RW buffer. Read/Write command to the **Serial EEPROM Control** register (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 260h) results in a 4-byte Read/Write from/to the serial EEPROM device.	RW	Yes	0000_0000h

Register 12-87. 268h Serial EEPROM Clock Frequency (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
2:0	**EepFreq[2:0]** Serial EEPROM clock (EE_SK) frequency control. 000b = 1 MHz (default) 001b = 1.98 MHz 010b = 5 MHz 011b = 9.62 MHz 100b = 12.5 MHz 101b = 15.6 MHz 110b = 17.86 MHz 111b = ***Reserved***	RW	Yes	000b
7:3	***Reserved***	RsvdP	No	0-0h
10:8	**EepCsStHld[2:0]** CS to SCLK setup and hold timing, provided as a number of ½ EE_SK Clock cycles. 000b = Use default timing for EE_CS# setup and EE_CS# hold timing to the serial EEPROM, for EE_CS# active to EE_SK active delay, and EE_SK inactive to EE_CS# inactive delay, respectively 001b = Non-zero value adds that number of ½ EE_SK clocks delay to the default setup and hold timing, between EE_CS# active and EE_SK active, and between EE_SK inactive and EE_CS# inactive	RW	Yes	000b
15:11	***Reserved***	RsvdP	No	0-0h
16	**Expansion ROM Size** 0 = 16 KB 1 = 32 KB	RW	Yes	0
31:17	***Reserved***	RsvdP	No	0-0h

Register 12-88. 26Ch Serial EEPROM 3rd Address Byte (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Serial EEPROM 3rd Address Byte**	RW	Yes	00h
15:8	***Reserved***	RsvdP	No	00h
31:16	**Expansion ROM Base Address** Indicates the NT Port Expansion ROM Base address within the serial EEPROM. The value is dependent upon the **Serial EEPROM Clock Frequency** register *Expansion ROM Size* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 268h[16]) value. The lower six bits, [21:16], map to serial EEPROM byte Address bits [15:10] (aligned to a 256-DWord (1-KB) boundary). The NT Port Expansion ROM must not straddle a 64-KB boundary within the serial EEPROM. 0020h = Default Base address in serial EEPROM for a 16-KB NT Port Expansion ROM (*Expansion ROM Size* bit is Cleared) is 2000h (8 KB). The serial EEPROM size must be at least 32 KB. 0040h = Default Base address in serial EEPROM for a 32-KB NT Port Expansion ROM (*Expansion ROM Size* bit is Set) is 4000h (16 KB). The serial EEPROM size must be at least 64 KB.	RW	Yes	0020h

12.14.4 Device-Specific Registers – Physical Layer (Offsets 270h – 28Ch)

This section details the Device-Specific PHY registers located at offsets 270h through 28Ch. Table 12-29 defines the register map.

Other Device-Specific PHY registers are detailed in Section 12.14.2, "Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)."

Table 12-29. Device-Specific Physical Layer Register Map (Offsets 270h – 28Ch)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved	***Factory Test Only***	Station 2 Software Lane Status	270h
Station 0/1 Lane Enable		274h
Reserved	***Factory Test Only***	Station 2 Lane Enable	278h
Factory Test Only		27Ch – 28Ch

Register 12-89. 270h Station 2 Software Lane Status (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Lane 32 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
1	**Lane 33 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
2	**Lane 34 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
3	**Lane 35 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
4	**Lane 36 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
5	**Lane 37 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
6	**Lane 38 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
7	**Lane 39 Up Status** 0 = Lane is down 1 = Lane is up	RO	No	1
15:8	***Factory Test Only***	RsvdP	No	00h
31:16	***Reserved***	RsvdP	No	0000h

Register 12-90. 274h Station 0/1 Lane Enable (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**Lane 0 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
1	**Lane 1 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
2	**Lane 2 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
3	**Lane 3 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
4	**Lane 4 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
5	**Lane 5 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
6	**Lane 6 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
7	**Lane 7 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
23:8	***Factory Test Only***	RsvdP	No	0000h

Register 12-90. 274h Station 0/1 Lane Enable (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
24	**Lane 24 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
25	**Lane 25 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
26	**Lane 26 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
27	**Lane 27 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
28	**Lane 28 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
29	**Lane 29 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
30	**Lane 30 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
31	**Lane 31 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1

Register 12-91. 278h Station 2 Lane Enable (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**Lane 32 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
1	**Lane 33 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
2	**Lane 34 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
3	**Lane 35 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
4	**Lane 36 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
5	**Lane 37 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
6	**Lane 38 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
7	**Lane 39 Lane Enable** 0 = Disables Lane 1 = Enables Lane	RWS	Yes	1
15:8	***Factory Test Only***	RsvdP	No	00h
31:16	***Reserved***	RsvdP	No	0000h

12.14.5 Device-Specific Registers – I2C Slave Interface (Offsets 290h – 2C4h)

This section details the Device-Specific I2C Slave Interface register. Table 12-30 defines the register map.

The I2C Slave Interface is described, in detail, in Section 7, "I2C Slave Interface Operation."

Table 12-30. Device-Specific I2C Slave Interface Register Map (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Factory Test Only		290h
I2C Configuration		294h
Factory Test Only/Reserved		298h – 2C4h

Register 12-92. 294h I2C Configuration (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I2C	Default	
2:0	**Slave Address** Bits [6:0] comprise the I2C Slave address, 6Fh or 68h – value of bits [2:0] defaults to 111b or 000b, depending upon whether I2C_ADDR[2:0] are externally pulled High or Low, respectively. ***Note: The I2C Slave address must not be changed by an I2C Write command.***	HwInit	Yes	111b or 000b	6Fh or 68h
6:3	**Slave Address** Bits [6:0] comprise the I2C Slave address, 6Fh or 68h – bits [6:3] default to 1101b. ***Note: The I2C Slave address must not be changed by an I2C Write command.***	RW	Yes	1101b	
9:7	***Reserved***	RsvdP	No	000b	
10	***Factory Test Only***	RW	Yes	0	
31:11	***Reserved***	RW	Yes	0000_00h	

12.14.6 Device-Specific Registers – Bus Number CAM (Offsets 2C8h – 304h)

This section details the Device-Specific Bus Number Content-Addressable Memory (BusNoCAM) registers, which are used to determine the Configuration TLP Completion routing. These registers contain mirror copies of the **Primary Bus Number**, **Secondary Bus Number**, and **Subordinate Bus Number** registers (offset 18h[23:16, 15:8, and 7:0], respectively), for each PEX 8624 Port. Table 12-31 defines the register map.

The BusNoCAM registers are automatically updated by hardware. ***Modifying these registers by writing to the addresses listed here is not recommended.***

Table 12-31. Device-Specific BusNoCAM Register Map (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved	BusNoCAM0		2C8h
Reserved	BusNoCAM1		2CCh
Factory Test Only			2D0h – 2D4h
Reserved	BusNoCAM4		2D8h
Reserved	BusNoCAM5		2DCh
Reserved	BusNoCAM6		2E0h
Factory Test Only			2E4h
Reserved	BusNoCAM8		2E8h
Reserved	BusNoCAM9		2ECh
Factory Test Only			2F0h – 2F4h
Reserved			2F8h – 304h

Register 12-93. 2C8h BusNoCAM0 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Primary Bus Number** Mirror copy of Port 0 Primary Bus Number.	RW	Yes	00h
15:8	**Secondary Bus Number** Mirror copy of Port 0 Secondary Bus Number.	RW	Yes	00h
23:16	**Subordinate Bus Number** Mirror copy of Port 0 Subordinate Bus Number.	RW	Yes	00h
31:24	***Reserved***	RsvdP	No	00h

Register 12-94. 2CCh BusNoCAM1 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Primary Bus Number** Mirror copy of Port 1 Primary Bus Number.	RW	Yes	00h
15:8	**Secondary Bus Number** Mirror copy of Port 1 Secondary Bus Number.	RW	Yes	00h
23:16	**Subordinate Bus Number** Mirror copy of Port 1 Subordinate Bus Number.	RW	Yes	00h
31:24	***Reserved***	RsvdP	No	00h

Register 12-95. 2D8h BusNoCAM4 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Primary Bus Number** Mirror copy of Port 4 Primary Bus Number.	RW	Yes	00h
15:8	**Secondary Bus Number** Mirror copy of Port 4 Secondary Bus Number.	RW	Yes	00h
23:16	**Subordinate Bus Number** Mirror copy of Port 4 Subordinate Bus Number.	RW	Yes	00h
31:24	***Reserved***	RsvdP	No	00h

Register 12-96. 2DCh BusNoCAM5 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Primary Bus Number** Mirror copy of Port 5 Primary Bus Number.	RW	Yes	00h
15:8	**Secondary Bus Number** Mirror copy of Port 5 Secondary Bus Number.	RW	Yes	00h
23:16	**Subordinate Bus Number** Mirror copy of Port 5 Subordinate Bus Number.	RW	Yes	00h
31:24	***Reserved***	RsvdP	No	00h

Register 12-97. 2E0h BusNoCAM6 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Primary Bus Number** Mirror copy of Port 6 Primary Bus Number.	RW	Yes	00h
15:8	**Secondary Bus Number** Mirror copy of Port 6 Secondary Bus Number.	RW	Yes	00h
23:16	**Subordinate Bus Number** Mirror copy of Port 6 Subordinate Bus Number.	RW	Yes	00h
31:24	***Reserved***	RsvdP	No	00h

Register 12-98. 2E8h BusNoCAM8 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Primary Bus Number** Mirror copy of Port 8 Primary Bus Number.	RW	Yes	00h
15:8	**Secondary Bus Number** Mirror copy of Port 8 Secondary Bus Number.	RW	Yes	00h
23:16	**Subordinate Bus Number** Mirror copy of Port 8 Subordinate Bus Number.	RW	Yes	00h
31:24	***Reserved***	RsvdP	No	00h

Register 12-99. 2ECh BusNoCAM9 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Primary Bus Number** Mirror copy of Port 9 Primary Bus Number.	RW	Yes	00h
15:8	**Secondary Bus Number** Mirror copy of Port 9 Secondary Bus Number.	RW	Yes	00h
23:16	**Subordinate Bus Number** Mirror copy of Port 9 Subordinate Bus Number.	RW	Yes	00h
31:24	***Reserved***	RsvdP	No	00h

12.14.7 Device-Specific Registers – I/O CAM (Offsets 308h – 344h)

This section details the Device-Specific I/O Content-Addressable Memory (IOCAM) registers, which are used to determine I/O Request routing. These registers contain mirror copies of the **I/O Base** and **I/O Limit** registers (offset 1Ch[7:0 and 15:8], respectively), for each PEX 8624 Port. Table 12-32 defines the register map.

The IOCAM registers are automatically updated by hardware. ***Modifying these registers by writing to the addresses listed here is not recommended.***

Table 12-32. Device-Specific IOCAM Register Map (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
IOCAM1		IOCAM0		308h
Factory Test Only				30Ch
IOCAM5		IOCAM4		310h
Factory Test Only		IOCAM6		314h
IOCAM9		IOCAM8		318h
Factory Test Only				31Ch
Reserved				320h – 344h

Register 12-100. 308h IOCAM0 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
3:0	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
7:4	**I/O Base** Mirror copy of Port 0 I/O Base value.	RW	Yes	Fh
11:8	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
15:12	**I/O Limit** Mirror copy of Port 0 I/O Limit value.	RW	Yes	0h

Register 12-101. 30Ah IOCAM1 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
3:0	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
7:4	**I/O Base** Mirror copy of Port 1 I/O Base value.	RW	Yes	Fh
11:8	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
15:12	**I/O Limit** Mirror copy of Port 1 I/O Limit value.	RW	Yes	0h

Register 12-102. 310h IOCAM4 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
3:0	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
7:4	**I/O Base** Mirror copy of Port 4 I/O Base value.	RW	Yes	Fh
11:8	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
15:12	**I/O Limit** Mirror copy of Port 4 I/O Limit value.	RW	Yes	0h

Register 12-103. 312h IOCAM5 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
3:0	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
7:4	**I/O Base** Mirror copy of Port 5 I/O Base value.	RW	Yes	Fh
11:8	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
15:12	**I/O Limit** Mirror copy of Port 5 I/O Limit value.	RW	Yes	0h

Register 12-104. 314h IOCAM6 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
3:0	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
7:4	**I/O Base** Mirror copy of Port 6 I/O Base value.	RW	Yes	Fh
11:8	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
15:12	**I/O Limit** Mirror copy of Port 6 I/O Limit value.	RW	Yes	0h

Register 12-105. 318h IOCAM8 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
3:0	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
7:4	**I/O Base** Mirror copy of Port 8 I/O Base value.	RW	Yes	Fh
11:8	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
15:12	**I/O Limit** Mirror copy of Port 8 I/O Limit value.	RW	Yes	0h

Register 12-106. 31Ah IOCAM9 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
3:0	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
7:4	**I/O Base** Mirror copy of Port 9 I/O Base value.	RW	Yes	Fh
11:8	**I/O Addressing Capability** 0h = 16-bit I/O addressing 1h = 32-bit I/O addressing	RO	Yes	1h
15:12	**I/O Limit** Mirror copy of Port 9 I/O Limit value.	RW	Yes	0h

12.14.8 Device-Specific Registers – Address-Mapping CAM (Offsets 348h – 444h)

This section details the Device-Specific Address-Mapping Content-Addressable Memory (AMCAM) registers, which are used to used to determine Memory Request routing. These registers contain mirror copies of the **Memory Base and Limit**, **Prefetchable Memory Base and Limit**, **Prefetchable Memory Upper Base Address**, and **Prefetchable Memory Upper Limit Address** registers (offsets 20h, 24h, 28h, and 2Ch, respectively), for each PEX 8624 Port. Table 12-33 defines the register map.

The AMCAM registers are automatically updated by hardware. ***Modifying these registers by writing to the addresses listed here is not recommended.***

Table 12-33. Device-Specific AMCAM Register Map (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
AMCAM0 Memory Limit		AMCAM0 Memory Base		348h
AMCAM0 Prefetchable Memory Limit		AMCAM0 Prefetchable Memory Base		34Ch
AMCAM0 Prefetchable Memory Base Upper 32 Bits				350h
AMCAM0 Prefetchable Memory Limit Upper 32 Bits				354h
AMCAM1 Memory Limit		AMCAM1 Memory Base		358h
AMCAM1 Prefetchable Memory Limit		AMCAM1 Prefetchable Memory Base		35Ch
AMCAM1 Prefetchable Memory Base Upper 32 Bits				360h
AMCAM1 Prefetchable Memory Limit Upper 32 Bits				364h
Factory Test Only				368h – 384h
AMCAM4 Memory Limit		AMCAM4 Memory Base		388h
AMCAM4 Prefetchable Memory Limit		AMCAM4 Prefetchable Memory Base		38Ch
AMCAM4 Prefetchable Memory Base Upper 32 Bits				390h
AMCAM4 Prefetchable Memory Limit Upper 32 Bits				394h
AMCAM5 Memory Limit		AMCAM5 Memory Base		398h
AMCAM5 Prefetchable Memory Limit		AMCAM5 Prefetchable Memory Base		39Ch
AMCAM5 Prefetchable Memory Base Upper 32 Bits				3A0h
AMCAM5 Prefetchable Memory Limit Upper 32 Bits				3A4h
AMCAM6 Memory Limit		AMCAM6 Memory Base		3A8h
AMCAM6 Prefetchable Memory Limit		AMCAM6 Prefetchable Memory Base		3ACh
AMCAM6 Prefetchable Memory Base Upper 32 Bits				3B0h
AMCAM6 Prefetchable Memory Limit Upper 32 Bits				3B4h
Factory Test Only				3B8h – 3C4h
AMCAM8 Memory Limit		AMCAM8 Memory Base		3C8h
AMCAM8 Prefetchable Memory Limit		AMCAM8 Prefetchable Memory Base		3CCh

Table 12-33. Device-Specific AMCAM Register Map (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
AMCAM8 Prefetchable Memory Base Upper 32 Bits				3D0h
AMCAM8 Prefetchable Memory Limit Upper 32 Bits				3D4h
AMCAM9 Memory Limit		AMCAM9 Memory Base		3D8h
AMCAM9 Prefetchable Memory Limit		AMCAM9 Prefetchable Memory Base		3DCh
AMCAM9 Prefetchable Memory Base Upper 32 Bits				3E0h
AMCAM9 Prefetchable Memory Limit Upper 32 Bits				3E4h
Factory Test Only				3E8h – 404h
Reserved				408h – 444h

Register 12-107. 348h AMCAM0 Memory Base and Limit (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM0 Memory Base				
3:0	***Reserved***	RsvdP	No	0h
15:4	**AMCAM0 Memory Base** Mirror copy of Port 0 Memory Base value.	RW	Yes	FFFh
AMCAM0 Memory Limit				
19:16	***Reserved***	RsvdP	No	0h
31:20	**AMCAM0 Memory Limit** Mirror copy of Port 0 Memory Limit value.	RW	Yes	000h

Register 12-108. 34Ch AMCAM0 Prefetchable Memory Base and Limit (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM0 Prefetchable Memory Base				
3:0	**AMCAM0 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
15:4	**AMCAM0 Prefetchable Memory Base** AMCAM0 Port 0 Prefetchable Memory Base[31:20].	RW	Yes	FFFh
AMCAM0 Prefetchable Memory Limit				
19:16	**AMCAM0 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
31:20	**AMCAM0 Prefetchable Memory Limit** AMCAM0 Port 0 Prefetchable Memory Limit[31:20].	RW	Yes	000h

Register 12-109. 350h AMCAM0 Prefetchable Memory Base Upper 32 Bits (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**AMCAM0 Prefetchable Memory Base Upper 32 Bits** AMCAM0 Port 0 Prefetchable Memory Base[63:32].	RW	Yes	0000_0000h

Register 12-110. 354h AMCAM0 Prefetchable Memory Limit Upper 32 Bits (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**AMCAM0 Prefetchable Memory Limit Upper 32 Bits** AMCAM0 Port 0 Prefetchable Memory Limit[63:32].	RW	Yes	0000_0000h

Register 12-111. 358h AMCAM1 Memory Base and Limit (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM1 Memory Base				
3:0	***Reserved***	RsvdP	No	0h
15:4	**AMCAM1 Memory Base** Mirror copy of Port 1 Memory Base value.	RW	Yes	FFFh
AMCAM1 Memory Limit				
19:16	***Reserved***	RsvdP	No	0h
31:20	**AMCAM1 Memory Limit** Mirror copy of Port 1 Memory Limit value.	RW	Yes	000h

Register 12-112. 35Ch AMCAM1 Prefetchable Memory Base and Limit (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM1 Prefetchable Memory Base				
3:0	**AMCAM1 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
15:4	**AMCAM1 Prefetchable Memory Base** AMCAM1 Port 1 Prefetchable Memory Base[31:20].	RW	Yes	FFFh
AMCAM1 Prefetchable Memory Limit				
19:16	**AMCAM1 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
31:20	**AMCAM1 Prefetchable Memory Limit** AMCAM1 Port 1 Prefetchable Memory Limit[31:20].	RW	Yes	000h

Register 12-113. 360h AMCAM1 Prefetchable Memory Base Upper 32 Bits (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**AMCAM1 Prefetchable Memory Base Upper 32 Bits** AMCAM1 Port 1 Prefetchable Memory Base[63:32].	RW	Yes	0000_0000h

Register 12-114. 364h AMCAM1 Prefetchable Memory Limit Upper 32 Bits (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**AMCAM1 Prefetchable Memory Limit Upper 32 Bits** AMCAM1 Port 1 Prefetchable Memory Limit[63:32].	RW	Yes	0000_0000h

Register 12-115. 388h AMCAM4 Memory Base and Limit (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM4 Memory Base				
3:0	***Reserved***	RsvdP	No	0h
15:4	**AMCAM4 Memory Base** Mirror copy of Port 4 Memory Base value.	RW	Yes	FFFh
AMCAM4 Memory Limit				
19:16	***Reserved***	RsvdP	No	0h
31:20	**AMCAM4 Memory Limit** Mirror copy of Port 4 Memory Limit value.	RW	Yes	000h

Register 12-116. 38Ch AMCAM4 Prefetchable Memory Base and Limit (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM4 Prefetchable Memory Base				
3:0	**AMCAM4 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
15:4	**AMCAM4 Prefetchable Memory Base** AMCAM4 Port 4 Prefetchable Memory Base[31:20].	RW	Yes	FFFh
AMCAM4 Prefetchable Memory Limit				
19:16	**AMCAM4 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
31:20	**AMCAM4 Prefetchable Memory Limit** AMCAM4 Port 4 Prefetchable Memory Limit[31:20].	RW	Yes	000h

Register 12-117. 390h AMCAM4 Prefetchable Memory Base Upper 32 Bits (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**AMCAM4 Prefetchable Memory Base Upper 32 Bits** AMCAM4 Port 4 Prefetchable Memory Base[63:32].	RW	Yes	0000_0000h

Register 12-118. 394h AMCAM4 Prefetchable Memory Limit Upper 32 Bits (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**AMCAM4 Prefetchable Memory Limit Upper 32 Bits** AMCAM4 Port 4 Prefetchable Memory Limit[63:32].	RW	Yes	0000_0000h

Register 12-119. 398h AMCAM5 Memory Base and Limit (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM5 Memory Base				
3:0	***Reserved***	RsvdP	No	0h
15:4	**AMCAM5 Memory Base** Mirror copy of Port 5 Memory Base value.	RW	Yes	FFFh
AMCAM5 Memory Limit				
19:16	***Reserved***	RsvdP	No	0h
31:20	**AMCAM5 Memory Limit** Mirror copy of Port 5 Memory Limit value.	RW	Yes	000h

Register 12-120. 39Ch AMCAM5 Prefetchable Memory Base and Limit (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM5 Prefetchable Memory Base				
3:0	**AMCAM5 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
15:4	**AMCAM5 Prefetchable Memory Base** AMCAM5 Port 5 Prefetchable Memory Base[31:20].	RW	Yes	FFFh
AMCAM5 Prefetchable Memory Limit				
19:16	**AMCAM5 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
31:20	**AMCAM5 Prefetchable Memory Limit** AMCAM5 Port 5 Prefetchable Memory Limit[31:20].	RW	Yes	000h

Register 12-121. 3A0h AMCAM5 Prefetchable Memory Base Upper 32 Bits (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**AMCAM5 Prefetchable Memory Base Upper 32 Bits** AMCAM5 Port 5 Prefetchable Memory Base[63:32].	RW	Yes	0000_0000h

Register 12-122. 3A4h AMCAM5 Prefetchable Memory Limit Upper 32 Bits (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**AMCAM5 Prefetchable Memory Limit Upper 32 Bits** AMCAM5 Port 5 Prefetchable Memory Limit[63:32].	RW	Yes	0000_0000h

Register 12-123. 3A8h AMCAM6 Memory Base and Limit (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM6 Memory Base				
3:0	***Reserved***	RsvdP	No	0h
15:4	**AMCAM6 Memory Base** Mirror copy of Port 6 Memory Base value.	RW	Yes	FFFh
AMCAM6 Memory Limit				
19:16	***Reserved***	RsvdP	No	0h
31:20	**AMCAM6 Memory Limit** Mirror copy of Port 6 Memory Limit value.	RW	Yes	000h

Register 12-124. 3ACh AMCAM6 Prefetchable Memory Base and Limit (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM6 Prefetchable Memory Base				
3:0	**AMCAM6 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
15:4	**AMCAM6 Prefetchable Memory Base** AMCAM6 Port 6 Prefetchable Memory Base[31:20].	RW	Yes	FFFh
AMCAM6 Prefetchable Memory Limit				
19:16	**AMCAM6 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
31:20	**AMCAM6 Prefetchable Memory Limit** AMCAM6 Port 6 Prefetchable Memory Limit[31:20].	RW	Yes	000h

Register 12-125. 3B0h AMCAM6 Prefetchable Memory Base Upper 32 Bits (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**AMCAM6 Prefetchable Memory Base Upper 32 Bits** AMCAM6 Port 6 Prefetchable Memory Base[63:32].	RW	Yes	0000_0000h

Register 12-126. 3B4h AMCAM6 Prefetchable Memory Limit Upper 32 Bits (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**AMCAM6 Prefetchable Memory Limit Upper 32 Bits** AMCAM6 Port 6 Prefetchable Memory Limit[63:32].	RW	Yes	0000_0000h

Register 12-127. 3C8h AMCAM8 Memory Base and Limit (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM8 Memory Base				
3:0	***Reserved***	RsvdP	No	0h
15:4	**AMCAM8 Memory Base** Mirror copy of Port 8 Memory Base value.	RW	Yes	FFFh
AMCAM8 Memory Limit				
19:16	***Reserved***	RsvdP	No	0h
31:20	**AMCAM8 Memory Limit** Mirror copy of Port 8 Memory Limit value.	RW	Yes	000h

Register 12-128. 3CCh AMCAM8 Prefetchable Memory Base and Limit (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM8 Prefetchable Memory Base				
3:0	**AMCAM8 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
15:4	**AMCAM8 Prefetchable Memory Base** AMCAM8 Port 8 Prefetchable Memory Base[31:20].	RW	Yes	FFFh
AMCAM8 Prefetchable Memory Limit				
19:16	**AMCAM8 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
31:20	**AMCAM8 Prefetchable Memory Limit** AMCAM8 Port 8 Prefetchable Memory Limit[31:20].	RW	Yes	000h

Register 12-129. 3D0h AMCAM8 Prefetchable Memory Base Upper 32 Bits (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**AMCAM8 Prefetchable Memory Base Upper 32 Bits** AMCAM8 Port 8 Prefetchable Memory Base[63:32].	RW	Yes	0000_0000h

Register 12-130. 3D4h AMCAM8 Prefetchable Memory Limit Upper 32 Bits (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**AMCAM8 Prefetchable Memory Limit Upper 32 Bits** AMCAM8 Port 8 Prefetchable Memory Limit[63:32].	RW	Yes	0000_0000h

Register 12-131. 3D8h AMCAM9 Memory Base and Limit (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM9 Memory Base				
3:0	***Reserved***	RsvdP	No	0h
15:4	**AMCAM9 Memory Base** Mirror copy of Port 9 Memory Base value.	RW	Yes	FFFh
AMCAM9 Memory Limit				
19:16	***Reserved***	RsvdP	No	0h
31:20	**AMCAM9 Memory Limit** Mirror copy of Port 9 Memory Limit value.	RW	Yes	000h

Register 12-132. 3DCh AMCAM9 Prefetchable Memory Base and Limit (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
AMCAM9 Prefetchable Memory Base				
3:0	**AMCAM9 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
15:4	**AMCAM9 Prefetchable Memory Base** AMCAM9 Port 9 Prefetchable Memory Base[31:20].	RW	Yes	FFFh
AMCAM9 Prefetchable Memory Limit				
19:16	**AMCAM9 Addressing Support** 0h = 32-bit addressing is supported 1h = 64-bit addressing is supported	RO	Yes	1h
31:20	**AMCAM9 Prefetchable Memory Limit** AMCAM9 Port 9 Prefetchable Memory Limit[31:20].	RW	Yes	000h

Register 12-133. 3E0h AMCAM9 Prefetchable Memory Base Upper 32 Bits (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**AMCAM9 Prefetchable Memory Base Upper 32 Bits** AMCAM9 Port 9 Prefetchable Memory Base[63:32].	RW	Yes	0000_0000h

Register 12-134. 3E4h AMCAM9 Prefetchable Memory Limit Upper 32 Bits (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**AMCAM9 Prefetchable Memory Limit Upper 32 Bits** AMCAM9 Port 9 Prefetchable Memory Limit[63:32].	RW	Yes	0000_0000h

12.14.9 Device-Specific Registers – Vendor-Specific Dual Cast Extended Capability (Offsets 448h – 51Ch)

This section details the Device-Specific, Vendor-Specific Dual Cast Extended Capability registers. Table 12-34 defines the register map.

The Dual Cast registers exist in Port 0. A copy of these registers (excluding the Header at offsets 448h and 44Ch) also exists in Stations 1 and 2 (*that is*, at the same respective offsets in Ports 4 and 8). When software programs the Port 0 registers, the PEX 8624 automatically copies the values to each Station. However, if the Dual Cast registers are programmed by serial EEPROM or I^2C, the values are not copied to the other Stations, and therefore software, serial EEPROM, or I^2C must perform the copy operation.

If the Dual Cast registers (in Port 0) are programmed by serial EEPROM or I^2C, either:

- Program the serial EEPROM or I^2C to additionally program the values into the same respective offsets in Ports 4 and 8, –or–
- Trigger an automatic copy operation, by causing software to read and write back the same values into the Port 0 registers

Table 12-34. Device-Specific, Vendor-Specific Dual Cast Extended Capability Register Map (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (950h or 520h)	Capability Version (1h) / PCI Express Extended Capability ID (000Bh)	448h
Vendor-Specific Header 1		44Ch
Dual Cast Low BAR0		450h
Dual Cast High BAR0		454h
Dual Cast Low BAR0 Translation		458h
Dual Cast High BAR0 Translation		45Ch
Dual Cast Low BAR0 Setup		460h
Dual Cast High BAR0 Setup		464h
Dual Cast Low BAR1		468h
Dual Cast High BAR1		46Ch
Dual Cast Low BAR1 Translation		470h
Dual Cast High BAR1 Translation		474h
Dual Cast Low BAR1 Setup		478h
Dual Cast High BAR1 Setup		47Ch
Dual Cast Low BAR2		480h
Dual Cast High BAR2		484h
Dual Cast Low BAR2 Translation		488h
Dual Cast High BAR2 Translation		48Ch
Dual Cast Low BAR2 Setup		490h
Dual Cast High BAR2 Setup		494h
Dual Cast Low BAR3		498h
Dual Cast High BAR3		49Ch

Table 12-34. Device-Specific, Vendor-Specific Dual Cast Extended Capability Register Map (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Dual Cast Low BAR3 Translation	4A0h
Dual Cast High BAR3 Translation	4A4h
Dual Cast Low BAR3 Setup	4A8h
Dual Cast High BAR3 Setup	4ACh
Dual Cast Low BAR4	4B0h
Dual Cast High BAR4	4B4h
Dual Cast Low BAR4 Translation	4B8h
Dual Cast High BAR4 Translation	4BCh
Dual Cast Low BAR4 Setup	4C0h
Dual Cast High BAR4 Setup	4C4h
Dual Cast Low BAR5	4C8h
Dual Cast High BAR5	4CCh
Dual Cast Low BAR5 Translation	4D0h
Dual Cast High BAR5 Translation	4D4h
Dual Cast Low BAR5 Setup	4D8h
Dual Cast High BAR5 Setup	4DCh
Dual Cast Low BAR6	4E0h
Dual Cast High BAR6	4E4h
Dual Cast Low BAR6 Translation	4E8h
Dual Cast High BAR6 Translation	4ECh
Dual Cast Low BAR6 Setup	4F0h
Dual Cast High BAR6 Setup	4F4h
Dual Cast Low BAR7	4F8h
Dual Cast High BAR7	4FCh
Dual Cast Low BAR7 Translation	500h
Dual Cast High BAR7 Translation	504h
Dual Cast Low BAR7 Setup	508h
Dual Cast High BAR7 Setup	50Ch
Dual Cast Source Destination Port	510h
Reserved	514h – 51Ch

Register 12-135. 448h Vendor-Specific Extended Capability Header (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
15:0	**PCI Express Extended Capability ID** Programmed to 000Bh, indicating that the Capability structure is the **Vendor-Specific Extended Capability** structure.		RO	Yes	000Bh
19:16	**Capability Version**		RO	Yes	1h
31:20	**Next Capability Offset** Next extended capability is the **Vendor-Specific Extended Capability 2** structure, offset 950h.	Upstream	RO	Yes	950h
	Next extended capability is the **ACS Extended Capability** structure, offset 520h.	Downstream	RO	No	520h

Register 12-136. 44Ch Vendor-Specific Header 1 (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**Vendor-Specific ID** ID Number of this **Vendor-Specific Extended Capability** (**VSEC**) structure.	RO	Yes	0000h
19:16	**Vendor-Specific Rev** Version Number of this **VSEC** structure.	RO	Yes	0h
31:20	**Vendor-Specific Length** Number of bytes in the entire **VSEC** structure.	RO	Yes	0CCh

Register 12-137. 450h Dual Cast Low BAR0 (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	No	10b
3	**Prefetchable** Not used, but included for software compatibility with respect to Base Address Register (BAR) definition.	RO	Yes	1
19:4	***Reserved***	RO	No	0_000h
31:20	**Dual Cast BAR**	RW	Yes	000h

Register 12-138. 454h Dual Cast High BAR0 (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper Base Address** Dual Cast's Upper Base Address (BAR[63:32]).	RW	No	0000_0000h

Register 12-139. 458h Dual Cast Low BAR0 Translation (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Translation Address**	RW	Yes	000h

Register 12-140. 45Ch Dual Cast High BAR0 Translation (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Base Translation Upper Address** RW when the **Dual Cast Low BAR0** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 450h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR0** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 450h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 12-141. 460h Dual Cast Low BAR0 Setup
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Setup**	RW	Yes	000h

Register 12-142. 464h Dual Cast High BAR0 Setup
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper BAR Setup** RW when the **Dual Cast Low BAR0** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 450h[2:1]) is programmed to 10b. Bit 31 values: 0 = BAR is disabled 1 = BAR is enabled	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR0** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 450h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 12-143. 468h Dual Cast Low BAR1
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	No	10b
3	***Reserved***	RO	Yes	1
19:4	***Reserved***	RO	No	0_000h
31:20	**Dual Cast BAR**	RW	Yes	000h

Register 12-144. 46Ch Dual Cast High BAR1
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper Base Address** Dual Cast's Upper Base Address (BAR[63:32]).	RW	No	0000_0000h

Register 12-145. 470h Dual Cast Low BAR1 Translation
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Translation Address**	RW	Yes	000h

Register 12-146. 474h Dual Cast High BAR1 Translation
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Base Translation Upper Address** RW when the **Dual Cast Low BAR1** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 468h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR1** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 468h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 12-147. 478h Dual Cast Low BAR1 Setup (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Setup**	RW	Yes	000h

Register 12-148. 47Ch Dual Cast High BAR1 Setup (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper BAR Setup** RW when the **Dual Cast Low BAR1** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 468h[2:1]) is programmed to 10b. Bit 31 values: 0 = BAR is disabled 1 = BAR is enabled	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR1** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 468h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 12-149. 480h Dual Cast Low BAR2
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	No	10b
3	***Reserved***	RO	Yes	1
19:4	***Reserved***	RO	No	0_000h
31:20	**Dual Cast BAR**	RW	Yes	000h

Register 12-150. 484h Dual Cast High BAR2
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper Base Address** Dual Cast's Upper Base Address (BAR[63:32]).	RW	No	0000_0000h

Register 12-151. 488h Dual Cast Low BAR2 Translation
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Translation Address**	RW	Yes	000h

Register 12-152. 48Ch Dual Cast High BAR2 Translation
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Base Translation Upper Address** RW when the **Dual Cast Low BAR2** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 480h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR2** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 480h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 12-153. 490h Dual Cast Low BAR2 Setup
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Setup**	RW	Yes	000h

Register 12-154. 494h Dual Cast High BAR2 Setup
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper BAR Setup** RW when the **Dual Cast Low BAR2** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 480h[2:1]) is programmed to 10b. Bit 31 values: 0 = BAR is disabled 1 = BAR is enabled	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR2** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 480h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 12-155. 498h Dual Cast Low BAR3
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	No	10b
3	***Reserved***	RO	Yes	1
19:4	***Reserved***	RO	No	0_000h
31:20	**Dual Cast BAR**	RW	Yes	000h

Register 12-156. 49Ch Dual Cast High BAR3
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper Base Address** Dual Cast's Upper Base Address (BAR[63:32]).	RW	No	0000_0000h

Register 12-157. 4A0h Dual Cast Low BAR3 Translation
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Translation Address**	RW	Yes	000h

Register 12-158. 4A4h Dual Cast High BAR3 Translation
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Base Translation Upper Address** RW when the **Dual Cast Low BAR3** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 498h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR3** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 498h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 12-159. 4A8h Dual Cast Low BAR3 Setup (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Setup**	RW	Yes	000h

Register 12-160. 4ACh Dual Cast High BAR3 Setup (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper BAR Setup** RW when the **Dual Cast Low BAR3** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 498h[2:1]) is programmed to 10b. Bit 31 values: 0 = BAR is disabled 1 = BAR is enabled	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR3** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 498h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 12-161. 4B0h Dual Cast Low BAR4
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	No	10b
3	***Reserved***	RO	Yes	1
19:4	***Reserved***	RO	No	0_000h
31:20	**Dual Cast BAR**	RW	Yes	000h

Register 12-162. 4B4h Dual Cast High BAR4
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper Base Address** Dual Cast's Upper Base Address (BAR[63:32]).	RW	No	0000_0000h

Register 12-163. 4B8h Dual Cast Low BAR4 Translation
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Translation Address**	RW	Yes	000h

Register 12-164. 4BCh Dual Cast High BAR4 Translation
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Base Translation Upper Address** RW when the **Dual Cast Low BAR4** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 4B0h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR4** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 4B0h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 12-165. 4C0h Dual Cast Low BAR4 Setup
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Setup**	RW	Yes	000h

Register 12-166. 4C4h Dual Cast High BAR4 Setup
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper BAR Setup** RW when the **Dual Cast Low BAR4** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 4B0h[2:1]) is programmed to 10b. Bit 31 values: 0 = BAR is disabled 1 = BAR is enabled	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR4** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 4B0h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 12-167. 4C8h Dual Cast Low BAR5 (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	No	10b
3	***Reserved***	RO	Yes	1
19:4	***Reserved***	RO	No	0_000h
31:20	**Dual Cast BAR**	RW	Yes	000h

Register 12-168. 4CCh Dual Cast High BAR5 (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper Base Address** Dual Cast's Upper Base Address (BAR[63:32]).	RW	No	0000_0000h

Register 12-169. 4D0h Dual Cast Low BAR5 Translation (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Translation Address**	RW	Yes	000h

Register 12-170. 4D4h Dual Cast High BAR5 Translation (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Base Translation Upper Address** RW when the **Dual Cast Low BAR5** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 4C8h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR5** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 4C8h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 12-171. 4D8h Dual Cast Low BAR5 Setup (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Setup**	RW	Yes	000h

Register 12-172. 4DCh Dual Cast High BAR5 Setup (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper BAR Setup** RW when the **Dual Cast Low BAR5** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 4C8h[2:1]) is programmed to 10b. Bit 31 values: 0 = BAR is disabled 1 = BAR is enabled	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR5** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 4C8h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 12-173. 4E0h Dual Cast Low BAR6 (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	No	10b
3	***Reserved***	RO	Yes	1
19:4	***Reserved***	RO	No	0_000h
31:20	**Dual Cast BAR**	RW	Yes	000h

Register 12-174. 4E4h Dual Cast High BAR6 (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper Base Address** Dual Cast's Upper Base Address (BAR[63:32]).	RW	No	0000_0000h

Register 12-175. 4E8h Dual Cast Low BAR6 Translation (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Translation Address**	RW	Yes	000h

Register 12-176. 4ECh Dual Cast High BAR6 Translation (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Base Translation Upper Address** RW when the **Dual Cast Low BAR6** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 4E0h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR6** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 4E0h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 12-177. 4F0h Dual Cast Low BAR6 Setup (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Setup**	RW	Yes	000h

Register 12-178. 4F4h Dual Cast High BAR6 Setup (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper BAR Setup** RW when the **Dual Cast Low BAR6** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 4E0h[2:1]) is programmed to 10b. Bit 31 values: 0 = BAR is disabled 1 = BAR is enabled	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR6** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 4E0h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 12-179. 4F8h Dual Cast Low BAR7
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	No	10b
3	***Reserved***	RO	Yes	1
19:4	***Reserved***	RO	No	0_000h
31:20	**Dual Cast BAR**	RW	Yes	000h

Register 12-180. 4FCh Dual Cast High BAR7
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper Base Address** Dual Cast's Upper Base Address (BAR[63:32]).	RW	No	0000_0000h

Register 12-181. 500h Dual Cast Low BAR7 Translation
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Translation Address**	RW	Yes	000h

Register 12-182. 504h Dual Cast High BAR7 Translation
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Base Translation Upper Address** RW when the **Dual Cast Low BAR7** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 4F8h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR7** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 4F8h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 12-183. 508h Dual Cast Low BAR7 Setup
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**Base Setup**	RW	Yes	000h

Register 12-184. 50Ch Dual Cast High BAR7 Setup
(Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Dual Cast Upper BAR Setup** RW when the **Dual Cast Low BAR7** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 4F8h[2:1]) is programmed to 10b. Bit 31 values: 0 = BAR is disabled 1 = BAR is enabled	RW	Yes	0000_0000h
	Reserved when the **Dual Cast Low BAR7** register *Memory Map Type* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 4F8h[2:1]) is Cleared.	RsvdP	No	0000_0000h

Register 12-185. 510h Dual Cast Source Destination Port (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port; *Reserved* (RsvdP) for Dual Cast BAR Limit Lower Register)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
1:0	**Dual Cast Source Port #** Valid only when bit 8 (*Dual Cast Source Port Enable*) is Set. Specifies the source (ingress) Port Number upon which Dual Cast BARs are applied. Refer to Table 12-35 for Source Port # to Source Station # mapping.	RW	Yes	00b

3:2	**Dual Cast Source Station #**
	Specifies the source (ingress) Station Number upon which Dual Cast BARs are applied.
	Refer to Table 12-35 for Source Port # to Source Station # mapping.
	00b = Station 0
	01b = Station 1
	10b = Station 2
	11b = ***Reserved***
		RW	Yes	00b

7:4	**Dual Cast Destination Port #** Specifies the destination (egress) Port Number to which Dual Cast BAR Translation addresses are mapped, and to which Dual Cast Copy TLPs will be queued. 0h = Port 0 1h = Port 1 5h = Port 5 6h = Port 6 8h = Port 8 9h = Port 9 All other encodings are ***reserved***.	RW	Yes	0h
8	**Dual Cast Source Port Enable** 0 = Dual Cast applies to Write TLPs entering any Port on the Dual Cast Source Station specified in field [3:2] (*Dual Cast Source Station #*). In that case, the field [1:0] (*Dual Cast Source Port #*) value is "Don't Care." 1 = Dual Cast applies only to Write TLPs entering the PEX 8624, by way of the Dual Cast Source Port Number specified in field [1:0].	RW	Yes	0
31:9	***Reserved***	RsvdP	No	0-0h

Table 12-35. Dual Cast Source Destination Port Register – Source Port # and Source Station Field Values, by Port (Offset 510h)

Port	Dual Cast Source Port # (Field [1:0] Value)	Dual Cast Source Station # (Field [3:2] Value)
0	00b	00b
1	01b	00b
5	01b	01b
6	10b	01b
8	00b	10b
9	01b	10b

12.15 ACS Extended Capability Registers (Offsets 520h – 528h)

This section details the ACS Extended Capability registers. Table 12-36 defines the register map.

Table 12-36. ACS Extended Capability Register Map (All Downstream Ports; *Reserved* (RsvdP) for the Upstream Port)

31 30 29 28 27 26 25 24 23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved (Upstream)			
Next Capability Offset (950h) (Downstream)	Capability Version (1h) (Downstream)	PCI Express Extended Capability ID (000Dh) (Downstream)	520h
Reserved (Upstream)			
ACS Control (Downstream)		ACS Capability (Downstream)	524h
Reserved (Upstream) Egress Control Vector (Downstream)			528h

Register 12-186. 520h ACS Extended Capability Header (All Downstream Ports; *Reserved* (RsvdP) for the Upstream Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Note: *Because this register is implemented as one physical register common to all Ports, the upstream Port's register (which is **reserved**) has the same value as the downstream Ports' registers. However, in the upstream Port, the ACS Extended Capability is excluded from the Linked List of PCI Express Extended Capabilities, and therefore, the upstream Port's register is effectively hidden from system software and the non-zero value has no significant consequence.*					
15:0	***Reserved***	Upstream	RsvdP	No	0000h
	PCI Express Extended Capability ID	Downstream	RO	Yes	000Dh
19:16	***Reserved***	Upstream	RsvdP	No	0h
	Capability Version	RO	Yes	1h	1h
31:20	***Reserved***	Upstream	RsvdP	No	000h
	Next Capability Offset Programmed to 950h, which addresses the **Vendor-Specific Extended Capability 2** structure.	Downstream	RO	Yes	950h

Register 12-187. 524h ACS Control and Capability (All Downstream Ports; *Reserved* (RsvdP) for the Upstream Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Capability					
0	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation	Downstream	RO	Yes	1
1	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking	Downstream	RO	Yes	1
2	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect ACS Peer-to-Peer Request redirect.	Downstream	RO	Yes	1
3	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect ACS Peer-to-Peer Completion redirect.	Downstream	RO	Yes	1
4	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding	Downstream	RO	Yes	1
5	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Egress Control ACS Peer-to-Peer Egress control.	Downstream	RO	Yes	1
6	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P ACS Direct Translated Peer-to-Peer.	Downstream	RO	Yes	1
7	***Reserved***		RsvdP	No	0
11:8	***Reserved***	Upstream	RsvdP	No	0
	Egress Control Vector Size Encodings 1h through Fh directly indicate the number of each downstream Port's **Egress Control Vector** register *Peer-to-Peer Port x Control* bit (Downstream Ports, offset 528h[9, 8, 6, 5, 1, 0]). ***Note:*** *The ACS Egress Control Vector Size value must be adjusted for the specific Port configuration.*	Downstream	HwInit	Yes	Ch
15:12	***Reserved***		RsvdP	No	0h

Register 12-187. 524h ACS Control and Capability
(All Downstream Ports; *Reserved* (RsvdP) for the Upstream Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
ACS Control					
16	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation Enable 0 = Disables 1 = Enables	Downstream	RW	Yes	0
17	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking Enable 0 = Disables 1 = Enables	Downstream	RW	Yes	0
18	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect Enable Enables or disables ACS Peer-to-Peer Request redirect. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
19	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect Enable Enables or disables ACS Peer-to-Peer Completion redirect. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
20	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding Enable 0 = Disables 1 = Enables	Downstream	RW	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Egress Control Enable Enables or disables ACS Peer-to-Peer Egress control. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
22	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P Enable Enables or disables ACS Direct Translated Peer-to-Peer. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
31:23	***Reserved***		RsvdP	No	0-0h

Register 12-188. 528h Egress Control Vector (All Downstream Ports; *Reserved* (RsvdP) for the Upstream Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
0	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 0 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset 524h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
1	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 1 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset 524h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
3:2	***Factory Test Only***		RsvdP	No	00b
4	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 4 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset 524h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
5	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 5 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset 524h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
6	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 6 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset 524h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
7	***Factory Test Only***		RsvdP	No	0

Register 12-188. 528h Egress Control Vector (All Downstream Ports; *Reserved* (RsvdP) for the Upstream Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
8	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 8 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset 524h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
9	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 9 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset 524h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
11:10	***Factory Test Only***		RsvdP	No	00b
31:12	***Reserved***		RsvdP	No	0000_0h

12.16 Device-Specific Registers (Offsets 54Ch – F8Ch)

This section details the Device-Specific registers located at offsets 54Ch through F8Ch. Device-Specific registers are unique to the PEX 8624 and not referenced in the *PCI Express Base r2.0*. Table 12-37 defines the register map.

Other Device-Specific registers are detailed in Section 12.14, "Device-Specific Registers (Offsets 1C0h – 51Ch)."

Note: It is recommended that these registers not be changed from their default values.

Table 12-37. Device-Specific Register Map (Offsets 54Ch – F8Ch)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Factory Test Only/Reserved		54Ch – 570h
Device-Specific Registers – Port Configuration (Offsets 574h – 628h)		574h … 628h
Device-Specific Registers – General-Purpose Input/Output (Offsets 62Ch – 65Ch)		62Ch … 65Ch
Device-Specific Registers – Ingress Control and Port Enable (Offsets 660h – 67Ch)		660h … 67Ch
Device-Specific Registers – IOCAM Base and Limit Upper 16 Bits (Offsets 680h – 6BCh)		680h … 6BCh
Device-Specific Registers – Base Address Shadow (Offsets 6C0h – 73Ch)		6C0h … 73Ch
Device-Specific Registers – Virtual Channel Resource Control Shadow (Offsets 740h – 83Ch)		740h … 83Ch
Reserved		840h – 93Ch
Device-Specific Registers – Ingress Credit Handler Port Pool (Offsets 940h – 94Ch)		940h … 94Ch
Next Capability Offset 2 (000h)	1h PCI Express Extended Capability ID 2 (000Bh)	950h
Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)		… 95Ch
Factory Test Only		960h – 97Ch
Device-Specific Registers – ACS Extended Capability (Offsets 980h – 9FCh)		980h … 9FCh

Table 12-37. Device-Specific Register Map (Offsets 54Ch – F8Ch) *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Device-Specific Registers – Ingress Credit Handler Threshold (Offsets A00h – B7Ch)		A00h … B7Ch
Device-Specific Registers – SerDes Support (Offsets B80h – BFCh)		B80h … BFCh
Reserved		C00h – DFCh
Device-Specific Registers – Port Configuration Header (Offsets E00h – E3Ch)		E00h … E3Ch
Reserved		E40h – EFCh
Device-Specific Registers – Source Queue Weight and Soft Error (Offsets F00h – F30h)		F00h … F30h
Device-Specific Registers – Read Pacing (Offsets F34h – F3Ch)		F34h … F3Ch
Device-Specific Registers – Error Reporting (Offsets F40h – F4Ch)		F40h … F4Ch
Device-Specific Registers – ARI Capability (Offsets F50h – F8Ch)		F50h … F8Ch

12.16.1 Device-Specific Registers – Port Configuration (Offsets 574h – 628h)

This section details the Device-Specific Port Configuration register. Table 12-38 defines the register map.

Table 12-38. Device-Specific Port Configuration Register Map (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Port Configuration				574h
Factory Test Only				578h – 628h

Register 12-189. 574h Port Configuration (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The Port configuration for each Station is provided in Table 12-39. Yellow-highlighted table cells indicate the default Hot Plug Port for each configuration.*				
1:0	**Port Configuration for Station 0** Port Configuration Link width, per Port, for Station 0. The serial EEPROM bit values always override the STRAP_STN0_PORTCFG1 Strapping input (if the serial EEPROM values are loaded; refer to Table 12-39). This register is reset only by a Fundamental Reset (PEX_PERST# assertion). **STRAP_STN0_PORTCFG1 controls the Bit 1 value. Bit 0 value must be 0.** 00b = x4, x4 10b = x8 All other encodings are ***reserved***.	RO	Yes	Set by STRAP_STN0_PORTCFG1 input level
3:2	**Port Configuration for Station 1** Port Configuration Link width, per Port, for Station 1. The serial EEPROM bit values always override the STRAP_STN1_PORTCFG0 Strapping input (if the serial EEPROM values are loaded; refer to Table 12-39). This register is reset only by a Fundamental Reset (PEX_PERST# assertion). **STRAP_STN1_PORTCFG0 controls the Bit 2 value. Bit 3 value must be 1.** 10b = x8 11b = x4, x4 All other encodings are ***reserved***.	RO	Yes	Set by STRAP_STN1_PORTCFG0 input level

Register 12-189. 574h Port Configuration (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
5:4	**Port Configuration for Station 2** Port Configuration Link width, per Port, for Station 2. The serial EEPROM bit values always override the STRAP_STN2_PORTCFG1 Strapping input (if the serial EEPROM values are loaded; refer to Table 12-39). This register is reset only by a Fundamental Reset (PEX_PERST# assertion). **STRAP_STN2_PORTCFG1 controls the Bit 5 value. Bit 4 value must be 0.** 00b = x4, x4 10b = x8 All other encodings are ***reserved***.	RO	Yes	Set by STRAP_STN2_PORTCFG1 input level
7:6	***Reserved***	RsvdP	No	00b
19:8	***Factory Test Only***	RO	Yes	0-0h
23:20	**Native x2 for Station 0** Initializes with serial EEPROM (if present).	RO	Yes	0h
27:24	**Native x2 for Station 1** Initializes with serial EEPROM (if present).	RO	Yes	0h
31:28	**Native x2 for Station 2** Initializes with serial EEPROM (if present).	RO	Yes	0h

Table 12-39. Port Configurations

Port Configuration Strapping STRAP_STN0_PORTCFG1, STRAP_RESERVED4	Port Configuration Register Value Port 0, Offset 574h[23:20, 1:0]	Station 0 Link Width/Port		
		Port 0	Port 1	–
0, 0	0h, 00b	x4	x4	
1, 0	0h, 10b	x8		
Port Configuration Strapping **STRAP_RESERVED7, STRAP_STN1_PORTCFG0**	**Port Configuration Register Value** **Port 0, Offset 574h[27:24, 3:2]**	**Station 1 Link Width/Port**		
		Port 4	**Port 5**	**Port 6**
1, 0	0h, 10b	***Software Only***	x8	
1, 1	0h, 11b	***Software Only***	x4	x4
Port Configuration Strapping **STRAP_STN2_PORTCFG1, STRAP_RESERVED8**	**Port Configuration Register Value** **Port 0, Offset 574h[31:28, 5:4]**	**Station 1 Link Width/Port**		
		Port 8	**Port 9**	**–**
0, 0	0h, 00b	x4	x4	
1, 0	0h, 10b	x8		

12.16.2 Device-Specific Registers – General-Purpose Input/Output (Offsets 62Ch – 65Ch)

This section details the Device-Specific General-Purpose Input/Output (GPIO) Configuration, Status, and Control registers. Table 12-40 defines the register map.

Table 12-40. Device-Specific GPIO Register Map (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
GPIO 0_9 Direction Control				62Ch
GPIO 10_19 Direction Control				630h
Reserved				634h
GPIO 0_19 Input De-Bounce				638h
GPIO 0_11 Input Data				63Ch
Reserved		GPIO 12_19 Input Data		640h
GPIO 0_11 Output Data				644h
Reserved		GPIO 12_19 Output Data		648h
GPIO 0_19 Interrupt Polarity				64Ch
GPIO 0_19 Interrupt Status				650h
GPIO 0_19 Interrupt Mask				654h
Factory Test Only				658h – 65Ch

Register 12-190. 62Ch GPIO 0_9 Direction Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
1:0	**PEX_PORT_GOOD0# Source/Destination** **As Input:** 00b = To **PEX_PORT_GOOD0# Input Data** register (offset 63Ch[0]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **PEX_PORT_GOOD0# Output Data** register (offset 644h[0]) 01b = PEX_PORT_GOOD0# 10b, 11b = ***Reserved***	RWS	Yes	Default is 01b when STRAP_TESTMODE[3:0] =1011b or 1101b, and the Port is enabled Otherwise, default is 00b
2	**PEX_PORT_GOOD0# Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0] =1011b or 1101b, and the Port is enabled Otherwise, default is 0
4:3	**PEX_PORT_GOOD1# Source/Destination** **As Input:** 00b = To **PEX_PORT_GOOD1# Input Data** register (offset 63Ch[1]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **PEX_PORT_GOOD1# Output Data** register (offset 644h[1]) 01b = PEX_PORT_GOOD1# 10b, 11b = ***Reserved***	RWS	Yes	Default is 01b when STRAP_TESTMODE[3:0] =1011b or 1101b, and the Port is enabled Otherwise, default is 00b
5	**PEX_PORT_GOOD1# Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0] =1011b or 1101b, and the Port is enabled Otherwise, default is 0

Register 12-190. 62Ch GPIO 0_9 Direction Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:6	**GPIO2 Source/Destination** **As Input:** 00b = To **GPIO2 Input Data** register (offset 63Ch[2]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO2 Output Data** register (offset 644h[2]) 01b, 10b, 11b = ***Reserved***	RWS	Yes	00b
8	**GPIO2 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
10:9	**GPIO3 Source/Destination** **As Input:** 00b = To **GPIO3 Input Data** register (offset 63Ch[3]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO3 Output Data** register (offset 644h[3]) 01b, 10b, 11b = ***Reserved***	RWS	Yes	00b
11	**GPIO3 Direction Control** 0 = Input 1 = Output	RWS	Yes	0

Register 12-190. 62Ch GPIO 0_9 Direction Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
13:12	**GPIO4 Source/Destination** **As Input:** 00b = To **GPIO4 Input Data** register (offset 63Ch[4]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO4 Output Data** register (offset 644h[4]) 01b, 10b, 11b = ***Reserved***	RWS	Yes	00b
14	**GPIO4 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
16:15	**PEX_PORT_GOOD5# Source/Destination** **As Input:** 00b = To **PEX_PORT_GOOD5# Input Data** register (offset 63Ch[5]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **PEX_PORT_GOOD5# Output Data** register (offset 644h[5]) 01b = PEX_PORT_GOOD5# 10b, 11b = ***Reserved***	RWS	Yes	Default is 01b when STRAP_TESTMODE[3:0] =1011b or 1101b, and the Port is enabled Otherwise, default is 00b
17	**PEX_PORT_GOOD5# Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0] =1011b or 1101b, and the Port is enabled Otherwise, default is 0

Register 12-190. 62Ch GPIO 0_9 Direction Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:18	**PEX_PORT_GOOD6# Source/Destination** **As Input:** 00b = To **PEX_PORT_GOOD6# Input Data** register (offset 63Ch[6]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **PEX_PORT_GOOD6# Output Data** register (offset 644h[6]) 01b = PEX_PORT_GOOD6# 10b, 11b = ***Reserved***	RWS	Yes	Default is 01b when STRAP_TESTMODE[3:0] =1011b or 1101b, and the Port is enabled Otherwise, default is 00b
20	**PEX_PORT_GOOD6# Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0] =1011b or 1101b, and the Port is enabled Otherwise, default is 0
22:21	**GPIO7 Source/Destination** **As Input:** 00b = To **GPIO7 Input Data** register (offset 63Ch[7]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO7 Output Data** register (offset 644h[7]) 01b, 10b, 11b = ***Reserved***	RWS	Yes	00b
23	**GPIO7 Direction Control** 0 = Input 1 = Output	RWS	Yes	0

Register 12-190. 62Ch GPIO 0_9 Direction Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
25:24	**PEX_PORT_GOOD8# Source/Destination** **As Input:** 00b = To **PEX_PORT_GOOD8# Input Data** register (offset 63Ch[8]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **PEX_PORT_GOOD8# Output Data** register (offset 644h[8]) 01b = PEX_PORT_GOOD8# 10b, 11b = ***Reserved***	RWS	Yes	Default is 01b when STRAP_TESTMODE[3:0] =1011b or 1101b, and the Port is enabled Otherwise, default is 00b
26	**PEX_PORT_GOOD8# Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0] =1011b or 1101b, and the Port is enabled Otherwise, default is 0
28:27	**PEX_PORT_GOOD9# Source/Destination** **As Input:** 00b = To **PEX_PORT_GOOD9# Input Data** register (offset 63Ch[9]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **PEX_PORT_GOOD9# Output Data** register (offset 644h[9]) 01b = PEX_PORT_GOOD9# 10b, 11b = ***Reserved***	RWS	Yes	Default is 01b when STRAP_TESTMODE[3:0] =1011b or 1101b, and the Port is enabled Otherwise, default is 00b
29	**PEX_PORT_GOOD9# Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0] =1011b or 1101b, and the Port is enabled Otherwise, default is 0
31:30	***Reserved***	RsvdP	No	00b

Register 12-191. 630h GPIO 10_19 Direction Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
1:0	**GPIO10 Source/Destination** **As Input:** 00b = To **GPIO10 Input Data** register (offset 63Ch[10]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO10 Output Data** register (offset 644h[10]) 01b, 10b, 11b = ***Reserved***	RWS	Yes	00b
2	**GPIO10 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
4:3	**GPIO11 Source/Destination** **As Input:** 00b = To **GPIO11 Input Data** register (offset 63Ch[11]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO11 Output Data** register (offset 644h[11]) 01b, 10b, 11b = ***Reserved***	RWS	Yes	00b
5	**GPIO11 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
7:6	**GPIO12 Source/Destination** **As Input:** 00b = To **GPIO12 Input Data** register (offset 640h[0]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO12 Output Data** register (offset 648h[0]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	Default is 10b when STRAP_TESTMODE[3:0] =1100b or 1101b Otherwise, default is 00b
8	**GPIO12 Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0] =1100b or 1101b Otherwise, default is 0

Register 12-191. 630h GPIO 10_19 Direction Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
10:9	**GPIO13 Source/Destination** **As Input:** 00b = To **GPIO13 Input Data** register (offset 640h[1]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO13 Output Data** register (offset 648h[1]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	Default is 10b when STRAP_TESTMODE[3:0] =1100b or 1101b Otherwise, default is 00b
11	**GPIO13 Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0] =1100b or 1101b Otherwise, default is 0

Register 12-191. 630h GPIO 10_19 Direction Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
13:12	**GPIO14 Source/Destination** **As Input:** 00b = To **GPIO14 Input Data** register (offset 640h[2]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO14 Output Data** register (offset 648h[2]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	Default is 10b when STRAP_TESTMODE[3:0] =1100b or 1101b Otherwise, default is 00b
14	**GPIO14 Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0] =1100b or 1101b Otherwise, default is 0
16:15	**GPIO15 Source/Destination** **As Input:** 00b = To **GPIO15 Input Data** register (offset 640h[3]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO15 Output Data** register (offset 648h[3]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	Default is 10b when STRAP_TESTMODE[3:0] =1100b or 1101b Otherwise, default is 00b
17	**GPIO15 Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0] =1100b or 1101b Otherwise, default is 0
19:18	**GPIO16 Source/Destination** **As Input:** 00b = To **GPIO16 Input Data** register (offset 640h[4]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO16 Output Data** register (offset 648h[4]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	Default is 10b when STRAP_TESTMODE[3:0] =1100b or 1101b Otherwise, default is 00b

Register 12-191. 630h GPIO 10_19 Direction Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
20	**GPIO16 Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0] =1100b or 1101b Otherwise, default is 0
22:21	**GPIO17 Source/Destination** **As Input:** 00b = To **GPIO17 Input Data** register (offset 640h[5]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO17 Output Data** register (offset 648h[5]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	Default is 10b when STRAP_TESTMODE[3:0] =1100b or 1101b Otherwise, default is 00b
23	**GPIO17 Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0] =1100b or 1101b Otherwise, default is 0

Register 12-191. 630h GPIO 10_19 Direction Control (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
25:24	**GPIO18 Source/Destination** **As Input:** 00b = To **GPIO18 Input Data** register (offset 640h[6]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO18 Output Data** register (offset 648h[6]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	Default is 10b when STRAP_TESTMODE[3:0] =1100b or 1101b Otherwise, default is 00b
26	**GPIO18 Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0] =1100b or 1101b Otherwise, default is 0
28:27	**GPIO19 Source/Destination** **As Input:** 00b = To **GPIO19 Input Data** register (offset 640h[7]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO19 Output Data** register (offset 648h[7]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	Default is 10b when STRAP_TESTMODE[3:0] =1100b or 1101b Otherwise, default is 00b
29	**GPIO19 Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0] =1100b or 1101b Otherwise, default is 0
31:30	***Reserved***	RsvdP	No	00b

Register 12-192. 638h GPIO 0_19 Input De-Bounce (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**PEX_PORT_GOOD0# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD0# is configured as an input (offset 62Ch[2], is Cleared). 0 = PEX_PORT_GOOD0# input is not de-bounced 1 = PEX_PORT_GOOD0# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
1	**PEX_PORT_GOOD1# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD1# is configured as an input (offset 62Ch[5], is Cleared). 0 = PEX_PORT_GOOD1# input is not de-bounced 1 = PEX_PORT_GOOD1# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
2	**GPIO2 Input De-Bounce Control** Controls de-bounce when GPIO2 is configured as an input (offset 62Ch[8], is Cleared). 0 = GPIO2 input is not de-bounced 1 = GPIO2 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
3	**GPIO3 Input De-Bounce Control** Controls de-bounce when GPIO3 is configured as an input (offset 62Ch[11], is Cleared). 0 = GPIO3 input is not de-bounced 1 = GPIO3 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
4	**GPIO4 Input De-Bounce Control** Controls de-bounce when GPIO4 is configured as an input (offset 62Ch[14], is Cleared). 0 = GPIO4 input is not de-bounced 1 = GPIO4 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
5	**PEX_PORT_GOOD5# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD5# is configured as an input (offset 62Ch[17], is Cleared). 0 = PEX_PORT_GOOD5# input is not de-bounced 1 = PEX_PORT_GOOD5# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
6	**PEX_PORT_GOOD6# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD6# is configured as an input (offset 62Ch[20], is Cleared). 0 = PEX_PORT_GOOD6# input is not de-bounced 1 = PEX_PORT_GOOD6# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
7	**GPIO7 Input De-Bounce Control** Controls de-bounce when GPIO7 is configured as an input (offset 62Ch[23], is Cleared). 0 = GPIO7 input is not de-bounced 1 = GPIO7 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0

Register 12-192. 638h GPIO 0_19 Input De-Bounce (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**PEX_PORT_GOOD8# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD8# is configured as an input (offset 62Ch[26], is Cleared). 0 = PEX_PORT_GOOD8# input is not de-bounced 1 = PEX_PORT_GOOD8# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
9	**PEX_PORT_GOOD9# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD9# is configured as an input (offset 62Ch[29], is Cleared). 0 = PEX_PORT_GOOD9# input is not de-bounced 1 = PEX_PORT_GOOD9# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
10	**GPIO10 Input De-Bounce Control** Controls de-bounce when GPIO10 is configured as an input (offset 630h[2], is Cleared). 0 = GPIO10 input is not de-bounced 1 = GPIO10 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
11	**GPIO11 Input De-Bounce Control** Controls de-bounce when GPIO11 is configured as an input (offset 630h[5], is Cleared). 0 = GPIO11 input is not de-bounced 1 = GPIO11 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
12	**GPIO12 Input De-Bounce Control** Controls de-bounce when GPIO12 is configured as an input (offset 630h[8], is Cleared). 0 = GPIO12 input is not de-bounced 1 = GPIO12 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
13	**GPIO13 Input De-Bounce Control** Controls de-bounce when GPIO13 is configured as an input (offset 630h[11], is Cleared). 0 = GPIO13 input is not de-bounced 1 = GPIO13 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
14	**GPIO14 Input De-Bounce Control** Controls de-bounce when GPIO14 is configured as an input (offset 630h[14], is Cleared). 0 = GPIO14 input is not de-bounced 1 = GPIO14 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
15	**GPIO15 Input De-Bounce Control** Controls de-bounce when GPIO15 is configured as an input (offset 630h[17], is Cleared). 0 = GPIO15 input is not de-bounced 1 = GPIO15 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0

Register 12-192. 638h GPIO 0_19 Input De-Bounce (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
16	**GPIO16 Input De-Bounce Control** Controls de-bounce when GPIO16 is configured as an input (offset 630h[20], is Cleared). 0 = GPIO16 input is not de-bounced 1 = GPIO16 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
17	**GPIO17 Input De-Bounce Control** Controls de-bounce when GPIO17 is configured as an input (offset 630h[23], is Cleared). 0 = GPIO17 input is not de-bounced 1 = GPIO17 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
18	**GPIO18 Input De-Bounce Control** Controls de-bounce when GPIO18 is configured as an input (offset 630h[26], is Cleared). 0 = GPIO18 input is not de-bounced 1 = GPIO18 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
19	**GPIO19 Input De-Bounce Control** Controls de-bounce when GPIO19 is configured as an input (offset 630h[29], is Cleared). 0 = GPIO19 input is not de-bounced 1 = GPIO19 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
31:20	***Reserved***	RsvdP	No	000h

Register 12-193. 63Ch GPIO 0_11 Input Data (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**PEX_PORT_GOOD0# Input Data** If PEX_PORT_GOOD0# is configured as an output (offset 62Ch[2], is Set), Reads return 0. If PEX_PORT_GOOD0# is configured as an input (offset 62Ch[2], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD0#.	RO	No	0
1	**PEX_PORT_GOOD1# Input Data** If PEX_PORT_GOOD1# is configured as an output (offset 62Ch[5], is Set), Reads return 0. If PEX_PORT_GOOD1# is configured as an input (offset 62Ch[5], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD1#.	RO	No	0
2	**GPIO2 Input Data** If GPIO2 is configured as an output (offset 62Ch[8], is Set), Reads return 0. If GPIO2 is configured as an input (offset 62Ch[8], is Cleared), Reads return the logic value of the voltage on GPIO2.	RO	No	0
3	**GPIO3 Input Data** If GPIO3 is configured as an output (offset 62Ch[11], is Set), Reads return 0. If GPIO3 is configured as an input (offset 62Ch[11], is Cleared), Reads return the logic value of the voltage on GPIO3.	RO	No	0
4	**GPIO4 Input Data** If GPIO4 is configured as an output (offset 62Ch[14], is Set), Reads return 0. If GPIO is configured as an input (offset 62Ch[14], is Cleared), Reads return the logic value of the voltage on GPIO.	RO	No	0
5	**PEX_PORT_GOOD5# Input Data** If PEX_PORT_GOOD5# is configured as an output (offset 62Ch[17], is Set), Reads return 0. If PEX_PORT_GOOD5# is configured as an input (offset 62Ch[17], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD5#.	RO	No	0
6	**PEX_PORT_GOOD6# Input Data** If PEX_PORT_GOOD6# is configured as an output (offset 62Ch[20], is Set), Reads return 0. If PEX_PORT_GOOD6# is configured as an input (offset 62Ch[20], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD6#.	RO	No	0
7	**GPIO7 Input Data** If GPIO7 is configured as an output (offset 62Ch[23], is Set), Reads return 0. If GPIO7 is configured as an input (offset 62Ch[23], is Cleared), Reads return the logic value of the voltage on GPIO7.	RO	No	0

Register 12-193. 63Ch GPIO 0_11 Input Data (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
8	**PEX_PORT_GOOD8# Input Data** If PEX_PORT_GOOD8# is configured as an output (offset 62Ch[26], is Set), Reads return 0. If PEX_PORT_GOOD8# is configured as an input (offset 62Ch[26], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD8#.	RO	No	0
9	**PEX_PORT_GOOD9# Input Data** If PEX_PORT_GOOD9# is configured as an output (offset 62Ch[29], is Set), Reads return 0. If PEX_PORT_GOOD9# is configured as an input (offset 62Ch[29], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD9#.	RO	No	0
10	**GPIO10 Input Data** If GPIO10 is configured as an output (offset 630h[2], is Set), Reads return 0. If GPIO10 is configured as an input (offset 630h[2], is Cleared), Reads return the logic value of the voltage on GPIO10.	RO	No	0
11	**GPIO11 Input Data** If GPIO11 is configured as an output (offset 630h[5], is Set), Reads return 0. If GPIO11 is configured as an input (offset 630h[5], is Cleared), Reads return the logic value of the voltage on GPIO11.	RO	No	0
31:12	***Reserved***	RsvdP	No	0000_0h

Register 12-194. 640h GPIO 12_19 Input Data (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**GPIO12 Input Data** If GPIO12 is configured as an output (offset 630h[8], is Set), Reads return 0. If GPIO12 is configured as an input (offset 630h[8], is Cleared), Reads return the logic value of the voltage on GPIO12.	RO	No	0
1	**GPIO13 Input Data** If GPIO13 is configured as an output (offset 630h[11], is Set), Reads return 0. If GPIO13 is configured as an input (offset 630h[11], is Cleared), Reads return the logic value of the voltage on GPIO13.	RO	No	0
2	**GPIO14 Input Data** If GPIO14 is configured as an output (offset 630h[14], is Set), Reads return 0. If GPIO14 is configured as an input (offset 630h[14], is Cleared), Reads return the logic value of the voltage on GPIO14.	RO	No	0
3	**GPIO15 Input Data** If GPIO15 is configured as an output (offset 630h[17], is Set), Reads return 0. If GPIO15 is configured as an input (offset 630h[17], is Cleared), Reads return the logic value of the voltage on GPIO15.	RO	No	0
4	**GPIO16 Input Data** If GPIO16 is configured as an output (offset 630h[20], is Set), Reads return 0. If GPIO16 is configured as an input (offset 630h[20], is Cleared), Reads return the logic value of the voltage on GPIO16.	RO	No	0
5	**GPIO17 Input Data** If GPIO17 is configured as an output (offset 630h[23], is Set), Reads return 0. If GPIO17 is configured as an input (offset 630h[23], is Cleared), Reads return the logic value of the voltage on GPIO17.	RO	No	0
6	**GPIO18 Input Data** If GPIO18 is configured as an output (offset 630h[26], is Set), Reads return 0. If GPIO18 is configured as an input (offset 630h[26], is Cleared), Reads return the logic value of the voltage on GPIO18.	RO	No	0
7	**GPIO19 Input Data** If GPIO19 is configured as an output (offset 630h[29], is Set), Reads return 0. If GPIO19 is configured as an input (offset 630h[29], is Cleared), Reads return the logic value of the voltage on GPIO19.	RO	No	0
31:8	***Reserved***	RsvdP	No	0-0h

Register 12-195. 644h GPIO 0_11 Output Data (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**PEX_PORT_GOOD0# Output Data** If PEX_PORT_GOOD0# is configured as an output (offset 62Ch[2], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD0# output.	RWS	Yes	0
1	**PEX_PORT_GOOD1# Output Data** If PEX_PORT_GOOD1# is configured as an output (offset 62Ch[5], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD1# output.	RWS	Yes	0
2	**GPIO2 Output Data** If GPIO2 is configured as an output (offset 62Ch[8], is Set), the value written to this bit is immediately driven to the GPIO2 output.	RWS	Yes	0
3	**GPIO3 Output Data** If GPIO3 is configured as an output (offset 62Ch[11], is Set), the value written to this bit is immediately driven to the GPIO3 output.	RWS	Yes	0
4	**GPIO4 Output Data** If GPIO4 is configured as an output (offset 62Ch[14], is Set), the value written to this bit is immediately driven to the GPIO4 output.	RWS	Yes	0
5	**PEX_PORT_GOOD5# Output Data** If PEX_PORT_GOOD5# is configured as an output (offset 62Ch[17], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD5# output.	RWS	Yes	0
6	**PEX_PORT_GOOD6# Output Data** If PEX_PORT_GOOD6# is configured as an output (offset 62Ch[20], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD6# output.	RWS	Yes	0
7	**GPIO7 Output Data** If GPIO7 is configured as an output (offset 62Ch[23], is Set), the value written to this bit is immediately driven to the GPIO7 output.	RWS	Yes	0
8	**PEX_PORT_GOOD8# Output Data** If PEX_PORT_GOOD8# is configured as an output (offset 62Ch[26], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD8# output.	RWS	Yes	0
9	**PEX_PORT_GOOD9# Output Data** If PEX_PORT_GOOD9# is configured as an output (offset 62Ch[29], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD9# output.	RWS	Yes	0
10	**GPIO10 Output Data** If GPIO10 is configured as an output (offset 630h[2], is Set), the value written to this bit is immediately driven to the GPIO10 output.	RWS	Yes	0
11	**GPIO11 Output Data** If GPIO11 is configured as an output (offset 630h[5], is Set), the value written to this bit is immediately driven to the GPIO11 output.	RWS	Yes	0
31:12	***Reserved***	RsvdP	No	0000_0h

Register 12-196. 648h GPIO 12_19 Output Data (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**GPIO12 Output Data** If GPIO12 is configured as an output (offset 630h[8], is Set), the value written to this bit is immediately driven to the GPIO12 output.	RWS	Yes	0
1	**GPIO13 Output Data** If GPIO13 is configured as an output (offset 630h[11], is Set), the value written to this bit is immediately driven to the GPIO13 output.	RWS	Yes	0
2	**GPIO14 Output Data** If GPIO14 is configured as an output (offset 630h[14], is Set), the value written to this bit is immediately driven to the GPIO14 output.	RWS	Yes	0
3	**GPIO15 Output Data** If GPIO15 is configured as an output (offset 630h[17], is Set), the value written to this bit is immediately driven to the GPIO15 output.	RWS	Yes	0
4	**GPIO16 Output Data** If GPIO16 is configured as an output (offset 630h[20], is Set), the value written to this bit is immediately driven to the GPIO16 output.	RWS	Yes	0
5	**GPIO17 Output Data** If GPIO17 is configured as an output (offset 630h[23], is Set), the value written to this bit is immediately driven to the GPIO17 output.	RWS	Yes	0
6	**GPIO18 Output Data** If GPIO18 is configured as an output (offset 630h[26], is Set), the value written to this bit is immediately driven to the GPIO18 output.	RWS	Yes	0
7	**GPIO19 Output Data** If GPIO19 is configured as an output (offset 630h[29], is Set), the value written to this bit is immediately driven to the GPIO19 output.	RWS	Yes	0
31:8	***Reserved***	RsvdP	No	0-0h

Register 12-197. 64Ch GPIO 0_19 Interrupt Polarity (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	**GPIO Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the corresponding PEX_PORT_GOOD*x*# or GPIO*x* signal. Refer to Table 12-41 for the PEX_PORT_GOOD*x*# and GPIO*x* signal relationship. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0_0000h
31:20	***Reserved***	RsvdP	No	000h

Register 12-198. 650h GPIO 0_19 Interrupt Status (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	**GPIO Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the corresponding PEX_PORT_GOOD*x*# or GPIO*x* signal. Refer to Table 12-41 for the PEX_PORT_GOOD*x*# and GPIO*x* signal relationship. 0 = GPIO interrupt is inactive 1 = GPIO interrupt is active	RO	No	0_0000h
31:20	***Reserved***	RsvdP	No	000h

Register 12-199. 654h GPIO 0_19 Interrupt Mask (Only Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	**GPIO Interrupt Mask** Indicates whether GPIO interrupts are masked or not masked for the corresponding PEX_PORT_GOOD*x*# or GPIO*x* signal. Refer to Table 12-41 for the PEX_PORT_GOOD*x*# and GPIO*x* signal relationship. 0 = GPIO interrupt is not masked 1 = GPIO interrupt is masked	RWS	Yes	0_0000h
31:20	***Reserved***	RsvdP	No	000h

Table 12-41. Bit to PEX_PORT_GOOD*x*# and GPIO*x* Signal Relationship, for Register Offsets 64Ch, 650h, and 654h

Bit	Controls Signal
0	PEX_PORT_GOOD0#
1	PEX_PORT_GOOD1#
2	GPIO2
3	GPIO3
4	GPIO4
5	PEX_PORT_GOOD5#
6	PEX_PORT_GOOD6#
7	GPIO7
8	PEX_PORT_GOOD8#
9	PEX_PORT_GOOD9#
10	GPIO10
11	GPIO11
12	GPIO12
13	GPIO13
14	GPIO14
15	GPIO15
16	GPIO16
17	GPIO17
18	GPIO18
19	GPIO19

12.16.3 Device-Specific Registers – Ingress Control and Port Enable (Offsets 660h – 67Ch)

This section details the Device-Specific Ingress Control and Port Enable registers, which also include the **Negotiated Link Width**, and **Port Cut-Thru Enable Status** registers. Table 12-42 defines the register map.

Table 12-42. Device-Specific Ingress Control and Port Enable Register Map[a] [b]

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Ingress Control				660h
Ingress Control Shadow				664h
Port Enable Status				668h
Negotiated Link Width for Ports 0, 1, 5, 6				66Ch
Reserved		***Factory Test Only***	Negotiated Link Width for Ports 8, 9	670h
Port Cut-Thru Enable Status				674h
Factory Test Only				678h
Reserved				67Ch

a. Some registers in this structure are available in both the NT Port Virtual and Link Interfaces; others are available only in the NT Port Virtual Interface. Refer to the individual registers for details.

b. Register offset 674h is available in all Ports.

Register 12-200. 660h Ingress Control (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
22:0	***Factory Test Only***	RWS	Yes	0-0h
23	**Expansion ROM Virtual Side** 0 = Expansion ROM is located on the NT Port Link Interface 1 = Expansion ROM is located on the NT Port Virtual Interface	RWS	Yes	0
25:24	***Factory Test Only***	RWS	Yes	00b
26	**Disable Upstream Port BAR0 and BAR1** Valid for the NT Port if the upstream Port is in Station 0. 0 = Enables the upstream Port **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, Upstream Port, offsets 10h and 14h, respectively) 1 = Disables the upstream Port **BAR0** and **BAR1**	RWS	Yes	0
27	***Not used***	RWS	Yes	0
28	**Disable VGA BIOS Memory Access Decoding** Valid for the NT Port if the upstream Port is in Station 0. 0 = Enables the **Bridge Control** register *VGA 16-Bit Decode Enable*, *VGA Enable*, and *ISA Enable* bits (offset 3Ch[20:18], respectively), and enables decoding of the PC ROM shadow addresses C_0000h to C_FFFFh (packets destined to these addresses are blocked) 1 = Disables the **Bridge Control** register *VGA 16-Bit Decode Enable*, *VGA Enable*, and *ISA Enable* bits (offset 3Ch[20:18], respectively), and disables decoding of the PC ROM shadow addresses C_0000h to C_FFFFh (packets destined to these addresses are ***not*** blocked)	RWS	Yes	1
30:29	***Factory Test Only***	RWS	Yes	00b
31	***Not used***	RWS	Yes	0

Register 12-201. 664h Ingress Control Shadow (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	***Reserved***	RsvdP	No	0
1	**Use Serial EEPROM Values for Ingress Credit Initialization** Allow Configuration with a Device Number that is not 0, that is accessing downstream devices, to be forwarded. When the Device Number is 0, the Configuration terminates in a UR. 0 = Use default values for ingress credit initialization 1 = Use serial EEPROM values for ingress credit initialization	RWS	Yes	0
3:2	***Factory Test Only***	RWS	Yes	00b
4	**Drop EP TLPs** Drop Endpoint TLPs. 1 = Endpoint TLP was dropped	RWS	Yes	0
5	**No Special Treatment for Relaxed Ordering Traffic** The PEX 8624 supports Relaxed Ordering for Completions. By default, if the RO attribute is Set within a Completion, then that Completion can bypass Posted transactions, if Posted TLPs are blocked at the egress Port (due to insufficient Posted credits from the connected device). This behavior can be disabled by Setting this bit, in each Station. 1 = Device-Specific Relaxed Ordering Completion will not be flagged to the egress block	RWS	Yes	0
7:6	***Factory Test Only***	RWS	Yes	00b
8	**Drop ECRC TLPs** Drop End-to-end Cyclic Redundancy Check (ECRC) TLPs. 1 = ECRC TLP was dropped	RWS	Yes	0
10:9	**ACK TLP Counter Timeout** Sets the number of ingress TLP Acknowledges (ACKs) pending, which causes a high-priority ACK to be sent. 00b = 16 TLPs 01b = 8 TLPs 10b = 4 TLPs 11b = Feature is disabled	RWS	Yes	00b
14:11	***Factory Test Only***	RWS	Yes	0-0h
15	**INCH Credit Reserve Flag** A transition from 0 to 1 indicates that I^2C has finished with all CSR to INCH Initialization registers, and credit reservation can proceed.	RWS	Yes	0

Register 12-201. 664h Ingress Control Shadow (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
19:16	***Factory Test Only***	RWS	Yes	0h
20	**Ingress MWr32 Counter Disable** 0 = Enables Ingress Memory Write 32-Bit Counter 1 = Disables Ingress Memory Write 32-Bit Counter	RWS	Yes	0
21	**Ingress MWr64 Counter Disable** 0 = Enables Ingress Memory Write 64-Bit Counter 1 = Disables Ingress Memory Write 64-Bit Counter	RWS	Yes	0
22	**Ingress MSG Counter Disable** 0 = Enables Ingress Message Counter 1 = Disables Ingress Message Counter	RWS	Yes	0
23	**Ingress MRd32 Counter Disable** 0 = Enables Ingress Memory Read 32-Bit Counter 1 = Disables Ingress Memory Read 32-Bit Counter	RWS	Yes	0
24	**Ingress MRd64 Counter Disable** 0 = Enables Ingress Memory Read 64-Bit Counter 1 = Disables Ingress Memory Read 64-Bit Counter	RWS	Yes	0
25	**Ingress Other Non-Posted Counter Disable** 0 = Enables Ingress Other Non-Posted Counter 1 = Disables Ingress Other Non-Posted Counter	RWS	Yes	0
26	**Ingress and Egress DLLP ACK Counter Disable** 0 = Enables Ingress and Egress DLLP ACK Counter 1 = Disables Ingress and Egress DLLP ACK Counter	RWS	Yes	0
27	**Ingress and Egress DLLP UpdateFC-P Counter Disable** 0 = Enables Ingress and Egress DLLP UpdateFC-Posted Counter 1 = Disables Ingress and Egress DLLP UpdateFC-Posted Counter	RWS	Yes	0
28	**Ingress and Egress DLLP UpdateFC-NP Counter Disable** 0 = Enables Ingress and Egress DLLP UpdateFC-Non-Posted Counter 1 = Disables Ingress and Egress DLLP UpdateFC-Non-Posted Counter	RWS	Yes	0
29	**Ingress and Egress DLLP UpdateFC-CPL Counter Disable** 0 = Enables Ingress and Egress DLLP UpdateFC-Completion Counter 1 = Disables Ingress and Egress DLLP UpdateFC-Completion Counter	RWS	Yes	0
31:30	***Not used***	RWS	Yes	00b

Register 12-202. 668h Port Enable Status (Only Ports 0, 4, and 8, and also NT Port if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Notes: *The value of this register depends upon the Port configuration (refer to Table 12-43 for a sample mapping). Yellow-highlighted table cells indicate the default Hot Plug Port for each configuration.* *This register, in all Stations (Ports 0, 4, and 8), must be programmed to the same value, to reflect the configuration of all Ports.*				
0	**Port 0 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	Set by STRAP_STN0_PORTCFG1 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 0* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[1:0])
1	**Port 1 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	Set by STRAP_STN0_PORTCFG1 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 0* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[1:0])
4:2	***Factory Test Only***	RsvdP	No	000b
5	**Port 5 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	Set by STRAP_STN1_PORTCFG0 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 1* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[3:2])
6	**Port 6 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	Set by STRAP_STN1_PORTCFG0 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 1* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[3:2])
7	***Factory Test Only***	RsvdP	No	0
8	**Port 8 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	Set by STRAP_STN2_PORTCFG1 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 2* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[5:4])
9	**Port 9 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	Set by STRAP_STN2_PORTCFG1 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 2* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[5:4])
11:10	***Factory Test Only***	RsvdP	No	00b
31:12	***Reserved***	RsvdP	No	0000_0h

Table 12-43. Port Configurations

Port Configuration Strapping STRAP_STN0_PORTCFG1, STRAP_RESERVED4	Port Configuration Register Value Port 0, Offset 574h[23:20, 1:0]	Station 0 Link Width/Port			Port Enable Status Register Value (Port 0, 4, or 8, and also NT Port if Port 0 is the NT Port, Offset 668h)
		Port 0	Port 1	–	
0, 0	0h, 00b	x4	x4		Program the upper 16 bits to FFFFh. To determine the value for the lower 16 bits, start with 0h and Set only those bit positions that correspond to the enabled Ports. Bits [15:10, 7, 4:2] must be Cleared. Program the same values into each Station Port – Ports 0, 4, and 8.
1, 0	0h, 10b	x8			
Port Configuration Strapping **STRAP_RESERVED7, STRAP_STN1_PORTCFG0**	**Port Configuration Register Value** **Port 0, Offset 574h[27:24, 3:2]**	**Station 1 Link Width/Port**			
		Port 4	**Port 5**	**Port 6**	
1, 0	0h, 10b	***Software Only***	x8		
1, 1	0h, 11b	***Software Only***	x4	x4	
Port Configuration Strapping **STRAP_STN2_PORTCFG1, STRAP_RESERVED8**	**Port Configuration Register Value** **Port 0, Offset 574h[31:28, 5:4]**	**Station 1 Link Width/Port**			
		Port 8	**Port 9**	**–**	
0, 0	0h, 00b	x4	x4		
1, 0	0h, 10b	x8			

Register 12-203. 66Ch Negotiated Link Width for Ports 0, 1, 5, 6 (Only Ports 0, 4, and 8, and also NT Port if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
2:0	**Negotiated Link Width for Port 0** 000b = x1 001b = x2 010b = x4 011b = x8 All other encodings are ***reserved***.	RO	No	000b
3	**Link Speed for Port 0** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
6:4	**Negotiated Link Width for Port 1** 000b = x1 001b = x2 010b = x4 All other encodings are ***reserved***.	RO	No	000b
7	**Valid Negotiated Link Width for Port 1** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
15:8	***Factory Test Only***	RsvdP	No	00h
19:16	***Factory Test Only***	RO	No	0h
22:20	**Negotiated Link Width for Port 5** 000b = x1 001b = x2 010b = x4 011b = x8 All other encodings are ***reserved***.	RO	No	000b
23	**Valid Negotiated Link Width for Port 5** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
26:24	**Negotiated Link Width for Port 6** 000b = x1 001b = x2 010b = x4 All other encodings are ***reserved***.	RO	No	000b
27	**Valid Negotiated Link Width for Port 6** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
31:28	***Factory Test Only***	RsvdP	No	0h

Register 12-204. 670h Negotiated Link Width for Ports 8, 9 (Only Ports 0, 4, and 8, and also NT Port if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
2:0	**Negotiated Link Width for Port 8** 000b = x1 001b = x2 010b = x4 011b = x8 All other encodings are ***reserved***.	RO	No	000b
3	**Valid Negotiated Link Width for Port 8** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
6:4	**Negotiated Link Width for Port 9** 000b = x1 001b = x2 010b = x4 All other encodings are ***reserved***.	RO	No	000b
7	**Valid Negotiated Link Width for Port 9** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
15:8	***Factory Test Only***	RsvdP	No	00h
31:16	***Reserved***	RsvdP	No	0000h

Register 12-205. 674h Port Cut-Thru Enable Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Port 0 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	Set by STRAP_STN0_PORTCFG1 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 0* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[1:0])
1	**Port 1 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	Set by STRAP_STN0_PORTCFG1 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 0* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[1:0])
4:2	***Factory Test Only***	RsvdP	No	000b
5	**Port 5 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	Set by STRAP_STN1_PORTCFG0 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 1* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[3:2])
6	**Port 6 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	Set by STRAP_STN1_PORTCFG0 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 1* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[3:2])
7	***Factory Test Only***	RsvdP	No	0
8	**Port 8 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	Set by STRAP_STN2_PORTCFG1 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 2* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[5:4])
9	**Port 9 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	Set by STRAP_STN2_PORTCFG1 input level, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 2* field (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[5:4])
11:10	***Factory Test Only***	RsvdP	No	00b
31:12	***Reserved***	RsvdP	No	0000_0h

12.16.4 Device-Specific Registers – IOCAM Base and Limit Upper 16 Bits (Offsets 680h – 6BCh)

This section details the Device-Specific IOCAM Base and Limit Upper 16-Bit registers. Table 12-44 defines the register map.

Table 12-44. Device-Specific IOCAM Base and Limit Upper 16 Bits Register Map (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
IOCAM UP 0		680h
IOCAM UP 1		684h
Factory Test Only		688h – 68Ch
IOCAM UP 4		690h
IOCAM UP 5		694h
IOCAM UP 6		698h
Factory Test Only		69Ch
IOCAM UP 8		6A0h
IOCAM UP 9		6A4h
Factory Test Only		6A8h – 6ACh
Reserved		6B0h – 6BCh

Register 12-206. 680h IOCAM UP 0 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**I/O Base Upper 16 Bits** I/O Base Upper 16 bits, IOCAM Base[31:16].	RW	Yes	0000h
31:16	**I/O Limit Upper 16 Bits** I/O Limit Upper 16 bits, IOCAM Limit[31:16].	RW	Yes	0000h

Register 12-207. 684h IOCAM UP 1 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**I/O Base Upper 16 Bits** I/O Base Upper 16 bits, IOCAM Base[31:16].	RW	Yes	0000h
31:16	**I/O Limit Upper 16 Bits** I/O Limit Upper 16 bits, IOCAM Limit[31:16].	RW	Yes	0000h

Register 12-208. 690h IOCAM UP 4 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**I/O Base Upper 16 Bits** I/O Base Upper 16 bits, IOCAM Base[31:16].	RW	Yes	0000h
31:16	**I/O Limit Upper 16 Bits** I/O Limit Upper 16 bits, IOCAM Limit[31:16].	RW	Yes	0000h

Register 12-209. 694h IOCAM UP 5 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**I/O Base Upper 16 Bits** I/O Base Upper 16 bits, IOCAM Base[31:16].	RW	Yes	0000h
31:16	**I/O Limit Upper 16 Bits** I/O Limit Upper 16 bits, IOCAM Limit[31:16].	RW	Yes	0000h

Register 12-210. 698h IOCAM UP 6 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**I/O Base Upper 16 Bits** I/O Base Upper 16 bits, IOCAM Base[31:16].	RW	Yes	0000h
31:16	**I/O Limit Upper 16 Bits** I/O Limit Upper 16 bits, IOCAM Limit[31:16].	RW	Yes	0000h

Register 12-211. 6A0h IOCAM UP 8 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**I/O Base Upper 16 Bits** I/O Base Upper 16 bits, IOCAM Base[31:16].	RW	Yes	0000h
31:16	**I/O Limit Upper 16 Bits** I/O Limit Upper 16 bits, IOCAM Limit[31:16].	RW	Yes	0000h

Register 12-212. 6A4h IOCAM UP 9 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**I/O Base Upper 16 Bits** I/O Base Upper 16 bits, IOCAM Base[31:16].	RW	Yes	0000h
31:16	**I/O Limit Upper 16 Bits** I/O Limit Upper 16 bits, IOCAM Limit[31:16].	RW	Yes	0000h

12.16.5 Device-Specific Registers – Base Address Shadow (Offsets 6C0h – 73Ch)

This section details the Device-Specific Base Address Shadow registers, which are a shadow copy of the two Type 1 Configuration Base Address registers (**BAR0** and **BAR1**) for each Port. Table 12-45 defines the register map.

Table 12-45. Device-Specific BAR Shadow Register Map (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
BAR0 Shadow for Port 0	6C0h
BAR1 Shadow for Port 0	6C4h
BAR0 Shadow for Port 1	6C8h
BAR1 Shadow for Port 1	6CCh
Factory Test Only	6D0h – 6DCh
BAR0 Shadow for Port 4	6E0h
BAR1 Shadow for Port 4	6E4h
BAR0 Shadow for Port 5	6E8h
BAR1 Shadow for Port 5	6ECh
BAR0 Shadow for Port 6	6F0h
BAR1 Shadow for Port 6	6F4h
Factory Test Only	6F8h – 6FCh
BAR0 Shadow for Port 8	700h
BAR1 Shadow for Port 8	704h
BAR0 Shadow for Port 9	708h
BAR1 Shadow for Port 9	70Ch
Factory Test Only	710h – 71Ch
Reserved	720h – 73Ch

Register 12-213. 6C0h BAR0 Shadow for Port 0 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Memory Space Indicator** 0 = Memory BAR ***Note:*** *Hardwired to 0.*	RO	No	0
2:1	**Memory Map Type** Memory Mapping for Port 0. 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Not Prefetchable 1 = Prefetchable ***Note:*** *Hardwired to 0.*	RO	Yes	0
16:4	***Reserved***	RsvdP	No	000h
31:17	**Base Address 0** Shadow copy of Port 0 Base Address 0.	RW	Yes	0000h

Register 12-214. 6C4h BAR1 Shadow for Port 0 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Base Address 1[63:32]** When the **BAR0 Shadow for Port 0** register *Memory Map Type* field (offset 6C0h[2:1]) is programmed to 10b, 64-bit mode is enabled and this register becomes a Shadow copy of Port 0 Base Address 1[63:32].	RW	Yes	0000_0000h
	Reserved when the **BAR0 Shadow for Port 0** register *Memory Map Type* field (offset 6C0h[2:1]) is not programmed to 10b.	RsvdP	Yes	0000_0000h

Register 12-215. 6C8h BAR0 Shadow for Port 1 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Memory Space Indicator** 0 = Memory BAR ***Note:*** *Hardwired to 0.*	RO	No	0
2:1	**Memory Map Type** Memory Mapping for Port 1. 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Not Prefetchable 1 = Prefetchable ***Note:*** *Hardwired to 0.*	RO	Yes	0
16:4	***Reserved***	RsvdP	No	000h
31:17	**Base Address 0** Shadow copy of Port 1 Base Address 0.	RW	Yes	0000h

Register 12-216. 6CCh BAR1 Shadow for Port 1 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Base Address 1[63:32]** When the **BAR0 Shadow for Port 1** register *Memory Map Type* field (offset 6C8h[2:1]) is programmed to 10b, 64-bit mode is enabled and this register becomes a Shadow copy of Port 1 Base Address 1[63:32].	RW	Yes	0000_0000h
	Reserved when the **BAR0 Shadow for Port 1** register *Memory Map Type* field (offset 6C8h[2:1]) is not programmed to 10b.	RsvdP	Yes	0000_0000h

Register 12-217. 6E0h BAR0 Shadow for Port 4 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Memory Space Indicator** 0 = Memory BAR ***Note:*** *Hardwired to 0.*	RO	No	0
2:1	**Memory Map Type** Memory Mapping for Port 4. 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Not Prefetchable 1 = Prefetchable ***Note:*** *Hardwired to 0.*	RO	Yes	0
16:4	***Reserved***	RsvdP	No	000h
31:17	**Base Address 0** Shadow copy of Port 4 Base Address 0.	RW	Yes	0000h

Register 12-218. 6E4h BAR1 Shadow for Port 4 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Base Address 1[63:32]** When the **BAR0 Shadow for Port 4** register *Memory Map Type* field (offset 6E0h[2:1]) is programmed to 10b, 64-bit mode is enabled and this register becomes a Shadow copy of Port 4 Base Address 1[63:32].	RW	Yes	0000_0000h
	Reserved when the **BAR0 Shadow for Port 4** register *Memory Map Type* field (offset 6E0h[2:1]) is not programmed to 10b.	RsvdP	Yes	0000_0000h

Register 12-219. 6E8h BAR0 Shadow for Port 5 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Memory Space Indicator** 0 = Memory BAR ***Note:*** *Hardwired to 0.*	RO	No	0
2:1	**Memory Map Type** Memory Mapping for Port 5. 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Not Prefetchable 1 = Prefetchable ***Note:*** *Hardwired to 0.*	RO	Yes	0
16:4	***Reserved***	RsvdP	No	000h
31:17	**Base Address 0** Shadow copy of Port 5 Base Address 0.	RW	Yes	0000h

Register 12-220. 6ECh BAR1 Shadow for Port 5 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Base Address 1[63:32]** When the **BAR0 Shadow for Port 5** register *Memory Map Type* field (offset 6E8h[2:1]) is programmed to 10b, 64-bit mode is enabled and this register becomes a Shadow copy of Port 5 Base Address 1[63:32].	RW	Yes	0000_0000h
	Reserved when the **BAR0 Shadow for Port 5** register *Memory Map Type* field (offset 6E8h[2:1]) is not programmed to 10b.	RsvdP	Yes	0000_0000h

Register 12-221. 6F0h BAR0 Shadow for Port 6 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Memory Space Indicator** 0 = Memory BAR ***Note:*** *Hardwired to 0.*	RO	No	0
2:1	**Memory Map Type** Memory Mapping for Port 6. 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Not Prefetchable 1 = Prefetchable ***Note:*** *Hardwired to 0.*	RO	Yes	0
16:4	***Reserved***	RsvdP	No	000h
31:17	**Base Address 0** Shadow copy of Port 6 Base Address 0.	RW	Yes	0000h

Register 12-222. 6F4h BAR1 Shadow for Port 6 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Base Address 1[63:32]** When the **BAR0 Shadow for Port 6** register *Memory Map Type* field (offset 6F0h[2:1]) is programmed to 10b, 64-bit mode is enabled and this register becomes a Shadow copy of Port 6 Base Address 1[63:32].	RW	Yes	0000_0000h
	Reserved when the **BAR0 Shadow for Port 6** register *Memory Map Type* field (offset 6F0h[2:1]) is not programmed to 10b.	RsvdP	Yes	0000_0000h

Register 12-223. 700h BAR0 Shadow for Port 8 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Memory Space Indicator** 0 = Memory BAR ***Note:*** *Hardwired to 0.*	RO	No	0
2:1	**Memory Map Type** Memory Mapping for Port 8. 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Not Prefetchable 1 = Prefetchable ***Note:*** *Hardwired to 0.*	RO	Yes	0
16:4	***Reserved***	RsvdP	No	000h
31:17	**Base Address 0** Shadow copy of Port 8 Base Address 0.	RW	Yes	0000h

Register 12-224. 704h BAR1 Shadow for Port 8 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Base Address 1[63:32]** When the **BAR0 Shadow for Port 8** register *Memory Map Type* field (offset 700h[2:1]) is programmed to 10b, 64-bit mode is enabled and this register becomes a Shadow copy of Port 8 Base Address 1[63:32].	RW	Yes	0000_0000h
	Reserved when the **BAR0 Shadow for Port 8** register *Memory Map Type* field (offset 700h[2:1]) is not programmed to 10b.	RsvdP	Yes	0000_0000h

Register 12-225. 708h BAR0 Shadow for Port 9 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Memory Space Indicator** 0 = Memory BAR ***Note:*** *Hardwired to 0.*	RO	No	0
2:1	**Memory Map Type** Memory Mapping for Port 9. 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Not Prefetchable 1 = Prefetchable ***Note:*** *Hardwired to 0.*	RO	Yes	0
16:4	***Reserved***	RsvdP	No	000h
31:17	**Base Address 0** Shadow copy of Port 9 Base Address 0.	RW	Yes	0000h

Register 12-226. 70Ch BAR1 Shadow for Port 9 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Base Address 1[63:32]** When the **BAR0 Shadow for Port 9** register *Memory Map Type* field (offset 708h[2:1]) is programmed to 10b, 64-bit mode is enabled and this register becomes a Shadow copy of Port 9 Base Address 1[63:32].	RW	Yes	0000_0000h
	Reserved when the **BAR0 Shadow for Port 9** register *Memory Map Type* field (offset 708h[2:1]) is not programmed to 10b.	RsvdP	Yes	0000_0000h

12.16.6 Device-Specific Registers – Virtual Channel Resource Control Shadow (Offsets 740h – 83Ch)

This section details the Device-Specific Virtual Channel (VC) Resource Control Shadow registers, for each Port, which shadow register offset 15Ch. Table 12-46 defines the register map.

Table 12-46. Device-Specific VC Resource Control Shadow Register Map (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Port 0 VC0 Resource Control	740h
Reserved	744h
Port 1 VC0 Resource Control	748h
Reserved	74Ch
Factory Test Only/Reserved	750h – 75Ch
Port 4 VC0 Resource Control	760h
Reserved	764h
Port 5 VC0 Resource Control	768h
Reserved	76Ch
Port 6 VC0 Resource Control	770h
Reserved	774h
Factory Test Only/Reserved	778h – 77Ch
Port 8 VC0 Resource Control	780h
Reserved	784h
Port 9 VC0 Resource Control	788h
Reserved	78Ch
Factory Test Only/Reserved	790h – 798h
Reserved	79Ch – 83Ch

Register 12-227. 740h Port 0 VC0 Resource Control (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
0	**TC/VC Map** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped to VC0.		RO	No	1
7:1	Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.		RW	Yes	7Fh
15:8	***Reserved***		RsvdP	No	00h
16	**Load Port Arbitration Table** Software writes this bit, to load the updated WRR Port Arbitration Table value to the internal logic. Software Read always returns 0.		RW	Yes	0
19:17	**Port Arbitration Select** Selects the Port Arbitration type for Port 0. Indicates the bit number in the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[1:0]) that corresponds to the arbitration type. 0 = Round-Robin (Hardware-Fixed) arbitration scheme 1 = Weighted Round-Robin with 32 Phases ***Note:*** *This field's value is 001b for upstream Port 0, and 000b for all other Ports.*	Upstream Port 0 (refer to Note)	RW	Yes	001b
		All other Ports	RW	Yes	000b
23:20	***Reserved***		RsvdP	No	0h
24	**VC ID** Defines the Port 0 VC0 ID code. Cleared, because VC0 is the only/default VC.		RO	No	0
30:25	***Reserved***		RsvdP	No	0-0h
31	**VC Enable** 0 = Not allowed 1 = Enables Port 0 VC0		RO	No	1

Register 12-228. 748h Port 1 VC0 Resource Control (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
0	**TC/VC Map** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped to VC0. Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.		RO	No	1
7:1			RW	Yes	7Fh
15:8	***Reserved***		RsvdP	No	00h
16	**Load Port Arbitration Table** Software writes this bit, to load the updated WRR Port Arbitration Table value to the internal logic. Software Read always returns 0.		RW	Yes	0
19:17	**Port Arbitration Select** Selects the Port Arbitration type for Port 1. Indicates the bit number in the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[1:0]) that corresponds to the arbitration type. 0 = Round-Robin (Hardware-Fixed) arbitration scheme 1 = Weighted Round-Robin with 32 Phases ***Note:*** *This field's value is 001b for upstream Port 0, and 000b for all other Ports.*	Upstream Port 0 (refer to Note)	RW	Yes	001b
		All other Ports	RW	Yes	000b
23:20	***Reserved***		RsvdP	No	0h
24	**VC ID** Defines the Port 1 VC0 ID code. Cleared, because VC0 is the only/default VC.		RO	No	0
30:25	***Reserved***		RsvdP	No	0-0h
31	**VC Enable** 0 = Not allowed 1 = Enables Port 1 VC0		RO	No	1

Register 12-229. 760h Port 4 VC0 Resource Control (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
0	**TC/VC Map** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped to VC0.		RO	No	1
7:1	Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.		RW	Yes	7Fh
15:8	***Reserved***		RsvdP	No	00h
16	**Load Port Arbitration Table** Software writes this bit, to load the updated WRR Port Arbitration Table value to the internal logic. Software Read always returns 0.		RW	Yes	0
19:17	**Port Arbitration Select** Selects the Port Arbitration type for Port 4. Indicates the bit number in the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[1:0]) that corresponds to the arbitration type. 0 = Round-Robin (Hardware-Fixed) arbitration scheme 1 = Weighted Round-Robin with 32 Phases ***Note:*** *This field's value is 001b for upstream Port 0, and 000b for all other Ports.*	Upstream Port 0 (refer to Note)	RW	Yes	001b
		All other Ports	RW	Yes	000b
23:20	***Reserved***		RsvdP	No	0h
24	**VC ID** Defines the Port 4 VC0 ID code. Cleared, because VC0 is the only/default VC.		RO	No	0
30:25	***Reserved***		RsvdP	No	0-0h
31	**VC Enable** 0 = Not allowed 1 = Enables Port 4 VC0		RO	No	1

Register 12-230. 768h Port 5 VC0 Resource Control (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
0	**TC/VC Map** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped to VC0.		RO	No	1
7:1	Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.		RW	Yes	7Fh
15:8	***Reserved***		RsvdP	No	00h
16	**Load Port Arbitration Table** Software writes this bit, to load the updated WRR Port Arbitration Table value to the internal logic. Software Read always returns 0.		RW	Yes	0
19:17	**Port Arbitration Select** Selects the Port Arbitration type for Port 5. Indicates the bit number in the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[1:0]) that corresponds to the arbitration type. 0 = Round-Robin (Hardware-Fixed) arbitration scheme 1 = Weighted Round-Robin with 32 Phases ***Note:*** *This field's value is 001b for upstream Port 0, and 000b for all other Ports.*	Upstream Port 0 (refer to Note)	RW	Yes	001b
		All other Ports	RW	Yes	000b
23:20	***Reserved***		RsvdP	No	0h
24	**VC ID** Defines the Port 5 VC0 ID code. Cleared, because VC0 is the only/default VC.		RO	No	0
30:25	***Reserved***		RsvdP	No	0-0h
31	**VC Enable** 0 = Not allowed 1 = Enables Port 5 VC0		RO	No	1

Register 12-231. 770h Port 6 VC0 Resource Control (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
0	**TC/VC Map** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped to VC0.		RO	No	1
7:1	Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.		RW	Yes	7Fh
15:8	***Reserved***		RsvdP	No	00h
16	**Load Port Arbitration Table** Software writes this bit, to load the updated WRR Port Arbitration Table value to the internal logic. Software Read always returns 0.		RW	Yes	0
19:17	**Port Arbitration Select** Selects the Port Arbitration type for Port 6. Indicates the bit number in the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[1:0]) that corresponds to the arbitration type. 0 = Round-Robin (Hardware-Fixed) arbitration scheme 1 = Weighted Round-Robin with 32 Phases ***Note:*** *This field's value is 001b for upstream Port 0, and 000b for all other Ports.*	Upstream Port 0 (refer to Note)	RW	Yes	001b
		All other Ports	RW	Yes	000b
23:20	***Reserved***		RsvdP	No	0h
24	**VC ID** Defines the Port 6 VC0 ID code. Cleared, because VC0 is the only/default VC.		RO	No	0
30:25	***Reserved***		RsvdP	No	0-0h
31	**VC Enable** 0 = Not allowed 1 = Enables Port 6 VC0		RO	No	1

Register 12-232. 780h Port 8 VC0 Resource Control (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
0	**TC/VC Map** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped to VC0. Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.		RO	No	1
7:1			RW	Yes	7Fh
15:8	***Reserved***		RsvdP	No	00h
16	**Load Port Arbitration Table** Software writes this bit, to load the updated WRR Port Arbitration Table value to the internal logic. Software Read always returns 0.		RW	Yes	0
19:17	**Port Arbitration Select** Selects the Port Arbitration type for Port 8. Indicates the bit number in the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[1:0]) that corresponds to the arbitration type. 0 = Round-Robin (Hardware-Fixed) arbitration scheme 1 = Weighted Round-Robin with 32 Phases ***Note:*** *This field's value is 001b for upstream Port 0, and 000b for all other Ports.*	Upstream Port 0 (refer to Note)	RW	Yes	001b
		All other Ports	RW	Yes	000b
23:20	***Reserved***		RsvdP	No	0h
24	**VC ID** Defines the Port 8 VC0 ID code. Cleared, because VC0 is the only/default VC.		RO	No	0
30:25	***Reserved***		RsvdP	No	0-0h
31	**VC Enable** 0 = Not allowed 1 = Enables Port 8 VC0		RO	No	1

Register 12-233. 788h Port 9 VC0 Resource Control (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
0	**TC/VC Map** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped to VC0. Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.		RO	No	1
7:1			RW	Yes	7Fh
15:8	***Reserved***		RsvdP	No	00h
16	**Load Port Arbitration Table** Software writes this bit, to load the updated WRR Port Arbitration Table value to the internal logic. Software Read always returns 0.		RW	Yes	0
19:17	**Port Arbitration Select** Selects the Port Arbitration type for Port 9. Indicates the bit number in the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[1:0]) that corresponds to the arbitration type. 0 = Round-Robin (Hardware-Fixed) arbitration scheme 1 = Weighted Round-Robin with 32 Phases ***Note:*** *This field's value is 001b for upstream Port 0, and 000b for all other Ports.*	Upstream Port 0 (refer to Note)	RW	Yes	001b
		All other Ports	RW	Yes	000b
23:20	***Reserved***		RsvdP	No	0h
24	**VC ID** Defines the Port 9 VC0 ID code. Cleared, because VC0 is the only/default VC.		RO	No	0
30:25	***Reserved***		RsvdP	No	0-0h
31	**VC Enable** 0 = Not allowed 1 = Enables Port 9 VC0		RO	No	1

12.16.7 Device-Specific Registers – Ingress Credit Handler Port Pool (Offsets 940h – 94Ch)

This section details the Device-Specific Ingress Credit Handler (INCH) Port Pool registers. Table 12-47 defines the register map.

The original intent for the INCH Port Pool registers was to provide another level of reservation of the Common Pool credits. These registers are essentially redundant to what is accomplished by changing the values of the **INCH Threshold** registers. (Refer to Section 12.16.10.)

Consider the INCH Port Pool registers to be *reserved* and only change the credit Settings, using the INCH Threshold registers. Do not change the INCH Port Pool registers from their default values, unless directed otherwise by PLX Technical Support.

Refer to Section 8.4, "Ingress Resources," and its sub-sections, for further details regarding credits and credit allocation.

Table 12-47. Device-Specific INCH Port Pool Register Map (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Factory Test Only	INCH Port Pool Setting for Stations 0, 1, and 2		940h
Reserved			944h – 94Ch

Register 12-234. 940h INCH Port Pool Setting for Stations 0, 1, and 2 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Notes: *The Port bit controls individual Ports within each Station, as defined in Table 12-48.* ***Factory Test Only*** *bits are RsvdP and not serial EEPROM nor I²C writable.* ***Consider the INCH Port Pool registers to be reserved and only change the credit Settings, using the INCH Threshold registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets A00h through A38h). Do not change the INCH Port Pool registers from their default values, unless directed otherwise by PLX Technical Support.***				
2:0	**Port 0 or 8 Payload Pool** Payload credits (other than the initial credits) for Posted/Completion TLPs dedicated to Port 0 or 8. The Port 4 bit is ***Factory Test Only*** (RsvdP and not serial EEPROM nor I²C writable). 000b = 0 001b = 32 010b = 64 011b = 96 100b = 128 101b = 192 110b, 111b = 256	RWS	Yes	000b
3	**Unused 0** Keep value at 0. Additional bit for Port 0 or 8 Payload Pool. The Port 4 bit is ***Factory Test Only*** (RsvdP and not serial EEPROM nor I²C writable).	RWS	Yes	0
6:4	**Port 0 or 8 Header Pool** Combined Header credits (other than the initial credits) dedicated to Port 0 or 8. The Port 4 bit is ***Factory Test Only*** (RsvdP and not serial EEPROM nor I²C writable). 000b = 0 TLP 001b = 4 TLPs 010b = 8 TLPs 011b = 16 TLPs 100b = 32 TLPs 101b = 48 TLPs 110b, 111b = 64 TLPs	RWS	Yes	000b
7	**Unused 1** Keep value at 0. Additional bit for Port 0 or 8 Header Pool. The Port 4 bit is ***Factory Test Only*** (RsvdP and not serial EEPROM nor I²C writable).	RWS	Yes	0

Register 12-234. 940h INCH Port Pool Setting for Stations 0, 1, and 2 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
10:8	**Port 1, 5, or 9 Payload Pool** Payload credits (other than the initial credits) for Posted/Completion TLPs dedicated to Port 1, 5, or 9. 000b = 0 001b = 32 010b = 64 011b = 96 100b = 128 101b = 192 110b, 111b = 256	RWS	Yes	000b
11	**Unused 2** Keep value at 0. Additional bit for Port 1, 5, or 9 Payload Pool.	RWS	Yes	0
14:12	**Port 1, 5, or 9 Header Pool** Combined Header credits (other than the initial credits) dedicated to Port 1, 5, or 9. 000b = 0 TLP 001b = 4 TLPs 010b = 8 TLPs 011b = 16 TLPs 100b = 32 TLPs 101b = 48 TLPs 110b, 111b = 64 TLPs	RWS	Yes	000b
15	**Unused 3** Keep value at 0. Additional bit for Port 1, 5, or 9 Header Pool.	RWS	Yes	0

Register 12-234. 940h INCH Port Pool Setting for Stations 0, 1, and 2 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
18:16	**Port 6 Payload Pool** Payload credits (other than the initial credits) for Posted/Completion TLPs dedicated to Port 6. 000b = 0 001b = 32 010b = 64 011b = 96 100b = 128 101b = 192 110b, 111b = 256	RWS	Yes	000b
19	**Unused 4** Keep value at 0. Additional bit for Port 6 Payload Pool.	RWS	Yes	0
22:20	**Port 6 Header Pool** Combined Header credits (other than the initial credits) dedicated to Port 6. 000b = 0 TLP 001b = 4 TLPs 010b = 8 TLPs 011b = 16 TLPs 100b = 32 TLPs 101b = 48 TLPs 110b, 111b = 64 TLPs	RWS	Yes	000b
23	**Unused 5** Keep value at 0. Additional bit for Port 6 Header Pool.	RWS	Yes	0
31:24	***Factory Test Only***	RsvdP	No	00h

Table 12-48. Port Bit to Port Control Relationship, by Station, for Register Offset 940h

Bit(s)	Station 0 Port 0 Bit Controls Port	Station 1 Port 4 Bit Controls Port	Station 2 Port 8 Bit Controls Port
7:0	0	***Factory Test Only***	8
15:8	1	5	9
23:16	***Factory Test Only***	6	***Factory Test Only***

12.16.8 Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)

This section details the Device-Specific Vendor-Specific Extended Capability 2 registers. Table 12-49 defines the register map.

Table 12-49. Device-Specific, Vendor-Specific Extended Capability 2 Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset 2 (000h) / Capability Version 2 (1h)	PCI Express Extended Capability ID 2 (000Bh)	950h
Vendor-Specific Header 2		954h
Hardwired Device ID	Hardwired Vendor ID	958h
Reserved	Hardwired Revision ID	95Ch

Register 12-235. 950h Vendor-Specific Extended Capability 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**PCI Express Extended Capability ID 2** Programmed to 000Bh, indicating that the Capability structure is the **Vendor-Specific Extended Capability** structure.	RO	Yes	000Bh
19:16	**Capability Version 2**	RO	Yes	1h
31:20	**Next Capability Offset 2** 000h = This extended capability is the last capability in the PEX 8624 Extended Capabilities list	RO	Yes	000h

Register 12-236. 954h Vendor-Specific Header 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**Vendor-Specific ID 2** ID Number of this **Vendor-Specific Extended Capability** (**VSEC**) structure.	RO	Yes	0001h
19:16	**Vendor-Specific Rev 2** Version Number of this **VSEC** structure.	RO	Yes	0h
31:20	**Vendor-Specific Rev 2** Number of bytes in the entire **VSEC** structure.	RO	Yes	010h

Register 12-237. 958h PLX Hardwired Configuration ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**Hardwired Vendor ID** Always returns the PLX PCI-SIG-assigned Vendor ID value, 10B5h.	RO	No	10B5h
31:16	**Hardwired Device ID** Always returns the PEX 8624 default Device ID value, 8624h.	RO	No	8624h

Register 12-238. 95Ch PLX Hardwired Revision ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Hardwired Revision ID** Returns AAh for all Silicon Revisions.	RO	No	AAh
31:8	***Reserved***	RsvdP	No	0000_00h

12.16.9 Device-Specific Registers – ACS Extended Capability (Offsets 980h – 9FCh)

This section details the Device-Specific ACS Extended Capability registers. The registers in this structure are shadow copies of the Port 0 registers located at offsets 524h and 528h, for each Port. Table 12-50 defines the register map.

Table 12-50. Device-Specific ACS Extended Capability Register Map (Only Ports 0, 4, and 8)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
ACS Port 0 Control		ACS Port 0 Capability		980h
ACS Port 0 Egress Control Vector				984h
ACS Port 1 Control		ACS Port 1 Capability		988h
ACS Port 1 Egress Control Vector				98Ch
Factory Test Only				990h – 99Ch
ACS Port 4 Control		ACS Port 4 Capability		9A0h
ACS Port 4 Egress Control Vector				9A4h
ACS Port 5 Control		ACS Port 5 Capability		9A8h
ACS Port 5 Egress Control Vector				9ACh
ACS Port 6 Control		ACS Port 6 Capability		9B0h
ACS Port 6 Egress Control Vector				9B4h
Factory Test Only				9B8h – 9BCh
ACS Port 8 Control		ACS Port 8 Capability		9C0h
ACS Port 8 Egress Control Vector				9C4h
ACS Port 9 Control		ACS Port 9 Capability		9C8h
ACS Port 9 Egress Control Vector				9CCh
Factory Test Only				9D0h – 9DCh
Reserved				9E0h – 9FCh

Register 12-239. 980h ACS Port 0 Control and Capability (Only Ports 0, 4, and 8)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Port 0 Capability					
0	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation	Downstream	RO	Yes	1
1	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking	Downstream	RO	Yes	1
2	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect ACS Peer-to-Peer Request redirect.	Downstream	RO	Yes	1
3	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect ACS Peer-to-Peer Completion redirect.	Downstream	RO	Yes	1
4	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding	Downstream	RO	Yes	1
5	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Egress Control ACS Peer-to-Peer Egress Control.	Downstream	RO	Yes	1
6	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P ACS Direct Translated Peer-to-Peer.	Downstream	RO	Yes	1
7	***Reserved***		RsvdP	No	0
11:8	***Reserved***	Upstream	RsvdP	No	0
	Egress Control Vector Size Port configuration-dependent. Sum of all Ports. Maximum value is Ch. ***Note:*** *The ACS Egress Control Vector Size value must be adjusted for the specific Port configuration.*	Downstream	RO	Yes	Ch
15:12	***Reserved***		RsvdP	No	0h

Register 12-239. 980h ACS Port 0 Control and Capability (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Port 0 Control					
	Reserved	Upstream	RsvdP	No	0
16	**ACS Source Validation Enable** RW operation is masked by bit 0 (*ACS Source Validation*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
17	**ACS Translation Blocking Enable** RW operation is masked by bit 1 (*ACS Translation Blocking*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
18	**ACS P2P Request Redirect Enable** RW operation is masked by bit 2 (*ACS P2P Request Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
19	**ACS P2P Completion Redirect Enable** RW operation is masked by bit 3 (*ACS P2P Completion Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0

Register 12-239. 980h ACS Port 0 Control and Capability (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding Enable RW operation is masked by bit 4 (*ACS Upstream Forwarding*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Egress Control Enable RW operation is masked by bit 5 (*ACS P2P Egress Control*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
22	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P Enable RW operation is masked by bit 6 (*ACS Direct Translated P2P*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
31:23	***Reserved***		RsvdP	No	0-0h

Register 12-240. 984h ACS Port 0 Egress Control Vector (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
This register's RW bits are valid when the **ACS Port 0 Control** register *ACS Egress Control Enable* bit (offset 980h[21]) is Set.				
0	**Port 0 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
1	**Port 1 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
3:2	***Factory Test Only***	RsvdP	No	00b
4	**Port 4 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
5	**Port 5 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
6	**Port 6 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
7	***Factory Test Only***	RsvdP	No	0
8	**Port 8 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
9	**Port 9 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
11:10	***Factory Test Only***	RsvdP	No	00b
31:12	***Reserved***	RsvdP	No	0000_0h

Register 12-241. 988h ACS Port 1 Control and Capability (Only Ports 0, 4, and 8)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Port 1 Capability					
0	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation	Downstream	RO	Yes	1
1	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking	Downstream	RO	Yes	1
2	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect ACS Peer-to-Peer Request redirect.	Downstream	RO	Yes	1
3	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect ACS Peer-to-Peer Completion redirect.	Downstream	RO	Yes	1
4	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding	Downstream	RO	Yes	1
5	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Egress Control ACS Peer-to-Peer Egress Control.	Downstream	RO	Yes	1
6	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P ACS Direct Translated Peer-to-Peer.	Downstream	RO	Yes	1
7	***Reserved***		RsvdP	No	0
11:8	***Reserved***	Upstream	RsvdP	No	0
	Egress Control Vector Size Port configuration-dependent. Sum of all Ports. Maximum value is Ch. ***Note:*** *The ACS Egress Control Vector Size value must be adjusted for the specific Port configuration.*	Downstream	RO	Yes	10h
15:12	***Reserved***		RsvdP	No	0h

Register 12-241. 988h ACS Port 1 Control and Capability (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Port 1 Control					
	Reserved	Upstream	RsvdP	No	0
16	**ACS Source Validation Enable** RW operation is masked by bit 0 (*ACS Source Validation*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
17	**ACS Translation Blocking Enable** RW operation is masked by bit 1 (*ACS Translation Blocking*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
18	**ACS P2P Request Redirect Enable** RW operation is masked by bit 2 (*ACS P2P Request Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
19	**ACS P2P Completion Redirect Enable** RW operation is masked by bit 3 (*ACS P2P Completion Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0

Register 12-241. 988h ACS Port 1 Control and Capability (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding Enable RW operation is masked by bit 4 (*ACS Upstream Forwarding*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Egress Control Enable RW operation is masked by bit 5 (*ACS P2P Egress Control*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
22	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P Enable RW operation is masked by bit 6 (*ACS Direct Translated P2P*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
31:23	***Reserved***		RsvdP	No	0-0h

Register 12-242. 98Ch ACS Port 1 Egress Control Vector (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register's RW bits are valid when the **ACS Port 1 Control** register *ACS Egress Control Enable* bit (offset 988h[21]) is Set.				
0	**Port 0 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
1	**Port 1 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
3:2	***Factory Test Only***	RsvdP	No	00b
4	**Port 4 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
5	**Port 5 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
6	**Port 6 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
7	***Factory Test Only***	RsvdP	No	0
8	**Port 8 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
9	**Port 9 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
11:10	***Factory Test Only***	RsvdP	No	00b
31:12	***Reserved***	RsvdP	No	0000_0h

Register 12-243. 9A0h ACS Port 4 Control and Capability (Only Ports 0, 4, and 8)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Port 4 Capability					
0	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation	Downstream	RO	Yes	1
1	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking	Downstream	RO	Yes	1
2	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect ACS Peer-to-Peer Request redirect.	Downstream	RO	Yes	1
3	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect ACS Peer-to-Peer Completion redirect.	Downstream	RO	Yes	1
4	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding	Downstream	RO	Yes	1
5	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Egress Control ACS Peer-to-Peer Egress Control.	Downstream	RO	Yes	1
6	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P ACS Direct Translated Peer-to-Peer.	Downstream	RO	Yes	1
7	***Reserved***		RsvdP	No	0
11:8	***Reserved***	Upstream	RsvdP	No	0
	Egress Control Vector Size Port configuration-dependent. Sum of all Ports. Maximum value is Ch. ***Note:*** *The ACS Egress Control Vector Size value must be adjusted for the specific Port configuration.*	Downstream	RO	Yes	10h
15:12	***Reserved***		RsvdP	No	0h

Register 12-243. 9A0h ACS Port 4 Control and Capability (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
ACS Port 4 Control					
	Reserved	Upstream	RsvdP	No	0
16	**ACS Source Validation Enable** RW operation is masked by bit 0 (*ACS Source Validation*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
17	**ACS Translation Blocking Enable** RW operation is masked by bit 1 (*ACS Translation Blocking*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
18	**ACS P2P Request Redirect Enable** RW operation is masked by bit 2 (*ACS P2P Request Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
19	**ACS P2P Completion Redirect Enable** RW operation is masked by bit 3 (*ACS P2P Completion Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0

Register 12-243. 9A0h ACS Port 4 Control and Capability (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding Enable RW operation is masked by bit 4 (*ACS Upstream Forwarding*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Egress Control Enable RW operation is masked by bit 5 (*ACS P2P Egress Control*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
22	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P Enable RW operation is masked by bit 6 (*ACS Direct Translated P2P*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
31:23	***Reserved***		RsvdP	No	0-0h

Register 12-244. 9A4h ACS Port 4 Egress Control Vector (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register's RW bits are valid when the **ACS Port 4 Control** register *ACS Egress Control Enable* bit (offset 9A0h[21]) is Set.				
0	**Port 0 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
1	**Port 1 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
3:2	***Factory Test Only***	RsvdP	No	00b
4	**Port 4 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
5	**Port 5 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
6	**Port 6 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
7	***Factory Test Only***	RsvdP	No	0
8	**Port 8 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
9	**Port 9 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
11:10	***Factory Test Only***	RsvdP	No	00b
31:12	***Reserved***	RsvdP	No	0000_0h

Register 12-245. 9A8h ACS Port 5 Control and Capability (Only Ports 0, 4, and 8)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Port 5 Capability					
0	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation	Downstream	RO	Yes	1
1	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking	Downstream	RO	Yes	1
2	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect ACS Peer-to-Peer Request redirect.	Downstream	RO	Yes	1
3	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect ACS Peer-to-Peer Completion redirect.	Downstream	RO	Yes	1
4	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding	Downstream	RO	Yes	1
5	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Egress Control ACS Peer-to-Peer Egress Control.	Downstream	RO	Yes	1
6	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P ACS Direct Translated Peer-to-Peer.	Downstream	RO	Yes	1
7	***Reserved***		RsvdP	No	0
11:8	***Reserved***	Upstream	RsvdP	No	0
	Egress Control Vector Size Port configuration-dependent. Sum of all Ports. Maximum value is Ch. ***Note:*** *The ACS Egress Control Vector Size value must be adjusted for the specific Port configuration.*	Downstream	RO	Yes	10h
15:12	***Reserved***		RsvdP	No	0h

Register 12-245. 9A8h ACS Port 5 Control and Capability (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
ACS Port 5 Control					
	Reserved	Upstream	RsvdP	No	0
16	**ACS Source Validation Enable** RW operation is masked by bit 0 (*ACS Source Validation*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
17	**ACS Translation Blocking Enable** RW operation is masked by bit 1 (*ACS Translation Blocking*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
18	**ACS P2P Request Redirect Enable** RW operation is masked by bit 2 (*ACS P2P Request Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
19	**ACS P2P Completion Redirect Enable** RW operation is masked by bit 3 (*ACS P2P Completion Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0

Register 12-245. 9A8h ACS Port 5 Control and Capability (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding Enable RW operation is masked by bit 4 (*ACS Upstream Forwarding*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Egress Control Enable RW operation is masked by bit 5 (*ACS P2P Egress Control*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
22	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P Enable RW operation is masked by bit 6 (*ACS Direct Translated P2P*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
31:23	***Reserved***		RsvdP	No	0-0h

Register 12-246. 9ACh ACS Port 5 Egress Control Vector (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register's RW bits are valid when the **ACS Port 5 Control** register *ACS Egress Control Enable* bit (offset 9A8h[21]) is Set.				
0	**Port 0 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
1	**Port 1 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
3:2	***Factory Test Only***	RsvdP	No	00b
4	**Port 4 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
5	**Port 5 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
6	**Port 6 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
7	***Factory Test Only***	RsvdP	No	0
8	**Port 8 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
9	**Port 9 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
11:10	***Factory Test Only***	RsvdP	No	00b
31:12	***Reserved***	RsvdP	No	0000_0h

Register 12-247. 9B0h ACS Port 6 Control and Capability (Only Ports 0, 4, and 8)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Port 6 Capability					
0	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation	Downstream	RO	Yes	1
1	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking	Downstream	RO	Yes	1
2	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect ACS Peer-to-Peer Request redirect.	Downstream	RO	Yes	1
3	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect ACS Peer-to-Peer Completion redirect.	Downstream	RO	Yes	1
4	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding	Downstream	RO	Yes	1
5	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Egress Control ACS Peer-to-Peer Egress Control.	Downstream	RO	Yes	1
6	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P ACS Direct Translated Peer-to-Peer.	Downstream	RO	Yes	1
7	***Reserved***		RsvdP	No	0
11:8	***Reserved***	Upstream	RsvdP	No	0
	Egress Control Vector Size Port configuration-dependent. Sum of all Ports. Maximum value is Ch. ***Note:*** *The ACS Egress Control Vector Size value must be adjusted for the specific Port configuration.*	Downstream	RO	Yes	10h
15:12	***Reserved***		RsvdP	No	0h

Register 12-247. 9B0h ACS Port 6 Control and Capability (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Port 6 Control					
	Reserved	Upstream	RsvdP	No	0
16	**ACS Source Validation Enable** RW operation is masked by bit 0 (*ACS Source Validation*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
17	**ACS Translation Blocking Enable** RW operation is masked by bit 1 (*ACS Translation Blocking*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
18	**ACS P2P Request Redirect Enable** RW operation is masked by bit 2 (*ACS P2P Request Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
19	**ACS P2P Completion Redirect Enable** RW operation is masked by bit 3 (*ACS P2P Completion Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0

Register 12-247. 9B0h ACS Port 6 Control and Capability (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding Enable RW operation is masked by bit 4 (*ACS Upstream Forwarding*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Egress Control Enable RW operation is masked by bit 5 (*ACS P2P Egress Control*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
22	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P Enable RW operation is masked by bit 6 (*ACS Direct Translated P2P*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
31:23	***Reserved***		RsvdP	No	0-0h

Register 12-248. 9B4h ACS Port 6 Egress Control Vector (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register's RW bits are valid when the **ACS Port 6 Control** register *ACS Egress Control Enable* bit (offset 9B0h[21]) is Set.				
0	**Port 0 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
1	**Port 1 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
3:2	***Factory Test Only***	RsvdP	No	00b
4	**Port 4 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
5	**Port 5 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
6	**Port 6 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
7	***Factory Test Only***	RsvdP	No	0
8	**Port 8 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
9	**Port 9 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
11:10	***Factory Test Only***	RsvdP	No	00b
31:12	***Reserved***	RsvdP	No	0000_0h

Register 12-249. 9C0h ACS Port 8 Control and Capability (Only Ports 0, 4, and 8)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Port 8 Capability					
0	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation	Downstream	RO	Yes	1
1	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking	Downstream	RO	Yes	1
2	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect ACS Peer-to-Peer Request redirect.	Downstream	RO	Yes	1
3	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect ACS Peer-to-Peer Completion redirect.	Downstream	RO	Yes	1
4	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding	Downstream	RO	Yes	1
5	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Egress Control ACS Peer-to-Peer Egress Control.	Downstream	RO	Yes	1
6	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P ACS Direct Translated Peer-to-Peer.	Downstream	RO	Yes	1
7	***Reserved***		RsvdP	No	0
11:8	***Reserved***	Upstream	RsvdP	No	0
	Egress Control Vector Size Port configuration-dependent. Sum of all Ports. Maximum value is Ch. ***Note:*** *The ACS Egress Control Vector Size value must be adjusted for the specific Port configuration.*	Downstream	RO	Yes	10h
15:12	***Reserved***		RsvdP	No	0h

Register 12-249. 9C0h ACS Port 8 Control and Capability (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Port 8 Control					
	Reserved	Upstream	RsvdP	No	0
16	**ACS Source Validation Enable** RW operation is masked by bit 0 (*ACS Source Validation*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
17	**ACS Translation Blocking Enable** RW operation is masked by bit 1 (*ACS Translation Blocking*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
18	**ACS P2P Request Redirect Enable** RW operation is masked by bit 2 (*ACS P2P Request Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
19	**ACS P2P Completion Redirect Enable** RW operation is masked by bit 3 (*ACS P2P Completion Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0

Register 12-249. 9C0h ACS Port 8 Control and Capability (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding Enable RW operation is masked by bit 4 (*ACS Upstream Forwarding*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Egress Control Enable RW operation is masked by bit 5 (*ACS P2P Egress Control*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
22	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P Enable RW operation is masked by bit 6 (*ACS Direct Translated P2P*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
31:23	***Reserved***		RsvdP	No	0-0h

Register 12-250. 9C4h ACS Port 8 Egress Control Vector (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register's RW bits are valid when the **ACS Port 8 Control** register *ACS Egress Control Enable* bit (offset 9C0h[21]) is Set.				
0	**Port 0 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
1	**Port 1 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
3:2	***Factory Test Only***	RsvdP	No	00b
4	**Port 4 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
5	**Port 5 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
6	**Port 6 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
7	***Factory Test Only***	RsvdP	No	0
8	**Port 8 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
9	**Port 9 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
11:10	***Factory Test Only***	RsvdP	No	00b
31:12	***Reserved***	RsvdP	No	0000_0h

Register 12-251. 9C8h ACS Port 9 Control and Capability (Only Ports 0, 4, and 8)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Port 9 Capability					
0	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation	Downstream	RO	Yes	1
1	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking	Downstream	RO	Yes	1
2	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect ACS Peer-to-Peer Request redirect.	Downstream	RO	Yes	1
3	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect ACS Peer-to-Peer Completion redirect.	Downstream	RO	Yes	1
4	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding	Downstream	RO	Yes	1
5	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Egress Control ACS Peer-to-Peer Egress Control.	Downstream	RO	Yes	1
6	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P ACS Direct Translated Peer-to-Peer.	Downstream	RO	Yes	1
7	***Reserved***		RsvdP	No	0
11:8	***Reserved***	Upstream	RsvdP	No	0
	Egress Control Vector Size Port configuration-dependent. Sum of all Ports. Maximum value is Ch. ***Note:*** *The ACS Egress Control Vector Size value must be adjusted for the specific Port configuration.*	Downstream	RO	Yes	10h
15:12	***Reserved***		RsvdP	No	0h

Register 12-251. 9C8h ACS Port 9 Control and Capability (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
ACS Port 9 Control					
	Reserved	Upstream	RsvdP	No	0
16	**ACS Source Validation Enable** RW operation is masked by bit 0 (*ACS Source Validation*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
17	**ACS Translation Blocking Enable** RW operation is masked by bit 1 (*ACS Translation Blocking*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
18	**ACS P2P Request Redirect Enable** RW operation is masked by bit 2 (*ACS P2P Request Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
	Reserved	Upstream	RsvdP	No	0
19	**ACS P2P Completion Redirect Enable** RW operation is masked by bit 3 (*ACS P2P Completion Redirect*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0

Register 12-251. 9C8h ACS Port 9 Control and Capability (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding Enable RW operation is masked by bit 4 (*ACS Upstream Forwarding*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Egress Control Enable RW operation is masked by bit 5 (*ACS P2P Egress Control*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
22	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P Enable RW operation is masked by bit 6 (*ACS Direct Translated P2P*). 0 = Disables 1 = Enables	Downstream	RW	Yes	0
31:23	***Reserved***		RsvdP	No	0-0h

Register 12-252. 9CCh ACS Port 9 Egress Control Vector (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register's RW bits are valid when the **ACS Port 9 Control** register *ACS Egress Control Enable* bit (offset 9C8h[21]) is Set.				
0	**Port 0 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
1	**Port 1 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
3:2	***Factory Test Only***	RsvdP	No	00b
4	**Port 4 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
5	**Port 5 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
6	**Port 6 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
7	***Factory Test Only***	RsvdP	No	0
8	**Port 8 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
9	**Port 9 ACS Egress Control Vector** 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	RW	Yes	0
11:10	***Factory Test Only***	RsvdP	No	00b
31:12	***Reserved***	RsvdP	No	0000_0h

12.16.10 Device-Specific Registers – Ingress Credit Handler Threshold (Offsets A00h – B7Ch)

This section details the Device-Specific Ingress Credit Handler (INCH) Threshold registers. **Changing credit values from default register values must be done carefully; otherwise the PEX 8624 will not properly function.** Refer to Section 8.4, "Ingress Resources," and its sub-sections, for detailed information regarding rules associated with changing the **INCH Threshold** registers. Table 12-51 defines the register map.

Table 12-51. Device-Specific INCH Threshold Register Map (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
INCH Threshold Station 0, Port 0 / Station 2, Port 8 VC0 Posted	A00h
INCH Threshold Station 0, Port 0 / Station 2, Port 8 VC0 Non-Posted	A04h
INCH Threshold Station 0, Port 0 / Station 2, Port 8 VC0 Completion	A08h
Reserved	A0Ch – A14h
INCH Threshold Station 0, Port 1 / Station 1, Port 5 / Station 2, Port 9 VC0 Posted	A18h
INCH Threshold Station 0, Port 1 / Station 1, Port 5 / Station 2, Port 9 VC0 Non-Posted	A1Ch
INCH Threshold Station 0, Port 1 / Station 1, Port 5 / Station 2, Port 9 VC0 Completion	A20h
Reserved	A24h – A2Ch
INCH Threshold Station 1, Port 6 VC0 Posted	A30h
INCH Threshold Station 1, Port 6 VC0 Non-Posted	A34h
INCH Threshold Station 1, Port 6 VC0 Completion	A38h
Factory Test Only	A3Ch – A50h
Reserved	A54h – B7Ch

Register 12-253. A00h, A18h, and A30h INCH Threshold Station *x* Port *x* VC0 Posted (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td colspan="5">Notes: Port 5 and Port 6 registers are accessed through software-only Port 4.
Leave Port 4 register offset A00h at its default value (0h); otherwise, RAM will be allocated to unused Port 4.
Posted credits are used for VC0 Memory Write and Message transactions.
Station x Port x are Ports 0 and 1 for Station 0, Ports 5 and 6 for Station 1, and Ports 8 and 9 for Station 2. (Refer to Table 12-51.)</td></tr>
<tr><td>2:0</td><td>Reserved</td><td>RsvdP</td><td>No</td><td>000b</td><td rowspan="2">Upstream:
x4 = 2080h
x8 = 4080h

Downstream:
x4 = 3280h
x8 = 5C90h</td></tr>
<tr><td>8:3</td><td>Posted Payload Credit
Default advertised Posted Payload credit. Actual value is dependent upon Link width and Port configuration.
Bit resolution is in units of 8. Each increment provides 8 Posted Payload credits (for example, Ah = 80 Posted Payload credits). Each credit means that 16 bytes of storage are reserved for Posted TLP Payload data. The default value is based upon strapped/programmed Link width/ configuration.
<table>
<tr><th rowspan="2">Port</th><th colspan="2">Default Value (in Credits), by Strapped or Programmed Link Width</th></tr>
<tr><th>x4</th><th>x8</th></tr>
<tr><td>Upstream</td><td>10h = 128</td><td>10h = 128</td></tr>
<tr><td>Downstream</td><td>10h = 128</td><td>12h = 144</td></tr>
</table></td><td>RWS</td><td>Yes</td><td>Refer to Table</td></tr>
<tr><td>15:9</td><td>Posted Header Credit
Default advertised Posted Header credit. Actual value is dependent upon Link width and Port configuration.
Bit resolution is 1 for 1. Each increment provides 1 Posted Header credit (for example, Ah = 10 Posted Header credits). Each credit means that storage is reserved for the entire Header of a Posted TLP. The default value is based upon strapped/programmed Link width/configuration.
<table>
<tr><th rowspan="2">Port</th><th colspan="2">Default Value (in Credits), by Strapped or Programmed Link Width</th></tr>
<tr><th>x4</th><th>x8</th></tr>
<tr><td>Upstream</td><td>10h = 16</td><td>20h = 32</td></tr>
<tr><td>Downstream</td><td>19h = 25</td><td>2Eh = 46</td></tr>
</table></td><td>RWS</td><td>Yes</td><td>Refer to Table</td></tr>
</table>

Register 12-253. A00h, A18h, and A30h INCH Threshold Station *x* Port *x* VC0 Posted (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
17:16	**UpdateFC High-Priority Threshold for Posted Payload Credit** Refer to Section 8.3.2, "UpdateFC DLLP Policy," for details. 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
19:18	**UpdateFC High-Priority Threshold for Posted Header Credit** Refer to Section 8.3.2, "UpdateFC DLLP Policy," for details. 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
22:20	**Congested Port Weight** If the effective rate setting times the negotiated Link width equates to less than x1 or greater than x8, the internal Credit Allocation logic rounds to x1 or x8, respectively. Refer to Section 8.4.5, "Credit Allocation When Common Pool Is Consumed," for further details. 000b = Request is weighted, based upon the Port's Link width relative to the effective Link widths of the other Stations' Ports 001b = Increases the weight of a Request by 2x 010b = Increases the weight of a Request by 4x 011b = Increases the weight of a Request by 8x 100b = Port receives no credit out of the common pool, until a decongested state is reached 101b = Decreases the weight of a Request by 2x 110b = Decreases the weight of a Request by 4x 111b = Decreases the weight of a Request by 8x	RWS	Yes	000b
31:23	***Reserved***	RsvdP	No	0-0h

Register 12-254. A04h, A1Ch, and A34h INCH Threshold Station *x* Port *x* VC0 Non-Posted (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td colspan="5">Notes: Port 5 and Port 6 registers are accessed through software-only Port 4.
Leave Port 4 register offset A04h at its default value (0h); otherwise, RAM will be allocated to unused Port 4.
Non-Posted credits are used for VC0 Memory Read, I/O Read, I/O Write, Configuration Read, and Configuration Write transactions.
Station x Port x are Ports 0 and 1 for Station 0, Ports 5 and 6 for Station 1, and Ports 8 and 9 for Station 2. (Refer to Table 12-51.)</td></tr>
<tr><td>8:0</td><td>Non-Posted Payload Credit
The Non-Posted Payload is stored with the Non-Posted Header; therefore Non-Posted Payload credit is always available. Because of this, the PEX 8624 hardwires this field to 000h (infinite credits).</td><td>RsvdP</td><td>No</td><td>000h</td><td rowspan="2"></td></tr>
<tr><td>15:9</td><td>Non-Posted Header Credit
Default advertised Non-Posted Header credit. Actual value is dependent upon Link width and Port configuration.
Bit resolution is 1 for 1. Each increment provides 1 Non-Posted Header credit (for example, Ah = 10 Non-Posted Header credits). Each credit means that storage is reserved for the entire Header of a Non-Posted TLP. The default value is based upon strapped/programmed Link width/configuration.
<table>
<tr><th rowspan="2">Port</th><th colspan="2">Default Value (in Credits), by Strapped or Programmed Link Width</th></tr>
<tr><th>x4</th><th>x8</th></tr>
<tr><td>Upstream</td><td>0Ch = 12</td><td>16h = 22</td></tr>
<tr><td>Downstream</td><td>10h = 16</td><td>1Dh = 29</td></tr>
</table></td><td>RWS</td><td>Yes</td><td>Refer to Table</td><td>Upstream:
x4 = 1800h
x8 = 2C00h

Downstream:
x4 = 2000h
x8 = 3A00h</td></tr>
<tr><td>17:16</td><td>Reserved</td><td>RWS</td><td>Yes</td><td colspan="2">00b</td></tr>
<tr><td>19:18</td><td>UpdateFC High-Priority Threshold for Non-Posted Header Credit
Refer to Section 8.3.2, “UpdateFC DLLP Policy,” for details.
00b = 75% (default)
01b = 50%
10b = 25%
11b = 100%</td><td>RWS</td><td>Yes</td><td colspan="2">00b</td></tr>
<tr><td>22:20</td><td>Not used</td><td>RWS</td><td>Yes</td><td colspan="2">000b</td></tr>
<tr><td>23</td><td>Reserved</td><td>RsvdP</td><td>No</td><td colspan="2">0</td></tr>
<tr><td>29:24</td><td>Factory Test Only</td><td>RWS</td><td>Yes</td><td colspan="2">0-0h</td></tr>
<tr><td>31:30</td><td>Factory Test Only</td><td>RW1C</td><td>No</td><td colspan="2">00b</td></tr>
</table>

Register 12-255. A08h, A20h, and A38h INCH Threshold Station *x* Port *x* VC0 Completion (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td colspan="5">Notes: Port 5 and Port 6 registers are accessed through software-only Port 4.
Leave Port 4 register offset A08h at its default value (0h); otherwise, RAM will be allocated to unused Port 4.
Completion credits are used for VC0 Memory Read, I/O Read, I/O Write, Configuration Read, and Configuration Write transaction Completions.
Station x Port x are Ports 0 and 1 for Station 0, Ports 5 and 6 for Station 1, and Ports 8 and 9 for Station 2. (Refer to Table 12-51.)</td></tr>
<tr><td>2:0</td><td>Reserved</td><td>RsvdP</td><td>No</td><td>000b</td><td rowspan="2">Upstream:
x4 = 2480h
x8 = 4090h

Downstream:
x4 = 1880h
x8 = 2C80h</td></tr>
<tr><td>8:3</td><td>Completion Payload Credit
Default advertised Completion Payload credit. Actual value is dependent upon Link width and Port configuration.
Bit resolution is in units of 8. Each increment provides 8 Completion Payload credits (for example, Ah = 80 Completion Payload credits). Each credit means that 16 bytes of storage are reserved for Completion TLP Payload data. The default value is based upon strapped/programmed Link width/configuration.
<table>
<tr><th rowspan="2">Port</th><th colspan="2">Default Value (in Credits), by Strapped or Programmed Link Width</th></tr>
<tr><th>x4</th><th>x8</th></tr>
<tr><td>Upstream</td><td>10h = 128</td><td>10h = 128</td></tr>
<tr><td>Downstream</td><td>10h = 128</td><td>12h = 144</td></tr>
</table></td><td>RWS</td><td>Yes</td><td>Refer to Table</td></tr>
<tr><td>15:9</td><td>Completion Header Credit
Default advertised Completion Header credit. Actual value is dependent upon Link width and Port configuration.
Bit resolution is 1 for 1. Each increment provides 1 Completion Header credit (for example, Ah = 10 Completion Header credits). Each credit means that storage is reserved for the entire Header of a Completion TLP. The default value is based upon strapped/programmed Link width/configuration.
<table>
<tr><th rowspan="2">Port</th><th colspan="2">Default Value (in Credits), by Strapped or Programmed Link Width</th></tr>
<tr><th>x4</th><th>x8</th></tr>
<tr><td>Upstream</td><td>12h = 18</td><td>20h = 32</td></tr>
<tr><td>Downstream</td><td>0Ch = 12</td><td>16h = 22</td></tr>
</table></td><td>RWS</td><td>Yes</td><td>Refer to Table</td></tr>
</table>

Register 12-255. A08h, A20h, and A38h INCH Threshold Station *x* Port *x* VC0 Completion (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
17:16	**UpdateFC High-Priority Threshold for Completion Payload Credit** 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
19:18	**UpdateFC High-Priority Threshold for Completion Header Credit** 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
22:20	***Not used***	RWS	Yes	000b
31:23	***Reserved***	RsvdP	No	0-0h

12.16.11 Device-Specific Registers – SerDes Support (Offsets B80h – BFCh)

This section details the Device-Specific SerDes Support registers. Table 12-52 defines the register map.

Table 12-53 defines the relationship between the SerDes Support registers' Port 0, 4, or 8 parameters and SerDes modules and Lanes, when all Ports are enabled. SerDes modules and Lanes marked "***Factory Test Only***" are associated with bits that are RsvdP and not serial EEPROM nor I^2C writable.

Table 12-52. Device-Specific SerDes Support Register Map (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved			SerDes Control	B80h
SerDes Drive Level 0				B84h
SerDes Drive Level 1				B88h
SerDes Drive Level 2				B8Ch
SerDes Drive Level 3				B90h
Post-Cursor Emphasis Level 0				B94h
Post-Cursor Emphasis Level 1				B98h
Post-Cursor Emphasis Level 2				B9Ch
Post-Cursor Emphasis Level 3				BA0h
Receiver Equalization Level 0				BA4h
Receiver Equalization Level 1				BA8h
Signal Detect Level				BACh
Factory Test Only				BB0h – BF4h
Reserved				BF8h – BFCh

Note: *The six PEX 8624 Ports that connect to PCI Express Transmitters and Receivers are Ports 0, 1, 5, 6, 8, and 9, and each Port has its own set of registers. An additional set of Port 4 registers is visible to software, although the Port is not connected to external signals. The Port 4 registers include:*

- *Other Device-Specific registers.*
- *"Station" registers, that control all Ports in Station 1 (Ports 5 and 6), and are identical to the corresponding Port 0 registers that control all Ports in Station 0 (Ports 0 and 1) and Port 8 registers that control all Ports in Station 2 (Ports 8 and 9). The Station registers include Physical Layer registers, Device-Specific Error registers, and internal mapping (CAM) registers.*

Table 12-53. Port/Physical Lane/SerDes Module/Station/SerDes Quad Relationship, when All Ports Are Enabled, for Offsets B84h through BACh

Physical Lanes and SerDes Modules, by Port						SerDes Quad
Station 0, Port 0		Station 1, Port 4		Station 2, Port 8		
Port	Physical Lanes and SerDes Modules	Port	Physical Lanes and SerDes Modules	Port	Physical Lanes and SerDes Modules	
0	0-3	–	***Factory Test Only***	8	32-35	0
1	4-7	–	***Factory Test Only***	9	36-39	1
–	***Factory Test Only***	5	24-27	–	***Factory Test Only***	2
–	***Factory Test Only***	6	28-31	–	***Factory Test Only***	3

Register 12-256. B80h SerDes Control (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
This register controls SerDes logic parameters.				
2:0	**Receiver Detect Time Select** Selects the Receiver Detect timing. 000b = 1.0 s 001b = 2.0 s 010b = 4.0 s (default) 011b = 5.0 s 100b = 10.0 s 101b = 20.0 s 110b = 40.0 s 111b = 50.0 s	RWS	Yes	010b
3	***Reserved***	RsvdP	No	0
6:4	***Factory Test Only***	RWS	Yes	111b
7	**Electrical Idle Detect Disable** 1 = Electrical Idle Detect circuit is disabled on all SerDes	RWS	Yes	0
31:8	***Reserved***	RsvdP	No	0000_00h

Register 12-257. B84h SerDes Drive Level 0 (Only Ports 0, 4, and 8 (Port 4 is *Factory Test Only*), and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The default value of this register, when combined with the **Post-Cursor Emphasis Level 0** register (Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset B94h) default value, provides -3.5 dB of de-emphasis. However, it is also a Status register with provisional read-back data. The power-up reset default values of this register correspond to -3.5 dB drive levels, and can be overwritten by serial EEPROM or Configuration Space register transactions. However, when read back, the returned data always represents the ***current value being applied to the Lane***. That is because the Write Data value is written into a holding register for the -3.5 dB value, but cannot be directly read from the register. The Read Data value is always sourced from an active Drive register that is loaded dynamically upon de-emphasis changes. ***Notes:*** *Refer to Table 12-53 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules and Lanes. SerDes modules and Lanes marked "**Factory Test Only**" are associated with bits that are RsvdP and not serial EEPROM nor I^2C writable.* *Refer to Section 17.7, "Transmit Drive Characteristics," for a complete breakout of the default values, and their relationship with the **Post-Cursor Emphasis Level 0**.*				
4:0	**SerDes 0 or 32 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Dh (Silicon Revision AA) or 0Eh (Silicon Revisions AB and BB). ***Note: Silicon Revisions AB and BB only*** *– Bits 0 and 1 of this register are swapped when written. Therefore, bits 0 and 1 of the intended value must be swapped prior to writing to this register. The value read from this register reflects the actual value that is used.*	RWS	Yes	Silicon Revision AA: 0Fh (2.5 GT/s, -3.5 dB) 0Dh (5.0 GT/s, -6 dB) Silicon Revisions AB and BB: 0Fh (2.5 GT/s, -3.5 dB) 0Eh (5.0 GT/s, -6 dB)
6:5	***Reserved***	RsvdP	No	00b
7	**SerDes 0 or 32 Auto Load Disable**	RWS	Yes	0
12:8	**SerDes 1 or 33 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Dh (Silicon Revision AA) or 0Eh (Silicon Revisions AB and BB). ***Note: Silicon Revisions AB and BB only*** *– Bits 8 and 9 of this register are swapped when written. Therefore, bits 8 and 9 of the intended value must be swapped prior to writing to this register. The value read from this register reflects the actual value that is used.*	RWS	Yes	Silicon Revision AA: 0Fh (2.5 GT/s, -3.5 dB) 0Dh (5.0 GT/s, -6 dB) Silicon Revisions AB and BB: 0Fh (2.5 GT/s, -3.5 dB) 0Eh (5.0 GT/s, -6 dB)
14:13	***Reserved***	RsvdP	No	00b
15	**SerDes 1 or 33 Auto Load Disable**	RWS	Yes	0

Register 12-257. B84h SerDes Drive Level 0 (Only Ports 0, 4, and 8 (Port 4 is *Factory Test Only*), and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
20:16	**SerDes 2 or 34 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Dh (Silicon Revision AA) or 0Eh (Silicon Revisions AB and BB). ***Note:*** ***Silicon Revisions AB and BB only*** *– Bits 16 and 17 of this register are swapped when written. Therefore, bits 16 and 17 of the intended value must be swapped prior to writing to this register. The value read from this register reflects the actual value that is used.*	RWS	Yes	Silicon Revision AA: 0Fh (2.5 GT/s, -3.5 dB) 0Dh (5.0 GT/s, -6 dB) Silicon Revisions AB and BB: 0Fh (2.5 GT/s, -3.5 dB) 0Eh (5.0 GT/s, -6 dB)
22:21	***Reserved***	RsvdP	No	00b
23	**SerDes 2 or 34 Auto Load Disable**	RWS	Yes	0
28:24	**SerDes 3 or 35 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Dh (Silicon Revision AA) or 0Eh (Silicon Revisions AB and BB). ***Note:*** ***Silicon Revisions AB and BB only*** *– Bits 24 and 25 of this register are swapped when written. Therefore, bits 24 and 25 of the intended value must be swapped prior to writing to this register. The value read from this register reflects the actual value that is used.*	RWS	Yes	Silicon Revision AA: 0Fh (2.5 GT/s, -3.5 dB) 0Dh (5.0 GT/s, -6 dB) Silicon Revisions AB and BB: 0Fh (2.5 GT/s, -3.5 dB) 0Eh (5.0 GT/s, -6 dB)
30:29	***Reserved***	RsvdP	No	00b
31	**SerDes 3 or 35 Auto Load Disable**	RWS	Yes	0

Register 12-258. B88h SerDes Drive Level 1 (Only Ports 0, 4, and 8 (Port 4 is *Factory Test Only*), and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The default value of this register, when combined with the **Post-Cursor Emphasis Level 1** register (Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset B98h) default value, provides -3.5 dB of de-emphasis. However, it is also a Status register with provisional read-back data. The power-up reset default values of this register correspond to -3.5 dB drive levels, and can be overwritten by serial EEPROM or Configuration Space register transactions. However, when read back, the returned data always represents the ***current value being applied to the Lane***. That is because the Write Data value is written into a holding register for the -3.5 dB value, but cannot be directly read from the register. The Read Data value is always sourced from an active Drive register that is loaded dynamically upon de-emphasis changes. ***Notes:*** *Refer to Table 12-53 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules and Lanes. SerDes modules and Lanes marked "**Factory Test Only**" are associated with bits that are RsvdP and not serial EEPROM nor I^2C writable.* *Refer to Section 17.7, "Transmit Drive Characteristics," for a complete breakout of the default values, and their relationship with the **Post-Cursor Emphasis Level 1** register.*				
4:0	**SerDes 4 or 36 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Dh (Silicon Revision AA) or 0Eh (Silicon Revisions AB and BB). ***Note: Silicon Revisions AB and BB only*** *– Bits 0 and 1 of this register are swapped when written. Therefore, bits 0 and 1 of the intended value must be swapped prior to writing to this register. The value read from this register reflects the actual value that is used.*	RWS	Yes	Silicon Revision AA: 0Fh (2.5 GT/s, -3.5 dB) 0Dh (5.0 GT/s, -6 dB) Silicon Revisions AB and BB: 0Fh (2.5 GT/s, -3.5 dB) 0Eh (5.0 GT/s, -6 dB)
6:5	***Reserved***	RsvdP	No	00b
7	**SerDes 4 or 36 Auto Load Disable**	RWS	Yes	0
12:8	**SerDes 5 or 37 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Dh (Silicon Revision AA) or 0Eh (Silicon Revisions AB and BB). ***Note: Silicon Revisions AB and BB only*** *– Bits 8 and 9 of this register are swapped when written. Therefore, bits 8 and 9 of the intended value must be swapped prior to writing to this register. The value read from this register reflects the actual value that is used.*	RWS	Yes	Silicon Revision AA: 0Fh (2.5 GT/s, -3.5 dB) 0Dh (5.0 GT/s, -6 dB) Silicon Revisions AB and BB: 0Fh (2.5 GT/s, -3.5 dB) 0Eh (5.0 GT/s, -6 dB)
14:13	***Reserved***	RsvdP	No	00b
15	**SerDes 5 or 37 Auto Load Disable**	RWS	Yes	0

Register 12-258. B88h SerDes Drive Level 1 (Only Ports 0, 4, and 8 (Port 4 is *Factory Test Only*), and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
20:16	**SerDes 6 or 38 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Dh (Silicon Revision AA) or 0Eh (Silicon Revisions AB and BB). ***Note:*** ***Silicon Revisions AB and BB only*** *– Bits 16 and 17 of this register are swapped when written. Therefore, bits 16 and 17 of the intended value must be swapped prior to writing to this register. The value read from this register reflects the actual value that is used.*	RWS	Yes	Silicon Revision AA: 0Fh (2.5 GT/s, -3.5 dB) 0Dh (5.0 GT/s, -6 dB) Silicon Revisions AB and BB: 0Fh (2.5 GT/s, -3.5 dB) 0Eh (5.0 GT/s, -6 dB)
22:21	***Reserved***	RsvdP	No	00b
23	**SerDes 6 or 38 Auto Load Disable**	RWS	Yes	0
28:24	**SerDes 7 or 39 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Dh (Silicon Revision AA) or 0Eh (Silicon Revisions AB and BB). ***Note:*** ***Silicon Revisions AB and BB only*** *– Bits 24 and 25 of this register are swapped when written. Therefore, bits 24 and 25 of the intended value must be swapped prior to writing to this register. The value read from this register reflects the actual value that is used.*	RWS	Yes	Silicon Revision AA: 0Fh (2.5 GT/s, -3.5 dB) 0Dh (5.0 GT/s, -6 dB) Silicon Revisions AB and BB: 0Fh (2.5 GT/s, -3.5 dB) 0Eh (5.0 GT/s, -6 dB)
30:29	***Reserved***	RsvdP	No	00b
31	**SerDes 7 or 39 Auto Load Disable**	RWS	Yes	0

Register 12-259. B8Ch SerDes Drive Level 2 (Only Ports 0, 4, and 8 (Ports 0 and 8 are *Factory Test Only*), and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The default value of this register, when combined with the **Post-Cursor Emphasis Level 2** register (Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset B9Ch) default value, provides -3.5 dB of de-emphasis. However, it is also a Status register with provisional read-back data. The power-up reset default values of this register correspond to -3.5 dB drive levels, and can be overwritten by serial EEPROM or Configuration Space register transactions. However, when read back, the returned data always represents the ***current value being applied to the Lane***. That is because the Write Data value is written into a holding register for the -3.5 dB value, but cannot be directly read from the register. The Read Data value is always sourced from an active Drive register that is loaded dynamically upon de-emphasis changes. ***Notes:*** *Refer to Table 12-53 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules and Lanes. SerDes modules and Lanes marked "**Factory Test Only**" are associated with bits that are RsvdP and not serial EEPROM nor I^2C writable.* *Refer to Section 17.7, "Transmit Drive Characteristics," for a complete breakout of the default values, and their relationship with the **Post-Cursor Emphasis Level 2** register.*				
4:0	**SerDes 24 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Dh (Silicon Revision AA) or 0Eh (Silicon Revisions AB and BB). ***Note: Silicon Revisions AB and BB only*** *– Bits 0 and 1 of this register are swapped when written. Therefore, bits 0 and 1 of the intended value must be swapped prior to writing to this register. The value read from this register reflects the actual value that is used.*	RWS	Yes	Silicon Revision AA: 0Fh (2.5 GT/s, -3.5 dB) 0Dh (5.0 GT/s, -6 dB) Silicon Revisions AB and BB: 0Fh (2.5 GT/s, -3.5 dB) 0Eh (5.0 GT/s, -6 dB)
6:5	***Reserved***	RsvdP	No	00b
7	**SerDes 24 Auto Load Disable**	RWS	Yes	0
12:8	**SerDes 25 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Dh (Silicon Revision AA) or 0Eh (Silicon Revisions AB and BB). ***Note: Silicon Revisions AB and BB only*** *– Bits 8 and 9 of this register are swapped when written. Therefore, bits 8 and 9 of the intended value must be swapped prior to writing to this register. The value read from this register reflects the actual value that is used.*	RWS	Yes	Silicon Revision AA: 0Fh (2.5 GT/s, -3.5 dB) 0Dh (5.0 GT/s, -6 dB) Silicon Revisions AB and BB: 0Fh (2.5 GT/s, -3.5 dB) 0Eh (5.0 GT/s, -6 dB)
14:13	***Reserved***	RsvdP	No	00b
15	**SerDes 25 Auto Load Disable**	RWS	Yes	0

Register 12-259. B8Ch SerDes Drive Level 2 (Only Ports 0, 4, and 8 (Ports 0 and 8 are *Factory Test Only*), and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
20:16	**SerDes 26 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Dh (Silicon Revision AA) or 0Eh (Silicon Revisions AB and BB). ***Note: Silicon Revisions AB and BB only** – Bits 16 and 17 of this register are swapped when written. Therefore, bits 16 and 17 of the intended value must be swapped prior to writing to this register. The value read from this register reflects the actual value that is used.*	RWS	Yes	Silicon Revision AA: 0Fh (2.5 GT/s, -3.5 dB) 0Dh (5.0 GT/s, -6 dB) Silicon Revisions AB and BB: 0Fh (2.5 GT/s, -3.5 dB) 0Eh (5.0 GT/s, -6 dB)
22:21	***Reserved***	RsvdP	No	00b
23	**SerDes 26 Auto Load Disable**	RWS	Yes	0
28:24	**SerDes 27 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Dh (Silicon Revision AA) or 0Eh (Silicon Revisions AB and BB). ***Note: Silicon Revisions AB and BB only** – Bits 24 and 25 of this register are swapped when written. Therefore, bits 24 and 25 of the intended value must be swapped prior to writing to this register. The value read from this register reflects the actual value that is used.*	RWS	Yes	Silicon Revision AA: 0Fh (2.5 GT/s, -3.5 dB) 0Dh (5.0 GT/s, -6 dB) Silicon Revisions AB and BB: 0Fh (2.5 GT/s, -3.5 dB) 0Eh (5.0 GT/s, -6 dB)
30:29	***Reserved***	RsvdP	No	00b
31	**SerDes 27 Auto Load Disable**	RWS	Yes	0

Register 12-260. B90h SerDes Drive Level 3 (Only Ports 0, 4, and 8 (Ports 0 and 8 are *Factory Test Only*), and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The default value of this register, when combined with the **Post-Cursor Emphasis Level 3** register (Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset BA0h) default value, provides -3.5 dB of de-emphasis. However, it is also a Status register with provisional read-back data. The power-up reset default values of this register correspond to -3.5 dB drive levels, and can be overwritten by serial EEPROM or Configuration Space register transactions. However, when read back, the returned data always represents the ***current value being applied to the Lane***. That is because the Write Data value is written into a holding register for the -3.5 dB value, but cannot be directly read from the register. The Read Data value is always sourced from an active Drive register that is loaded dynamically upon de-emphasis changes. ***Notes:*** *Refer to Table 12-53 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules and Lanes. SerDes modules and Lanes marked "**Factory Test Only**" are associated with bits that are RsvdP and not serial EEPROM nor I^2C writable.* *Refer to Section 17.7, "Transmit Drive Characteristics," for a complete breakout of the default values, and their relationship with the **Post-Cursor Emphasis Level 3** register.*				
4:0	**SerDes 28 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Dh (Silicon Revision AA) or 0Eh (Silicon Revisions AB and BB). ***Note: Silicon Revisions AB and BB only*** *– Bits 0 and 1 of this register are swapped when written. Therefore, bits 0 and 1 of the intended value must be swapped prior to writing to this register. The value read from this register reflects the actual value that is used.*	RWS	Yes	Silicon Revision AA: 0Fh (2.5 GT/s, -3.5 dB) 0Dh (5.0 GT/s, -6 dB) Silicon Revisions AB and BB: 0Fh (2.5 GT/s, -3.5 dB) 0Eh (5.0 GT/s, -6 dB)
6:5	***Reserved***	RsvdP	No	00b
7	**SerDes 28 Auto Load Disable**	RWS	Yes	0
12:8	**SerDes 29 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Dh (Silicon Revision AA) or 0Eh (Silicon Revisions AB and BB). ***Note: Silicon Revisions AB and BB only*** *– Bits 8 and 9 of this register are swapped when written. Therefore, bits 8 and 9 of the intended value must be swapped prior to writing to this register. The value read from this register reflects the actual value that is used.*	RWS	Yes	Silicon Revision AA: 0Fh (2.5 GT/s, -3.5 dB) 0Dh (5.0 GT/s, -6 dB) Silicon Revisions AB and BB: 0Fh (2.5 GT/s, -3.5 dB) 0Eh (5.0 GT/s, -6 dB)
14:13	***Reserved***	RsvdP	No	00b
15	**SerDes 29 Auto Load Disable**	RWS	Yes	0

Register 12-260. B90h SerDes Drive Level 3 (Only Ports 0, 4, and 8 (Ports 0 and 8 are *Factory Test Only*), and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
20:16	**SerDes 30 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Dh (Silicon Revision AA) or 0Eh (Silicon Revisions AB and BB). ***Note: Silicon Revisions AB and BB only** – Bits 16 and 17 of this register are swapped when written. Therefore, bits 16 and 17 of the intended value must be swapped prior to writing to this register. The value read from this register reflects the actual value that is used.*	RWS	Yes	Silicon Revision AA: 0Fh (2.5 GT/s, -3.5 dB) 0Dh (5.0 GT/s, -6 dB) Silicon Revisions AB and BB: 0Fh (2.5 GT/s, -3.5 dB) 0Eh (5.0 GT/s, -6 dB)
22:21	***Reserved***	RsvdP	No	00b
23	**SerDes 30 Auto Load Disable**	RWS	Yes	0
28:24	**SerDes 31 Drive Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 0Dh (Silicon Revision AA) or 0Eh (Silicon Revisions AB and BB). ***Note: Silicon Revisions AB and BB only** – Bits 24 and 25 of this register are swapped when written. Therefore, bits 24 and 25 of the intended value must be swapped prior to writing to this register. The value read from this register reflects the actual value that is used.*	RWS	Yes	Silicon Revision AA: 0Fh (2.5 GT/s, -3.5 dB) 0Dh (5.0 GT/s, -6 dB) Silicon Revisions AB and BB: 0Fh (2.5 GT/s, -3.5 dB) 0Eh (5.0 GT/s, -6 dB)
30:29	***Reserved***	RsvdP	No	00b
31	**SerDes 31 Auto Load Disable**	RWS	Yes	0

Register 12-261. B94h Post-Cursor Emphasis Level 0 (Only Ports 0, 4, and 8 (Port 4 is *Factory Test Only*), and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The default value of this register, when combined with the **SerDes Drive Level 0** register (Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset B84h) default value, provides -3.5 dB of de-emphasis. The power-up value can be overwritten by serial EEPROM or Configuration Space register transactions. However, when read back, the returned data always represents the ***current value being applied to the Lane***. That is because the Write Data value is written into a holding register for the -3.5 dB value, but cannot be directly read from the register. The Read Data value is always sourced from an active Drive register that is loaded dynamically upon de-emphasis changes. ***Notes:*** *Refer to Table 12-53 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules and Lanes. SerDes modules and Lanes marked "**Factory Test Only**" are associated with bits that are RsvdP and not serial EEPROM nor I^2C writable.* *Refer to Section 17.7, "Transmit Drive Characteristics," for a complete breakout of the default values, and their relationship with the **SerDes Drive Level 0** register.*				
4:0	**SerDes 0 or 32 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 dB) 15h (5.0 GT/s, -6 dB)
6:5	***Reserved***	RsvdP	No	00b
7	**SerDes 0 or 32 Auto Load Disable**	RWS	Yes	0
12:8	**SerDes 1 or 33 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 dB) 15h (5.0 GT/s, -6 dB)
14:13	***Reserved***	RsvdP	No	00b
15	**SerDes 1 or 33 Auto Load Disable**	RWS	Yes	0

Register 12-261. B94h Post-Cursor Emphasis Level 0 (Only Ports 0, 4, and 8 (Port 4 is *Factory Test Only*), and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
20:16	**SerDes 2 or 34 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 dB) 15h (5.0 GT/s, -6 dB)
22:21	***Reserved***	RsvdP	No	00b
23	**SerDes 2 or 34 Auto Load Disable**	RWS	Yes	0
28:24	**SerDes 3 or 35 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 dB) 15h (5.0 GT/s, -6 dB)
30:29	***Reserved***	RsvdP	No	00b
31	**SerDes 3 or 35 Auto Load Disable**	RWS	Yes	0

Register 12-262. B98h Post-Cursor Emphasis Level 1 (Only Ports 0, 4, and 8 (Port 4 is *Factory Test Only*), and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The default value of this register, when combined with the **SerDes Drive Level 1** register (Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset B88h) default value, provides -3.5 dB of de-emphasis. The power-up value can be overwritten by serial EEPROM or Configuration Space register transactions. However, when read back, the returned data always represents the ***current value being applied to the Lane***. That is because the Write Data value is written into a holding register for the -3.5 dB value, but cannot be directly read from the register. The Read Data value is always sourced from an active Drive register that is loaded dynamically upon de-emphasis changes. ***Notes:*** *Refer to Table 12-53 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules and Lanes. SerDes modules and Lanes marked "**Factory Test Only**" are associated with bits that are RsvdP and not serial EEPROM nor I^2C writable.* *Refer to Section 17.7, "Transmit Drive Characteristics," for a complete breakout of the default values, and their relationship with the **SerDes Drive Level 1** register.*				
4:0	**SerDes 4 or 36 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 dB) 15h (5.0 GT/s, -6 dB)
6:5	***Reserved***	RsvdP	No	00b
7	**SerDes 4 or 36 Auto Load Disable**	RWS	Yes	0
12:8	**SerDes 5 or 37 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 dB) 15h (5.0 GT/s, -6 dB)
14:13	***Reserved***	RsvdP	No	00b
15	**SerDes 5 or 37 Auto Load Disable**	RWS	Yes	0

Register 12-262. B98h Post-Cursor Emphasis Level 1 (Only Ports 0, 4, and 8 (Port 4 is *Factory Test Only*), and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
20:16	**SerDes 6 or 38 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 dB) 15h (5.0 GT/s, -6 dB)
22:21	***Reserved***	RsvdP	No	00b
23	**SerDes 6 or 38 Auto Load Disable**	RWS	Yes	0
28:24	**SerDes 7 or 39 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 dB) 15h (5.0 GT/s, -6 dB)
30:29	***Reserved***	RsvdP	No	00b
31	**SerDes 7 or 39 Auto Load Disable**	RWS	Yes	0

Register 12-263. B9Ch Post-Cursor Emphasis Level 2 (Only Ports 0, 4, and 8 (Ports 0 and 8 are *Factory Test Only*), and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The default value of this register, when combined with the **SerDes Drive Level 2** register (Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset B8Ch) default value, provides -3.5 dB of de-emphasis. The power-up value can be overwritten by serial EEPROM or Configuration Space register transactions. However, when read back, the returned data always represents the ***current value being applied to the Lane***. That is because the Write Data value is written into a holding register for the -3.5 dB value, but cannot be directly read from the register. The Read Data value is always sourced from an active Drive register that is loaded dynamically upon de-emphasis changes. ***Notes:*** *Refer to Table 12-53 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules and Lanes. SerDes modules and Lanes marked "**Factory Test Only**" are associated with bits that are RsvdP and not serial EEPROM nor I^2C writable.* *Refer to Section 17.7, "Transmit Drive Characteristics," for a complete breakout of the default values, and their relationship with the **SerDes Drive Level 2** register.*				
4:0	**SerDes 24 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 dB) 15h (5.0 GT/s, -6 dB)
6:5	***Reserved***	RsvdP	No	00b
7	**SerDes 24 Auto Load Disable**	RWS	Yes	0
12:8	**SerDes 25 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 dB) 15h (5.0 GT/s, -6 dB)
14:13	***Reserved***	RsvdP	No	00b
15	**SerDes 25 Auto Load Disable**	RWS	Yes	0

Register 12-263. B9Ch Post-Cursor Emphasis Level 2 (Only Ports 0, 4, and 8 (Ports 0 and 8 are *Factory Test Only*), and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
20:16	**SerDes 26 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 dB) 15h (5.0 GT/s, -6 dB)
22:21	***Reserved***	RsvdP	No	00b
23	**SerDes 26 Auto Load Disable**	RWS	Yes	0
28:24	**SerDes 27 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 dB) 15h (5.0 GT/s, -6 dB)
30:29	***Reserved***	RsvdP	No	00b
31	**SerDes 27 Auto Load Disable**	RWS	Yes	0

Register 12-264. BA0h Post-Cursor Emphasis Level 3 (Only Ports 0, 4, and 8 (Ports 0 and 8 are *Factory Test Only*), and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The default value of this register, when combined with the **SerDes Drive Level 3** register (Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset B90h) default value, provides -3.5 dB of de-emphasis. The power-up value can be overwritten by serial EEPROM or Configuration Space register transactions. However, when read back, the returned data always represents the ***current value being applied to the Lane***. That is because the Write Data value is written into a holding register for the -3.5 dB value, but cannot be directly read from the register. The Read Data value is always sourced from an active Drive register that is loaded dynamically upon de-emphasis changes. ***Notes:*** *Refer to Table 12-53 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules and Lanes. SerDes modules and Lanes marked "**Factory Test Only**" are associated with bits that are RsvdP and not serial EEPROM nor I^2C writable.* *Refer to Section 17.7, "Transmit Drive Characteristics," for a complete breakout of the default values, and their relationship with the **SerDes Drive Level 3** register.*				
4:0	**SerDes 28 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 dB) 15h (5.0 GT/s, -6 dB)
6:5	***Reserved***	RsvdP	No	00b
7	**SerDes 28 Auto Load Disable**	RWS	Yes	0
12:8	**SerDes 29 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 dB) 15h (5.0 GT/s, -6 dB)
14:13	***Reserved***	RsvdP	No	00b
15	**SerDes 29 Auto Load Disable**	RWS	Yes	0

Register 12-264. BA0h Post-Cursor Emphasis Level 3 (Only Ports 0, 4, and 8 (Ports 0 and 8 are *Factory Test Only*), and also NT Port Virtual Interface if Port 0 is the NT Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
20:16	**SerDes 30 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 dB) 15h (5.0 GT/s, -6 dB)
22:21	***Reserved***	RsvdP	No	00b
23	**SerDes 30 Auto Load Disable**	RWS	Yes	0
28:24	**SerDes 31 Post-Cursor Emphasis Level** If 5.0 GT/s -6 dB is selected (Port's **Link Control 2** register *Selectable De-Emphasis* bit, offset 98h[6], is Cleared, provided that the Current Link Speed is 5.0 GT/s (Port's **Link Status** register *Current Link Speed* field, offset 78h[19:16], is programmed to 0010b)), this register is automatically loaded with default value 15h.	RWS	Yes	0Dh (2.5 GT/s, -3.5 dB) 15h (5.0 GT/s, -6 dB)
30:29	***Reserved***	RsvdP	No	00b
31	**SerDes 31 Auto Load Disable**	RWS	Yes	0

Register 12-265. BA4h Receiver Equalization Level 0 (Only Ports 0, 4, and 8 (Port 4 is *Factory Test Only*), and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides the Receiver Equalization Level control for the lower SerDes within each Station. **Rx Equalization[3:0] / Equalization** 0h (default) – Off 1h – Minimum 2h to 3h – Low 4h to 6h – Low to Medium 7h to 9h – Medium Ah to Dh – High to Medium Eh to Fh – Maximum ***Note:*** *Refer to Table 12-53 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules and Lanes. SerDes modules and Lanes marked "**Factory Test Only**" are associated with bits that are RsvdP and not serial EEPROM nor I^2C writable.*				
3:0	**SerDes 0 or 32 Receiver Equalization Level**	RWS	Yes	0h
7:4	**SerDes 1 or 33 Receiver Equalization Level**	RWS	Yes	0h
11:8	**SerDes 2 or 34 Receiver Equalization Level**	RWS	Yes	0h
15:12	**SerDes 3 or 35 Receiver Equalization Level**	RWS	Yes	0h
19:16	**SerDes 4 or 36 Receiver Equalization Level**	RWS	Yes	0h
23:20	**SerDes 5 or 37 Receiver Equalization Level**	RWS	Yes	0h
27:24	**SerDes 6 or 38 Receiver Equalization Level**	RWS	Yes	0h
31:28	**SerDes 7 or 39 Receiver Equalization Level**	RWS	Yes	0h

Register 12-266. BA8h Receiver Equalization Level 1 (Only Ports 0, 4, and 8 (Ports 0 and 8 are *Factory Test Only*), and also NT Port Virtual Interface if Port 0 is the NT Port)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td colspan="5">This register provides the Receiver Equalization Level control for the upper SerDes within each Station.
<table>
<tr><th>Rx Equalization[3:0]</th><th>Equalization</th><th>Rx Equalization[3:0]</th><th>Equalization</th></tr>
<tr><td>0h (default)</td><td>Off</td><td>7h to 9h</td><td>Medium</td></tr>
<tr><td>1h</td><td>Minimum</td><td>Ah to Dh</td><td>High to Medium</td></tr>
<tr><td>2h to 3h</td><td>Low</td><td>Eh to Fh</td><td>Maximum</td></tr>
<tr><td>4h to 6h</td><td>Low to Medium</td><td></td><td></td></tr>
</table>
Note: Refer to Table 12-53 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules and Lanes. SerDes modules and Lanes marked “Factory Test Only” are associated with bits that are RsvdP and not serial EEPROM nor I²C writable. </td></tr>
<tr><td>3:0</td><td>SerDes 24 Receiver Equalization Level</td><td>RWS</td><td>Yes</td><td>0h</td></tr>
<tr><td>7:4</td><td>SerDes 25 Receiver Equalization Level</td><td>RWS</td><td>Yes</td><td>0h</td></tr>
<tr><td>11:8</td><td>SerDes 26 Receiver Equalization Level</td><td>RWS</td><td>Yes</td><td>0h</td></tr>
<tr><td>15:12</td><td>SerDes 27 Receiver Equalization Level</td><td>RWS</td><td>Yes</td><td>0h</td></tr>
<tr><td>19:16</td><td>SerDes 28 Receiver Equalization Level</td><td>RWS</td><td>Yes</td><td>0h</td></tr>
<tr><td>23:20</td><td>SerDes 29 Receiver Equalization Level</td><td>RWS</td><td>Yes</td><td>0h</td></tr>
<tr><td>27:24</td><td>SerDes 30 Receiver Equalization Level</td><td>RWS</td><td>Yes</td><td>0h</td></tr>
<tr><td>31:28</td><td>SerDes 31 Receiver Equalization Level</td><td>RWS</td><td>Yes</td><td>0h</td></tr>
</table>

Register 12-267. BACh Signal Detect Level (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides the Receiver Signal Detect Level select. Each two-bit field in this register provides four Settings for detecting Electrical Idle Analog, for the corresponding SerDes. 00b = Approximately 50 to 80 mV 01b = Approximately 65 to 175 mV (default) 10b = Approximately 75 to 200 mV 11b = Approximately 120 to 240 mV ***Note:*** *Refer to Table 12-53 for the relationship between the Port 0, 4, or 8 parameters and SerDes modules and Lanes. SerDes modules and Lanes marked "**Factory Test Only**" are associated with bits that are RsvdP and not serial EEPROM nor I^2C writable.*				
1:0	**SerDes 0 or 32 Signal Detect Level**	RWS	Yes	01b
3:2	**SerDes 1 or 33 Signal Detect Level**	RWS	Yes	01b
5:4	**SerDes 2 or 34 Signal Detect Level**	RWS	Yes	01b
7:6	**SerDes 3 or 35 Signal Detect Level**	RWS	Yes	01b
9:8	**SerDes 4 or 36 Signal Detect Level**	RWS	Yes	01b
11:10	**SerDes 5 or 37 Signal Detect Level**	RWS	Yes	01b
13:12	**SerDes 6 or 38 Signal Detect Level**	RWS	Yes	01b
15:14	**SerDes 7 or 39 Signal Detect Level**	RWS	Yes	01b
17:16	**SerDes 24 Signal Detect Level**	RWS	Yes	01b
19:18	**SerDes 25 Signal Detect Level**	RWS	Yes	01b
21:20	**SerDes 26 Signal Detect Level**	RWS	Yes	01b
23:22	**SerDes 27 Signal Detect Level**	RWS	Yes	01b
25:24	**SerDes 28 Signal Detect Level**	RWS	Yes	01b
27:26	**SerDes 29 Signal Detect Level**	RWS	Yes	01b
29:28	**SerDes 30 Signal Detect Level**	RWS	Yes	01b
31:30	**SerDes 31 Signal Detect Level**	RWS	Yes	01b

12.16.12 Device-Specific Registers – Port Configuration Header (Offsets E00h – E3Ch)

This section details the Device-Specific Port Configuration Header registers, for each Port. Table 12-54 defines the register map.

Table 12-54. Device-Specific Port Configuration Header Register Map (Only Ports 0, 4, and 8)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Command Port 1		PCI Command Port 0		E00h
Factory Test Only				E04h
PCI Command Port 5		PCI Command Port 4		E08h
Factory Test Only		PCI Command Port 6		E0Ch
PCI Command Port 9		PCI Command Port 8		E10h
Factory Test Only				E14h
Reserved				E18h – E1Ch
Bridge Control Port 1		Bridge Control Port 0		E20h
Factory Test Only				E24h
Bridge Control Port 5		Bridge Control Port 4		E28h
Factory Test Only		Bridge Control Port 6		E2Ch
Bridge Control Port 9		Bridge Control Port 8		E30h
Factory Test Only				E34h
Reserved				E38h – E3Ch

Register 12-268. E00h PCI Command Port 0 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**I/O Access Enable** 0 = PEX 8624 ignores I/O Space accesses on Port 0's primary interface 1 = PEX 8624 responds to I/O Space accesses on Port 0's primary interface	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8624 ignores Memory Space accesses on Port 0's primary interface 1 = PEX 8624 responds to Memory Space accesses on Port 0's primary interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8624 Memory and I/O Request forwarding upstream. Neither affect Message forwarding nor Completions traveling upstream or downstream. 0 = PEX 8624 handles Memory and I/O Requests received on Port 0's downstream/secondary interface as URs; for Non-Posted Requests, the PEX 8624 returns a Completion with UR Completion status 1 = PEX 8624 forwards Memory and I/O Requests upstream	RW	Yes	0
7:3	***Reserved***	RsvdP	No	0-0h
8	**SERR# Enable** Controls the **PCI Status** register *Signaled System Error* bit (offset 04h[30]). 0 = No error is detected 1 = Enables reporting of Fatal and Non-Fatal errors detected by the device to the Root Complex	RW	Yes	0
15:9	***Reserved***	RsvdP	No	0-0h

Register 12-269. E02h PCI Command Port 1 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**I/O Access Enable** 0 = PEX 8624 ignores I/O Space accesses on Port 1's primary interface 1 = PEX 8624 responds to I/O Space accesses on Port 1's primary interface	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8624 ignores Memory Space accesses on Port 1's primary interface 1 = PEX 8624 responds to Memory Space accesses on Port 1's primary interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8624 Memory and I/O Request forwarding upstream. Neither affect Message forwarding nor Completions traveling upstream or downstream. 0 = PEX 8624 handles Memory and I/O Requests received on Port 1's downstream/secondary interface as URs; for Non-Posted Requests, the PEX 8624 returns a Completion with UR Completion status 1 = PEX 8624 forwards Memory and I/O Requests upstream	RW	Yes	0
7:3	***Reserved***	RsvdP	No	0-0h
8	**SERR# Enable** Controls the **PCI Status** register *Signaled System Error* bit (offset 04h[30]). 0 = No error is detected 1 = Enables reporting of Fatal and Non-Fatal errors detected by the device to the Root Complex	RW	Yes	0
15:9	***Reserved***	RsvdP	No	0-0h

Register 12-270. E08h PCI Command Port 4 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**I/O Access Enable** 0 = PEX 8624 ignores I/O Space accesses on Port 4's primary interface 1 = PEX 8624 responds to I/O Space accesses on Port 4's primary interface	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8624 ignores Memory Space accesses on Port 4's primary interface 1 = PEX 8624 responds to Memory Space accesses on Port 4's primary interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8624 Memory and I/O Request forwarding upstream. Neither affect Message forwarding nor Completions traveling upstream or downstream. 0 = PEX 8624 handles Memory and I/O Requests received on Port 4's downstream/secondary interface as URs; for Non-Posted Requests, the PEX 8624 returns a Completion with UR Completion status 1 = PEX 8624 forwards Memory and I/O Requests upstream	RW	Yes	0
7:3	***Reserved***	RsvdP	No	0-0h
8	**SERR# Enable** Controls the **PCI Status** register *Signaled System Error* bit (offset 04h[30]). 0 = No error is detected 1 = Enables reporting of Fatal and Non-Fatal errors detected by the device to the Root Complex	RW	Yes	0
15:9	***Reserved***	RsvdP	No	0-0h

Register 12-271. E0Ah PCI Command Port 5 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**I/O Access Enable** 0 = PEX 8624 ignores I/O Space accesses on Port 5's primary interface 1 = PEX 8624 responds to I/O Space accesses on Port 5's primary interface	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8624 ignores Memory Space accesses on Port 5's primary interface 1 = PEX 8624 responds to Memory Space accesses on Port 5's primary interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8624 Memory and I/O Request forwarding upstream. Neither affect Message forwarding nor Completions traveling upstream or downstream. 0 = PEX 8624 handles Memory and I/O Requests received on Port 5's downstream/secondary interface as URs; for Non-Posted Requests, the PEX 8624 returns a Completion with UR Completion status 1 = PEX 8624 forwards Memory and I/O Requests upstream	RW	Yes	0
7:3	***Reserved***	RsvdP	No	0-0h
8	**SERR# Enable** Controls the **PCI Status** register *Signaled System Error* bit (offset 04h[30]). 0 = No error is detected 1 = Enables reporting of Fatal and Non-Fatal errors detected by the device to the Root Complex	RW	Yes	0
15:9	***Reserved***	RsvdP	No	0-0h

Register 12-272. E0Ch PCI Command Port 6 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**I/O Access Enable** 0 = PEX 8624 ignores I/O Space accesses on Port 6's primary interface 1 = PEX 8624 responds to I/O Space accesses on Port 6's primary interface	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8624 ignores Memory Space accesses on Port 6's primary interface 1 = PEX 8624 responds to Memory Space accesses on Port 6's primary interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8624 Memory and I/O Request forwarding upstream. Neither affect Message forwarding nor Completions traveling upstream or downstream. 0 = PEX 8624 handles Memory and I/O Requests received on Port 6's downstream/secondary interface as URs; for Non-Posted Requests, the PEX 8624 returns a Completion with UR Completion status 1 = PEX 8624 forwards Memory and I/O Requests upstream	RW	Yes	0
7:3	***Reserved***	RsvdP	No	0-0h
8	**SERR# Enable** Controls the **PCI Status** register *Signaled System Error* bit (offset 04h[30]). 0 = No error is detected 1 = Enables reporting of Fatal and Non-Fatal errors detected by the device to the Root Complex	RW	Yes	0
15:9	***Reserved***	RsvdP	No	0-0h

Register 12-273. E10h PCI Command Port 8 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**I/O Access Enable** 0 = PEX 8624 ignores I/O Space accesses on Port 8's primary interface 1 = PEX 8624 responds to I/O Space accesses on Port 8's primary interface	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8624 ignores Memory Space accesses on Port 8's primary interface 1 = PEX 8624 responds to Memory Space accesses on Port 8's primary interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8624 Memory and I/O Request forwarding upstream. Neither affect Message forwarding nor Completions traveling upstream or downstream. 0 = PEX 8624 handles Memory and I/O Requests received on Port 8's downstream/secondary interface as URs; for Non-Posted Requests, the PEX 8624 returns a Completion with UR Completion status 1 = PEX 8624 forwards Memory and I/O Requests upstream	RW	Yes	0
7:3	***Reserved***	RsvdP	No	0-0h
8	**SERR# Enable** Controls the **PCI Status** register *Signaled System Error* bit (offset 04h[30]). 0 = No error is detected 1 = Enables reporting of Fatal and Non-Fatal errors detected by the device to the Root Complex	RW	Yes	0
15:9	***Reserved***	RsvdP	No	0-0h

Register 12-274. E12h PCI Command Port 9 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**I/O Access Enable** 0 = PEX 8624 ignores I/O Space accesses on Port 9's primary interface 1 = PEX 8624 responds to I/O Space accesses on Port 9's primary interface	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8624 ignores Memory Space accesses on Port 9's primary interface 1 = PEX 8624 responds to Memory Space accesses on Port 9's primary interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8624 Memory and I/O Request forwarding upstream. Neither affect Message forwarding nor Completions traveling upstream or downstream. 0 = PEX 8624 handles Memory and I/O Requests received on Port 9's downstream/secondary interface as URs; for Non-Posted Requests, the PEX 8624 returns a Completion with UR Completion status 1 = PEX 8624 forwards Memory and I/O Requests upstream	RW	Yes	0
7:3	***Reserved***	RsvdP	No	0-0h
8	**SERR# Enable** Controls the **PCI Status** register *Signaled System Error* bit (offset 04h[30]). 0 = No error is detected 1 = Enables reporting of Fatal and Non-Fatal errors detected by the device to the Root Complex	RW	Yes	0
15:9	***Reserved***	RsvdP	No	0-0h

Register 12-275. E20h Bridge Control Port 0 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RsvdP	No	0
1	**SERR# Enable** Controls forwarding of ERR_COR, ERR_FATAL, and ERR_NONFATAL from the secondary interface to the primary interface. When Set, and the **PCI Command Port 0** register *SERR# Enable* bit is also Set, enables the **PCI Status** register *Signaled System Error* bit.	RW	Yes	0
2	**ISA Enable** Modifies the bridge response to ISA I/O addresses. Applies only to I/O addresses, enabled by the **I/O Base** and **I/O Limit** registers, that are within the first 64 KB of PCI I/O Address space (0000_0000h to 0000_FFFFh). When Set, the bridge blocks forwarding of I/O transactions from the primary to secondary interface that address the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary interface), I/O transactions are forwarded if they address the last 768 bytes in each 1-KB block. The default state of this bit after reset must be 0. 0 = Forward downstream all I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers 1 = Forward upstream ISA I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers that are within the first 64 KB of PCI I/O Address space (top 768 bytes of each 1-KB block)	RW	Yes	0
3	**VGA Enable** Modifies the bridge response to VGA-compatible addresses. When Set, the bridge positively decodes and forwards the following addresses on the primary interface to the secondary interface (and, conversely, blocks forwarding of these addresses from the secondary interface to the primary interface): • Memory addresses within the range 000A_0000h to 000B_FFFFh • I/O addresses in the first 64 KB of the I/O Address space (AD[31:16] is 0000h), where AD[9:0] is within the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – AD[15:10] is not decoded) Additionally, when Set, forwarding of these addresses is independent of the: • Memory and I/O Address ranges defined by the bridge **I/O Base**, **I/O Limit**, **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers • Bit 2 (*ISA Enable*) Setting Forwarding of these addresses is qualified by the **PCI Command Port 0** register *I/O Access Enable* and *Memory Access Enable* bits. The default state of this bit after reset must be 0. 0 = Do not forward VGA-compatible Memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined Memory and I/O Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (when the *I/O Access Enable* and *Memory Access Enable* bits are Set), independent of the Memory and I/O Address ranges and independent of the *ISA Enable* bit	RW	Yes	0

Register 12-275. E20h Bridge Control Port 0 (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**VGA 16-Bit Enable** Used only when bit 3 (*VGA Enable*) is also Set, enabling VGA I/O decoding and forwarding by the bridge. Status after reset is 0. Enables system configuration software to select between 10- and 16-bit I/O address decoding, for VGA I/O register accesses forwarded from the primary interface to the secondary interface. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	Yes	0
15:5	***Reserved***	RsvdP	No	0-0h

Register 12-276. E22h Bridge Control Port 1 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RsvdP	No	0
1	**SERR# Enable** Controls forwarding of ERR_COR, ERR_FATAL, and ERR_NONFATAL from the secondary interface to the primary interface. When Set, and the **PCI Command Port 1** register *SERR# Enable* bit is also Set, enables the **PCI Status** register *Signaled System Error* bit.	RW	Yes	0
2	**ISA Enable** Modifies the bridge response to ISA I/O addresses. Applies only to I/O addresses, enabled by the **I/O Base** and **I/O Limit** registers, that are within the first 64 KB of PCI I/O Address space (0000_0000h to 0000_FFFFh). When Set, the bridge blocks forwarding of I/O transactions from the primary to secondary interface that address the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary interface), I/O transactions are forwarded if they address the last 768 bytes in each 1-KB block. The default state of this bit after reset must be 0. 0 = Forward downstream all I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers 1 = Forward upstream ISA I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers that are within the first 64 KB of PCI I/O Address space (top 768 bytes of each 1-KB block)	RW	Yes	0
3	**VGA Enable** Modifies the bridge response to VGA-compatible addresses. When Set, the bridge positively decodes and forwards the following addresses on the primary interface to the secondary interface (and, conversely, blocks forwarding of these addresses from the secondary interface to the primary interface): • Memory addresses within the range 000A_0000h to 000B_FFFFh • I/O addresses in the first 64 KB of the I/O Address space (AD[31:16] is 0000h), where AD[9:0] is within the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – AD[15:10] is not decoded) Additionally, when Set, forwarding of these addresses is independent of the: • Memory and I/O Address ranges defined by the bridge **I/O Base**, **I/O Limit**, **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers • Bit 2 (*ISA Enable*) Setting Forwarding of these addresses is qualified by the **PCI Command Port 1** register *I/O Access Enable* and *Memory Access Enable* bits. The default state of this bit after reset must be 0. 0 = Do not forward VGA-compatible Memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined Memory and I/O Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (when the *I/O Access Enable* and *Memory Access Enable* bits are Set), independent of the Memory and I/O Address ranges and independent of the *ISA Enable* bit	RW	Yes	0

Register 12-276. E22h Bridge Control Port 1 (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**VGA 16-Bit Enable** Used only when bit 3 (*VGA Enable*) is also Set, enabling VGA I/O decoding and forwarding by the bridge. Status after reset is 0. Enables system configuration software to select between 10- and 16-bit I/O address decoding, for VGA I/O register accesses forwarded from the primary interface to the secondary interface. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	Yes	0
15:5	***Reserved***	RsvdP	No	0-0h

Register 12-277. E28h Bridge Control Port 4 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RsvdP	No	0
1	**SERR# Enable** Controls forwarding of ERR_COR, ERR_FATAL, and ERR_NONFATAL from the secondary interface to the primary interface. When Set, and the **PCI Command Port 4** register *SERR# Enable* bit is also Set, enables the **PCI Status** register *Signaled System Error* bit.	RW	Yes	0
2	**ISA Enable** Modifies the bridge response to ISA I/O addresses. Applies only to I/O addresses, enabled by the **I/O Base** and **I/O Limit** registers, that are within the first 64 KB of PCI I/O Address space (0000_0000h to 0000_FFFFh). When Set, the bridge blocks forwarding of I/O transactions from the primary to secondary interface that address the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary interface), I/O transactions are forwarded if they address the last 768 bytes in each 1-KB block. The default state of this bit after reset must be 0. 0 = Forward downstream all I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers 1 = Forward upstream ISA I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers that are within the first 64 KB of PCI I/O Address space (top 768 bytes of each 1-KB block)	RW	Yes	0
3	**VGA Enable** Modifies the bridge response to VGA-compatible addresses. When Set, the bridge positively decodes and forwards the following addresses on the primary interface to the secondary interface (and, conversely, blocks forwarding of these addresses from the secondary interface to the primary interface): • Memory addresses within the range 000A_0000h to 000B_FFFFh • I/O addresses in the first 64 KB of the I/O Address space (AD[31:16] is 0000h), where AD[9:0] is within the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – AD[15:10] is not decoded) Additionally, when Set, forwarding of these addresses is independent of the: • Memory and I/O Address ranges defined by the bridge **I/O Base**, **I/O Limit**, **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers • Bit 2 (*ISA Enable*) Setting Forwarding of these addresses is qualified by the **PCI Command Port 4** register *I/O Access Enable* and *Memory Access Enable* bits. The default state of this bit after reset must be 0. 0 = Do not forward VGA-compatible Memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined Memory and I/O Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (when the *I/O Access Enable* and *Memory Access Enable* bits are Set), independent of the Memory and I/O Address ranges and independent of the *ISA Enable* bit	RW	Yes	0

Register 12-277. E28h Bridge Control Port 4 (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**VGA 16-Bit Enable** Used only when bit 3 (*VGA Enable*) is also Set, enabling VGA I/O decoding and forwarding by the bridge. Status after reset is 0. Enables system configuration software to select between 10- and 16-bit I/O address decoding, for VGA I/O register accesses forwarded from the primary interface to the secondary interface. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	Yes	0
15:5	***Reserved***	RsvdP	No	0-0h

Register 12-278. E2Ah Bridge Control Port 5 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RsvdP	No	0
1	**SERR# Enable** Controls forwarding of ERR_COR, ERR_FATAL, and ERR_NONFATAL from the secondary interface to the primary interface. When Set, and the **PCI Command Port 5** register *SERR# Enable* bit is also Set, enables the **PCI Status** register *Signaled System Error* bit.	RW	Yes	0
2	**ISA Enable** Modifies the bridge response to ISA I/O addresses. Applies only to I/O addresses, enabled by the **I/O Base** and **I/O Limit** registers, that are within the first 64 KB of PCI I/O Address space (0000_0000h to 0000_FFFFh). When Set, the bridge blocks forwarding of I/O transactions from the primary to secondary interface that address the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary interface), I/O transactions are forwarded if they address the last 768 bytes in each 1-KB block. The default state of this bit after reset must be 0. 0 = Forward downstream all I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers 1 = Forward upstream ISA I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers that are within the first 64 KB of PCI I/O Address space (top 768 bytes of each 1-KB block)	RW	Yes	0
3	**VGA Enable** Modifies the bridge response to VGA-compatible addresses. When Set, the bridge positively decodes and forwards the following addresses on the primary interface to the secondary interface (and, conversely, blocks forwarding of these addresses from the secondary interface to the primary interface): • Memory addresses within the range 000A_0000h to 000B_FFFFh • I/O addresses in the first 64 KB of the I/O Address space (AD[31:16] is 0000h), where AD[9:0] is within the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – AD[15:10] is not decoded) Additionally, when Set, forwarding of these addresses is independent of the: • Memory and I/O Address ranges defined by the bridge **I/O Base**, **I/O Limit**, **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers • Bit 2 (*ISA Enable*) Setting Forwarding of these addresses is qualified by the **PCI Command Port 5** register *I/O Access Enable* and *Memory Access Enable* bits. The default state of this bit after reset must be 0. 0 = Do not forward VGA-compatible Memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined Memory and I/O Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (when the *I/O Access Enable* and *Memory Access Enable* bits are Set), independent of the Memory and I/O Address ranges and independent of the *ISA Enable* bit	RW	Yes	0

Register 12-278. E2Ah Bridge Control Port 5 (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**VGA 16-Bit Enable** Used only when bit 3 (*VGA Enable*) is also Set, enabling VGA I/O decoding and forwarding by the bridge. Status after reset is 0. Enables system configuration software to select between 10- and 16-bit I/O address decoding, for VGA I/O register accesses forwarded from the primary interface to the secondary interface. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	Yes	0
15:5	***Reserved***	RsvdP	No	0-0h

Register 12-279. E2Ch Bridge Control Port 6 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RsvdP	No	0
1	**SERR# Enable** Controls forwarding of ERR_COR, ERR_FATAL, and ERR_NONFATAL from the secondary interface to the primary interface. When Set, and the **PCI Command Port 6** register *SERR# Enable* bit is also Set, enables the **PCI Status** register *Signaled System Error* bit.	RW	Yes	0
2	**ISA Enable** Modifies the bridge response to ISA I/O addresses. Applies only to I/O addresses, enabled by the **I/O Base** and **I/O Limit** registers, that are within the first 64 KB of PCI I/O Address space (0000_0000h to 0000_FFFFh). When Set, the bridge blocks forwarding of I/O transactions from the primary to secondary interface that address the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary interface), I/O transactions are forwarded if they address the last 768 bytes in each 1-KB block. The default state of this bit after reset must be 0. 0 = Forward downstream all I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers 1 = Forward upstream ISA I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers that are within the first 64 KB of PCI I/O Address space (top 768 bytes of each 1-KB block)	RW	Yes	0
3	**VGA Enable** Modifies the bridge response to VGA-compatible addresses. When Set, the bridge positively decodes and forwards the following addresses on the primary interface to the secondary interface (and, conversely, blocks forwarding of these addresses from the secondary interface to the primary interface): • Memory addresses within the range 000A_0000h to 000B_FFFFh • I/O addresses in the first 64 KB of the I/O Address space (AD[31:16] is 0000h), where AD[9:0] is within the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – AD[15:10] is not decoded) Additionally, when Set, forwarding of these addresses is independent of the: • Memory and I/O Address ranges defined by the bridge **I/O Base**, **I/O Limit**, **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers • Bit 2 (*ISA Enable*) Setting Forwarding of these addresses is qualified by the **PCI Command Port 6** register *I/O Access Enable* and *Memory Access Enable* bits. The default state of this bit after reset must be 0. 0 = Do not forward VGA-compatible Memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined Memory and I/O Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (when the *I/O Access Enable* and *Memory Access Enable* bits are Set), independent of the Memory and I/O Address ranges and independent of the *ISA Enable* bit	RW	Yes	0

Register 12-279. E2Ch Bridge Control Port 6 (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**VGA 16-Bit Enable** Used only when bit 3 (*VGA Enable*) is also Set, enabling VGA I/O decoding and forwarding by the bridge. Status after reset is 0. Enables system configuration software to select between 10- and 16-bit I/O address decoding, for VGA I/O register accesses forwarded from the primary interface to the secondary interface. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	Yes	0
15:5	***Reserved***	RsvdP	No	0-0h

Register 12-280. E30h Bridge Control Port 8 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RsvdP	No	0
1	**SERR# Enable** Controls forwarding of ERR_COR, ERR_FATAL, and ERR_NONFATAL from the secondary interface to the primary interface. When Set, and the **PCI Command Port 8** register *SERR# Enable* bit is also Set, enables the **PCI Status** register *Signaled System Error* bit.	RW	Yes	0
2	**ISA Enable** Modifies the bridge response to ISA I/O addresses. Applies only to I/O addresses, enabled by the **I/O Base** and **I/O Limit** registers, that are within the first 64 KB of PCI I/O Address space (0000_0000h to 0000_FFFFh). When Set, the bridge blocks forwarding of I/O transactions from the primary to secondary interface that address the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary interface), I/O transactions are forwarded if they address the last 768 bytes in each 1-KB block. The default state of this bit after reset must be 0. 0 = Forward downstream all I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers 1 = Forward upstream ISA I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers that are within the first 64 KB of PCI I/O Address space (top 768 bytes of each 1-KB block)	RW	Yes	0
3	**VGA Enable** Modifies the bridge response to VGA-compatible addresses. When Set, the bridge positively decodes and forwards the following addresses on the primary interface to the secondary interface (and, conversely, blocks forwarding of these addresses from the secondary interface to the primary interface): • Memory addresses within the range 000A_0000h to 000B_FFFFh • I/O addresses in the first 64 KB of the I/O Address space (AD[31:16] is 0000h), where AD[9:0] is within the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – AD[15:10] is not decoded) Additionally, when Set, forwarding of these addresses is independent of the: • Memory and I/O Address ranges defined by the bridge **I/O Base**, **I/O Limit**, **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers • Bit 2 (*ISA Enable*) Setting Forwarding of these addresses is qualified by the **PCI Command Port 8** register *I/O Access Enable* and *Memory Access Enable* bits. The default state of this bit after reset must be 0. 0 = Do not forward VGA-compatible Memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined Memory and I/O Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (when the *I/O Access Enable* and *Memory Access Enable* bits are Set), independent of the Memory and I/O Address ranges and independent of the *ISA Enable* bit	RW	Yes	0

Register 12-280. E30h Bridge Control Port 8 (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**VGA 16-Bit Enable** Used only when bit 3 (*VGA Enable*) is also Set, enabling VGA I/O decoding and forwarding by the bridge. Status after reset is 0. Enables system configuration software to select between 10- and 16-bit I/O address decoding, for VGA I/O register accesses forwarded from the primary interface to the secondary interface. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	Yes	0
15:5	***Reserved***	RsvdP	No	0-0h

Register 12-281. E32h Bridge Control Port 9 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Reserved***	RsvdP	No	0
1	**SERR# Enable** Controls forwarding of ERR_COR, ERR_FATAL, and ERR_NONFATAL from the secondary interface to the primary interface. When Set, and the **PCI Command Port 9** register *SERR# Enable* bit is also Set, enables the **PCI Status** register *Signaled System Error* bit.	RW	Yes	0
2	**ISA Enable** Modifies the bridge response to ISA I/O addresses. Applies only to I/O addresses, enabled by the **I/O Base** and **I/O Limit** registers, that are within the first 64 KB of PCI I/O Address space (0000_0000h to 0000_FFFFh). When Set, the bridge blocks forwarding of I/O transactions from the primary to secondary interface that address the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary interface), I/O transactions are forwarded if they address the last 768 bytes in each 1-KB block. The default state of this bit after reset must be 0. 0 = Forward downstream all I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers 1 = Forward upstream ISA I/O addresses in the Address range defined by the **I/O Base** and **I/O Limit** registers that are within the first 64 KB of PCI I/O Address space (top 768 bytes of each 1-KB block)	RW	Yes	0
3	**VGA Enable** Modifies the bridge response to VGA-compatible addresses. When Set, the bridge positively decodes and forwards the following addresses on the primary interface to the secondary interface (and, conversely, blocks forwarding of these addresses from the secondary interface to the primary interface): • Memory addresses within the range 000A_0000h to 000B_FFFFh • I/O addresses in the first 64 KB of the I/O Address space (AD[31:16] is 0000h), where AD[9:0] is within the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – AD[15:10] is not decoded) Additionally, when Set, forwarding of these addresses is independent of the: • Memory and I/O Address ranges defined by the bridge **I/O Base**, **I/O Limit**, **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers • Bit 2 (*ISA Enable*) Setting Forwarding of these addresses is qualified by the **PCI Command Port 9** register *I/O Access Enable* and *Memory Access Enable* bits. The default state of this bit after reset must be 0. 0 = Do not forward VGA-compatible Memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined Memory and I/O Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (when the *I/O Access Enable* and *Memory Access Enable* bits are Set), independent of the Memory and I/O Address ranges and independent of the *ISA Enable* bit	RW	Yes	0

Register 12-281. E32h Bridge Control Port 9 (Only Ports 0, 4, and 8) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**VGA 16-Bit Enable** Used only when bit 3 (*VGA Enable*) is also Set, enabling VGA I/O decoding and forwarding by the bridge. Status after reset is 0. Enables system configuration software to select between 10- and 16-bit I/O address decoding, for VGA I/O register accesses forwarded from the primary interface to the secondary interface. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	Yes	0
15:5	***Reserved***	RsvdP	No	0-0h

12.16.13 Device-Specific Registers – Source Queue Weight and Soft Error (Offsets F00h – F30h)

This section details the Device-Specific Source Queue Weight and Soft Error registers. Table 12-55 defines the register map.

Table 12-55. Device-Specific Source Queue Weight and Soft Error Register Map[a]

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				F00h – F0Ch
Port Egress TLP Threshold				F10h
Reserved				F14h
Soft Error Counters 1				F18h
Factory Test Only		Soft Error Counters 2		F1Ch
Soft Error Counters 3			***Factory Test Only***	F20h
Soft Error Counters 4				F24h
Reserved		Soft Error Counters 5		F28h
Soft Error Counters 6			***Reserved***	F2Ch
Soft Error Injection				F30h

a. Register offset F10h is Port-specific, the remaining registers in this structure are Station-specific; all are device-specific.

Register 12-282. F10h Port Egress TLP Threshold (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Caution: Read Pacing and Source Queuing should not be concurrently enabled. The two features are incompatible and doing so can result in Fatal errors.				
10:0	**Port Lower TLP Counter** When Source Scheduling is disabled due to the Port Upper TLP Counter (threshold) being exceeded, Source Scheduling is re-enabled when the Port TLP Counter goes below the Port Lower TLP Counter (this threshold). Because the default Setting of this field is 7FFh (2,047), which is greater than the maximum amount of TLPs that can be queued in the PEX 8624, the Source Scheduler is disabled, by default.	RWS	Yes	7FFh
15:11	***Reserved***	RsvdP	No	00h
26:16	**Port Upper TLP Counter** When the Port TLP Counter is greater than or equal to this value, the Source Scheduler disables TLP Scheduling to this egress Port. Because the default Setting of this field is 7FFh (2,047), which is greater than the maximum amount of TLPs that can be queued in the PEX 8624, the Source Scheduler is disabled, by default.	RWS	Yes	7FFh
31:27	***Reserved***	RsvdP	No	00h

Register 12-283. F18h Soft Error Counters 1 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Station 0 Packet RAM0 Instance 0 1-Bit Soft Error Counter Value**	RO	No	00h
15:8	**Station 0 Packet RAM0 Instance 1 1-Bit Soft Error Counter Value**	RO	No	00h
23:16	**Station 1 Packet RAM0 Instance 0 1-Bit Soft Error Counter Value**	RO	No	00h
31:24	**Station 1 Packet RAM0 Instance 1 1-Bit Soft Error Counter Value**	RO	No	00h

Register 12-284. F1Ch Soft Error Counters 2 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Station 2 Packet RAM0 Instance 0 1-Bit Soft Error Counter Value**	RO	No	00h
15:8	**Station 2 Packet RAM0 Instance 1 1-Bit Soft Error Counter Value**	RO	No	00h
31:16	***Factory Test Only***	RO	No	0000h

Register 12-285. F20h Soft Error Counters 3 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	***Factory Test Only***	RO	No	00h
15:8	**Station 0 Header RAM 1-Bit Soft Error Counter Value**	RO	No	00h
23:16	**Station 1 Header RAM 1-Bit Soft Error Counter Value**	RO	No	00h
31:24	**Station 2 Header RAM 1-Bit Soft Error Counter Value**	RO	No	00h

Register 12-286. F24h Soft Error Counters 4 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Station 0 Packet RAM1 Instance 0 1-Bit Soft Error Counter Value**	RO	No	00h
15:8	**Station 0 Packet RAM1 Instance 1 1-Bit Soft Error Counter Value**	RO	No	00h
23:16	**Station 1 Packet RAM1 Instance 0 1-Bit Soft Error Counter Value**	RO	No	00h
31:24	**Station 1 Packet RAM1 Instance 1 1-Bit Soft Error Counter Value**	RO	No	00h

Register 12-287. F28h Soft Error Counters 5 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Station 2 Packet RAM1 Instance 0 1-Bit Soft Error Counter Value**	RO	No	00h
15:8	**Station 2 Packet RAM1 Instance 1 1-Bit Soft Error Counter Value**	RO	No	00h
31:16	***Reserved***	RsvdP	No	0000h

Register 12-288. F2Ch Soft Error Counters 6 (Only Ports 0, 4, and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	***Reserved***	RsvdP	No	00h
15:8	**Destination Queue Link List RAM 1-Bit Soft Error Counter Value**	RO	No	00h
23:16	**Source Queue Link List RAM 1-Bit Soft Error Counter Value**	RO	No	00h
31:24	**32 Entry Retry Buffer 1-Bit Soft Error Counter Value**	RO	No	00h

Register 12-289. F30h Soft Error Injection (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
0	**Destination Queue Link List RAM Instance 0 1-Bit Soft Error Injection Toggle** Every toggle injects an error.		RWS	Yes	0
1	**Destination Queue Link List RAM Instance 0 2-Bit Soft Error Injection Toggle** Every toggle injects an error.		RWS	Yes	0
2	**Destination Queue Link List RAM Instance 0 Error Injection Field Select** 0 = Inject Soft error in the *ECC Code* field 1 = Inject Soft error in the *Data* field		RWS	Yes	0
3	**Destination Queue Link List RAM Instance 1 1-Bit Soft Error Injection Toggle** Every toggle injects an error. ***Note:*** *This bit is valid only on upstream Port 0, and* ***reserved*** *on all other Ports.*	Upstream Port 0 (refer to Note)	RWS	Yes	0
	Reserved	All other Ports	RsvdP	No	0
4	**Destination Queue Link List RAM Instance 1 2-Bit Soft Error Injection Toggle** Every toggle injects an error.		RWS	Yes	0
5	**Destination Queue Link List RAM Instance 1 Error Injection Field Select** 0 = Inject Soft error in the *ECC Code* field 1 = Inject Soft error in the *Data* field		RWS	Yes	0
8:6	***Reserved***		RsvdP	No	000b
9	**32 Entry Retry Buffer 1-Bit Soft Error Injection Toggle** Every toggle injects an error.		RWS	Yes	0
10	**32 Entry Retry Buffer 2-Bit Soft Error Injection Toggle** Every toggle injects an error.		RWS	Yes	0
11	**32 Entry Retry Buffer Soft Error Injection Field Select** 0 = Inject Soft error in the *ECC Code* field 1 = Inject Soft error in the *Data* field		RWS	Yes	0
31:12	***Reserved***		RsvdP	No	0000_0h

12.16.14 Device-Specific Registers – Read Pacing (Offsets F34h – F3Ch)

Caution: ***Source Queuing and Read Pacing should not be concurrently enabled. The two features are incompatible and doing so can result in Fatal errors.***

This section details the Device-Specific Read Pacing registers. Although the Read Pacing feature is supported on all Ports, its registers are implemented as follows. If Port 0 is the NT Port, the NT Port Virtual Interface implements this register. Otherwise, Port 0 implements this register.

Read Pacing is described, in detail, in Section 8.7, "Read Pacing." Table 12-56 defines the register map.

Table 12-56. Device-Specific Read Pacing Register Map (Only Upstream Port 0, or NT Port Virtual Interface (if Port 0 is the NT Port); *Reserved* (RsvdP) for All Other Ports)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Read Pacing Control				F34h
Read Pacing Threshold 1		***Reserved***		F38h
Read Pacing Threshold 2				F3Ch

Register 12-290. F34h Read Pacing Control (Only Upstream Port 0, or NT Port Virtual Interface (if Port 0 is the NT Port); *Reserved* (RsvdP) for All Other Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Caution: ***Read Pacing and Source Queuing should not be concurrently enabled. The two features are incompatible and doing so can result in Fatal errors.*** ***Notes:*** *Read Pacing must be enabled for Read Spreading to be enabled. (That is, for a Port to have Read Spreading enabled, the corresponding Port bits within this register, for both Read Pacing and Read Spreading, must both be Cleared.)* *If Port 0 is the NT Port, the NT Port Virtual Interface implements this register. Otherwise, Port 0 implements this register.*				
0	**Port 0 Read Pacing Disable** 0 = Read Pacing is enabled for this Port 1 = Read Pacing is disabled for this Port	RWS	Yes	1
1	**Port 1 Read Pacing Disable** 0 = Read Pacing is enabled for this Port 1 = Read Pacing is disabled for this Port	RWS	Yes	1
4:2	***Factory Test Only***	RsvdP	No	000b
5	**Port 5 Read Pacing Disable** 0 = Read Pacing is enabled for this Port 1 = Read Pacing is disabled for this Port	RWS	Yes	1
6	**Port 6 Read Pacing Disable** 0 = Read Pacing is enabled for this Port 1 = Read Pacing is disabled for this Port	RWS	Yes	1
7	***Factory Test Only***	RsvdP	No	0
8	**Port 8 Read Pacing Disable** 0 = Read Pacing is enabled for this Port 1 = Read Pacing is disabled for this Port	RWS	Yes	1
9	**Port 9 Read Pacing Disable** 0 = Read Pacing is enabled for this Port 1 = Read Pacing is disabled for this Port	RWS	Yes	1
11:10	***Factory Test Only***	RsvdP	No	00b
15:12	***Reserved***	RsvdP	No	0h

Register 12-290. F34h Read Pacing Control (Only Upstream Port 0, or NT Port Virtual Interface (if Port 0 is the NT Port); *Reserved* (RsvdP) for All Other Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
16	**Port 0 Memory Read Spreading Disable** 0 = Memory Read Spreading is enabled for this Port 1 = Memory Read Spreading is disabled for this Port	RWS	Yes	0
17	**Port 1 Memory Read Spreading Disable** 0 = Memory Read Spreading is enabled for this Port 1 = Memory Read Spreading is disabled for this Port	RWS	Yes	0
20:18	***Factory Test Only***	RsvdP	No	000b
21	**Port 5 Memory Read Spreading Disable** 0 = Memory Read Spreading is enabled for this Port 1 = Memory Read Spreading is disabled for this Port	RWS	Yes	0
22	**Port 6 Memory Read Spreading Disable** 0 = Memory Read Spreading is enabled for this Port 1 = Memory Read Spreading is disabled for this Port	RWS	Yes	0
23	***Factory Test Only***	RsvdP	No	0
24	**Port 8 Memory Read Spreading Disable** 0 = Memory Read Spreading is enabled for this Port 1 = Memory Read Spreading is disabled for this Port	RWS	Yes	0
25	**Port 9 Memory Read Spreading Disable** 0 = Memory Read Spreading is enabled for this Port 1 = Memory Read Spreading is disabled for this Port	RWS	Yes	0
27:26	***Factory Test Only***	RsvdP	No	00b
31:28	***Reserved***	RsvdP	No	0h

Register 12-291. F38h Read Pacing Threshold 1 (Only Upstream Port 0, or NT Port Virtual Interface (if Port 0 is the NT Port); *Reserved* (RsvdP) for All Other Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *If Port 0 is the NT Port, the NT Port Virtual Interface implements this register. Otherwise, Port 0 implements this register.*				
15:0	***Reserved***	RsvdP	No	0000h
28:16	**x8 Port Memory Read Outstanding Threshold** Specified in DWords. Default value of 600h programs the threshold to 6 KB.	RWS	Yes	600h
31:29	***Reserved***	RsvdP	No	000b

Register 12-292. F3Ch Read Pacing Threshold 2 (Only Upstream Port 0, or NT Port Virtual Interface (if Port 0 is the NT Port); *Reserved* (RsvdP) for All Other Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *If Port 0 is the NT Port, the NT Port Virtual Interface implements this register. Otherwise, Port 0 implements this register.*				
12:0	**x4 Port Memory Read Outstanding Threshold** Specified in DWords. Default value of 400h programs the threshold to 4 KB, for x4, as well as x2, Ports.	RWS	Yes	400h
15:13	***Reserved***	RsvdP	No	000b
16	**Port 0 Memory Read Outstanding Counter Reset** Provides a mechanism for Clearing the Counter when an error condition occurs, with either the device that issued the Read Request, or the device that was to provide the Read Completions, where a System Level Reset will not be issued. If the Counter is not Cleared after an error condition such as this, the threshold will not be accurate. 0 = Read Outstanding Counter value increments, with each outstanding Read 1 = Resets Read Outstanding Counter	RWS	Yes	0
17	**Port 1 Memory Read Outstanding Counter Reset** Provides a mechanism for Clearing the Counter when an error condition occurs, with either the device that issued the Read Request, or the device that was to provide the Read Completions, where a System Level Reset will not be issued. If the Counter is not Cleared after an error condition such as this, the threshold will not be accurate. 0 = Read Outstanding Counter value increments, with each outstanding Read 1 = Resets Read Outstanding Counter	RWS	Yes	0
20:18	***Factory Test Only***	RsvdP	No	000b
21	**Port 5 Memory Read Outstanding Counter Reset** Provides a mechanism for Clearing the Counter when an error condition occurs, with either the device that issued the Read Request, or the device that was to provide the Read Completions, where a System Level Reset will not be issued. If the Counter is not Cleared after an error condition such as this, the threshold will not be accurate. 0 = Read Outstanding Counter value increments, with each outstanding Read 1 = Resets Read Outstanding Counter	RWS	Yes	0
22	**Port 6 Memory Read Outstanding Counter Reset** Provides a mechanism for Clearing the Counter when an error condition occurs, with either the device that issued the Read Request, or the device that was to provide the Read Completions, where a System Level Reset will not be issued. If the Counter is not Cleared after an error condition such as this, the threshold will not be accurate. 0 = Read Outstanding Counter value increments, with each outstanding Read 1 = Resets Read Outstanding Counter	RWS	Yes	0
23	***Factory Test Only***	RsvdP	No	0

Register 12-292. F3Ch Read Pacing Threshold 2 (Only Upstream Port 0, or NT Port Virtual Interface (if Port 0 is the NT Port); *Reserved* (RsvdP) for All Other Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
24	**Port 8 Memory Read Outstanding Counter Reset** Provides a mechanism for Clearing the Counter when an error condition occurs, with either the device that issued the Read Request, or the device that was to provide the Read Completions, where a System Level Reset will not be issued. If the Counter is not Cleared after an error condition such as this, the threshold will not be accurate. 0 = Read Outstanding Counter value increments, with each outstanding Read 1 = Resets Read Outstanding Counter	RWS	Yes	0
25	**Port 9 Memory Read Outstanding Counter Reset** Provides a mechanism for Clearing the Counter when an error condition occurs, with either the device that issued the Read Request, or the device that was to provide the Read Completions, where a System Level Reset will not be issued. If the Counter is not Cleared after an error condition such as this, the threshold will not be accurate. 0 = Read Outstanding Counter value increments, with each outstanding Read 1 = Resets Read Outstanding Counter	RWS	Yes	0
27:26	***Factory Test Only***	RsvdP	No	00b
31:28	***Reserved***	RsvdP	No	0h

12.16.15 Device-Specific Registers – Error Reporting (Offsets F40h – F4Ch)

This section details the Device-Specific Error Reporting registers. Table 12-57 defines the register map.

Table 12-57. Device-Specific Error Reporting Register Map (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Error Reporting Enable for Ports 0, 1				F40h
Error Reporting Enable for Ports 5, 6				F44h
Error Reporting Enable for Ports 8, 9				F48h
Reserved				F4Ch

Register 12-293. F40h Error Reporting Enable for Ports 0, 1 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**Port 0 Correctable Error Reporting Enable** Shadow copy of **Device Control** register *Correctable Error Reporting Enable* bit (offset 70h[0]), for Port 0.	RW	Yes	0
1	**Port 0 Non-Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Non-Fatal Error Reporting Enable* bit (offset 70h[1]), for Port 0.	RW	Yes	0
2	**Port 0 Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Fatal Error Reporting Enable* bit (offset 70h[2]), for Port 0.	RW	Yes	0
7:3	***Reserved***	RsvdP	No	0-0h
8	**Port 1 Correctable Error Reporting Enable** Shadow copy of **Device Control** register *Correctable Error Reporting Enable* bit (offset 70h[0]), for Port 1.	RW	Yes	0
9	**Port 1 Non-Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Non-Fatal Error Reporting Enable* bit (offset 70h[1]), for Port 1.	RW	Yes	0
10	**Port 1 Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Fatal Error Reporting Enable* bit (offset 70h[2]), for Port 1.	RW	Yes	0
31:11	***Reserved***	RsvdP	No	0-0h

Register 12-294. F44h Error Reporting Enable for Ports 5, 6 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Port 4 Correctable Error Reporting Enable** ***Factory Test Only***	RW	Yes	0
1	**Port 4 Non-Fatal Error Reporting Enable** ***Factory Test Only***	RW	Yes	0
2	**Port 4 Fatal Error Reporting Enable** ***Factory Test Only***	RW	Yes	0
7:3	***Reserved***	RsvdP	No	0-0h
8	**Port 5 Correctable Error Reporting Enable** Shadow copy of **Device Control** register *Correctable Error Reporting Enable* bit (offset 70h[0]), for Port 5.	RW	Yes	0
9	**Port 5 Non-Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Non-Fatal Error Reporting Enable* bit (offset 70h[1]), for Port 5.	RW	Yes	0
10	**Port 5 Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Fatal Error Reporting Enable* bit (offset 70h[2]), for Port 5.	RW	Yes	0
15:11	***Reserved***	RsvdP	No	0-0h
16	**Port 6 Correctable Error Reporting Enable** Shadow copy of **Device Control** register *Correctable Error Reporting Enable* bit (offset 70h[0]), for Port 6.	RW	Yes	0
17	**Port 6 Non-Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Non-Fatal Error Reporting Enable* bit (offset 70h[1]), for Port 6.	RW	Yes	0
18	**Port 6 Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Fatal Error Reporting Enable* bit (offset 70h[2]), for Port 6.	RW	Yes	0
31:19	***Reserved***	RsvdP	No	0-0h

Register 12-295. F48h Error Reporting Enable for Ports 8, 9 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**Port 8 Correctable Error Reporting Enable** Shadow copy of **Device Control** register *Correctable Error Reporting Enable* bit (offset 70h[0]), for Port 8.	RW	Yes	0
1	**Port 8 Non-Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Non-Fatal Error Reporting Enable* bit (offset 70h[1]), for Port 8.	RW	Yes	0
2	**Port 8 Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Fatal Error Reporting Enable* bit (offset 70h[2]), for Port 8.	RW	Yes	0
7:3	***Reserved***	RsvdP	No	0-0h
8	**Port 9 Correctable Error Reporting Enable** Shadow copy of **Device Control** register *Correctable Error Reporting Enable* bit (offset 70h[0]), for Port 9.	RW	Yes	0
9	**Port 9 Non-Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Non-Fatal Error Reporting Enable* bit (offset 70h[1]), for Port 9.	RW	Yes	0
10	**Port 9 Fatal Error Reporting Enable** Shadow copy of **Device Control** register *Fatal Error Reporting Enable* bit (offset 70h[2]), for Port 9.	RW	Yes	0
31:11	***Reserved***	RsvdP	No	0-0h

12.16.16 Device-Specific Registers – ARI Capability (Offsets F50h – F8Ch)

This section details the Device-Specific ARI Capability registers, which shadow ARI-related bits at offsets 8Ch[5] and 90h[5], for each Port. Table 12-58 defines the register map.

Table 12-58. Device-Specific ARI Capability Register Map (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device Control 2 for Port 0		Device Capability 2 for Port 0		F50h
Device Control 2 for Port 1		Device Capability 2 for Port 1		F54h
Factory Test Only				F58h – F5Ch
Device Control 2 for Port 4		Device Capability 2 for Port 4		F60h
Device Control 2 for Port 5		Device Capability 2 for Port 5		F64h
Device Control 2 for Port 6		Device Capability 2 for Port 6		F68h
Factory Test Only				F6Ch
Device Control 2 for Port 8		Device Capability 2 for Port 8		F70h
Device Control 2 for Port 9		Device Capability 2 for Port 9		F74h
Factory Test Only				F78h – F7Ch
Reserved				F80h – F8Ch

Register 12-296. F50h Device Capability and Control 2 for Port 0 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 0				
4:0	***Reserved***	RsvdP	No	0-0h
5	**ARI Forwarding Supported** 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	RO	Yes	1
15:6	***Reserved***	RsvdP	No	0-0h
Device Control 2 for Port 0				
20:16	***Reserved***	RsvdP	No	0-0h
21	**ARI Forwarding Enable** 0 = Disables 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0	RW	Yes	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 12-297. F54h Device Capability and Control 2 for Port 1 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 1				
4:0	***Reserved***	RsvdP	No	0-0h
5	**ARI Forwarding Supported** 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	RO	Yes	1
15:6	***Reserved***	RsvdP	No	0-0h
Device Control 2 for Port 1				
20:16	***Reserved***	RsvdP	No	0-0h
21	**ARI Forwarding Enable** 0 = Disables 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0	RW	Yes	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 12-298. F60h Device Capability and Control 2 for Port 4 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 4				
4:0	***Reserved***	RsvdP	No	0-0h
5	**ARI Forwarding Supported** 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	RO	Yes	1
15:6	***Reserved***	RsvdP	No	0-0h
Device Control 2 for Port 4				
20:16	***Reserved***	RsvdP	No	0-0h
21	**ARI Forwarding Enable** 0 = Disables 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0	RW	Yes	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 12-299. F64h Device Capability and Control 2 for Port 5 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 5				
4:0	***Reserved***	RsvdP	No	0-0h
5	**ARI Forwarding Supported** 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	RO	Yes	1
15:6	***Reserved***	RsvdP	No	0-0h
Device Control 2 for Port 5				
20:16	***Reserved***	RsvdP	No	0-0h
21	**ARI Forwarding Enable** 0 = Disables 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0	RW	Yes	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 12-300. F68h Device Capability and Control 2 for Port 6 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 6				
4:0	***Reserved***	RsvdP	No	0-0h
5	**ARI Forwarding Supported** 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	RO	Yes	1
15:6	***Reserved***	RsvdP	No	0-0h
Device Control 2 for Port 6				
20:16	***Reserved***	RsvdP	No	0-0h
21	**ARI Forwarding Enable** 0 = Disables 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0	RW	Yes	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 12-301. F70h Device Capability and Control 2 for Port 8 (Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 8				
4:0	***Reserved***	RsvdP	No	0-0h
5	**ARI Forwarding Supported** 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	RO	Yes	1
15:6	***Reserved***	RsvdP	No	0-0h
Device Control 2 for Port 8				
20:16	***Reserved***	RsvdP	No	0-0h
21	**ARI Forwarding Enable** 0 = Disables 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0	RW	Yes	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 12-302. F74h Device Capability and Control 2 for Port 9
(Only Ports 0, 4, and 8, and also NT Port Virtual Interface if Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Device Capability 2 for Port 9				
4:0	***Reserved***	RsvdP	No	0-0h
5	**ARI Forwarding Supported** 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	RO	Yes	1
15:6	***Reserved***	RsvdP	No	0-0h
Device Control 2 for Port 9				
20:16	***Reserved***	RsvdP	No	0-0h
21	**ARI Forwarding Enable** 0 = Disables 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0	RW	Yes	0
31:22	***Reserved***	RsvdP	No	0-0h

12.17 Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)

This section details the Advanced Error Reporting Extended Capability registers. Table 12-59 defines the register map.

Table 12-59. Advanced Error Reporting Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Next Capability Offset (138h or 148h)	Capability Version (1h)	PCI Express Extended Capability ID (0001h)	FB4h
Uncorrectable Error Status			FB8h
Uncorrectable Error Mask			FBCh
Uncorrectable Error Severity			FC0h
Correctable Error Status			FC4h
Correctable Error Mask			FC8h
Advanced Error Capabilities and Control			FCCh
Header Log 0			FD0h
Header Log 1			FD4h
Header Log 2			FD8h
Header Log 3			FDCh

Register 12-303. FB4h Advanced Error Reporting Extended Capability Header (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
15:0	**PCI Express Extended Capability ID**		RO	Yes	0001h
19:16	**Capability Version**		RO	Yes	1h
31:20	**Next Capability Offset** Programmed to 138h, which addresses the upstream Port/NT Port Link Interface **Power Budget Extended Capability** structure.	Upstream and NT Port Link Interface	RO	Yes	138h
	Programmed to 148h, which addresses the **Virtual Channel Extended Capability** structure.	Downstream and NT Port Virtual Interface	RO	Yes	148h

Register 12-304. FB8h Uncorrectable Error Status (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
3:0	***Reserved***		RsvdP	No	0h
4	**Data Link Protocol Error Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
5	***Reserved***	Upstream	RsvdP	No	0
	Surprise Down Error Status 0 = No error is detected 1 = Error is detected	Downstream	RW1CS[a]	Yes	0
11:6	***Reserved***		RsvdP	No	0-0h
12	**Poisoned TLP Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
13	**Flow Control Protocol Error Status** ***Reserved/Not supported***		RsvdP	No	0
14	**Completion Timeout Status** ***Not applicable to switches.***		RsvdP	No	0
15	**Completer Abort Status**		RW1CS[a]	Yes	0
16	**Unexpected Completion Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
17	**Receiver Overflow Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
18	**Malformed TLP Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
19	**ECRC Error Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
20	**Unsupported Request Error Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Violation Error Status 0 = No violation is detected 1 = Violation is detected	Downstream	RW1CS[a]	Yes	0
31:22	***Reserved***		RsvdP	No	0-0h

*a. When the **ECC Error Check Disable** register Software Force Error Enable bit (offset 1C8h[2]) is Set, Type changes from RW1CS to RW.*

Register 12-305. FBCh Uncorrectable Error Mask (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
3:0	***Reserved***		RsvdP	No	0h
4	**Data Link Protocol Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
5	***Reserved***	Upstream	RsvdP	No	0
	Surprise Down Error Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	Downstream	RWS	Yes	0
11:6	***Reserved***		RsvdP	No	0-0h
12	**Poisoned TLP Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
13	**Flow Control Protocol Error Mask** ***Reserved/Not supported***		RsvdP	No	0
14	**Completion Timeout Mask** ***Not applicable to switches.***		RsvdP	No	0
15	**Completer Abort Mask**		RWS	Yes	0
16	**Unexpected Completion Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
17	**Receiver Overflow Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
18	**Malformed TLP Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
19	**ECRC Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
20	**Unsupported Request Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Violation Error Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	Downstream	RWS	Yes	0
31:22	***Reserved***		RsvdP	No	0-0h

Register 12-306. FC0h Uncorrectable Error Severity (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
3:0	***Reserved***		RsvdP	No	0h
4	**Data Link Protocol Error Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	1
5	**Surprise Down Error Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal	Upstream	RsvdP	No	1
		Downstream	RWS	Yes	1
11:6	***Reserved***		RsvdP	No	0-0h
12	**Poisoned TLP Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
13	**Flow Control Protocol Error Severity** ***Reserved/Not supported***		RsvdP	No	1
14	**Completion Timeout Severity** ***Not applicable to switches.*** Because the Status and Mask are both ***reserved*** for this bit, Severity can be ignored.		RsvdP	No	0
15	**Completer Abort Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
16	**Unexpected Completion Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
17	**Receiver Overflow Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	1
18	**Malformed TLP Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	1
19	**ECRC Error Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0

Register 12-306. FC0h Uncorrectable Error Severity (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
20	**Unsupported Request Error Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Violation Error Severity 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal	Downstream	RWS	Yes	0
31:22	***Reserved***		RsvdP	No	0-0h

Register 12-307. FC4h Correctable Error Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Receiver Error Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
5:1	***Reserved***	RsvdP	No	0-0h
6	**Bad TLP Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
7	**Bad DLLP Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
8	**REPLAY NUM Rollover Status** Replay Number Rollover status. 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
11:9	***Reserved***	RsvdP	No	000b
12	**Replay Timer Timeout Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
13	**Advisory Non-Fatal Error Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
31:14	***Reserved***	RsvdP	No	0-0h

*a. When the **ECC Error Check Disable** register Software Force Error Enable bit (offset 1C8h[2]) is Set, Type changes from RW1CS to RW.*

Register 12-308. FC8h Correctable Error Mask (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Receiver Error Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
5:1	***Reserved***	RsvdP	No	0-0h
6	**Bad TLP Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
7	**Bad DLLP Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
8	**REPLAY NUM Rollover Mask** Replay Number Rollover mask. 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
11:9	***Reserved***	RsvdP	No	000b
12	**Replay Timer Timeout Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
13	**Advisory Non-Fatal Error Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	1
31:14	***Reserved***	RsvdP	No	0-0h

Register 12-309. FCCh Advanced Error Capabilities and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4:0	**First Error Pointer** Identifies the bit position of the first error reported in the **Uncorrectable Error Status** register (offset FB8h).	ROS	No	1Fh
5	**ECRC Generation Capable** 0 = ECRC generation is not supported 1 = ECRC generation is supported, but must be enabled	RO	Yes	1
6	**ECRC Generation Enable** 0 = ECRC generation is disabled 1 = ECRC generation is enabled	RWS	Yes	0
7	**ECRC Check Capable** 0 = ECRC checking is not supported 1 = ECRC checking is supported, but must be enabled	RO	Yes	1
8	**ECRC Check Enable** 0 = ECRC checking is disabled 1 = ECRC checking is enabled	RWS	Yes	0
31:9	***Reserved***	RsvdP	No	0-0h

Register 12-310. FD0h Header Log 0 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**TLP Header 0** First DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

Register 12-311. FD4h Header Log 1 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**TLP Header 1** Second DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

Register 12-312. FD8h Header Log 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**TLP Header 2** Third DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

Register 12-313. FDCh Header Log 3 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**TLP Header 3** Fourth DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

Chapter 13 Non-Transparent Bridging – NT Mode Only

13.1 Introduction

Note: *Check the latest design guides, application notes and errata list for Non-Transparent (NT) usage.*

The PEX 8624 supports NT bridge functionality (NT mode), which is used to implement High-Availability systems or Intelligent I/O modules using PCI Express technology. The following discusses the basic NT bridging concept, as it applies to a PCI Express system.

NT bridges allow systems to isolate Address spaces, by appearing as an endpoint to the Host. The NT bridge exposes a Type 0 Configuration Space register (CSR) Header and forwards transactions from one domain to the other, using address translation. The NT bridge is used to connect two independent address/Host domains. The NT bridge includes **Doorbell** registers, for transmitting interrupts from one side of the bridge to the other. The bridge also includes **Scratchpad** registers, accessible from both domains for inter-Host communication. The PEX 8624, with a single Port configured to operate in NT mode, supports the Intelligent Adapter Mode system model. NT mode is enabled/disabled by the STRAP_NT_ENABLE# input.

The following are PEX 8624 Non-Transparent Bridging (NTB) key elements:

- Device Type Identification
- NT Port Features
- Intelligent Adapter Mode
- NT Port Reset
- NT Port Memory-Mapped Base Address Registers
- Doorbell Registers
- Scratchpad Registers
- NT Base Address Registers
- Address Translation

13.1.1 Device Type Identification

Devices identify themselves by way of the Conventional PCI CSR Header **PCI Class Code** register. A Transparent PCI-to-PCI bridge identifies itself as a PCI Class Code 060400h. An NT bridge identifies itself as "Other Bridge," 068000h, with a Type 0 Header, which is consistent with the use of other NT bridges available in the industry.

The **PCI Express Capability** register includes a *Device/Port Type* field (offset 68h[23:20]). In this register, a Transparent bridge/switch Port identifies itself as an *upstream* or *downstream Port*, while an NT bridge/switch NT Port identifies itself as a *PCI Express endpoint*.

13.1.2 NT Port Features

- Maps PEX 8624 Configuration registers into either 32- or 64-bit Memory space
- Base Address registers (BARs)
  - Implements four 32-bit, two 32-bit and one 64-bit, or two 64-bit BARs
  - Supports BAR Size programming, through the **BAR*x* Setup** register(s)
  - Allows BARs to be individually disabled, including Memory-Mapped BARs
- Supports Direct Address Translation
  - 32-to-32-bit address conversion
  - 32-to-64-bit address conversion
  - 64-to-32-bit address conversion
  - 64-to-64-bit address conversion
  - Requester ID (Bus Number, Device Number, and Function Number) conversion across the NT bridge
- **Doorbell** registers
- **Scratchpad** registers
- Supports Requester ID and Completion ID translation
- NT Port Link Interface *DL_Active* state change generates interrupt to Local Host
- Supports Cursor mechanism
- Supports Expansion ROM on either NT Port interface
- Supports End-to-end Cyclic Redundancy Check (ECRC)
- Provides ability to Clear *No Snoop* Transaction Layer Packet (TLP) attribute (if enabled)
- Programmable upstream Port and NT Port for the enabling of High Availability systems (Failover and Redundant systems)
- Brings down the NT Port Link when the Local Host domain is down (if enabled)
- Supports the Fencing mechanism
- Signals Device-Specific interrupt to the Local Host when the NT Port Link Interface detects TLP errors
- Signals Device-Specific interrupt to the Local Host when the NT Port Link Interface receives Error Messages (Safety bit-controllable)
- Disables NT Port Link Interface Hot Reset effect (enabled, by default)
- Supports Configuration Space access control

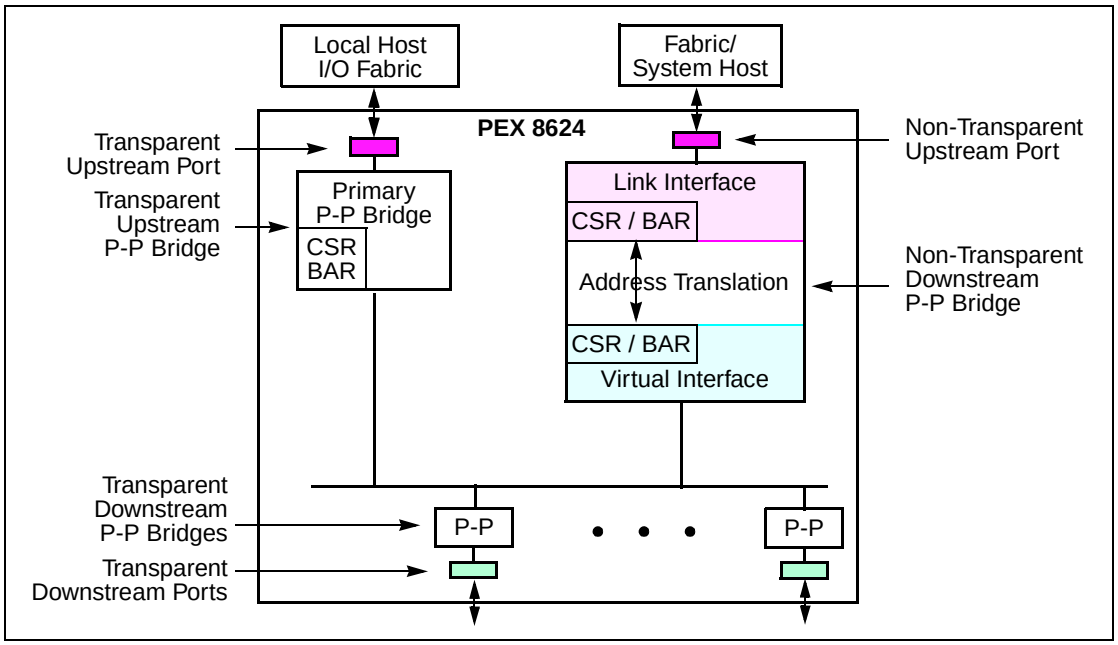
13.1.3 Intelligent Adapter Mode

The use of NT bridges in PCI systems is well-established for supporting intelligent adapters in enterprise and multi-Host systems. The same concept is used in PCI Express bridges and switches.

In Figure 13-1, there are two Type 0 CSR Headers in the NT bridge. The one nearer the internal virtual PCI Bus is referred to as the *Virtual Interface*. The one nearer the PCI Express Link is referred to as the *Link Interface*.

In Intelligent Adapter mode, the NT Port Link Interface is connected to the System Host domain. The System Host manages only the NT Port Link Interface Type 0 function. The Local Host manages all PEX 8624 Transparent Port Type 1 and NT Port Virtual Interface Type 0 functions. Cross-domain traffic is routed through an Address Translation mechanism. (Refer to Section 13.1.9.)

Figure 13-1. Intelligent Adapter Software Model



13.1.4 NT Port Reset

The section discusses NT mode exceptions and enhancements to Transparent mode PCI Express (standard) reset behavior.

13.1.4.1 Fundamental Reset (PEX_PERST#)

PEX_PERST# resets all PEX 8624 states, including NT Port states. This reset initializes all Sticky bits and Configuration registers in Virtual and Link spaces to default values.

13.1.4.2 Intelligent Adapter Mode NT Port Reset

When the Transparent upstream Port receives a Hot Reset or enters the *DL_Down* state, the PEX 8624, by default, propagates the in-band reset to all Transparent downstream Ports and connected downstream devices (to reset the downstream hierarchy), then resets the internal switch fabric and the NT Port Virtual Interface. There is no reset propagation to the NT Port Link Interface, and the Link-side remains intact.

When the NT Port Link Interface receives a Hot Reset or enters the *DL_Down* state, the NT Port Link Interface registers are reset, by default. This Soft Reset does not reset the Transparent Ports nor the NT Port Virtual Interface. Instead, when the NT Port Link Interface receives a Hot Reset (or enters the *DL_Down* state), the PEX_NT_RESET# output is asserted Low for 1 s. The system can use this signal to trigger a reset of the entire Local subsystem.

The PEX 8624 supports an option that allows these Hot Reset conditions at its Transparent upstream Port and NT Port Link Interface to be masked (disabled) for all Ports, including the NT Port, by Setting the **Debug Control** register *Upstream Port and NT-Link DL_Down Reset Propagation Disable* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 1DCh[20]).

When software writes to the PEX 8624 Transparent upstream Port's **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]), the resulting Secondary Bus Reset is (as above) propagated to all PEX 8624 Transparent downstream Ports, and the Port states and NT Port Virtual Interface states are reset.

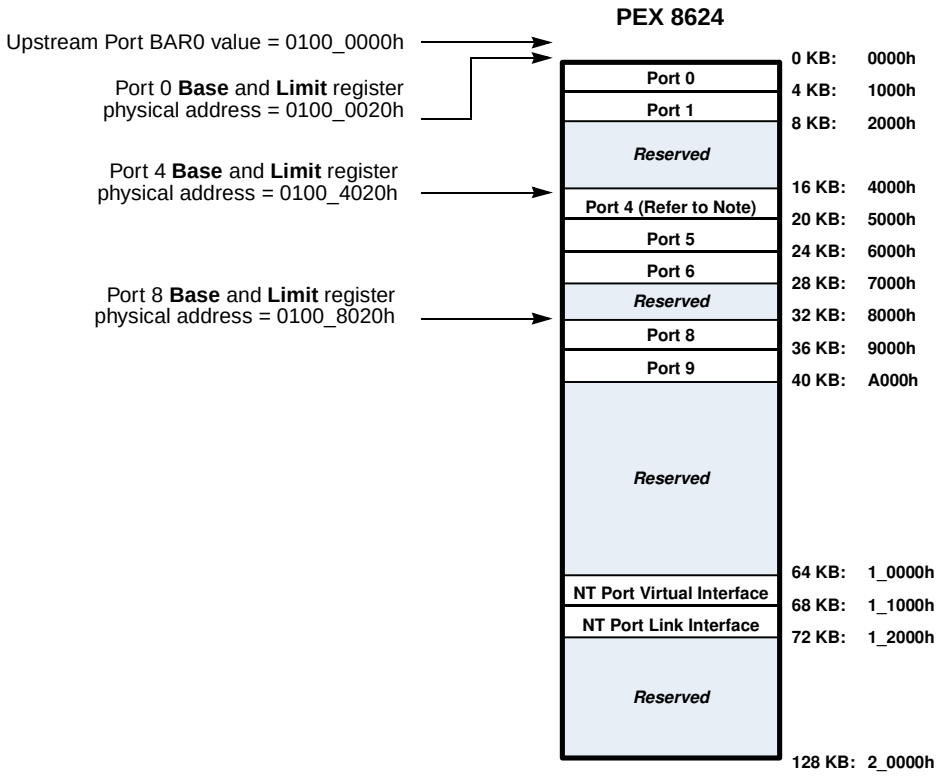
13.1.5 NT Port Memory-Mapped Base Address Registers

The NT Port Virtual and Link Interfaces individually claim 128 KB of memory, using **BAR0** and **BAR1**. The 128-KB space contains the CSRs for all PEX 8624 Ports. **BAR0** and **BAR1** can be programmed as one of the following:

- 32-bit BAR (**BAR1** is ***reserved***; default mode)
- 64-bit BAR, by programming the Configuration **BAR0/1 Setup** register (the NT Port Virtual Interface offset is D0h; the NT Port Link Interface offset is E4h)
- **BAR0** and **BAR1** can be completely disabled

Figure 13-2 provides a memory-mapped view of the PEX 8624 CSRs. This view is the same from the upstream Port, NT Port Virtual Interface, or NT Port Link Interface.

Figure 13-2. NT Mode Configuration Register Mapping to Memory-Mapped BAR



Note: *Port 4 does not connect to a downstream device; therefore, no Memory nor I/O resources should be defined in Port 4 registers.*

13.1.6 Doorbell Registers

Doorbell registers are used to signal interrupts from one side of the NT bridge to the other. This section describes a typical set of Doorbell Control registers.

A 16-bit software-controlled Interrupt Request register and associated 16-bit Mask register are implemented for the NT Port Virtual and Link Interfaces. The Doorbell mechanisms consist of the following registers:

- **Virtual Interface IRQ Set**
- **Virtual Interface IRQ Clear**
- **Virtual Interface IRQ Mask Set**
- **Virtual Interface IRQ Mask Clear**
- **Link Interface IRQ Set**
- **Link Interface IRQ Clear**
- **Link Interface IRQ Mask Set**
- **Link Interface IRQ Mask Clear**

The Virtual Interface IRQ is for interrupts that exit the NT Port Virtual Interface. An interrupt is asserted on the NT Port Virtual Interface when one or more of the **Virtual Interface IRQ Set** register bits are Set by the NT Port Link Interface and their corresponding **Virtual Interface IRQ Mask Set** register bits are Cleared. An interrupt is de-asserted on the NT Port Virtual Interface when one or more of the **Virtual Interface IRQ Clear** register bits are Set from the NT Port Virtual Interface and their corresponding **Virtual Interface IRQ Mask Clear** register bits are Cleared. The interrupt is de-asserted when all Set bits are masked or Cleared.

The Link Interface IRQ is for interrupts that exit the NT Port Link Interface. An interrupt is asserted on the NT Port Link Interface when one or more of the **Link Interface IRQ Set** register bits are Set by the NT Port Virtual Interface and their corresponding **Link Interface IRQ Mask Set** register bits are Cleared. An interrupt is de-asserted on the NT Port Link Interface when one or more of the **Link Interface IRQ Clear** register bits are Set from the NT Port Link Interface and their corresponding **Link Interface IRQ Mask Clear** register bits are Cleared. The interrupt is de-asserted when all Set bits are masked or Cleared.

Because Memory Requests can access both sets of NT-Virtual and NT-Link Doorbell registers, software in either domain can generate Doorbell interrupts to both domains.

Internally, the **Set IRQ** and **Clear IRQ** registers are the same register. One location is used to Set bits and the other is used to Clear bits. The status can be read from either register.

In a PCI Express switch, interrupt state transitions (from Setting to Clearing, or vice versa) result in packets being transmitted upstream on the appropriate side of the bridge, when INT*x* are enabled (**PCI Command** register *Interrupt Disable* bit, offset 04h[10], is Cleared). Standard PCI Express Capability structures allow these interrupts to be configured as MSIs or INT*x*. When MSIs are enabled (**MSI Control** register *MSI Enable* bit, offset 48h[16], is Set), packets are transmitted only when interrupts transition from Clear IRQ to Set IRQ.

NT Port Doorbell interrupts can optionally use the PEX_INTA# output for interrupt signaling, instead of the INT*x* or MSI signaling mechanisms. PEX_INTA# output can be enabled for NT Port Doorbell interrupts, by Setting the **ECC Error Check Disable** register *Enable PEX_INTA# Interrupt Output(s) for NT-Virtual Doorbell-Generated Interrupts* bit (NT Port Virtual Interface, or Port 0 if Port 0 is the NT Port, offset 1C8h[7]).

The PEX 8624 Virtual interrupts are de-asserted when the NT Port goes to the *DL_Down* state.

13.1.7 Scratchpad Registers

Scratchpad registers are readable and writable from both sides of the NT bridge, providing a generic means for inter-Host communication. A block of eight registers are provided, accessible in Memory space from the NT Port Virtual and Link Interfaces. These registers pass Control and Status information between Virtual and Link Interface devices or they can be generic RW registers. Reading from or writing to **Scratchpad** registers does not cause interrupts to assert – **Doorbell** registers are used for that purpose. **Scratchpad** registers are reset only by a Fundamental Reset (PEX_PERST#).

13.1.8 NT Base Address Registers

There are two sets of NT Base Address registers (BARs) – one each for the NT Port Virtual and Link Interfaces. Each BAR has its own **Setup** and **Address Translation** register:

- **BAR*x* Setup** registers enable/disable the BAR and define the window size and type. Program the **BAR*x* Setup** registers prior to allowing configuration software to assign a resource for these BARs. (Discussed further in Section 13.1.8.1.)
- **Memory BAR*x* Address Translation** registers allow for an address change on the upper bits (up to the size of the space). Program the **Memory BAR*x* Address Translation** registers, before generating traffic across the NT Port. This programming is typically performed by information downloaded from I^2C, software, or an optional serial EEPROM (if present) on the destination side. The source side does not need to know what the Address Translation is.
- The address could change size. *For example*, the PEX 8624 NT Port allows a 32-bit device to communicate to a 64-bit device, and vice versa. (The same is true when the addresses are the same size, as well – a 32-bit device can communicate with a 32-bit device, and a 64-bit can communicate with a 64-bit device.)

13.1.8.1 NT BAR*x* Setup Registers

PCI defines Base Address Registers (BARs) for a PCI device to claim Address space. For the PEX 8624, **BAR0** and **BAR1** provide Memory-Mapped access to the CSRs, while **BAR2**, **BAR3**, **BAR4**, and **BAR5** provide programmable window sizes to the other side of the NTB.

The **BAR*x* Setup** registers are used to program the window size of each BAR. Table 13-1 briefly describes each NT Port BAR. **BAR2**, **BAR3**, **BAR4**, and **BAR5** can be configured for accessing the Address space across the NT Port Virtual and Link Interfaces.

Each **BAR*x* Setup** register defines the memory window size that is to be assigned by a system enumerator (*that is*, BIOS or firmware). *For example*, if the window size must be 1 MB, Memory space, and cacheable region, the **BAR*x* Setup** register in 32-bit space will be FFF0_0008h (FFF0_0000h indicates the 1-MB space Request, bit 3 is the cacheable region, and bit 0 must be Memory space).

In most cases, the **BAR*x* Setup** registers are programmed using an optional serial EEPROM (if present), before the BIOS or firmware allocates the resources (because resource enumeration is done before the system software can access these devices).

Table 13-1. NT Port Virtual and Link Interface BARs

BAR	NT Port Virtual Interface Description	NT Port Link Interface Description
BAR0	All PEX 8624 Port Configuration registers are mapped into Memory space, using **BAR0** and **BAR1**. The Local Host, connected to the Transparent upstream Port, can use the Transparent upstream Port **BAR0**/**1** or NT Port Virtual Interface **BAR0/1** to access the PEX 8624 Port Configuration registers. The **NT Port Virtual Interface BAR0/1 Setup** register controls the **BAR0** and **BAR1** implementation, as follows: • Disables **BAR0** and **BAR1** • Enables **BAR0** and disables **BAR1** (**BAR0** is a 32-bit BAR) • Enables **BAR0** and **BAR1** (**BAR0/1** is a 64-bit BAR) **BAR0** and **BAR1** claim 128-KB Memory space to the system.	All PEX 8624 Port Configuration registers are mapped into Memory space, using **BAR0** and **BAR1**. The System Host, connected to the NT Port, can use **BAR0**/**1** to access the PEX 8624 Port Configuration registers. The **NT Port Link Interface BAR0/1 Setup** register controls the **BAR0** and **BAR1** implementation, as follows: • Disables **BAR0** and **BAR1** • Enables **BAR0** and disables **BAR1** (**BAR0** is a 32-bit BAR) • Enables **BAR0** and **BAR1** (**BAR0/1** is a 64-bit BAR) **BAR0** and **BAR1** claim 128-KB Memory space to the system.
BAR1	Configured by the **NT Port Virtual Interface BAR0/1 Setup** register. **BAR1** is implemented as an upper 32-bit address of the NT Port Virtual Interface memory-mapped 64-bit BAR; otherwise, it is ***reserved***.	Configured by the **NT Port Link Interface BAR0/1 Setup** register. **BAR1** is implemented as an upper 32-bit address of the NT Port Link Interface memory-mapped 64-bit BAR; otherwise, it is ***reserved***.
BAR2	Configured by the **NT Port Virtual Interface Memory BAR2 Setup** register. **BAR2** can be implemented as a 32-bit BAR or lower half of a 64-bit BAR, by combining it with **BAR3** (**BAR2**/**3**). **BAR2** uses Direct Address Translation.	Configured by the **NT Port Link Interface Memory BAR2 Setup** register. **BAR2** can be implemented as a 32-bit BAR or lower half of a 64-bit BAR, by combining it with **BAR3** (**BAR2**/**3**). **BAR2** uses Direct Address Translation.
BAR3	Configured by the **NT Port Virtual Interface Memory BAR2/3 Setup** register. **BAR3** can be implemented as a 32-bit BAR or upper half of a 64-bit BAR, by combining it with **BAR2** (**BAR2**/**3**). **BAR3** uses Direct Address Translation.	Configured by the **NT Port Link Interface Memory BAR2/3 Setup** register. **BAR3** can be implemented as a 32-bit BAR or upper half of a 64-bit BAR, by combining it with **BAR2** (**BAR2**/**3**). **BAR3** uses Direct Address Translation.
BAR4	Configured by the **NT Port Virtual Interface Memory BAR4 Setup** register. **BAR4** can be implemented as a 32-bit BAR or lower half of a 64-bit BAR, by combining it with **BAR5** (**BAR4**/**5**). **BAR4** uses Direct Address Translation.	Configured by the **NT Port Link Interface Memory BAR4 Setup** register. **BAR4** can be implemented as a 32-bit BAR or lower half of a 64-bit BAR, by combining it with **BAR5** (**BAR4**/**5**). **BAR4** uses Direct Address Translation.
BAR5	Configured by the **NT Port Virtual Interface Memory BAR4/5 Setup** register. **BAR5** can be implemented as a 32-bit BAR or upper half of a 64-bit BAR, by combining it with **BAR4** (**BAR4**/**5**). **BAR5** uses Direct Address Translation.	Configured by the **NT Port Link Interface Memory BAR4/5 Setup** register. **BAR5** can be implemented as a 32-bit BAR or upper half of a 64-bit BAR, by combining it with **BAR4** (**BAR4**/**5**). **BAR5** uses Direct Address Translation.

13.1.9 Address Translation

The Transparent bridge uses **Base** and **Limit** registers in I/O space, Non-Prefetchable Memory space, and Prefetchable Memory space to map transactions downstream, across the bridge. All downstream devices must be mapped in contiguous address regions, such that a single Address range in each space is sufficient. Upstream mapping is done by way of inverse decode, relative to the same registers. A Transparent bridge does not translate the addresses of forwarded transactions/packets.

In multi-domain systems, each Host domain has its own Address space, that is different from that of other Host domain(s). Hence, any transaction crossing the inter-domain boundary, by way of an NTB or other means, must support address, as well as Requester ID, translations.

Before a transaction (PCI Express packet) can go through the NT bridge (either from the Virtual-side to Link-side, or from Link-side to Virtual-side) in an inter-domain system, one or more sets of Memory resources must be assigned to the NT bridge. To request this resource from the system enumerator (BIOS or firmware), the NT bridge must be programmed with the **BAR*x* Setup** register(s). (Refer to Section 13.1.8.1.) The **BAR*x* Setup** register(s) requests the window space size, memory type, 32- or 64-bit space, prefetchable or non-prefetchable area, using one 32-bit register for 32-bit Address space or the two 32-bit registers (**BAR2/3** or **BAR4/5**) for 64-bit Address space. In return, the system enumerator assigns resources to the NT bridge in **BAR0** through **BAR5**. Any transactions that target **BAR2** through **BAR5** on the NT Port Link Interface result in a transaction across the NT bridge, to the secondary address domain.

Similarly, in NT PCI-to-PCI Bridge mode, the NT PCI-to-PCI bridge must be enumerated to accommodate the resources assigned to the NT endpoint, to allow packets to logically traverse the bridge. Its Device Number (on the Internal Virtual PCI Bus) value is the Port Number of the NT Port. Device enumeration minimally includes the **PCI Command**, **Bus Number**, and **Memory Base and Limit** and/or **Prefetchable Memory Base and Limit** registers (offsets 04h, 18h, and 20h, and/or 24h). The Internal NT Virtual Bus (connecting the NT PCI-to-PCI secondary interface and NT endpoint) can be assigned any available Bus Number within the upstream Port's range of Subordinate Bus Numbers.

In addition, the Lookup Table (LUT) register(s) and **Memory BAR*x* Address Translation** register(s) must be programmed. The LUTs are the Requester ID (Bus Number, Device Number, and Function Number) with the ability to disable features that allow Requester's transaction go through the NT bridge (if enabled). This adds security to the NT bridge, limiting the devices that can generate transactions across the NT bridge. LUTs also play a crucial role, because the Requester ID is also used to complete PCI Express Read Requests – during the PCI Express Read Request to the other domain side, the NT bridge uses its own Requester ID to translate the original PCI Read Request, and when the Completion returns, the NT bridge uses the original Requester ID to complete the transaction.

The Address Translation is used to re-direct the address of the PCI Express packet to a programmer-reserved area (instead of using the same address for both Host domains). Hence, any transaction targeting **BAR2** through **BAR5** can be translated (re-mapped) on the other side of the NT bridge while maintaining the offsets. These Translation registers can be changed during runtime, as long as there are no pending transactions.

The PEX 8624 NT Port Virtual and Link Interfaces support Direct Address Translation, described in the following section.

13.1.9.1 Direct Address Translation

The **BAR*x* Setup** registers define a mask that splits the address into an upper *Base* field and a lower *Offset* field. Translation then consists of replacing, under the maskable portion of the **BAR*x* Setup** register, the Address Base register bits with the corresponding Address Translation register bits. Accordingly, the Address Translation register value must be a multiple of the corresponding BAR size. Figure 13-3 illustrates Direct Address Translation.

The device(s) on the originating Host domain can communicate to a single device or multiple devices mapped to consecutive Memory Address space on the target Host domain, by using the Direct Address Translation mechanism. Figure 13-4 illustrates the entire Address map, claimed by the NT Port, mapped into the single target device. Figure 13-5 illustrates the entire Address map claimed by the NT Port, mapped into multiple target devices. Multiple devices must be in contiguous Memory ranges.

Figure 13-3. Direct Address Translation

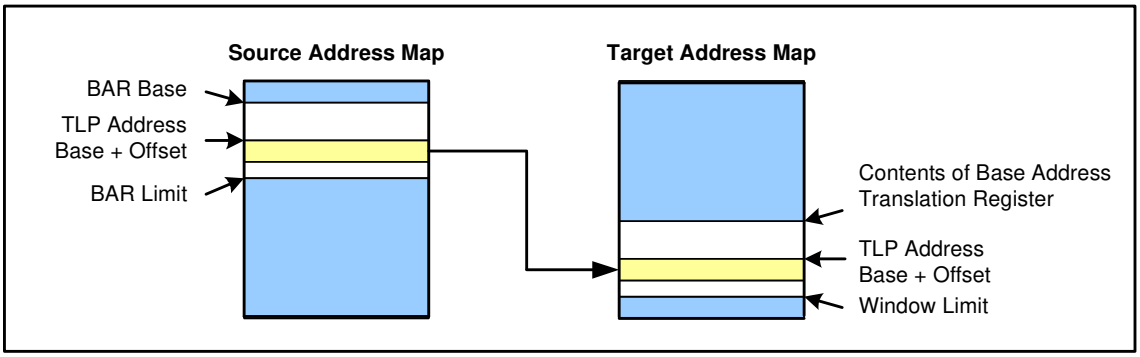


Figure 13-4. NT Port Mapped into Single Target Device

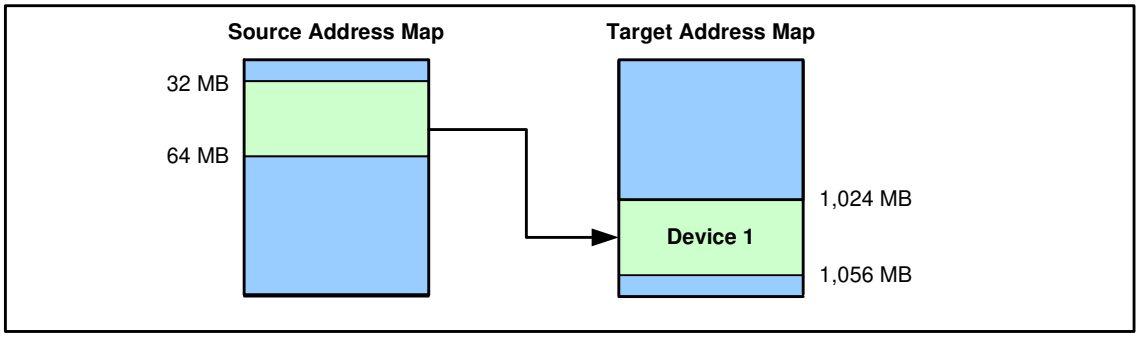
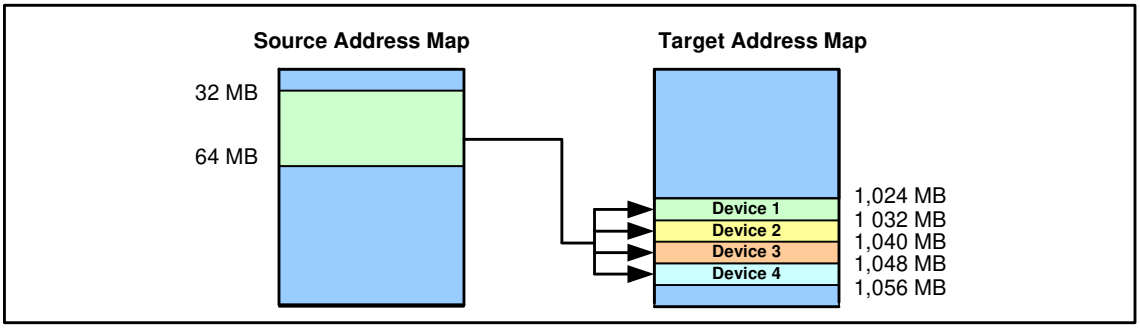


Figure 13-5. NT Port Mapped into Multiple Target Devices



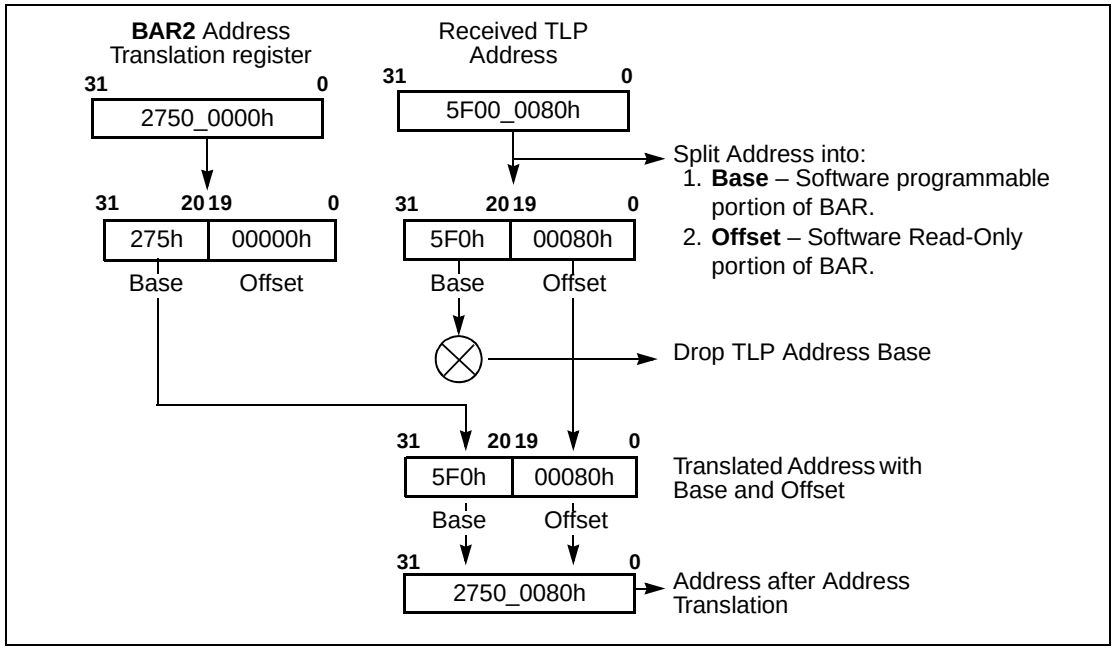
Address Translation Example

Assume the following:

1. NT Port Virtual Interface **BAR2** claims 128-KB Memory space (**BAR2 Setup** register = FFFE_0000h).
2. Configuration software assigns the 5F00_0000h address value to NT Port Virtual Interface **BAR2** and it is within the Transparent upstream Port Memory window.
3. Device driver software programs the **BAR2** Address Translation register to 2750_0000h.

The PEX 8624 receives a transaction to the NT Port Virtual Interface, with address 5F00_0080h. The received transaction address is hitting the NT Port Virtual Interface **BAR2**. The PEX 8624 claims the transaction and executes the address translation described in Figure 13-6.

Figure 13-6. Address Translation Example



13.2 Requester ID Translation

Configuration, Message, and Completion transactions are ID-routed instead of address-routed. Of these, the NT Port forwards only the Completion transaction between the two Host domains. PCI Express switches and bridges use the Requester ID (defined in the Completion TLP Header) to route these packets.

The Requester ID consists of the following:

- Requester's PCI Bus Number
- Device Number
- Function Number

The Completer ID consists of the following:

- Completer's PCI Bus Number
- Device Number
- Function Number

Note: *The PCI Bus Number is unique for each Host domain.*

Figure 13-7 illustrates the Memory Request TLP Header format. Figure 13-8 illustrates the Completion TLP Header format.

Figure 13-7. Memory Request TLP Header Format

	Byte 0								Byte 1								Byte 2								Byte 3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Bytes 0-3	R	Fmtx1		Type					R	TC			R				TD	EP	Attr		R				Length							
Bytes 4-7	Requester ID																Tag												Last DW BE			
Bytes 8-11	Address[63:32]																															
Bytes 12-15	Address[31:0]																															R

Figure 13-8. Completion TLP Header Format

	Byte 0								Byte 1								Byte 2								Byte 3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Bytes 0-3	R	Fmt		Type					R	TC			R				TD	EP	Attr		R				Length							
Bytes 4-7	Completer ID																Completer Status			BCM	Byte Count											
Bytes 8-11	Requester ID																Tag								R	Lower Address						

13.2.1 Transaction Sequence

To implement a transaction sequence:

1. Requester inserts ID information into the Memory Read TLP that it generates on the initiating Host domain.
2. Switches and bridges between the transaction initiator and PEX 8624 NT Port route this Memory Read TLP, based upon the address.
3. NT Port replaces the Memory Read TLP Requester ID with its ID, and conducts the address translation before it forwards this Requester ID-translated TLP to the target Host domain, because the NT Port is the transaction initiator in the target Host domain.
4. Switches and bridges between the PEX 8624 NT Port and target device route this Memory Read TLP, based upon the address.
5. When the target device generates the Completion TLP, it copies the Memory Read TLP Requester ID into the corresponding Completion TLP *Requester ID* field and inserts its ID into the TLP *Completer ID* field.
6. Switches and bridges between the target device and PEX 8624 NT Port route the Completion TLP, based upon Requester ID (in this case, NT Bridge ID) information.
7. NT Port restores the original Requester ID value from the Configuration register and implements another Requester ID and Completer ID translation for the Completion TLP, before it forwards the Completion TLP to the Requester Host domain.
8. Switches and bridges between the PEX 8624 NT Port and Requester route the Completion TLP, based upon the Requester ID.
9. Requester accepts and processes the Completion TLP.

13.2.2 Transaction Originating in Local Host Domain

The translation of outgoing requests from the NT Port Virtual Interface to the NT Port Link Interface uses an 8-entry Lookup Table (LUT), as discussed in Section 14.15.2, "NT Port Virtual Interface NT Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Addresses D94h – DB0h)." Each LUT entry supports all outgoing requests and any number of outstanding requests made by a single device or function. If a device uses Phantom Function Numbers to increase the maximum number of outstanding transactions, each phantom function consumes an LUT entry. Configure the LUT by a serial EEPROM, I^2C, or local firmware, so it is possible to transmit requests to the System Host domain, which provides a measure of security and protection.

When a Memory Request arrives at the NT Port Virtual Interface, the packet Requester ID is associated with this LUT. If it attains one of the enabled LUT entries, the corresponding entry address (TxIndex) is inserted into the *Function Number* field of the packet's Requester ID. Conversely, if it does not match one of the enabled LUT entries, an Unsupported Request (UR) Completion is returned.

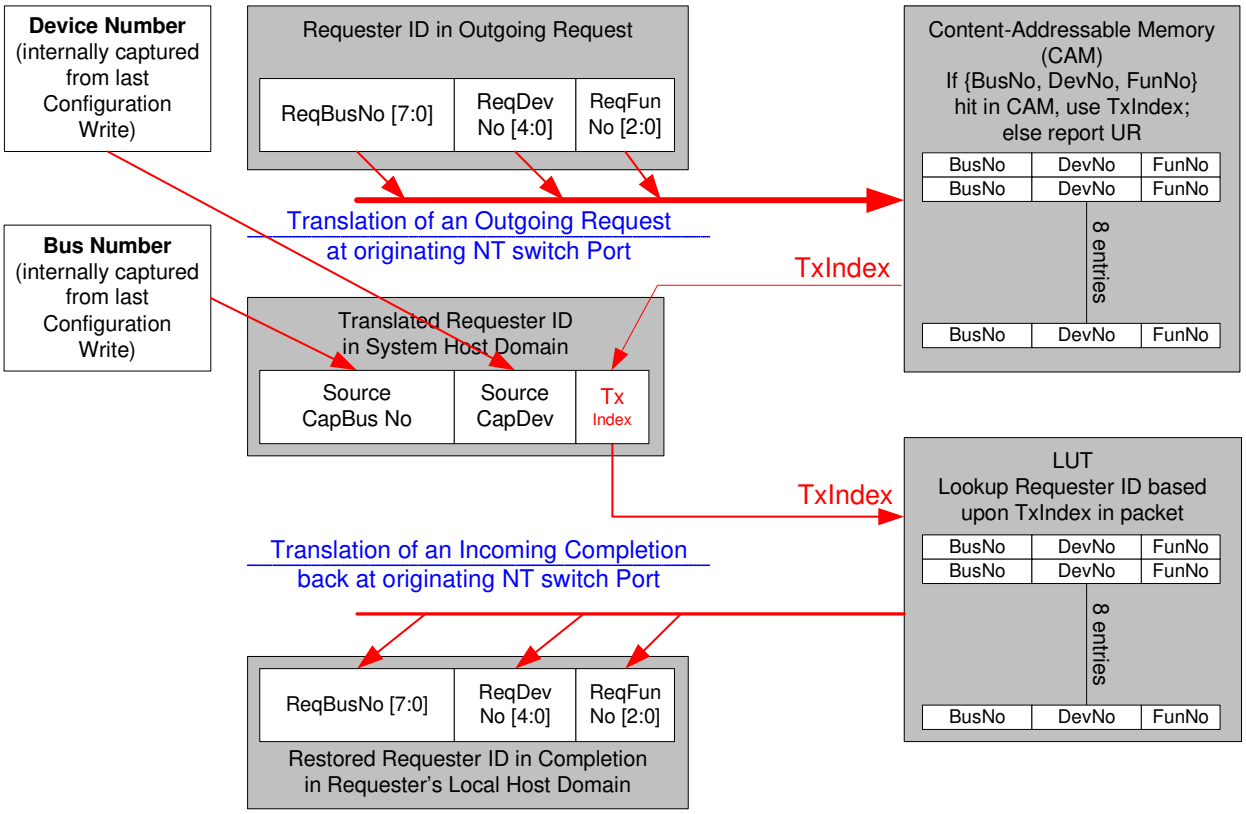
At the same time, the contents of the NT Port Link Interface **Bus Number** and **Device Number Capture** registers (the values used during the last CSR Write to the Port) are copied into the packet Requester ID's *Bus Number* and *Device Number* fields.

A Completion, with translated Requester ID, returned from the System Host domain to the PEX 8624, is recognized when its Requester ID Bus Number and Device Number match the NT Port Link Interface captured Bus Number and Device Number. (Refer to Figure 13-9.)

When the original Requester ID is restored, the following occurs:

1. TxIndex is retrieved from the *Function Number* field of the Completion TLP Requester ID.
2. TxIndex is used to look up the same 8-entry LUT, to restore the original Requester ID.
3. If the selected entry is valid, the restored Requester ID is placed into the Completion *TLP Requester* field; otherwise, an Unexpected Completion is reported.
4. Completion TLP *Completer ID* field is replaced by the NT Port Virtual Interface captured Bus Number, Device Number, and Function Number.
5. Translated Completion TLP is forwarded to the original Requester, in the Local Host domain.

Figure 13-9. Requester ID Translation for Request Originating in Local Host Domain



13.2.3 Transaction Originating in System Host Domain

Transactions originating in the System Host domain use a Receive LUT, with 32 entries, as discussed in Section 15.15.1, "NT Port Link Interface NT Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Addresses DB4h – DF0h)." This data structure supports up to 32 devices (elsewhere in the System Host domain) that are transmitting requests through the associated NT Port. Because the Function Number is not used in the LUT association, a separate LUT entry is not required for each requesting or phantom function device. Configure the LUT before transmitting requests through the NT Port. This Requester registration process, which cannot be accomplished by a peer, is an effective security and protection mechanism.

When a Request is received from the System Host domain and routed to the NT Port, its Requester ID is translated again – Bus Number and Device Number, but not Function Number. The received Memory Request TLP Requester ID is associated with this LUT, and the address (RxIndex) of the corresponding matching entry is substituted into the *Device Number* field of the Memory Request's TLP *Requester ID* field. (Refer to Figure 13-10.)

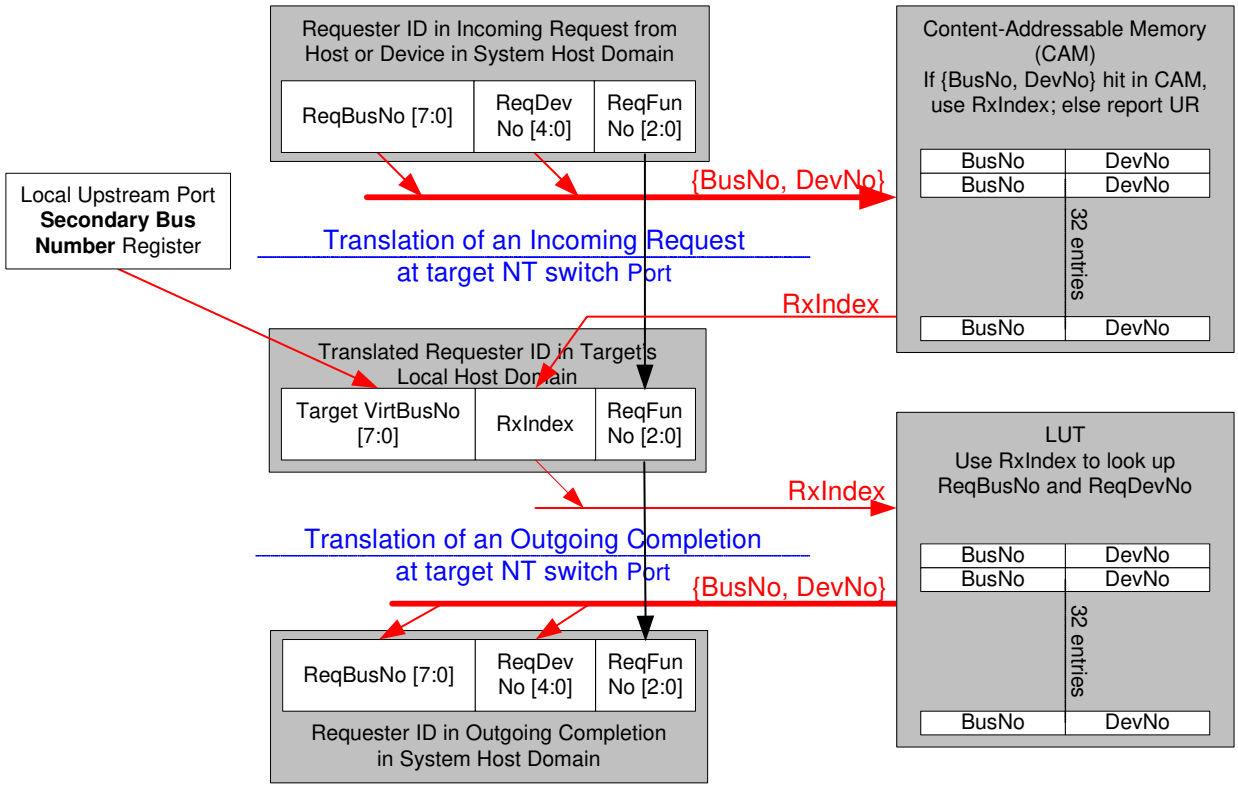
If no match is found, or the matched entry is not enabled, the Request receives a UR response. If a match is found, and matched entry is enabled, the PEX 8624 internal virtual PCI Bus Number is copied into the packet Requester ID's *Bus Number* field. The translated Memory Request TLP is address-translated and forwarded into the Local Host domain.

The PEX 8624 internal virtual PCI Bus Number is sufficient to route the Completion from the Completer back to the NT Port in the Completer's domain, because the NT Port is the only possible Requester on the switch internal virtual PCI Bus. Elsewhere in the PCI Express hierarchy, the Bus Number is sufficient to route the Completion back into the switch containing the NT Port.

The inverse translation occurs when a Completion passes through the NT bridge from the Local Host domain to the System Host domain. The RxIndex is retrieved from the *Device Number* field of the received Completion TLP *Requester ID* Header field, and used to look up the 32-entry LUT. The Completion TLP *Requester ID*, *Bus Number*, and *Device Number* fields are replaced by the decoded LUT-entry Bus Number and Device Number values, if the entry is valid; otherwise, an Unexpected Completion is reported.

The Completion TLP Completer ID is replaced by the NT Port Link Interface captured Bus Number, Device Number, and Function Number values before forwarding the Completion TLP to the System Host domain.

Figure 13-10. Requester ID Translation for Request Originating in System Host Domain



13.3 NT Port Power Management Handling

13.3.1 Active State Power Management

The NT Port Link Interface endpoint supports the Active State Power Management (ASPM) L0s and L1 Link PM states. The NT Port Virtual Interface endpoint implements the CSRs for ASPM support. However, it does not enter into the low-power states, because there is no physical Link associated with it.

13.3.2 PCI-PM and PME Turn Off Support

When NT mode is enabled, the NT Port Link Interface Type 0 endpoint behaves as any other endpoints in the PCI Express PCI-PM D3hot Device PM state. Once in the D3hot Device PM state, the NT Port Link Interface Type 0 endpoint requests PCI-PM L1 Link PM state entry, and finally settles in the L1 Link PM state. Only Configuration accesses and Messages to the NT Port Link Interface Type 0 endpoint are supported in the D3hot Device PM state. The Root Complex transmits PME_Turn_Off Messages when the NT Host decides to turn Off the main power and Reference Clock. The PEX 8624 NT Port Link Interface Type 0 endpoint indicates its readiness to lose power, by transmitting a PME_TO_Ack Message toward the upstream device. The PME_TO_Ack Message is transmitted when there are no pending TLPs to transmit upstream, toward the NT Port Link Interface. The Port requests the L2/L3 Ready Link PM state, by transmitting PM_Enter_L23 Data Link Layer Packets (DLLPs) to the upstream device after transmitting a PME_TO_Ack TLP. The Port settles into the L3 Link PM state when the Power Controller removes the main power and Reference Clock.

When the PME_Turn_Off Message is received on the PEX 8624 Transparent upstream Port, the Port broadcasts this Message to all PEX 8624 downstream devices, including the NT Port Virtual Interface Type 0 endpoint. After the PME_TO_Ack Message is received from all downstream devices and the PEX 8624 NT Port Virtual Interface Type 0 endpoint, the PEX 8624 Transparent upstream Port transmits an aggregated PME_TO_Ack Message to the upstream component after it finishes transmitting all pending TLPs to the upstream component. When NT mode is enabled, the PEX 8624 Transparent downstream Ports allow the attached devices to enter the PCI-PM-compatible L1 Link PM state. The PEX 8624 NT Port Virtual Interface Type 0 endpoint never enters the PCI-PM L1 Link PM state.

13.3.3 Message Generation

The PEX 8624 NT Port Link Interface Type 0 endpoint never generates PM_PME Messages. The PEX 8624 NT Port Virtual Interface Type 0 endpoint never receives Set_Slot_Power_Limit Messages nor generates PM_PME Messages.

13.4 Expansion ROM

The NT Port Link Interface supports Expansion ROM, by default. Expansion ROM support can be moved from the NT Port Link Interface to the NT Port Virtual Interface, by Setting the **Ingress Control** register *Expansion ROM Virtual Side* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 660h[23]).

The NT Port supports 16- or 32-KB-sized Expansion ROM, based upon the **Serial EEPROM Clock Frequency** register *Expansion ROM Size* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 268h[16]) value.

Note: *Expansion ROM can be enabled in either the NT Port Virtual Interface or NT Port Link Interface, but not both simultaneously. Expansion ROM is enabled, by default, in the NT Port Link Interface (**Ingress Control** register Expansion ROM Virtual Side bit is Cleared).*

13.5 NT Port Interrupts

The NT Port Virtual and Link Interfaces can both generate interrupts in response to specific events. The NT Port must not receive any INT*x* Message Requests. If the NT Port receives an INT*x* Message Request, the Request is handled as a Malformed TLP error.

13.5.1 NT Port Virtual Interface Interrupts

The NT Port Virtual Interface generates interrupts to the Local Host for the following reasons (all are masked, by default, and must not be masked, to be enabled):

- Doorbell interrupts
- NT Port Link Interface detected an Correctable TLP error
- NT Port Link Interface detected an Uncorrectable TLP error (option to signal Fatal and/or Non-Fatal)
- NT Port Link Interface *DL_Active* state change
- NT Port Link Interface received an Uncorrectable Error Message

NT-Virtual Doorbell interrupts and NT-Link errors and events can use the INT*x*, MSI, or PEX_INTA# signaling mechanisms (all mutually exclusive), as follows:

- PEX_INTA# output can be enabled for NT Port Virtual Interface Doorbell interrupts, by Setting the **ECC Error Check Disable** register *Enable PEX_INTA# Interrupt Output(s) for NT-Virtual Doorbell-Generated Interrupts* bit (NT Port Virtual Interface, or Port 0 if Port 0 is the NT Port, offset 1C8h[7])
- PEX_INTA# output can be enabled for NT-Link Error and Event interrupts, by Setting the register's *Enable PEX_INTA# Interrupt Output(s) for Device-Specific Error- and Event-Triggered Interrupts* bit (All Ports, offset 1C8h[5])

Refer to Section 13.1.6 for Doorbell interrupt details.

The NT Port Virtual Interface de-asserts INT*x* or PEX_INTA# interrupts in response to one or more of the following conditions:

- NT Port Virtual Interface **PCI Command** register *Interrupt Disable* bit (offset 04h[10]) is Set
- Corresponding *Interrupt Mask* bit is Set
- NT Port Link goes down (DL_Down condition) or the NT Port Link Interface receives a Hot Reset
- Software Clears the *Interrupt Status* bit, or Sets the *Doorbell Interrupt Request Clear* bit

When the NT Port Link Interface detects Correctable TLP errors, the NT Port Virtual Interface signals the interrupt to the Local Host, if the interrupt signaling is enabled and not masked (**Link Error Status Virtual** register *Link Side Correctable Error Status* bit is Set, and **Link Error Mask Virtual** register *Link Side Correctable Error Mask* bit is Cleared (NT Port Virtual Interface as Port 0, offsets FE0h[0] and FE4h[0]), respectively).

When the NT Port Link Interface detects Uncorrectable TLP errors, the NT Port Virtual Interface signals the interrupt to the Local Host, if the interrupt signaling is enabled and not masked (**Link Error Status Virtual** register *Link Side Uncorrectable Error Status* bit is Set, and **Link Error Mask Virtual** register *Link Side Uncorrectable Error Mask* bit is Cleared (NT Port Virtual Interface as Port 0, offsets FE0h[1] and FE4h[1]), respectively).

An NT Port Link Interface *DL_Active* state change occurs upon detection of an NT Port Link Interface *DL_Down* state rise edge and fall edge. This signals the interrupt to the Local Host, if the interrupt signaling enabled and not masked (**Link Error Status Virtual** register *Link Side DL Active Change Status* bit is Set, and **Link Error Mask Virtual** register *Link Side DL Active Change Mask* bit is Cleared (NT Port Virtual Interface as Port 0, offsets FE0h[2] and FE4h[2]), respectively).

When the NT Port Link Interface receives an Uncorrectable Error Message, the NT Port Virtual Interface signals the interrupt to the Local Host, if the interrupt signaling is enabled and not masked (**Link Error Status Virtual** register *Link Side Uncorrectable Error Message Drop Status* bit is Set, and **Link Error Mask Virtual** register *Link Side Uncorrectable Error Message Drop Mask* bit is Cleared (NT Port Virtual Interface as Port 0, offsets FE0h[3] and FE4h[3]), respectively).

13.5.2 NT Port Link Interface Interrupts

The NT Port Link Interface generates interrupts to the System Host for NT-Link Doorbell interrupts detected at the NT Port Link Interface ingress Port (interrupts are masked, by default). The NT Port Link Interface should not detect any Device-Specific errors.

NT-Link Doorbell interrupts can use the INT*x*, MSI, or PEX_INTA# signaling mechanisms (all mutually exclusive). PEX_INTA# output can be enabled for NT Port Link Interface Doorbell interrupts, by Setting the **ECC Error Check Disable** register *Enable PEX_INTA# Interrupt Output(s) for NT-Link Doorbell-Generated Interrupts* bit (NT Port Link Interface, offset 1C8h[7]). Refer to Section 13.1.6 for Doorbell interrupt details.

The NT Port Link Interface de-asserts INT*x* or PEX_INTA# interrupts in response to one or more of the following conditions:

- NT Port Link Interface **PCI Command** register *Interrupt Disable* bit (offset 04h[10]) is Set
- Corresponding *Interrupt Mask* bit is Set
- NT Port Link goes down (DL_Down condition) or the NT Port Link Interface receives a Hot Reset
- Software Clears the *Interrupt Status* bit, or Sets the *Doorbell Interrupt Request Clear* bit

13.6 NT Port Error Handling

The PEX 8624 NT Port Virtual Interface endpoint logs TLP errors, for TLPs that travel from the NT Port Virtual Interface to the NT Port Link Interface. The PEX 8624 signals Error Messages to the Local Host (Host closest to the upstream Port). The PEX 8624 provides an option to communicate this error condition to the System Host (Host closest to the NT Port), by signaling an interrupt.

The PEX 8624 NT Port Link Interface endpoint logs TLP errors, for TLPs that travel from the NT Port Link Interface to the NT Port Virtual Interface. The PEX 8624 signals Error Messages to the System Host (Host closest to the NT Port).

When the PEX 8624 receives a TLP, it performs the following:

1. TLP integrity check,
2. Address decode,
3. Address translation,
4. Requester ID translation, and
5. ECRC re-generation,

before transmitting the TLP through the NT Port. If the PEX 8624 detects an ECRC error, it corrupts the re-generated ECRC before transmitting the TLP through the NT Port. The PEX 8624 also provides options for dropping error-detected ECRC or endpoint (EP) TLPs (**Ingress Control Shadow** register *Drop ECRC TLPs* and *Drop EP TLPs* bits (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 664h[8 and 4], respectively)).

The PEX 8624 does not generate the ECRC for a TLP that passes through the NT Port, if the received TLP does not have its *TD* bit Set.

The PEX 8624 drops all TLPs traveling from the NT Port Virtual Interface to the NT Port Link Interface, if the internal RAM Fatal ECC error is detected, until the PEX 8624 receives a Hot Reset from a Local Host.

13.7 Cursor Mechanism

A software application can use the Device-Specific Cursor Mechanism to access the PEX 8624 NT Port Configuration Space registers. The registers that support the Device-Specific Cursor Mechanism are the **Configuration Address Window** and **Configuration Data Window** registers (offsets F8h and FCh, respectively). A software application can also:

- Select the Configuration Register offset, by using the **Configuration Address Window** register
- Perform Read accesses to the **Configuration Data Window** register, to read to the selected Configuration register
- Perform Write accesses to the **Configuration Data Window** register, to write to the selected Configuration register

Configuration transactions have access to this Device-Specific Cursor Mechanism, if NT mode is enabled.

For details regarding the **Configuration Address Window** and **Configuration Data Window** registers, refer to:

- Section 14.10, "NT Port Virtual Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)"
- Section 15.10, "NT Port Link Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)"

13.8 Port Programmability

The PEX 8624 supports the capability of programming the upstream Port and NT Port Number. The Configuration register for the upstream Port and NT Port is in the **Debug Control** register *Upstream Port ID* and *NT Port Number* fields (NT Port Virtual Interface as Port 0, offset 1DCh[11:8 and 25:24], respectively). This register is updated, based upon the external STRAP_NT_ENABLE# and STRAP_NT_UPSTRM_PORTSEL[1:0] Strapping inputs, by default. A serial EEPROM, I^2C, and/or software can be used to override the external strap values.

A software application can change the upstream Port and NT Port location to another Port Number during runtime, or as part of a failover sequence. It is recommended that the PEX 8624 be in an Idle state (no traffic) when changing the upstream Port and NT Port Numbers during runtime. During a failover sequence, application software must be able to handle all spurious TLPs that it receives as a result of the failover process.

Chapter 14 NT Port Virtual Interface Registers – NT Mode Only

14.1 Introduction

Note: *Check the latest design guides, application notes and errata list for Non-Transparent (NT) usage.*

The NT Port includes two sets of Configuration, Capability, Control, and Status registers, to support the Virtual and Link Interfaces. This chapter defines the PEX 8624 NT Port Virtual Interface registers. Other registers are defined in:

- Chapter 12, "Transparent Port Registers"
- Chapter 15, "NT Port Link Interface Registers – NT Mode Only"

Note: *For Chip- and Station-specific registers (those that exist only in Port 0), if Port 0 is the NT Port, then those registers exist only in the NT Port Virtual Interface.*

All PEX 8624 registers can be accessed by Configuration or Memory Requests.

For further details regarding register names and descriptions, refer to the following specifications:

- *PCI r3.0*
- *PCI Power Mgmt. r1.2*
- *PCI Express Base r2.0*

14.2 NT Port Virtual Interface Type 0 Register Map

Table 14-1 defines the NT Port Virtual Interface Type 0 register mapping.

Table 14-1. NT Port Virtual Interface Type 0 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
NT Port Virtual Interface PCI-Compatible Type 0 Configuration Header Registers (Offsets 00h – 3Ch)			00h …
		Capability Pointer (40h)	34h …
			3Ch
	Next Capability Pointer (48h)	Capability ID (01h)	40h
NT Port Virtual Interface PCI Power Management Capability Registers (Offsets 40h – 44h)			44h
	Next Capability Pointer (68h)	Capability ID (05h)	48h
NT Port Virtual Interface MSI Capability Registers (Offsets 48h – 64h)			… 64h
	Next Capability Pointer (A4h)	Capability ID (10h)	68h
NT Port Virtual Interface PCI Express Capability Registers (Offsets 68h – A0h)			… A0h
	Next Capability Pointer (C8h)	SSID/SSVID Capability ID (0Dh)	A4h
NT Port Virtual Interface Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – C4h)			… C4h
	Next Capability Pointer 3 (00h)	Capability ID 3 (09h)	C8h
NT Port Virtual Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)			… FCh
Next Capability Offset (FB4h)	1h	PCI Express Extended Capability ID (0003h)	100h
NT Port Virtual Interface Device Serial Number Extended Capability Registers (Offsets 100h – 134h)			… 134h
Reserved			138h – 144h
Next Capability Offset (448h or 950h)	1h	PCI Express Extended Capability ID (0002h)	148h
NT Port Virtual Interface Virtual Channel Extended Capability Registers (Offsets 148h – 1A4h)			… 1A4h
NT Port Virtual Interface Port Arbitration Table Registers (Offsets 1A8h – 1BCh)			1A8h … 1BCh

Table 14-1. NT Port Virtual Interface Type 0 Register Map *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)		1C0h …
Next Capability Offset (950h)	1h / PCI Express Extended Capability ID (000Bh)	448h
NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)		…
Next Capability Offset 2 (C34h)	1h / PCI Express Extended Capability ID 2 (000Bh)	950h
NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)		…
Next Capability Offset 4 (000h)	1h / PCI Express Extended Capability ID 4 (000Bh)	C34h
NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)		… C88h
NT Port Virtual Interface NT Bridging-Specific Registers (Offsets C8Ch – F30h)		C8Ch … EFCh
Reserved		F00h – F30h
NT Port Virtual Interface Device-Specific Registers (Offsets F34h – F8Ch)		F34h … F8Ch
Reserved		F90h – FB0h
Next Capability Offset (148h)	1h / PCI Express Extended Capability ID (0001h)	FB4h
NT Port Virtual Interface Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)		… FDCh
NT Port Virtual Interface Device-Specific Registers – Link Error (Offsets FE0h – FFCh)		FE0h … FFCh

14.3 Register Access

The PEX 8624 NT Port Virtual Interface implements a 4-KB Configuration Space. The lower 256 bytes (offsets 00h through FFh) comprise the PCI-compatible Configuration Space, and the upper 960 Dwords (offsets 100h through FFFh) comprise the PCI Express Extended Configuration Space. The PEX 8624 supports three mechanisms for accessing the NT Port Virtual Interface registers:

- PCI Express Base r2.0 Configuration Mechanism
- Device-Specific Memory-Mapped Configuration Mechanism
- Device-Specific Cursor Mechanism

14.3.1 *PCI Express Base r2.0* Configuration Mechanism

The *PCI Express Base r2.0* Configuration mechanism is divided into two mechanisms:

- **PCI r3.0-Compatible Configuration Mechanism** – Provides Conventional PCI access to the first 256 bytes (the bytes at offsets 00h through FFh) of the NT Port Virtual Interface Configuration Register space
- **PCI Express Enhanced Configuration Access Mechanism** – Provides access to the entire 4-KB Configuration Space

Both are described in the sections that follow.

14.3.1.1 *PCI r3.0*-Compatible Configuration Mechanism

The *PCI r3.0*-Compatible Configuration mechanism provides standard access to the PEX 8624 NT Port Virtual Interface's first 256 bytes (the bytes at offsets 00h through FFh) of the PCI Express Configuration Space. (Refer to Figure 14-1.)

The mechanism uses PCI Type 0 and Type 1 Configuration transactions to access the PEX 8624 Configuration registers. All Ports capture the Bus Number and Device Number assigned by the upstream device on the PCI Express Link attached to the PEX 8624 upstream Port, as required by the *PCI Express Base r2.0*.

The PEX 8624 decodes all Type 1 Configuration accesses received on its upstream Port, when any of the following conditions exist:

- If the Bus Number specified in the Configuration access is the number of the PEX 8624 internal virtual PCI Bus, the PEX 8624 automatically converts the Type 1 Configuration access into the appropriate Type 0 Configuration access for the specified device.
  - If the specified device corresponds to the NT Port Virtual Interface (or to the PCI-to-PCI bridge in one of the PEX 8624 Transparent downstream Ports), the PEX 8624 processes the Read or Write Request
  - If the specified Device Number does not correspond to any of the PEX 8624 downstream Port Device Numbers nor NT Port Number, the PEX 8624 responds with an Unsupported Request (UR)

This mechanism uses the same Request format as the PCI Express Enhanced Configuration Access Mechanism. For PCI-compatible Configuration Requests, the *Extended Register Address* field must be all zeros (0).

Because the mechanism is limited to the first 256 bytes of the NT Port Virtual Interface Configuration register space, one of the following must be used to access beyond Byte FFh:

- PCI Express Enhanced Configuration Access Mechanism
- Device-Specific Memory-Mapped Configuration Mechanism
- Device-Specific Cursor Mechanism

14.3.1.2 PCI Express Enhanced Configuration Access Mechanism

The PCI Express Enhanced Configuration Access mechanism uses a flat, Root Complex Memory-Mapped Address space to access the device Configuration registers. In this case, the Memory address determines the Configuration register accessed, and the Memory data returns the addressed register's contents. The Root Complex converts the Memory transaction into a Configuration transaction.

This mechanism is used to access all PEX 8624 Configuration registers.

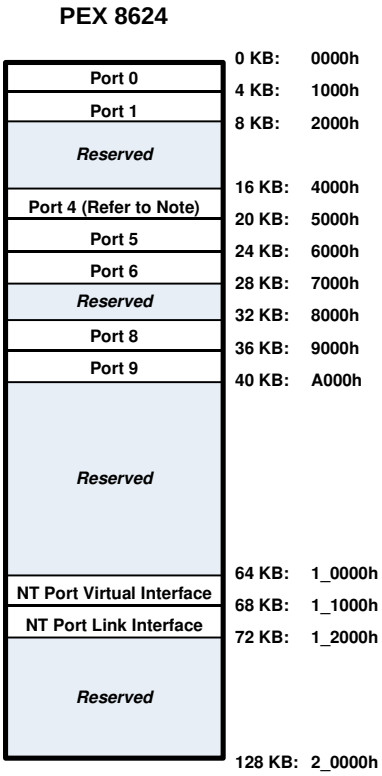
14.3.2 Device-Specific Memory-Mapped Configuration Mechanism

The Device-Specific Memory-Mapped Configuration mechanism provides a method to access the registers for all Ports within a single 128-KB Memory map, as illustrated in Figure 14-1. This Memory map is identical for Upstream Port **BAR0/1**, NT Port Virtual Interface **BAR0/1**, and NT Port Link Interface **BAR0/1**. The registers of each Port are located within a 4-KB range.

When the NT Port is enabled at Fundamental Reset, the NT Port Virtual and Link Interface registers use the *PCI r3.0* Type 0 Configuration Space Header.

To use this mechanism, use the PCI r3.0-Compatible Configuration Mechanism to program the PEX 8624 NT Port Virtual Interface **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively). After the PEX 8624 NT Port Virtual Interface Memory-Mapped register Base address is Set, the PEX 8624 Configuration Space registers are accessed, using Memory Reads and Writes to the 4-KB range, starting at offset 64 KB (1_0000h, Virtual Interface) and offset 68 KB (1_1000h, Link Interface).

Figure 14-1. NT Mode Configuration Register Mapping to Memory-Mapped BAR



Note: *Port 4 does not connect to a downstream device; therefore, no Memory nor I/O resources should be defined in Port 4 registers.*

14.3.3 Device-Specific Cursor Mechanism

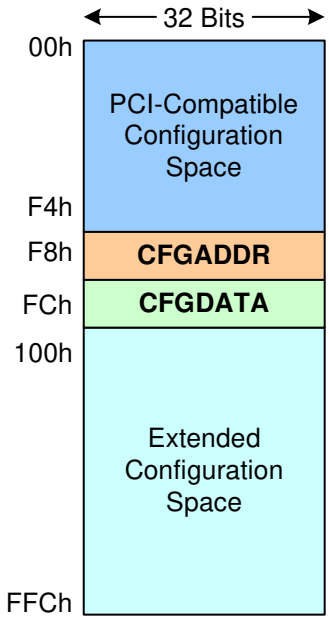
The Device-Specific Cursor mechanism is provided for use in development systems that can only generate *PCI r3.0* Configuration cycles (*that is*, the system cannot use either the Device-Specific Memory-Mapped Configuration Mechanism, nor generate Extended Configuration Requests to access the Extended Configuration Space).

In Figure 14-2, the software uses the **Configuration Address Window** (CFGADDR) register (offset F8h) to point to the NT Port Virtual or Link Interface Configuration Space registers, including the PCI Express Extended Configuration Space registers (offsets 100h through FFFh).

Software uses the **Configuration Data Window** (CFGDATA) register (offset FCh) to write to or read from the selected Configuration Space registers.

Refer to Section 14.10, "NT Port Virtual Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)," for the register descriptions.

Figure 14-2. Configuration Space View



14.4 Register Descriptions

The remainder of this chapter details the PEX 8624 NT Port Virtual Interface registers, including:

- Bit/field names
- Description of register functions in the PEX 8624 NT Port Virtual and Link Interfaces
- Type (*such as* RW or HwInit; refer to Table 12-5, "Register Types, Grouped by User Accessibility," for Type descriptions)
- Whether the power-on/reset value can be modified, by way of the PEX 8624 serial EEPROM and/or I^2C Initialization feature
- Default power-on/reset value

14.5 NT Port Virtual Interface PCI-Compatible Type 0 Configuration Header Registers (Offsets 00h – 3Ch)

This section details the NT Port Virtual Interface PCI-Compatible Type 0 Configuration Header registers. Table 14-2 defines the register map.

Table 14-2. NT Port Virtual Interface PCI-Compatible Type 0 Configuration Header Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device ID		Vendor ID		00h
PCI Status		PCI Command		04h
PCI Class Code			PCI Revision ID	08h
PCI BIST ***(Not Supported)***	PCI Header Type	Master Latency Timer ***(Not Supported)***	Cache Line Size	0Ch
Base Address 0				10h
Base Address 1				14h
Base Address 2				18h
Base Address 3				1Ch
Base Address 4				20h
Base Address 5				24h
Reserved				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			Capability Pointer (40h)	34h
Reserved				38h
Max_Lat ***(Reserved)***	Min_Gnt ***(Reserved)***	PCI Interrupt Pin	PCI Interrupt Line	3Ch

Register 14-1. 00h PCI Configuration ID

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**Vendor ID** Identifies the device manufacturer. Defaults to the PCI-SIG-issued Vendor ID of PLX (10B5h), if not overwritten by serial EEPROM and/or I^2C.	RO	Yes	10B5h
31:16	**Device ID** Identifies the particular device. Defaults to the PLX part number for the PEX 8624, if not overwritten by serial EEPROM and/or I^2C.	RO	Yes	8624h

Register 14-2. 04h PCI Command/Status

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	PCI Command			
0	**I/O Access Enable** The PEX 8624 does not claim I/O resources, nor does it forward I/O transactions through the NT Port. The value of this register is "Don't Care."	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8624 ignores Memory Space Requests on the NT Port Virtual Interface 1 = PEX 8624 accepts Memory Space Requests received on the NT Port Virtual Interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8624 forwarding of Memory Requests upstream. Does not affect Message forwarding nor Completions. 0 = PEX 8624 handles Memory Requests received on the NT Port Link Interface as Unsupported Requests (URs); for Non-Posted Requests, the PEX 8624 returns a Completion with UR Completion status 1 = PEX 8624 forwards Memory Requests upstream	RW	Yes	0
3	**Special Cycle Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
4	**Memory Write and Invalidate Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
5	**VGA Palette Snoop** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
6	**Parity Error Response Enable** Controls bit 24 (*Master Data Parity Error Detected*).	RW	Yes	0
7	**IDSEL Stepping/Wait Cycle Control** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
8	**SERR# Enable** Controls bit 30 (*Signaled System Error*). 1 = Enables reporting of Fatal and Non-Fatal errors detected by the NT Port Virtual Interface to the Root Complex	RW	Yes	0
9	**Fast Back-to-Back Transactions Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
10	**Interrupt Disable** 0 = NT Port Virtual Interface is enabled to generate INT*x* Interrupt Messages 1 = NT Port Virtual Interface is prevented from generating INT*x* Interrupt Messages	RW	Yes	0
15:11	***Reserved***	RsvdP	No	00h

Register 14-2. 04h PCI Command/Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
PCI Status				
18:16	***Reserved***	RsvdP	No	000b
19	**Interrupt Status** 0 = No INT*x* interrupt is pending 1 = INT*x* interrupt is pending internally to the NT Port Virtual Interface –or– PEX_INTA# (if enabled) is asserted	RO	No	0
20	**Capability List** Capability function is supported. Set as required by the *PCI Express Base r2.0*.	RO	Yes	1
21	**66 MHz Capable** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
22	***Reserved***	RsvdP	No	0
23	**Fast Back-to-Back Transactions Capable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0

Register 14-2. 04h PCI Command/Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
24	**Master Data Parity Error Detected** If bit 6 (*Parity Error Response Enable*) is Set, the NT Port Virtual Interface Sets this bit when the NT Port: • Forwards the poisoned Transaction Layer Packet (TLP) Write Request from the NT Port Link Interface to the NT Port Virtual Interface, –or– • Receives a Completion marked as poisoned on the NT Port Virtual Interface If the *Parity Error Response Enable* bit is Cleared, the PEX 8624 never Sets this bit. This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	**DEVSEL# Timing** ***Not supported*** Always Cleared.	RsvdP	No	00b
27	**Signaled Target Abort** The NT Port Virtual Interface Sets this bit if any of the following conditions exist: • NT Port Virtual Interface receives a Completion (from a Transparent Port) that has a Completion status of Completer Abort (CA), –or– • NT Port Virtual Interface receives a Memory Request targeting a PEX 8624 register, and the Payload Length (indicated within the Memory Request Header) is greater than 1 DWord • NT Port Virtual Interface receives a Memory Request targeting a PEX 8624 register address within a non-existent Port • NT Port Virtual Interface receives a Memory Write Request targeting enabled Expansion ROM Address space (Expansion ROM Base Address Register (BAR), offset 30h) ***Note:*** *When Set during a forwarded Completion, the* ***Uncorrectable Error Status*** *register Completer Abort Status bit (offset FB8h[15]) is not Set.*	RW1C	Yes	0
28	**Received Target Abort** Defaults to 0, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
29	**Received Master Abort** Defaults to 0, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
30	**Signaled System Error** If bit 8 (*SERR# Enable*) is Set, the NT Port Virtual Interface Sets this bit when transmitting an ERR_FATAL or ERR_NONFATAL Message to the upstream Port.	RW1C	Yes	0
31	**Detected Parity Error** The NT Port Virtual Interface Sets this bit when receiving a Poisoned TLP, regardless of the bit 6 (*Parity Error Response Enable*) state. This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0

Register 14-3. 08h PCI Class Code and Revision ID

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
PCI Revision ID				
7:0	**Revision ID** Unless overwritten by the serial EEPROM, returns the Silicon Revision (AAh, ABh, or BBh), the PLX-assigned Revision ID for this version of the PEX 8624. The PEX 8624 Serial EEPROM register Initialization capability is used to replace the PLX Revision ID with another Revision ID.	RO	Yes	AAh, ABh, or BBh
PCI Class Code				**068000h**
15:8	**Register-Level Programming Interface**	RO	Yes	00h
23:16	**Sub-Class Code** Other bridge devices.	RO	Yes	80h
31:24	**Base Class Code** Bridge devices.	RO	Yes	06h

Register 14-4. 0Ch Miscellaneous Control

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Cache Line Size				
7:0	**Cache Line Size** System Cache Line Size. Implemented as a RW field for Conventional PCI compatibility purposes and does not impact PEX 8624 functionality.	RW	Yes	00h
Master Latency Timer				
15:8	**Master Latency Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	00h
PCI Header Type				
22:16	**Configuration Layout Type** Type 0 Configuration Header for the NT Port.	RO	No	00h
23	**Multi-Function Device** 0 = Single-function device 1 = Indicates multiple (up to eight) functions (logical devices), each containing its own, individually addressable Configuration Space, 256 DWords in size	RO	No	0
PCI BIST				
31:24	**PCI BIST** ***Not supported*** Built-In Self-Test (BIST) Pass or Fail.	RsvdP	No	00h

Register 14-5. 10h Base Address 0 (NT Port Virtual Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Notes: *By default, NT Port Virtual Interface* ***BAR0*** *is enabled and* ***BAR1*** *is disabled, to provide a 32-bit* ***BAR0*** *for register access.* ***BAR1*** *can be enabled (by serial EEPROM or I²C), to provide a 64-bit* ***BAR0/1****, by programming the* ***NT Port Virtual Interface BAR0/1 Setup*** *register BAR0/1 Enable field (NT Port Virtual Interface, offset D0h[1:0]) to 11b (which enables both* ***BAR0*** *and* ***BAR1****).* *When software writes to the NT Port Virtual Interface* ***BAR0****, the value is automatically copied to the* ***NT Port Virtual Interface BAR0 (Shadow Copy)*** *register (NT Port Virtual Interface, offset D68h).*				
0	**Memory Space Indicator** When enabled, the Base Address register maps PEX 8624 Port Configuration registers into Memory space. ***Note:*** *Hardwired to 0.*	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Base Address register maps the PEX 8624 Port Configuration registers into Non-Prefetchable Memory space	RO	Yes	0
16:4	***Reserved***	RsvdP	No	0-0h
31:17	**Base Address 0** 128-KB-aligned Base address used for Memory-Mapped access to the 128-KB block of all PEX 8624 registers (4 KB, per Port).	RW	Yes	0-0h

Register 14-6. 14h Base Address 1 (NT Port Virtual Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *When software writes to the NT Port Virtual Interface* ***BAR1****, the value is automatically copied to the* ***NT Port Virtual Interface BAR1 (Shadow Copy)*** *register (NT Port Virtual Interface, offset D6Ch).*				
31:0	**Upper 32-Bit Address for Memory-Mapped BAR** For 64-bit addressing (**BAR0/1**), Base Address 1 (**BAR1**) extends Base Address 0 (**BAR0**) to provide the upper 32 Address bits when the **Base Address 0** register *Memory Map Type* field (offset 10h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	RO when the **Base Address 0** (**BAR0**) register is not enabled as a 64-bit BAR (*Memory Map Type* field (offset 10h[2:1]) is not programmed to 10b).	RO	Yes	0000_0000h

Register 14-7. 18h Base Address 2 (NT Port Virtual Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *When software writes to the NT Port Virtual Interface* ***Base Address 2*** *register (**BAR2**), the value is automatically copied to the* ***NT Port Virtual Interface BAR2 (Shadow Copy)*** *register (NT Port Virtual Interface, offset D70h).*				
0	**Memory Space Indicator** 0 = Implemented as a Memory BAR	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
19:4	***Reserved***	RsvdP	No	0_000h
31:20	**Base Address 2** Resolution is 1 MB.	RW	Yes	000h

Register 14-8. 1Ch Base Address 3 (NT Port Virtual Interface Memory Space)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Notes: *When software writes to the NT Port Virtual Interface* ***Base Address 3*** *register (**BAR3**), the value is automatically copied to the* ***NT Port Virtual Interface BAR3 (Shadow Copy)*** *register (NT Port Virtual Interface, offset D74h).* *This register has RW privilege if* ***BAR2/3*** *is configured as a 64-bit BAR (**Base Address 2** register Memory Map Type field (NT Port Virtual Interface, offset 18h[2:1]), is programmed to 10b).*					
0	**Memory Space Indicator** **BAR3** can be used as an independent 32-bit only BAR, or as the upper 32 bits of 64-bit **BAR2/3**. 0 = Memory BAR – only value supported	Offset 18h[2:1]=00b	RsvdP	No	0
		Offset 18h[2:1]=10b	RW	Yes	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space All other encodings are ***reserved***.	Offset 18h[2:1]=00b	RsvdP	No	00b
		Offset 18h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset 18h[2:1]=00b	RsvdP	No	0
		Offset 18h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset 18h[2:1]=00b	RsvdP	No	0_000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset 18h[2:1]=10b	RW	Yes	0_000h
31:20	**Base Address 3**		RW	Yes	000h

Register 14-9. 20h Base Address 4 (NT Port Virtual Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *When software writes to the NT Port Virtual Interface* ***Base Address 4*** *register (****BAR4****), the value is automatically copied to the* ***NT Port Virtual Interface BAR4 (Shadow Copy)*** *register (NT Port Virtual Interface, offset D78h).*				
0	**Memory Space Indicator** 0 = Memory BAR – only value supported	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
19:4	***Reserved***	RsvdP	No	0_000h
31:20	**Base Address 4**	RW	Yes	000h

Register 14-10. 24h Base Address 5 (NT Port Virtual Interface Memory Space)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Notes: *When software writes to the NT Port Virtual Interface* ***Base Address 5*** *register (****BAR5****), the value is automatically copied to the* ***NT Port Virtual Interface BAR5 (Shadow Copy)*** *register (NT Port Virtual Interface, offset D7Ch).* *This register has RW privilege if* ***BAR4/5*** *is configured as a 64-bit BAR (****Base Address 4*** *register Memory Map Type field (NT Port Virtual Interface, offset 20h[2:1]), is programmed to 10b).*					
0	**Memory Space Indicator** **BAR5** can be used as an independent 32-bit only BAR, or as the upper 32 bits of 64-bit **BAR4/5**. 0 = Memory BAR – only value supported	Offset 20h[2:1]=00b	RsvdP	No	0
		Offset 20h[2:1]=10b	RW	Yes	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space All other encodings are ***reserved***.	Offset 20h[2:1]=00b	RsvdP	No	00b
		Offset 20h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset 20h[2:1]=00b	RsvdP	Yes	0
		Offset 20h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset 20h[2:1]=00b	RsvdP	No	0_000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset 20h[2:1]=10b	RW	Yes	0_000h
31:20	**Base Address 5**		RW	Yes	000h

Register 14-11. 2Ch Subsystem ID and Subsystem Vendor ID

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Subsystem Vendor ID				
15:0	**Subsystem Vendor ID** Identifies the device manufacturer. Defaults to the PCI-SIG-issued Vendor ID of PLX (10B5h), if not overwritten by serial EEPROM and/or I²C.	RO	Yes	10B5h
Subsystem ID				
31:16	**Subsystem ID** Identifies the particular device. Defaults to the PLX part number for the PEX 8624, if not overwritten by serial EEPROM and/or I²C.	RO	Yes	8624h

Register 14-12. 30h Expansion ROM Base Address

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *Expansion ROM can be enabled in either the NT Port Virtual or Link Interface, but not both simultaneously. Expansion ROM is enabled, by default, in the NT Port Link Interface (**Ingress Control** register Expansion ROM Virtual Side bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 660h[23]) is Cleared).*					
0	**Expansion ROM Enable** 0 = NT Port Virtual Interface Expansion ROM is disabled	NT Port Link Interface, offset 30h[0]=1	RsvdP	No	0
	1 = NT Port Virtual Interface Expansion ROM is enabled, and NT Port Link Interface Expansion ROM is disabled	NT Port Link Interface, offset 30h[0]=0	RW	Yes	0
		NT Port Link Interface, offset 30h[0]=1	RsvdP	No	0
13:1	***Reserved***		RsvdP	No	0-0h
31:14	**Expansion ROM Base Address** If the **Serial EEPROM Clock Frequency** register *Expansion ROM Size* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 268h[16]) value is 0, the Expansion ROM size is 16 KB (default value is FFFF_C001h). Bit 14 is RW. If the *Expansion ROM Size* bit value is 1, the Expansion ROM size is 32 KB (default value is FFFF_8001h). Bit 14 is RO.	When Bit 0 = 0	RsvdP	No	0-0h
		When Bit 0 = 1	RW	Yes	0-0h

Register 14-13. 34h Capability Pointer

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Capability Pointer** Default 40h points to the **PCI Power Management Capability** structure.	RO	Yes	40h
31:8	***Reserved***	RsvdP	No	0000_00h

Register 14-14. 3Ch PCI Interrupt

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**PCI Interrupt Line** The Interrupt Line Routing value communicates interrupt line routing information. Values in this register are programmed by system software and are system architecture-specific. The value is used by device drivers and operating systems.	RW	Yes	00h
15:8	**PCI Interrupt Pin** Identifies the Conventional PCI Interrupt Message(s) the device (or device function) uses. Only value 00h or 01h is allowed in the PEX 8624. 00h = Indicates that the device does not use Conventional PCI Interrupt Message(s) 01h, 02h, 03h, and 04h = Maps to Conventional PCI Interrupt Messages for INTA#, INTB#, INTC#, and INTD#, respectively	RO	Yes	01h
23:16	**Min_Gnt** ***Reserved*** Minimum Grant. Does not apply to PCI Express.	RsvdP	No	00h
31:24	**Max_Lat** ***Reserved*** Maximum Latency. Does not apply to PCI Express.	RsvdP	No	00h

14.6 NT Port Virtual Interface PCI Power Management Capability Registers (Offsets 40h – 44h)

This section details the NT Port Virtual Interface PCI Power Management Capability registers. Table 14-3 defines the register map.

Table 14-3. NT Port Virtual Interface PCI Power Management Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Power Management Capability		Next Capability Pointer (48h)	Capability ID (01h)	40h
PCI Power Management Data	PCI Power Management Control/Status Bridge Extensions ***(Reserved)***	PCI Power Management Status and Control		44h

Register 14-15. 40h PCI Power Management Capability

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Capability ID** Default = 01h – only value allowed.	RO	Yes	01h
15:8	**Next Capability Pointer** Default 48h points to the **MSI Capability** structure.	RO	Yes	48h
18:16	**Version** Default = 011b – only value allowed.	RO	Yes	011b
19	**PME Clock** Power Management Event (PME) clock. Does not apply to PCI Express. Returns 0.	RsvdP	No	0
20	***Reserved***	RsvdP	No	0
21	**Device-Specific Initialization** Default 0 indicates that Device-Specific Initialization is ***not*** required.	RO	Yes	0
24:22	**AUX Current** The PEX 8624 does ***not support*** PME generation from the D3cold Device Power Management (PM) state; therefore, the serial EEPROM value for this field should be 000b.	RO	Yes	000b
25	**D1 Support** ***Not supported*** Default value of 0 indicates that the PEX 8624 does ***not support*** the D1 Device PM state.	RsvdP	No	0
26	**D2 Support** ***Not supported*** Default value of 0 indicates that the PEX 8624 does ***not support*** the D2 Device PM state.	RsvdP	No	0
31:27	**PME Support** The default value is applied to bits [31, 30, and 27] only. PME Messages are disabled, by default.	RO	Yes	0000_0b

Register 14-16. 44h PCI Power Management Status and Control

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
PCI Power Management Status and Control				
1:0	**Power State** Used to determine the Port's current Device PM state, and to Set the Port into a new Device PM state. 00b = D0 01b = D1 – ***Not supported*** 10b = D2 – ***Not supported*** 11b = D3hot If software attempts to write an unsupported state to this field, the Write operation completes normally; however, the data is discarded and no state change occurs.	RW	Yes	00b
2	***Reserved***	RsvdP	No	0
3	**No Soft Reset** 1 = Devices transitioning from the D3hot to D0 Device PM state, because of Power State commands, do not perform an internal reset	RO	Yes	1
7:4	***Reserved***	RsvdP	No	0h
8	**PME Enable** Tied to 0, because the PEX 8624 does ***not*** generate PME in PCI Express mode.	RsvdP	No	0
12:9	**Data Select** Initially writable by serial EEPROM and/or I²C only[a]. This Configuration Space register (CSR) access privilege changes to RW after a Serial EEPROM or I²C Write occurs to this register. Selects the **Data** and **Data Scale** registers (fields [31:24 and 14:13], respectively). 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated All other encodings are ***reserved***.	RO	Yes	0h
14:13	**Data Scale** Writable by serial EEPROM and/or I²C only[a]. Indicates the scaling factor to be used when interpreting the **Data** register value. The value and meaning of this field varies, depending upon which data value is selected by field [12:9] (*Data Select*). There are four internal **Data Scale** registers (one each, per *Data Select* values 0h, 3h, 4h, and 7h). For other *Data Select* values, the **Data Scale** value returned is 0h.	RO	Yes	00b
15	**PME Status** 0 = PME is not being generated by the NT Port	RsvdP	No	0

Register 14-16. 44h PCI Power Management Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
PCI Power Management Control/Status Bridge Extensions				
21:16	***Reserved***	RsvdP	No	0-0h
22	**B2/B3 Support** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
23	**Bus Power/Clock Control Enable** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
PCI Power Management Data				
31:24	**Data** Writable by serial EEPROM and/or I²C only[a]. There are four supported *Data Select* values (0h, 3h, 4h, and 7h). For other *Data Select* values, the **Data Scale** value returned is 0h. Selected by field [12:9] (*Data Select*).	RO	Yes	00h

*a. With no serial EEPROM nor previous I²C programming, Reads return 00h for the **Data** and **Data Scale** registers (for all Data Selects).*

14.7 NT Port Virtual Interface MSI Capability Registers (Offsets 48h – 64h)

The registers detailed in Section 12.8, "MSI Capability Registers (Offsets 48h – 64h)," are also applicable to the NT Port Virtual Interface, except as defined in Table 14-4 (register map), and Register 14-17 and Register 14-18.

Table 14-4. NT Port Virtual Interface MSI Capability Register Map[a]

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
MSI Control		Next Capability Pointer (68h)	Capability ID (05h)	48h
MSI Address				4Ch
MSI Upper Address				50h
Reserved		MSI Data		54h
MSI Mask				58h
MSI Status				5Ch
Reserved				60h – 64h

*a. Offsets 54h, 58h, and 5Ch change to 50h, 54h, and 58h, respectively, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.*

Register 14-17. 58h MSI Mask

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
The interrupt sources in the NT Port Virtual Interface are grouped into four categories – Power Management/Link State events, Device-Specific errors and events, GPIO-generated interrupts, and NT-Virtual Doorbell-generated interrupts. The number of allocated MSI Vectors is determined by the **MSI Control** register *Multiple Message Capable* and *Multiple Message Enable* fields (offset 48h[19:17 and 22:20], respectively). When the number of MSI Vectors that can be requested is: • **Four** – Device-Specific errors and events, Power Management/Link State events, and GPIO events each generate their own MSI Vector. • **Two** – Device-Specific errors and events generate their own MSI Vector, while all other categories are combined and generate the same Vector. • **One** – All interrupt categories generate the same MSI Vector. ***Note:*** *The offset for this register changes from 58h, to 54h, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.* *The bits in this register can be used to mask their respective **MSI Status** register bits (offset 5Ch).*					
0	**MSI Mask for Link State Events** MSI mask for Power Management event- or Link State event-generated interrupts.	Offset 48h[22:20]≥010b	RW	Yes	0
	MSI Mask for Shared Interrupt Sources MSI mask for all interrupt sources when the **MSI Control** register *Multiple Message Enable* field indicates that the Host has allocated one or two Vectors.	Offset 48h[22:20]≤001b	RW	Yes	0
1	**MSI Mask for Device-Specific Errors and Events** MSI mask for Device-Specific error- and event-generated interrupts. Enables MSIs for the RAM ECC errors defined in the **Device-Specific Error Status for Egress ECC Error**, **Device-Specific Error Mask for Egress ECC Error**, **Error Handler 32-Bit Error Status**, and **Error Handler 32-Bit Error Mask** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, unless noted otherwise, offsets 1C0h, 1C4h, 1CCh, and 1D0h, respectively). Also enables MSIs for the NT-Link Port events defined in the **Link Error Status Virtual** and **Link Error Mask Virtual** registers (NT Port Virtual Interface, offsets FE0h and FE4h, respectively). ***Note:*** *For further details, refer to Section 9.1.1, "Interrupt Sources or Events."*	Offset 48h[22:20]≥001b	RW	Yes	0
	Reserved	Offset 48h[22:20]=000b	RsvdP	No	0
2	**MSI Mask for GPIO-Generated Interrupts**	Offset 48h[22:20]≥010b	RW	Yes	0
	Reserved	Offset 48h[22:20]≤001b	RsvdP	No	0
3	**MSI Mask for NT-Virtual Doorbell-Generated Interrupts** Refer to the NT Port registers located at offsets C4Ch through C58h.	Offset 48h[22:20]≥010b	RW	Yes	0
	Reserved	Offset 48h[22:20]≤001b	RsvdP	No	0
31:4	***Reserved***		RsvdP	No	0000_000h

Register 14-18. 5Ch MSI Status

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
The interrupt sources in the NT Port Virtual Interface are grouped into four categories – Power Management/Link State events, Device-Specific errors and events, GPIO-generated interrupts, and NT-Virtual Doorbell-generated interrupts. The number of allocated MSI Vectors is determined by the **MSI Control** register *Multiple Message Capable* and *Multiple Message Enable* fields (offset 48h[19:17 and 22:20], respectively). When the number of MSI Vectors that can be requested is: • **Four** – Device-Specific errors and events, Power Management/Link State events, and GPIO events each generate their own MSI Vector. • **Two** – Device-Specific errors and events generate their own MSI Vector, while all other categories are combined and generate the same Vector. • **One** – All interrupt categories generate the same MSI Vector. ***Note:*** *The offset for this register changes from 5Ch, to 58h, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.* *The bits in this register can be masked by their respective **MSI Mask** register bits (offset 58h).*					
0	**MSI Pending Status for Link State Events** MSI pending status for Power Management event- or Link State event-generated interrupts.	Offset 48h[22:20]≥010b	RO	No	0
	MSI Pending Status for Shared Interrupt Sources MSI pending status for all interrupt sources when the **MSI Control** register *Multiple Message Enable* field indicates that the Host has allocated one or two Vectors.	Offset 48h[22:20]≤001b	RO	No	0
1	**MSI Pending Status for Device-Specific Errors and Events** MSI pending status for Device-Specific error- and event-generated interrupts. Reports status of enabled MSIs for the RAM ECC errors defined in the **Device-Specific Error Status for Egress ECC Error**, **Device-Specific Error Mask for Egress ECC Error**, **Error Handler 32-Bit Error Status**, and **Error Handler 32-Bit Error Mask** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, unless noted otherwise, offsets 1C0h, 1C4h, 1CCh, and 1D0h, respectively). Also reports status of enabled MSIs for the NT-Link Port events defined in the **Link Error Status Virtual** and **Link Error Mask Virtual** registers (NT Port Virtual Interface, offsets FE0h and FE4h, respectively). ***Note:*** *For further details, refer to Section 9.1.1, "Interrupt Sources or Events."*	Offset 48h[22:20]≥001b	RO	No	0
	Reserved	Offset 48h[22:20]=000b	RsvdP	No	0

Register 14-18. 5Ch MSI Status *(Cont.)*

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
2	**MSI Pending Status for GPIO-Generated Interrupts**	Offset 48h[22:20]≥010b	RO	No	0
	Reserved	Offset 48h[22:20]≤001b	RsvdP	No	0
3	**MSI Pending Status for NT-Virtual Doorbell-Generated Interrupts** Refer to the NT Port registers located at offsets C4Ch through C58h.	Offset 48h[22:20]≥010b	RO	No	0
	Reserved	Offset 48h[22:20]≤001b	RsvdP	No	0
31:4	***Reserved***		RsvdP	No	0000_000h

14.8 NT Port Virtual Interface PCI Express Capability Registers (Offsets 68h – A0h)

The registers detailed in Section 12.9, "PCI Express Capability Registers (Offsets 68h – A0h)," are also applicable to the NT Port Virtual Interface, except as defined in Table 14-5 (register map; offsets 7Ch and 80h are ***reserved***), and Register 14-19 through Register 14-24.

Table 14-5. NT Port Virtual Interface PCI Express Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Express Capability		Next Capability Pointer (A4h)	Capability ID (10h)	68h
Device Capability				6Ch
Device Status		***Not Supported/Reserved***	Device Control	70h
Link Capability				74h
Link Status		***Reserved***	Link Control	78h
Reserved				7Ch – 88h
Device Capability 2				8Ch
Device Status 2 ***(Reserved)***		Device Control 2		90h
Reserved				94h
Link Status 2		Link Control 2		98h
Reserved				9Ch – A0h

Register 14-19. 68h PCI Express Capability List and Capability

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
PCI Express Capability List				
7:0	**Capability ID** Program to 10h, by default, as required by the *PCI Express Base r2.0*.	RO	Yes	10h
15:8	**Next Capability Pointer** Program to A4h, to point to the **Subsystem Capability** structure.	RO	Yes	A4h
PCI Express Capability				
19:16	**Capability Version** The PEX 8624 NT Port Virtual Interface programs this field to 2h, as required by the *PCI Express Base r2.0*.	RO	Yes	2h
23:20	**Device/Port Type** Default = PCI Express endpoint device.	RO	Yes	0h
24	**Slot Implemented** ***Not valid for PCI Express endpoint devices***	RsvdP	No	0
29:25	**Interrupt Message Number** The serial EEPROM writes 00_000b, because the Base Message and MSI Messages are the same.	RO	Yes	00_000b
31:30	***Reserved***	RsvdP	No	00b

Register 14-20. 6Ch Device Capability

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
2:0	**Maximum Payload Size Supported** The Maximum Payload Size for the NT Port Virtual Interface is 2,048 bytes. 000b = NT Port Virtual Interface supports a 128-byte maximum payload 001b = NT Port Virtual Interface supports a 256-byte maximum payload 010b = NT Port Virtual Interface supports a 512-byte maximum payload 011b = NT Port Virtual Interface supports a 1,024-byte maximum payload 100b = NT Port Virtual Interface supports a 2,048-byte maximum payload No other encodings are supported.	HwInit	Yes	100b
4:3	**Phantom Functions Supported** ***Not supported***	RO	Yes	00b
5	**Extended Tag Field Supported** 0 = Maximum *Tag* field is 5 bits 1 = Maximum *Tag* field is 8 bits	RO	Yes	0
8:6	**Endpoint L0s Acceptable Latency** 111b = No Limit	RO	Yes	111b
11:9	**Endpoint L1 Acceptable Latency** 111b = No Limit	RO	Yes	111b
14:12	***Reserved***	RsvdP	No	000b
15	**Role-Based Error Reporting**	RO	Yes	1
17:16	***Reserved***	RsvdP	No	00b
25:18	**Captured Slot Power Limit Value** For the NT Port Virtual Interface, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [27:26] (*Captured Slot Power Limit Scale*).	RO	Yes	00h
27:26	**Captured Slot Power Limit Scale** For the NT Port Virtual Interface, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [25:18] (*Captured Slot Power Limit Value*). 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001	RO	Yes	00b
31:28	***Reserved***	RsvdP	No	0h

Register 14-21. 70h Device Status and Control

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	Device Control			
0	**Correctable Error Reporting Enable** 0 = Disables 1 = Enables the NT Port Virtual Interface to report Correctable errors to the Local Host	RW	Yes	0
1	**Non-Fatal Error Reporting Enable** 0 = Disables 1 = Enables the NT Port Virtual Interface to report Non-Fatal errors to the Local Host	RW	Yes	0
2	**Fatal Error Reporting Enable** 0 = Disables 1 = Enables the NT Port Virtual Interface to report Fatal errors to the Local Host	RW	Yes	0
3	**Unsupported Request Reporting Enable** 0 = Disables 1 = Enables the NT Port Virtual Interface to report UR errors to the Local Host	RW	Yes	0
4	**Enable Relaxed Ordering** ***Not supported***	RsvdP	No	0
7:5	**Maximum Payload Size** The NT Port Virtual Interface power-on/reset value is 000b, to support a Maximum Payload Size of 128 bytes. Software can change this field to configure the NT Port Virtual Interface to support other Payload sizes; however, software cannot change this field to a value larger than that indicated by the **Device Capability** register *Maximum Payload Size Supported* field (offset 6Ch[2:0]), for the NT Port Virtual and Link Interfaces. (Requester and Completer domains must possess the same Maximum Payload Size.) 000b = NT Port Virtual Interface supports a 128-byte maximum payload 001b = NT Port Virtual Interface supports a 256-byte maximum payload 010b = NT Port Virtual Interface supports a 512-byte maximum payload 011b = NT Port Virtual Interface supports a 1,024-byte maximum payload 100b = NT Port Virtual Interface supports a 2,048-byte maximum payload No other encodings are supported. ***Note:*** *Software must halt all transactions through the NT Port before changing this field.*	RW	Yes	000b
8	**Extended Tag Field Enable** ***Not supported***	RsvdP	No	0
9	**Phantom Functions Enable** ***Not supported***	RsvdP	No	0
10	**AUX Power PM Enable** ***Not supported***	RsvdP	No	0
11	**Enable No Snoop** ***Not supported***	RsvdP	No	0
14:12	**Maximum Read Request Size** ***Not supported***	RsvdP	No	000b
15	***Reserved***	RsvdP	No	0

Register 14-21. 70h Device Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	Device Status			
16	**Correctable Error Detected** Set when the NT Port Virtual Interface detects a Correctable error, regardless of the bit 0 (*Correctable Error Reporting Enable*) state. 0 = NT Port Virtual Interface did not detect a Correctable error 1 = NT Port Virtual Interface detected a Correctable error	RW1C	Yes	0
17	**Non-Fatal Error Detected** Set when the NT Port Virtual Interface detects a Non-Fatal error, regardless of the bit 1 (*Non-Fatal Error Reporting Enable*) state. 0 = NT Port Virtual Interface did not detect a Non-Fatal error 1 = NT Port Virtual Interface detected a Non-Fatal error	RW1C	Yes	0
18	**Fatal Error Detected** Set when the NT Port Virtual Interface detects a Fatal error, regardless of the bit 2 (*Fatal Error Reporting Enable*) state. 0 = NT Port Virtual Interface did not detect a Fatal error 1 = NT Port Virtual Interface detected a Fatal error	RW1C	Yes	0
19	**Unsupported Request Detected** Set when the NT Port Virtual Interface detects a UR, regardless of the bit 3 (*Unsupported Request Reporting Enable*) state. 0 = NT Port Virtual Interface did not detect a UR 1 = NT Port Virtual Interface detected a UR	RW1C	Yes	0
20	**AUX Power Detected** ***Not supported*** Initially Cleared.	RsvdP	No	0
21	**Transactions Pending** ***Not supported*** Because the PEX 8624 NT Port is a bridging device, it does not track Completion for the corresponding Non-Posted transactions. Therefore, the NT Port Virtual Interface does not implement Transactions Pending.	RsvdP	No	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 14-22. 74h Link Capability

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
3:0	**Supported Link Speeds** Indicates the NT Port Virtual Interface's supported Link speed. 0001b = 2.5 GT/s Link speed is supported 0010b = 5.0 GT/s and 2.5 GT/s Link speeds are supported All other encodings are ***reserved***.	RO	Yes	0010b (STRAP_RESERVED17#=H) 0001b (STRAP_RESERVED17#=L)
9:4	**Maximum Link Width** The PEX 8624 maximum Link width is x8 = 00_1000b. Actual maximum Link width is Set by the STRAP_STN*x*_PORTCFG*x* inputs. 00_0000b = ***Reserved*** 00_0001b = x1 00_0010b = x2 00_0100b = x4 00_1000b = x8 All other encodings are ***not supported***.	Refer to Default value	No	Set by STRAP_STN*x*_PORTCFG*x* input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station x* bits (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[5:0])
11:10	**Active State Power Management (ASPM) Support** Active State Link PM support. Indicates the level of ASPM supported by the Port. 01b = L0s Link PM state entry is supported All other encodings are ***reserved***.	RO	Yes	01b
14:12	**L0s Exit Latency** Indicates the L0s Link PM state exit latency for the given PCI Express Link. Value depends upon the **Physical Layer Command and Status** register *N_FTS Value* field (NT Port Virtual Interface, offset 220h[15:8]) value and Link speed. Exit latency is calculated, as follows: • **2.5 GHz** – Multiply *N_FTS Value* x 4 (4 symbol times in 1 N_FTS) x 4 ns (1 symbol time at 2.5 GT/s) • **5.0 GHz** – Multiply *N_FTS Value* x 4 (4 symbol times in 1 N_FTS) x 2 ns (1 symbol time at 5.0 GT/s) 100b = NT Port Virtual Interface L0s Link PM state Exit Latency is 512 ns to less than 1 s at 5.0 GT/s 101b = NT Port Virtual Interface L0s Link PM state Exit Latency is 1 s to less than 2 s at 2.5 GT/s All other encodings are ***reserved***. ***Note:*** *The NT Port Virtual Interface never enters the L0s Link PM state, because there is no physical Link attached to it.*	RO	No	100b (5.0 GT/s) 101b (2.5 GT/s)

Register 14-22. 74h Link Capability *(Cont.)*

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td>17:15</td><td>L1 Exit Latency
Indicates the L1 Link PM state exit latency for the given PCI Express Link. Value depends upon the Link speed.
001b = NT Port Virtual Interface L1 Link PM state Exit Latency is 1 s to less than 2 s at 5.0 GT/s
010b = NT Port Virtual Interface L1 Link PM state Exit Latency is 2 s to less than 4 s at 2.5 GT/s
All other encodings are reserved.
Note: The NT Port Virtual Interface never enters the L1 Link PM state, because there is no physical Link attached to it.</td><td>RO</td><td>Yes</td><td>001b
(5.0 GT/s)

010b
(2.5 GT/s)</td></tr>
<tr><td>18</td><td>Clock Power Management</td><td>RO</td><td>Yes</td><td>0</td></tr>
<tr><td>23:19</td><td>Reserved</td><td>RsvdP</td><td>No</td><td>0-0h</td></tr>
<tr><td>31:24</td><td>Port Number
The NT Port Number value is limited to the Station 0 Ports, and is selected by the STRAP_NT_UPSTRM_PORTSEL[1:0] Strapping inputs. All other encodings are reserved.
<table>
<tr><th>Register Value</th><th>Strapping Input Value</th><th>Port Number</th></tr>
<tr><td>00h</td><td>00b (LL)</td><td>0</td></tr>
<tr><td>01h</td><td>01b (LH)</td><td>1</td></tr>
</table></td><td>Refer to Default value</td><td>No</td><td>Set by STRAP_NT_UPSTRM_PORTSEL[1:0] input levels</td></tr>
</table>

Register 14-23. 78h Link Status and Control

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	Link Control			
1:0	**Active State Power Management (ASPM) Control** The NT Port Virtual Interface ignores this register value, because no external Port connection exists.	RW	Yes	00b
2	***Reserved***	RsvdP	No	0
3	**Read Request Return Parameter Control** Read Request Return Parameter "R" control. Read Completion Boundary (RCB). Cleared.	RO	Yes	0
4	**Link Disable** ***Reserved*** for the NT Port Virtual Interface.	RsvdP	No	0
5	**Retrain Link** ***Reserved*** for the NT Port Virtual Interface.	RsvdP	No	0
6	**Common Clock Configuration** The NT Port Virtual Interface ignores this register value, because no external Port connection exists.	RW	Yes	0
7	**Extended Sync** The NT Port Virtual Interface ignores this register value, because no external Port connection exists.	RW	Yes	0
15:8	***Reserved***	RsvdP	No	00h

Register 14-23. 78h Link Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	Link Status			
19:16	**Current Link Speed** Indicates the negotiated Link speed of the Port's PCI Express Link. 0001b = 2.5 GT/s Link speed 0010b = 5.0 GT/s Link speed All other encodings are ***reserved***. The value in this field is undefined when the Link is not up.	RO	No	0001b
25:20	**Negotiated Link Width** Reports the Link status of the NT Port Link Interface. Dependent upon the configuration of the physical Ports. Link width is determined by the negotiated value with the attached Lane/Port. 00_0000b = Link is down (default) 00_0001b = x1 or Port is in the *DL_Down* state 00_0010b = x2 00_0100b = x4 00_1000b = x8 All other encodings are ***not supported***.	RO	No	00_0000b
26	**Training Error** ***Reserved*** for the NT Port Virtual Interface.	RsvdP	No	0
27	**Link Training** ***Reserved*** for the NT Port Virtual Interface. Always read as 0.	RsvdP	No	0
28	**Slot Clock Configuration** Because there is no external connection to the NT Port Virtual Interface, this bit is always Cleared, which indicates that the PEX 8624 uses an independent clock.	HwInit	Yes	0
31:29	***Reserved***	RsvdP	No	000b

Register 14-24. 98h Link Status and Control 2

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Link Control 2				
3:0	**Target Link Speed** 0001b = 2.5 GT/s Link speed supported 0010b = 5.0 GT/s Link speed supported All other encodings are ***reserved***.	RWS	Yes	0010b
4	**Enter Compliance**	RWS	Yes	0
5	**Hardware Autonomous Speed Disable** ***Reserved*** Initial transition to the highest supported common Link speed is not blocked by this bit.	RsvdP	No	0
6	**Selectable De-Emphasis** ***Reserved***	RsvdP	Yes	0
9:7	**Transmit Margin** Intended for debug and compliance testing only.	RWS	Yes	000b
10	**Enter Modified Compliance** Intended for debug and compliance testing only.	RWS	Yes	0
11	**Compliance SOS** 1 = Link Training and Status State Machine (LTSSM) must periodically send SKIP Ordered-Sets between sequences when sending the Compliance Pattern or Modified Compliance Pattern	RWS	Yes	0
12	**Compliance De-Emphasis** Sets the de-emphasis level in the *Polling.Compliance* state, if the entry occurred due to bit 4 (*Enter Compliance*) being Set.	RWS	Yes	0
15:13	***Reserved***	RsvdP	No	000b
Link Status 2				
16	**Current De-Emphasis Level** Reflects the de-emphasis level. 0 = -6 dB (Link is operating at 5.0 GT/s) 1 = -3.5 dB	RO	Yes	0 (5.0 GT/s) 1 (2.5 GT/s)
31:17	***Reserved***	RsvdP	No	0-0h

14.9 NT Port Virtual Interface Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – C4h)

The registers detailed in Section 12.10, "Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)," are also applicable to the NT Port, except as defined in Table 14-6 (register map) and Register 14-25.

Table 14-6. NT Port Virtual Interface Subsystem ID and Subsystem Vendor ID Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved	Next Capability Pointer (C8h) / SSID/SSVID Capability ID (0Dh)	A4h
Subsystem ID	Subsystem Vendor ID	A8h
Reserved	ACh –	C4h

Register 14-25. A4h Subsystem Capability

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**SSID/SSVID Capability ID** SSID/SSVID registers for the PCI-to-PCI bridge. Program to 0Dh, as required by the *PCI-to-PCI Bridge r1.2*.	RO	Yes	0Dh
15:8	**Next Capability Pointer** Program to C8h, to point to the **Vendor-Specific Capability 3** structure.	RO	Yes	C8h
31:16	***Reserved***	RsvdP	No	0000h

14.10 NT Port Virtual Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)

This section details the NT Port Virtual Interface Vendor-Specific Capability 3 registers, which include the **Memory BAR*x* Setup** registers and **Configuration Address** and **Data Window** registers. Table 14-7 defines the register map used by the NT Port Virtual Interface.

The **NT Port Virtual Interface BAR*x* Setup** (offsets D0h through E0h) register values are shadowed in the corresponding **NT Port Virtual Interface BAR*x* Setup Shadow** registers (offsets D80h through D90h, respectively). When software writes to an **NT Port Virtual Interface BAR*x* Setup** register, the value is automatically copied to the corresponding **NT Port Virtual Interface BAR*x* Setup** (**Shadow Copy)** register. If the **NT Port Virtual Interface BAR*x* Setup** registers are programmed by serial EEPROM, the **NT Port Virtual Interface BAR*x* Setup** (**Shadow Copy)** registers must also be programmed by serial EEPROM, to the same respective register values.

The Cursor Mechanism registers at offsets F8h and FCh provide a means for accessing PCI Express Extended Configuration Space registers (offsets 100h through FFFh) within the NT Port Virtual and Link Interfaces, when only standard PCI Configuration transactions (that do not support the *Extended Register Number* field within the Completion Request Header) are available. The Cursor Mechanism can generally access only those registers that are defined by the *PCI Express Base r2.0*, and not the Device-Specific registers. However, if Port 0 is the NT Port, the Cursor Mechanism in the NT Port Virtual Interface registers can also access the Device-Specific registers.

Table 14-7. NT Port Virtual Interface Vendor-Specific Capability 3 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved / Vendor-Specific Capability 3	Next Capability Pointer 3 (00h) / Capability ID 3 (09h)	C8h
Vendor-Specific Header 3 ***(Reserved)***		CCh
NT Port Virtual Interface BAR0/1 Setup		D0h
NT Port Virtual Interface Memory BAR2 Setup		D4h
NT Port Virtual Interface Memory BAR2/3 Setup		D8h
NT Port Virtual Interface Memory BAR4 Setup		DCh
NT Port Virtual Interface Memory BAR4/5 Setup		E0h
Reserved		E4h – F4h
Configuration Address Window	***Reserved***	F8h
Configuration Data Window		FCh

Register 14-26. C8h Vendor-Specific Capability 3

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Capability ID 3**	RO	Yes	09h
15:8	**Next Capability Pointer 3** 00h = This capability is the last capability in the Linked List	RO	Yes	00h
23:16	**Length** Number of bytes in this Capability structure.	RO	Yes	38h
31:24	***Reserved***	RsvdP	Yes	00h

Register 14-27. CCh Vendor-Specific Header 3

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	***Reserved***	RO	Yes	0380_0002h

Register 14-28. D0h NT Port Virtual Interface BAR0/1 Setup

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The NT Port Virtual Interface **BAR0/1 Setup (Shadow Copy)** register (NT Port Virtual Interface, offset D80h) must be programmed with the same value as this register.*				
1:0	**BAR0/1 Enable** 00b = Disables Virtual Interface **BAR0** and **BAR1** 01b = ***Reserved*** 10b = Enables Virtual Interface **BAR0** and disables **BAR1** (**BAR0** is a 32-bit BAR) 11b = Enables Virtual Interface **BAR0** and **BAR1** (**BAR0/1** is a 64-bit BAR)	RW	Yes	10b
2	**BAR0 Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RW	Yes	0
31:3	***Reserved***	RsvdP	No	0-0h

Register 14-29. D4h NT Port Virtual Interface Memory BAR2 Setup

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *The NT Port Virtual Interface **Memory BAR2 Setup (Shadow Copy)** register (NT Port Virtual Interface, offset D84h) must be programmed with the same value as this register. This requirement applies only to the NT Port Virtual Interface.*					
0	**Type Selector**		RsvdP	No	0
2:1	**BAR2 Type** 00b = **BAR2** is implemented as a 32-bit Memory BAR 10b = **BAR2/3** is implemented as a 64-bit Memory BAR No other encodings are allowed.		RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0_000h
30:20	**BAR2 Size** Specifies the Address Range size requested by **BAR2**. 0 = Corresponding **BAR2** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR2** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is 2^n), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR2 Enable** 0 = **BAR2** is disabled, all **BAR2** bits read 0 1 = **BAR2** is enabled	Field [2:1] (*BAR2 Type*) = 00b	RW	Yes	0
	BAR2 Size Included with field [30:20] when this BAR is used as a 64-bit BAR, **BAR2/3**.	Field [2:1] (*BAR2 Type*) = 10b	RW	Yes	0

Register 14-30. D8h NT Port Virtual Interface Memory BAR2/3 Setup

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
Note: *The NT Port Virtual Interface **Memory BAR2/3 Setup (Shadow Copy)** register (NT Port Virtual Interface, offset D88h) must be programmed with the same value as this register. This requirement applies only to the NT Port Virtual Interface.*					
0	**Type Selector**		RsvdP	No	0
2:1	**BAR3 Type** 00b = Selects 32-bit Memory BAR (**BAR3**) No other encodings are allowed.		RO	No	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***	Offset D4h[2:1] (*BAR2 Type*) = 00b	RsvdP	No	0_000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset D4h[2:1] (*BAR2 Type*) = 10b	RW	Yes	0_000h
30:20	**BAR3 Size** Specifies the Address Range size requested by **BAR3**. 0 = Corresponding **BAR3** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR3** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is 2^n), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR3 Enable** **32-Bit BAR:** 0 = **BAR3** is disabled 1 = **BAR3** is enabled as a 32-bit BAR	Offset D4h[2:1] (*BAR2 Type*) = 00b	RW	Yes	0
	64-Bit BAR: 0 = **BAR2/3** is disabled, all **BAR2/3** bits read 0 1 = **BAR2/3** is enabled as a 64-bit BAR	Offset D4h[2:1] (*BAR2 Type*) = 10b	RW	Yes	0

Register 14-31. DCh NT Port Virtual Interface Memory BAR4 Setup

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *The NT Port Virtual Interface* ***Memory BAR4 Setup (Shadow Copy)*** *register (NT Port Virtual Interface, offset D8Ch) must be programmed with the same value as this register. This requirement applies only to the NT Port Virtual Interface.*					
0	**Type Selector**		RsvdP	No	0
2:1	**BAR4 Type** 00b = **BAR4** is implemented as a 32-bit Memory BAR (**BAR4**) 10b = **BAR4/5** is implemented as a 64-bit Memory BAR (**BAR4/5**) No other encodings are allowed.		RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0_000h
30:20	**BAR4 Size** Specifies the Address Range size requested by **BAR4**. 0 = Corresponding **BAR4** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR4** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is 2^n), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR4 Enable** 0 = **BAR4** is disabled, all **BAR4** bits read 0 1 = **BAR4** is enabled	Field [2:1] (*BAR4 Type*) = 00b	RW	Yes	0
	BAR4 Size Included with field [30:20] when this BAR is used as a 64-bit BAR, **BAR4/5**.	Field [2:1] (*BAR4 Type*) = 10b	RW	Yes	0

Register 14-32. E0h NT Port Virtual Interface Memory BAR4/5 Setup

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
Note: *The NT Port Virtual Interface* ***Memory BAR4/5 Setup (Shadow Copy)*** *register (NT Port Virtual Interface, offset D90h) must be programmed with the same value as this register. This requirement applies only to the NT Port Virtual Interface.*					
0	**Type Selector**		RsvdP	No	0
2:1	**BAR5 Type** 00b = Selects 32-bit Memory BAR (**BAR5**) No other encodings are allowed.		RO	No	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***	Offset DCh[2:1] (*BAR4 Type*) = 00b	RsvdP	No	0_000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset DCh[2:1] (*BAR4 Type*) = 10b	RW	Yes	0_000h
30:20	**BAR5 Size** Specifies the Address Range size requested by **BAR5**. 0 = Corresponding **BAR5** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR5** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is 2^n), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR5 Enable** **32-Bit BAR:** 0 = **BAR5** is disabled 1 = **BAR5** is enabled as a 32-bit BAR	Offset DCh[2:1] (*BAR4 Type*) = 00b	RW	Yes	0
	64-Bit BAR: 0 = **BAR4/5** is disabled, all **BAR4/5** bits read 0 1 = **BAR4/5** is enabled as a 64-bit BAR	Offset DCh[2:1] (*BAR4 Type*) = 10b	RW	Yes	0

Register 14-33. F8h Configuration Address Window (Device-Specific Cursor Mechanism)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	***Reserved***	RsvdP	No	0000h
25:16	**Register Offset**	RW	Yes	0-0h
30:26	***Reserved***	RsvdP	No	0-0h
31	**Interface Select** 0 = Access is to the NT Port Link Interface Type 0 Configuration Space register 1 = Access is to the NT Port Virtual Interface Type 0 Configuration Space register	RW	Yes	0

Register 14-34. FCh Configuration Data Window (Device-Specific Cursor Mechanism)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Register Data** Software selects a register by writing into the NT Port Virtual Interface Configuration Address window, then reads from or writes to that register using this register.	RW	Yes	0000_0000h

14.11 NT Port Virtual Interface Device Serial Number Extended Capability Registers (Offsets 100h – 134h)

The registers detailed in Section 12.11, "Device Serial Number Extended Capability Registers (Offsets 100h – 134h)," are also applicable to the NT Port. Table 14-8 defines the register map used by all Ports.

Table 14-8. NT Port Virtual Interface Device Serial Number Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (FB4h) / Capability Version (1h)	PCI Express Extended Capability ID (0003h)	100h
Serial Number (Lower DW)		104h
Serial Number (Upper DW)		108h
Reserved		10Ch – 134h

14.12 NT Port Virtual Interface Virtual Channel Extended Capability Registers (Offsets 148h – 1A4h)

The registers detailed in Section 12.13, "Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)," are also applicable to the NT Port Virtual Interface, except as defined in Table 14-9 (register map), and Register 14-35 through Register 14-39.

Table 14-9. NT Port Virtual Interface Virtual Channel Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (448h or 950h) / Capability Version (1h)	PCI Express Extended Capability ID (0002h)	148h
Port VC Capability 1		14Ch
Port VC Capability 2		150h
Port VC Status ***(Reserved)***	Port VC Control	154h
VC0 Resource Capability		158h
VC0 Resource Control		15Ch
VC0 Resource Status	***Reserved***	160h
Reserved		164h – 1A4h

Register 14-35. 148h Virtual Channel Extended Capability Header

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
15:0	**PCI Express Extended Capability ID** Program to 0002h, as required by the *PCI Express Base r2.0.*		RO	No	0002h
19:16	**Capability Version** Program to 1h, as required by the *PCI Express Base r2.0*.		RO	No	1h
31:20	**Next Capability Offset** Next extended capability is the **Vendor-Specific Extended Capability** structure, offset 448h.	NT Port is Port 0	RO	No	448h
	Next extended capability is the **Vendor-Specific Extended Capability 2** structure, offset 950h.	Otherwise	RO	No	950h

Register 14-36. 14Ch Port VC Capability 1

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
0	**Extended VC Counter** 0 = PEX 8624 Port supports only one Virtual Channel, VC0 1 = ***Reserved***		RO	No	0
3:1	***Reserved***		RsvdP	No	000b
4	**Low-Priority Extended VC Counter** For Strict Priority arbitration, indicates the number of extended VCs (those in addition to VC0) that belong to the Low-Priority Virtual Channel group for this PEX 8624 Port. 0 = For this PEX 8624 Port, only VC0 belongs to the Low-Priority Virtual Channel group 1 = ***Reserved***, because the PEX 8624 supports only one VC		RO	No	0
7:5	***Reserved***		RsvdP	No	000b
9:8	**Reference Clock** Cleared.		RsvdP	No	00b
11:10	**Port Arbitration Table Entry Size** 10b = Port Arbitration Table entry size is 4 bits	NT Port is Port 0	RW	Yes	10b
	00b = Port Arbitration Table entry size is 1 bit	Otherwise	RO	Yes	00b
31:12	***Reserved***		RsvdP	No	0000_0h

Register 14-37. 158h VC0 Resource Capability

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
1:0	**Port Arbitration Capability** Bit 0 = 1 – Non-configurable Round-Robin (Hardware-Fixed) arbitration Bit 1 = 1 – Weighted Round-Robin (WRR) arbitration with 32 Phases	NT Port is Port 0	RO	No	10b
		Otherwise	RO	No	01b
14:2	***Reserved***		RsvdP	No	0-0h
15	**Reject Snoop Transactions** Not a PCI Express switch feature; therefore, Cleared.		RsvdP	No	0
22:16	**Maximum Time Slots** ***Not supported***		RsvdP	No	000_0000b
23	***Reserved***		RsvdP	No	0
31:24	**Port Arbitration Table Offset** Offset of the Port Arbitration Table, as the number of DQWords from the Base address of the **Virtual Channel Extended Capability** structure. (Refer to Section 12.13.1, "Port Arbitration Table Registers (Offsets 1A8h – 1BCh)," for further details.) 00h = Port Arbitration Table is not present 06h = Port Arbitration Table is located at register offset 1A8h (148h + 6 x 4 DWords)	NT Port is Port 0	RO	No	06h
		Otherwise	RO	No	00h

Register 14-38. 15Ch VC0 Resource Control

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
0	**TC/VC Map** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped into VC0. Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.		RO	No	1
7:1			RW	Yes	7Fh
15:8	***Reserved***		RsvdP	No	00h
16	**Load Port Arbitration Table** Software writes this bit, to load the updated WRR Port Arbitration Table value to the internal logic. If the Port does not support the WRR Port Arbitration value, hardware ignores the Write to this register. Software Read always returns 0.		RW	Yes	0
19:17	**Port Arbitration Select** Selects the Port Arbitration type for the NT Port Virtual Interface. Indicates the bit number in the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[1:0]) that corresponds to the arbitration type. 0 = Round-Robin (Hardware-Fixed) arbitration scheme 1 = Weighted Round-Robin with 32 Phases ***Note:*** *If software programs other values, hardware ignores the value.*	NT Port is Port 0	RW	Yes	001b
		Otherwise	RW	Yes	000b
23:20	***Reserved***		RsvdP	No	0h
24	**VC ID** Defines the NT Port Virtual Interface VC0 ID code. Cleared, because there is only one VC.		RO	No	0
30:25	***Reserved***		RsvdP	No	0-0h
31	**VC Enable** 0 = Not allowed 1 = Enables the NT Port Virtual Interface VC0		RO	No	1

Register 14-39. 160h VC0 Resource Status

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	***Reserved***	RsvdP	No	0000h
16	**Port Arbitration Table Status** 0 = Hardware has finished loading values stored in the Port Arbitration Table, after software Sets the **VC0 Resource Control** register *Load Port Arbitration Table* bit (offset 15Ch[16]) 1 = Software updates to WRR Port Arbitration Table are pending update to the functional logic	RO	No	0
17	**VC0 Negotiation Pending** 0 = VC0 negotiation completed (NT Port Virtual Interface Link to the internal virtual PCI Bus is up) 1 = VC0 initialization is not complete for the NT Port Virtual Interface	RO	Yes	0
31:18	***Reserved***	RsvdP	No	0-0h

14.13 NT Port Virtual Interface Port Arbitration Table Registers (Offsets 1A8h – 1BCh)

The registers detailed in Section 12.13.1, "Port Arbitration Table Registers (Offsets 1A8h – 1BCh)," are also applicable to the NT Port Virtual Interface if the NT Port is Port 0. Port Arbitration Table phases are used to determine Port weighting during "Weighted Round-Robin with 32 Phases" Port arbitration. Table 14-10 defines the register map used by the NT Port Virtual Interface.

Note: ***The Port Arbitration Table is used only when Weighted Round-Robin with 32-phase Port Arbitration is selected, by way of the VC0 Resource Control register Port Arbitration Select field (offset 15Ch[19:17]=001b).***

Table 14-10. NT Port Virtual Interface Port Arbitration Table Register Map (Only Upstream Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port; *Reserved* (RsvdP) for All Other Ports)

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	
Phase 7	Phase 6	Phase 5	Phase 4	Phase 3	Phase 2	Phase 1	Phase 0	1A8h
Phase 15	Phase 14	Phase 13	Phase 12	Phase 11	Phase 10	Phase 9	Phase 8	1ACh
Phase 23	Phase 22	Phase 21	Phase 20	Phase 19	Phase 18	Phase 17	Phase 16	1B0h
Phase 31	Phase 30	Phase 29	Phase 28	Phase 27	Phase 26	Phase 25	Phase 24	1B4h
Reserved								1B8h – 1BCh

Register 14-40. 1A8h Port Arbitration Table Phases 0 to 7 (Only Upstream Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port; *Reserved* (RsvdP) for All Other Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Note: *The fields within this register are valid only on upstream Port 0, when the NT Port is Port 0, and* ***reserved*** *on all other Ports.*					
3:0	**Port Arbitration Table Phase 0**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
7:4	**Port Arbitration Table Phase 1**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
11:8	**Port Arbitration Table Phase 2**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
15:12	**Port Arbitration Table Phase 3**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
19:16	**Port Arbitration Table Phase 4**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
23:20	**Port Arbitration Table Phase 5**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
27:24	**Port Arbitration Table Phase 6**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
31:28	**Port Arbitration Table Phase 7**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h

Register 14-41. 1ACh Port Arbitration Table Phases 8 to 15 (Only Upstream Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port; *Reserved* (RsvdP) for All Other Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Note: *The fields within this register are valid only on upstream Port 0, when the NT Port is Port 0, and* ***reserved*** *on all other Ports.*					
3:0	**Port Arbitration Table Phase 8**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
7:4	**Port Arbitration Table Phase 9**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
11:8	**Port Arbitration Table Phase 10**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
15:12	**Port Arbitration Table Phase 11**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
19:16	**Port Arbitration Table Phase 12**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
23:20	**Port Arbitration Table Phase 13**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
27:24	**Port Arbitration Table Phase 14**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
31:28	**Port Arbitration Table Phase 15**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h

Register 14-42. 1B0h Port Arbitration Table Phases 16 to 23 (Only Upstream Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port; *Reserved* (RsvdP) for All Other Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Note: *The fields within this register are valid only on upstream Port 0, when the NT Port is Port 0, and* ***reserved*** *on all other Ports.*					
3:0	**Port Arbitration Table Phase 16**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
7:4	**Port Arbitration Table Phase 17**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
11:8	**Port Arbitration Table Phase 18**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
15:12	**Port Arbitration Table Phase 19**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
19:16	**Port Arbitration Table Phase 20**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
23:20	**Port Arbitration Table Phase 21**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
27:24	**Port Arbitration Table Phase 22**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
31:28	**Port Arbitration Table Phase 23**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h

Register 14-43. 1B4h Port Arbitration Table Phases 24 to 31 (Only Upstream Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port; *Reserved* (RsvdP) for All Other Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
Note: *The fields within this register are valid only on upstream Port 0, when the NT Port is Port 0, and* ***reserved*** *on all other Ports.*					
3:0	**Port Arbitration Table Phase 24**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
7:4	**Port Arbitration Table Phase 25**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
11:8	**Port Arbitration Table Phase 26**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
15:12	**Port Arbitration Table Phase 27**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
19:16	**Port Arbitration Table Phase 28**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
23:20	**Port Arbitration Table Phase 29**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
27:24	**Port Arbitration Table Phase 30**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h
31:28	**Port Arbitration Table Phase 31**	NT Port is Port 0 (refer to Note)	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
	Reserved	All other Ports	RsvdP	No	0h

14.14 NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)

The registers detailed in Section 12.14, "Device-Specific Registers (Offsets 1C0h – 51Ch)," and Section 12.16, "Device-Specific Registers (Offsets 54Ch – F8Ch)" (for offsets A00h through C88h), are unique to the PEX 8624 and not referenced in the *PCI Express Base r2.0*. These registers are also applicable to the NT Port Virtual Interface, except as defined in Table 14-11 (register map) through Table 14-15, and Register 14-45 through Register 14-72.

Other NT Port Virtual Interface Device-Specific registers are detailed in:

- Section 14.16, "NT Port Virtual Interface Device-Specific Registers (Offsets F34h – F8Ch)"
- Section 14.18, "NT Port Virtual Interface Device-Specific Registers – Link Error (Offsets FE0h – FFCh)"

Note: It is recommended that these registers not be changed from their default values.

Table 14-11. NT Port Virtual Interface Device-Specific Register Map (Offsets 1C0h – C88h)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

NT Port Virtual Interface Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)	1C0h … 1FCh
Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)	200h … 25Ch
Device-Specific Registers – Serial EEPROM (Offsets 260h – 26Ch)	260h … 26Ch
Device-Specific Registers – Physical Layer (Offsets 270h – 28Ch)	270h … 28Ch
Device-Specific Registers – I2C Slave Interface (Offsets 290h – 2C4h)	290h … 2C4h
Device-Specific Registers – Bus Number CAM (Offsets 2C8h – 304h)	2C8h … 304h
Device-Specific Registers – I/O CAM (Offsets 308h – 344h)	308h … 344h
Device-Specific Registers – Address-Mapping CAM (Offsets 348h – 444h)	348h … 444h

Table 14-11. NT Port Virtual Interface Device-Specific Register Map (Offsets 1C0h – C88h) *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (950h) / 1h	PCI Express Extended Capability ID (000Bh)	448h
Device-Specific Registers – Vendor-Specific Dual Cast Extended Capability (Offsets 448h – 51Ch)		… 51Ch
Reserved		520h – 570h
Device-Specific Registers – Port Configuration (Offsets 574h – 628h)		574h … 628h
Device-Specific Registers – General-Purpose Input/Output (Offsets 62Ch – 65Ch)		62Ch … 65Ch
NT Port Virtual Interface Device-Specific Registers – Ingress Control and Port Enable (Offsets 660h – 67Ch)		660h … 67Ch
Device-Specific Registers – IOCAM Base and Limit Upper 16 Bits (Offsets 680h – 6BCh)		680h … 6BCh
Device-Specific Registers – Base Address Shadow (Offsets 6C0h – 73Ch)		6C0h … 73Ch
Device-Specific Registers – Virtual Channel Resource Control Shadow (Offsets 740h – 83Ch)		740h … 83Ch
Reserved		840h – 93Ch
Device-Specific Registers – Ingress Credit Handler Port Pool (Offsets 940h – 94Ch)		940h … 94Ch
Next Capability Offset 2 (C34h) / 1h	PCI Express Extended Capability ID 2 (000Bh)	950h
NT Port Virtual Interface Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)		… 95Ch
Factory Test Only		960h – 97Ch
Reserved		980h – 9FCh

Table 14-11. NT Port Virtual Interface Device-Specific Register Map (Offsets 1C0h – C88h) *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Device-Specific Registers – Ingress Credit Handler Threshold (Offsets A00h – B7Ch)		A00h … B7Ch
Device-Specific Registers – SerDes Support (Offsets B80h – BFCh)		B80h … BFCh
Reserved		C00h – C30h
Next Capability Offset 4 (000h)	1h / PCI Express Extended Capability ID 4 (000Bh)	C34h
NT Port Virtual Interface Device-Specific Registers – Vendor-Specific Extended Capability 4 (Offsets C34h – C88h)		… C88h

14.14.1 NT Port Virtual Interface Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)

The registers detailed in Section 12.14.1, "Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)," are also applicable to the NT Port Virtual Interface, except as defined in Table 14-12 (register map), and Register 14-44 through Register 14-47.

Table 14-12. NT Port Virtual Interface Device-Specific Error Checking and Debug Register Map (Ports[a])

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device-Specific Error Status for Egress ECC Error				1C0h
Device-Specific Error Mask for Egress ECC Error				1C4h
ECC Error Check Disable				1C8h
Error Handler 32-Bit Error Status ***(Factory Test Only)***				1CCh
Error Handler 32-Bit Error Mask ***(Factory Test Only)***				1D0h
Factory Test Only				1D4h
Clock Enable				1D8h
Debug Control			***Factory Test Only/Reserved***	1DCh
Power Management Hot Plug User Configuration				1E0h
Factory Test Only				1E4h
Bad TLP Counter				1E8h
Bad DLLP Counter				1ECh
Reserved				1F0h
Station 0/1 Lane Status				1F4h
ACK Transmission Latency Limit				1F8h
Factory Test Only				1FCh

a. Certain registers are Port-specific, others are Station-specific or Chip-specific; all are device-specific.

Register 14-44. 1E0h Power Management Hot Plug User Configuration

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**L0s Entry Idle Counter** Traffic Idle time to meet, to enter the L0s Link PM state. 0 = Idle condition must last 1 s 1 = Idle condition must last 4 s	RW	Yes	0
1	***Factory Test Only***	RW	Yes	0
2	**NT Virtual MPS CSR Select** NT Port Virtual Interface Maximum Payload Size register select. 0 = NT Port Virtual Interface uses the NT Port Link Interface's Maximum Payload Size (offset 70h[7:5]) 1 = NT Port Virtual Interface uses its own Maximum Payload Size (offset 70h[7:5])	RW	Yes	0
7:3	***Factory Test Only***	RW	Yes	0-0h
8	**DLLP Timeout Link Retrain Disable** Disable Link retraining when no Data Link Layer Packets (DLLPs) are received for more than 256 s. 0 = Enables Link retraining when no DLLPs are received for more than 256 s (default) 1 = DLLP Timeout is disabled	RW	Yes	0
9	***Factory Test Only***	RW	Yes	0
10	**L0s Entry Disable** 0 = Enables entry into the L0s Link PM state on a Port when the L0s idle conditions are met 1 = Disables entry into the L0s Link PM state on a Port when the L0s idle conditions are met	RW	Yes	0
16:11	***Reserved***	RsvdP	No	0-0h
17	**40-Pin I/O Expander Enable** 0 = Enables 16-pin I/O Expanders for all downstream Ports that implement Serial Hot Plug 1 = Enables 40-pin I/O Expanders for all downstream Ports that implement Serial Hot Plug ***Note:*** *Value of 1 can be enabled only by serial EEPROM (that is, it cannot be enabled by software nor by I²C).*	RW	Yes (See Note)	0
31:18	***Reserved***	RsvdP	No	0-0h

Register 14-45. 1E8h Bad TLP Counter

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Bad TLP Counter** Value reflects errors detected on the NT Port Link Interface. Counts the number of TLPs received with bad Link Cyclic Redundancy Check (LCRC), or number of TLPs with a Sequence Number Mismatch error. The Counter saturates at FFFF_FFFFh and does not roll over to 0000_0000h.	RWS	Yes	0000_0000h

Register 14-46. 1ECh Bad DLLP Counter

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Bad DLLP Counter** Value reflects errors detected on the NT Port Link Interface. Counts the number of DLLPs received with bad LCRC, or number of Data Link Layer Packets (DLLPs) with a Sequence Number Mismatch error. The Counter saturates at FFFF_FFFFh and does not roll over to 0000_0000h.	RWS	Yes	0000_0000h

Register 14-47. 1F8h ACK Transmission Latency Limit

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
The value of this register should be valid after Link negotiation.				
11:0	**ACK Transmission Latency Limit** Acknowledge Control Packet (ACK) Transmission Latency Limit. The value of this field changes, based upon the NT Port's Link width and **Device Control** register *Maximum Payload Size* field (offset 70h[7:5]) value.	RWS	Yes	0EDh
15:12	***Reserved***	RsvdP	No	0h
23:16	**Upper 8 Bits of the Replay Timer Limit** The value in this register is a multiplier of the default internal timer values that are compliant to the *PCI Express Base r2.0*. These bits should normally remain the default value, 00h.	RWS	Yes	00h
30:24	***Reserved***	RsvdP	No	0-0h
31	**ACK Transmission Latency Timer Status** Indicates the written status of field [11:0] (*ACK Transmission Latency Limit*). After the register is written, either by software and/or serial EEPROM, this bit is Set, and Cleared only by a Fundamental Reset.	RO	No	0

14.14.2 NT Port Virtual Interface Device-Specific Registers – Ingress Control and Port Enable (Offsets 660h – 67Ch)

The registers detailed in Section 12.16.3, "Device-Specific Registers – Ingress Control and Port Enable (Offsets 660h – 67Ch)," are also applicable to the NT Port Virtual Interface, except as defined in Table 14-13 (register map; offset 678h is ***reserved***), and Register 14-48 and Register 14-49.

Table 14-13. NT Port Virtual Interface Device-Specific Ingress Control and Port Enable Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Ingress Control				660h
Ingress Control Shadow				664h
Port Enable Status				668h
Negotiated Link Width for Ports 0, 1, 5, 6				66Ch
Reserved		***Factory Test Only***	Negotiated Link Width for Ports 8, 9	670h
Port Cut-Thru Enable Status				674h
Reserved				678h – 67Ch

Register 14-48. 660h Ingress Control (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
25:0	***Factory Test Only***	RWS	Yes	0-0h
26	**Disable Upstream Port BAR0 and BAR1** 0 = Enables the upstream Port **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively) 1 = Disables the upstream Port **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively)	RWS	Yes	0
27	***Not used***	RWS	Yes	0
28	**Disable VGA BIOS Memory Access Decoding** 0 = Enables the **Bridge Control** register *VGA 16-Bit Decode Enable*, *VGA Enable*, and *ISA Enable* bits (offset 3Ch[20:18], respectively), and enables decoding of the PC ROM shadow addresses C_0000h to C_FFFFh (packets destined to these addresses are blocked) 1 = Disables the **Bridge Control** register *VGA 16-Bit Decode Enable*, *VGA Enable*, and *ISA Enable* bits (offset 3Ch[20:18], respectively), and disables decoding of the PC ROM shadow addresses C_0000h to C_FFFFh (packets destined to these addresses are ***not*** blocked)	RWS	Yes	0
30:29	***Factory Test Only***	RWS	Yes	00b
31	***Not used***	RWS	Yes	0

Register 14-49. 664h Ingress Control Shadow (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	***Factory Test Only***	RWS	Yes	0
1	**Use Serial EEPROM Values for Ingress Credit Initialization** Allow Configuration with a Device Number that is not 0, that is accessing downstream devices, to be forwarded. When the Device Number is 0, the Configuration terminates in a UR. 0 = Use default values for ingress credit initialization 1 = Use serial EEPROM values for ingress credit initialization	RWS	Yes	0
3:2	***Factory Test Only***	RWS	Yes	00b
4	**Drop EP TLPs** Drop Endpoint TLPs. 1 = Endpoint TLP was dropped	RWS	Yes	0
5	**No Special Treatment for Relaxed Ordering Traffic** The PEX 8624 supports Relaxed Ordering for Completions. By default, if the RO attribute is Set within a Completion, then that Completion can bypass Posted transactions, if Posted TLPs are blocked at the egress Port (due to insufficient Posted credits from the connected device). This behavior can be disabled by Setting this bit, in each Station. 1 = Device-Specific Relaxed Ordering Completion will not be flagged to the Egress block	RWS	Yes	0
7:6	***Factory Test Only***	RWS	Yes	00b
8	**Drop ECRC TLPs** Drop End-to-end Cyclic Redundancy Check (ECRC) TLPs. 1 = ECRC TLP was dropped	RWS	Yes	0
10:9	**ACK TLP Counter Timeout** Sets the number of ingress TLP Acknowledgements (ACKs) pending, which causes a high-priority ACK to be sent. 00b = 16 TLPs 01b = 8 TLPs 10b = 4 TLPs 11b = Feature is disabled	RWS	Yes	00b
31:11	***Factory Test Only***	RWS	Yes	0-0h

14.14.3 NT Port Virtual Interface Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)

The registers detailed in Section 12.16.8, "Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)," are also applicable to the NT Port, except for the Next Capability Offset value, as defined in Table 14-14 (register map) and Register 14-50.

Table 14-14. NT Port Virtual Interface Device-Specific, Vendor-Specific Extended Capability 2 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset 2 (C34h)	Capability Version 2 (1h) / PCI Express Extended Capability ID 2 (000Bh)	950h
Vendor-Specific Header 2		954h
Hardwired Device ID	Hardwired Vendor ID	958h
Reserved	PLX Hardwired Revision ID	95Ch

Register 14-50. 950h Vendor-Specific Extended Capability 2

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**PCI Express Extended Capability ID 2** Program to 000Bh, indicating that the Capability structure is the **Vendor-Specific Extended Capability** structure.	RO	Yes	000Bh
19:16	**Capability Version 2**	RO	Yes	1h
31:20	**Next Capability Offset 2** Program to C34h, which addresses the **Vendor-Specific Extended Capability 4** structure.	RO	Yes	C34h

14.14.4 NT Port Virtual Interface Device-Specific Registers – Vendor-Specific Extended Capability 4 (Offsets C34h – C88h)

This section details the NT Port Virtual Interface Device-Specific, Vendor-Specific Extended Capability 4 registers, which include the **Memory BAR*x* Address Translation**, **Doorbell**, and **Scratchpad** registers. Table 14-15 defines the register map used by the NT Port Virtual Interface.

Table 14-15. NT Port Virtual Interface Device-Specific, Vendor-Specific Extended Capability 4 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset 4 (000h)	Capability Version 4 (1h) / PCI Express Extended Capability ID 4 (000Bh)	C34h
Vendor-Specific Header 4		C38h
Memory BAR2 Address Translation Lower		C3Ch
Memory BAR3 Address Translation Upper		C40h
Memory BAR4 Address Translation Lower		C44h
Memory BAR5 Address Translation Upper		C48h
Reserved	Virtual Interface IRQ Set	C4Ch
Reserved	Virtual Interface IRQ Clear	C50h
Reserved	Virtual Interface IRQ Mask Set	C54h
Reserved	Virtual Interface IRQ Mask Clear	C58h
Reserved	Link Interface IRQ Set	C5Ch
Reserved	Link Interface IRQ Clear	C60h
Reserved	Link Interface IRQ Mask Set	C64h
Reserved	Link Interface IRQ Mask Clear	C68h
NT Port SCRATCH0		C6Ch
NT Port SCRATCH1		C70h
NT Port SCRATCH2		C74h
NT Port SCRATCH3		C78h
NT Port SCRATCH4		C7Ch
NT Port SCRATCH5		C80h
NT Port SCRATCH6		C84h
NT Port SCRATCH7		C88h

Register 14-51. C34h Vendor-Specific Extended Capability 4

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**PCI Express Extended Capability ID 4** Program to 000Bh, indicating that the Capability structure is the **Vendor-Specific Extended Capability** structure.	RO	Yes	000Bh
19:16	**Capability Version 4**	RO	Yes	1h
31:20	**Next Capability Offset 4** 000h = This extended capability is the last capability in the PEX 8624 Extended Capabilities list	RO	Yes	000h

Register 14-52. C38h Vendor-Specific Header 4

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**Vendor-Specific ID 4** ID Number of this Extended Capability structure.	RO	Yes	0003h
19:16	**Vendor-Specific Rev 4** Version Number of **this structure.**	RO	Yes	0h
31:20	**Vendor-Specific Length 4** Number of bytes i**n the entire structure.**	RO	Yes	078h

Register 14-53. C3Ch Memory BAR2 Address Translation Lower

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**NT Port Virtual-to-Link Interface BAR2 Base Translation Address** NT Port Virtual-to-Link Interface Base Translation address when **BAR2** is enabled (**NT Port Virtual Interface Memory BAR2 Setup** register *BAR2 Enable* bit, offset D4h[31], is Set).	RW	Yes	000h

Register 14-54. C40h Memory BAR3 Address Translation Upper

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	Offset D8h[31]=0	RsvdP	No	0_0000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:0]) are used as the upper 32 bits.	Offset D8h[31]=1	RW	Yes	0_0000h
31:20	**NT Port Virtual-to-Link Interface BAR3 Base Translation Address** NT Port Virtual-to-Link Interface Base Translation address when **BAR3** is enabled (**NT Port Virtual Interface Memory BAR2/3 Setup** register *BAR3 Enable* bit, offset D8h[31], is Set).		RW	Yes	000h

Register 14-55. C44h Memory BAR4 Address Translation Lower

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**NT Port Virtual-to-Link Interface BAR4 Base Translation Address** NT Port Virtual-to-Link Interface Base Translation address when **BAR4** is enabled (**NT Port Virtual Interface Memory BAR4 Setup** register *BAR4 Enable* bit, offset DCh[31], is Set).	RW	Yes	000h

Register 14-56. C48h Memory BAR5 Address Translation Upper

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	Offset E0h[31]=0	RsvdP	No	0_0000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:0]) are used as the upper 32 bits.	Offset E0h[31]=1	RW	Yes	0_0000h
31:20	**NT Port Virtual-to-Link Interface BAR5 Base Translation Address** NT Port Virtual-to-Link Interface Base Translation address when **BAR5** is enabled (**NT Port Virtual Interface Memory BAR4/5 Setup** register *BAR5 Enable* bit, offset E0h[31], is Set).		RW	Yes	000h

Register 14-57. C4Ch Virtual Interface IRQ Set

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note:	*The bits in this register can be masked by their respective **Virtual Interface IRQ Mask Set** register bits (offset C54h).*			
15:0	**SET_IRQ** Set Virtual IRQ. Controls the state of the Virtual Interface Doorbell Interrupt Request. Reading returns the status of the bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Sets the corresponding Interrupt Request. The Virtual Interface interrupt is asserted if the following conditions exist: • This register (offset C4Ch or C50h) value is non-zero, and, • Corresponding **Virtual Interface IRQ Mask Set** or **Virtual Interface IRQ Mask Clear** register (offset C54h or C58h, respectively) *Interrupt Mask* bit is not Set, and, • Interrupts (either INT*x* or MSIs) are enabled	RW1S	Yes	0000h
31:16	***Reserved***	RsvdP	No	0000h

Register 14-58. C50h Virtual Interface IRQ Clear

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note:	*The bits in this register can be masked by their respective **Virtual Interface IRQ Mask Clear** register bits (offset C58h).*			
15:0	**CLR_IRQ** Clear Virtual IRQ. Controls the state of the Virtual Interface Doorbell Interrupt Request. Reading returns the status of the bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Clears the corresponding Interrupt Request. The Virtual Interface interrupt is de-asserted if the following conditions exist: • This register (offset C50h or C4Ch) value is zero (0), –or– • **Virtual Interface IRQ Mask Set** or **Virtual Interface IRQ Mask Clear** register (offset C54h or C58h, respectively) masks all its **Set** or **Clear** register (offset C50h or C4Ch) *Set* bits, and • INT*x* interrupts are enabled	RW1C	Yes	0000h
31:16	***Reserved***	RsvdP	No	0000h

Register 14-59. C54h Virtual Interface IRQ Mask Set

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be used to mask their respective* ***Virtual Interface IRQ Set*** *register bits (offset C4Ch).*				
15:0	**SET_IRQM** Virtual Interface interrupt IRQ Mask Set. Reading returns the state of the *Interrupt Mask* bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Clears the corresponding *Interrupt Mask* bit. 0 = Corresponding **Virtual Interface IRQ Set** register (offset C4Ch) *Interrupt Request* bit is not masked 1 = Corresponding **Virtual Interface IRQ Set** register (offset C4Ch) *Interrupt Request* bit is masked/disabled	RW1S	Yes	FFFFh
31:16	***Reserved***	RsvdP	No	0000h

Register 14-60. C58h Virtual Interface IRQ Mask Clear

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be used to mask their respective* ***Virtual Interface IRQ Clear*** *register bits (offset C50h).*				
15:0	**CLR_IRQM** Clear Virtual IRQ Mask. Controls the state of the Virtual Interface *Interrupt Request* bits. Reading returns the state of the *Interrupt Mask* bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Clears the corresponding *Interrupt Mask* bit. 0 = Corresponding **Virtual Interface IRQ Clear** register (offset C50h) *Interrupt Request* bit is not masked 1 = Corresponding **Virtual Interface IRQ Clear** register (offset C50h) *Interrupt Request* bit is masked/disabled	RW1C	Yes	FFFFh
31:16	***Reserved***	RsvdP	No	0000h

Register 14-61. C5Ch Link Interface IRQ Set

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note:	*The bits in this register can be masked by their respective **Link Interface IRQ Mask Set** register bits (offset C64h).*			
15:0	**SET_IRQ** Set Link IRQ. Controls the state of the Link Interface Doorbell Interrupt Request. Reading returns the status of the bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Sets the corresponding Interrupt Request. The Link Interface interrupt is asserted if the following conditions exist: • This register (offset C5Ch or C60h) value is non-zero, and, • Corresponding **Link Interface IRQ Mask Set** or **Link Interface IRQ Mask Clear** register (offset C64h or C68h, respectively) *Interrupt Mask* bit is not Set, and, • Interrupts (either INT*x* or MSIs) are enabled	RW1S	Yes	0000h
31:16	***Reserved***	RsvdP	No	0000h

Register 14-62. C60h Link Interface IRQ Clear

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note:	*The bits in this register can be masked by their respective **Link Interface IRQ Mask Clear** register bits (offset C68h).*			
15:0	**CLR_IRQ** Clear Virtual IRQ. Controls the state of the Virtual Interface Doorbell Interrupt Request. Reading returns the status of the bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Clears the corresponding Interrupt Request. The Virtual Interface interrupt is de-asserted if the following conditions exist: • This register (offset C60h or C5Ch) value is zero (0), –or– • **Link Interface IRQ Mask Set** or **Link Interface IRQ Mask Clear** register (offset C64h or C68h, respectively) masks all its **Set** or **Clear** register (offset C60h or C5Ch) *Set* bits, and • INT*x* interrupts are enabled	RW1C	Yes	0000h
31:16	***Reserved***	RsvdP	No	0000h

Register 14-63. C64h Link Interface IRQ Mask Set

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be used to mask their respective* ***Link Interface IRQ Set*** *register bits (offset C5Ch).*				
15:0	**SET_IRQM** Link Interface Interrupt IRQ Mask Set. Reading returns the state of the *Interrupt Mask* bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Sets the corresponding *Interrupt Mask* bit. 0 = Corresponding **Link Interface IRQ Set** register (offset C5Ch) *Interrupt Request* bit is not masked 1 = Corresponding **Link Interface IRQ Set** register (offset C5Ch) *Interrupt Request* bit is masked/disabled	RW1S	Yes	FFFFh
31:16	***Reserved***	RsvdP	No	0000h

Register 14-64. C68h Link Interface IRQ Mask Clear

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be used to mask their respective* ***Link Interface IRQ Clear*** *register bits (offset C60h).*				
15:0	**CLR_IRQM** Link Interface Interrupt IRQ Mask Clear. Reading returns the state of the *Interrupt Mask* bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Clears the corresponding *Interrupt Mask* bit. 0 = Corresponding **Link Interface IRQ Clear** register (offset C60h) *Interrupt Request* bit is not masked 1 = Corresponding **Link Interface IRQ Clear** register (offset C60h) *Interrupt Request* bit is masked/disabled	RW1C	Yes	FFFFh
31:16	***Reserved***	RsvdP	No	0000h

Register 14-65. C6Ch NT Port SCRATCH0

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Scratchpad 0** 32-bit Scratchpad 0 register.	RW	Yes	0000_0000h

Register 14-66. C70h NT Port SCRATCH1

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Scratchpad 1** 32-bit Scratchpad 1 register.	RW	Yes	0000_0000h

Register 14-67. C74h NT Port SCRATCH2

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Scratchpad 2** 32-bit Scratchpad 2 register.	RW	Yes	0000_0000h

Register 14-68. C78h NT Port SCRATCH3

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Scratchpad 3** 32-bit Scratchpad 3 register.	RW	Yes	0000_0000h

Register 14-69. C7Ch NT Port SCRATCH4

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Scratchpad 4** 32-bit Scratchpad 4 register.	RW	Yes	0000_0000h

Register 14-70. C80h NT Port SCRATCH5

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Scratchpad 5** 32-bit Scratchpad 5 register.	RW	Yes	0000_0000h

Register 14-71. C84h NT Port SCRATCH6

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Scratchpad 6** 32-bit Scratchpad 6 register.	RW	Yes	0000_0000h

Register 14-72. C88h NT Port SCRATCH7

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Scratchpad 7** 32-bit Scratchpad 7 register.	RW	Yes	0000_0000h

14.15 NT Port Virtual Interface NT Bridging-Specific Registers (Offsets C8Ch – F30h)

Table 14-16 defines the register map of the NT Port Virtual Interface NT Bridging-Specific registers.

Table 14-16. NT Port Virtual Interface NT Bridging-Specific Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Reserved	C8Ch –	D64h
NT Port Virtual Interface NT Bridging-Specific Registers – Base Address and Base Address Setup (Offsets D68h – D90h) (Shadow Copy)	D68h … D90h	
NT Port Virtual Interface NT Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Addresses D94h – DB0h)	D94h … DB0h	
Reserved	DB4h –	F30h

14.15.1 NT Port Virtual Interface NT Bridging-Specific Registers – Base Address and Base Address Setup (Offsets D68h – D90h)

The registers in this section are shadow copies of the NT Port Virtual Interface Base Address register (BAR) and BAR Configuration registers, and valid only for Ports 0, 4, and 8. If Port 0 is the NT Port, the registers are in Virtual Interface Configuration Space. Table 14-17 defines the register map.

Note: It is recommended that these registers not be changed from their default values.

Table 14-17. NT Port Virtual Interface NT Bridging-Specific Base Address Register (BAR) and BAR Setup Register Map (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
BAR0 (Shadow Copy)				D68h
BAR1 (Shadow Copy)				D6Ch
BAR2 (Shadow Copy)				D70h
BAR3 (Shadow Copy)				D74h
BAR4 (Shadow Copy)				D78h
BAR5 (Shadow Copy)				D7Ch
BAR0/1 Setup (Shadow Copy)				D80h
Memory BAR2 Setup (Shadow Copy)				D84h
Memory BAR2/3 Setup (Shadow Copy)				D88h
Memory BAR4 Setup (Shadow Copy)				D8Ch
Memory BAR4/5 Setup (Shadow Copy)				D90h

Register 14-73. D68h BAR0 (Shadow Copy) (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *This register is a shadow copy of the NT Port Virtual Interface* ***Base Address 0*** *(**BAR0**) register (NT Port Virtual Interface, offset 10h).*				
0	**Memory Space Indicator** Virtual Side **BAR0** is configured by serial EEPROM and the Local Host. By default, Configuration **BAR0/1 Setup** register selects 32-bit Memory **BAR0**. 0 = Memory BAR – only value supported	RsvdP	No	0
2:1	**Memory Map Type** Reflection of the BAR configuration, as specified in the **BAR0/1 Setup (Shadow Copy)** register (offset D80h). 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
16:4	***Reserved***	RsvdP	No	0-0h
31:17	**Base Address 0** 128-KB Base address in which to map the PEX 8624 Configuration Space registers into Memory space.	RW	Yes	0-0h

Register 14-74. D6Ch BAR1 (Shadow Copy) (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *This register is a shadow copy of the NT Port Virtual Interface* ***Base Address 1*** *(**BAR1**) register (NT Port Virtual Interface, offset 14h).*				
31:0	**Upper 32-Bit BAR0 of Virtual NT Port** **BAR1** is the upper 32 bits of 64-bit **BAR0/1**, Base Address 1 extends Base Address 0 to provide the upper 32 Address bits when the **BAR0 (Shadow Copy)** register *Memory Map Type* field (offset D68h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Reserved when the **BAR0 (Shadow Copy)** register is not enabled as a 64-bit BAR (*Memory Map Type* field (offset D68h[2:1]) is not programmed to 10b).	RsvdP	Yes	0000_0000h

Register 14-75. D70h BAR2 (Shadow Copy) (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
*Note: This register is a shadow copy of the NT Port Virtual Interface **Base Address 2** (**BAR2**) register (NT Port Virtual Interface, offset 18h).*				
0	**Memory Space Indicator** 0 = Memory BAR – only value supported	RO	No	0
2:1	**Memory Map Type** Reflection of the BAR configuration, as specified in the **Memory BAR2 Setup (Shadow Copy)** register (offset D84h). 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
19:4	***Reserved***	RsvdP	No	0_000h
31:20	**Base Address 2**	RW	Yes	000h

Register 14-76. D74h BAR3 (Shadow Copy) (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
Notes: *This register is a shadow copy of the NT Port Virtual Interface* ***Base Address 3*** *(**BAR3**) register (NT Port Virtual Interface, offset 1Ch).* *This register has RW privilege if **BAR2/3** is configured as a 64-bit BAR (**BAR2 (Shadow Copy)** register Memory Map Type field (NT Port Virtual Interface, offset D70h[2:1]), is programmed to 10b).*					
0	**Memory Space Indicator** 0 = Memory BAR – only value supported	Offset D70h[2:1]=00b	RsvdP	No	0
		Offset D70h[2:1]=10b	RW	Yes	0
2:1	**Memory Map Type** Reflection of the BAR configuration, as specified in the **Memory BAR2/3 Setup (Shadow Copy)** register (offset D88h). 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space All other encodings are ***reserved***.	Offset D70h[2:1]=00b	RsvdP	No	00b
		Offset D70h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset D70h[2:1]=00b	RsvdP	No	0
		Offset D70h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset D70h[2:1]=00b	RsvdP	No	0_000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset D70h[2:1]=10b	RW	Yes	0_000h
31:20	**Base Address 3**		RW	Yes	000h

Register 14-77. D78h BAR4 (Shadow Copy) (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *This register is a shadow copy of the NT Port Virtual Interface* ***Base Address 4*** *(**BAR4**) register (NT Port Virtual Interface, offset 20h).*				
0	**Memory Space Indicator** 0 = Memory BAR – only value supported	RO	No	0
2:1	**Memory Map Type** Reflection of the BAR configuration, as specified in the **Memory BAR4 Setup (Shadow Copy)** register (offset D8Ch). 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
19:4	***Reserved***	RsvdP	No	0_000h
31:20	**Base Address 4**	RW	Yes	000h

Register 14-78. D7Ch BAR5 (Shadow Copy) (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
Notes: *This register is a shadow copy of the NT Port Virtual Interface* ***Base Address 5*** *(**BAR5**) register (NT Port Virtual Interface, offset 24h).* *This register has RW privilege if **BAR4/5** is configured as a 64-bit BAR (**BAR4 (Shadow Copy)** register Memory Map Type field (NT Port Virtual Interface, offset D78h[2:1]), is programmed to 10b).*					
0	**Memory Space Indicator** 0 = Memory BAR – only value supported	Offset D78h[2:1]=00b	RsvdP	No	0
		Offset D78h[2:1]=10b	RW	Yes	0
2:1	**Memory Map Type** Reflection of the BAR configuration, as specified in the **Memory BAR4/5 Setup (Shadow Copy)** register (offset D90h). 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space All other encodings are ***reserved***.	Offset D78h[2:1]=00b	RsvdP	No	00b
		Offset D78h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset D78h[2:1]=00b	RsvdP	No	0
		Offset D78h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset D78h[2:1]=00b	RsvdP	No	0_000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset D78h[2:1]=10b	RW	Yes	0_000h
31:20	**Base Address 5**		RW	Yes	000h

Register 14-79. D80h BAR0/1 Setup (Shadow Copy) (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: *This register must be programmed with the same value as the* ***NT Port Virtual Interface BAR0/1 Setup*** *register (NT Port Virtual Interface, offset D0h).*				
1:0	**Type Selector** 00b = Disables Virtual Interface **BAR0** and **BAR1** 01b = ***Reserved*** 10b = Enables Virtual Interface **BAR0** and disables **BAR1** (**BAR0** is a 32-bit BAR) 11b = Enables Virtual Interface **BAR0** and **BAR1** (**BAR0/1** is a 64-bit BAR)	RW	Yes	10b
2	**BAR0 Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RW	Yes	0
31:3	***Reserved***	RsvdP	No	0-0h

Register 14-80. D84h Memory BAR2 Setup (Shadow Copy) (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
Note: *This register must be programmed with the same value as the* ***NT Port Virtual Interface Memory BAR2 Setup*** *register (NT Port Virtual Interface, offset D4h). This requirement applies only to the NT Port Virtual Interface.*					
0	**Type Selector**		RsvdP	No	0
2:1	**BAR2 Type** 00b = **BAR2** is implemented as a 32-bit Memory BAR 10b = **BAR2/3** is implemented as a 64-bit Memory BAR No other encodings are allowed.		RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0-0h
30:20	**BAR2 Size** Specifies the Address Range size requested by **BAR2**. 0 = Corresponding **BAR2** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR2** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is 2^n), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR2 Enable** 0 = **BAR2** is disabled, all **BAR2** bits read 0 1 = **BAR2** is enabled	Field [2:1] (*BAR2 Type*) = 00b	RW	Yes	0
	BAR2 Size Included with field [30:20] when this BAR is used as a 64-bit BAR, **BAR2/3**.	Field [2:1] (*BAR2 Type*) = 10b	RW	Yes	0

Register 14-81. D88h Memory BAR2/3 Setup (Shadow Copy) (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *This register must be programmed with the same value as the* ***NT Port Virtual Interface Memory BAR2/3 Setup*** *register (NT Port Virtual Interface, offset D8h). This requirement applies only to the NT Port Virtual Interface.*					
0	**Type Selector**		RsvdP	No	0
2:1	**BAR3 Type** 00b = Selects 32-bit Memory BAR (**BAR3**) No other encodings are allowed.		RO	No	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0-0h
30:20	**BAR3 Size** Specifies the Address Range size requested by **BAR3**. 0 = Corresponding **BAR3** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR3** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is 2^n), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR3 Enable** **32-Bit BAR:** 0 = **BAR3** is disabled 1 = **BAR3** is enabled as a 32-bit BAR	Offset D84h[2:1] (*BAR2 Type*) = 00b	RW	Yes	0
	64-Bit BAR: 0 = **BAR2/3** is disabled, all **BAR2/3** bits read 0 1 = **BAR2/3** is enabled as a 64-bit BAR	Offset D84h[2:1] (*BAR2 Type*) = 10b	RW	Yes	0

Register 14-82. D8Ch Memory BAR4 Setup (Shadow Copy) (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
Note: *This register must be programmed with the same value as the* ***NT Port Virtual Interface Memory BAR4 Setup*** *register (NT Port Virtual Interface, offset DCh). This requirement applies only to the NT Port Virtual Interface.*					
0	**Type Selector**		RsvdP	No	0
2:1	**BAR4 Type** 00b = **BAR4** is implemented as a 32-bit Memory BAR 10b = **BAR4/5** is implemented as a 64-bit Memory BAR		RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0-0h
30:20	**BAR4 Size** Specifies the Address Range size requested by **BAR4**. 0 = Corresponding **BAR4** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR4** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is 2^n), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR4 Enable** 0 = **BAR4** is disabled, all **BAR4** bits read 0 1 = **BAR4** is enabled	Field [2:1] (*BAR4 Type*) = 00b	RW	Yes	0
	BAR4 Size Included with field [30:20] when this BAR is used as a 64-bit BAR, **BAR4/5**.	Field [2:1] (*BAR4 Type*) = 10b	RW	Yes	0

Register 14-83. D90h Memory BAR4/5 Setup (Shadow Copy) (Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *This register must be programmed with the same value as the* ***NT Port Virtual Interface Memory BAR4/5 Setup*** *register (NT Port Virtual Interface, offset E0h). This requirement applies only to the NT Port Virtual Interface.*					
0	**Type Selector**		RsvdP	No	0
2:1	**BAR5 Type** 00b = Selects 32-bit Memory BAR (**BAR5**) No other encodings are allowed.		RO	No	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0-0h
30:20	**BAR5 Size** Specifies the Address Range size requested by **BAR5**. 0 = Corresponding **BAR5** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR5** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is 2^n), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR5 Enable** **32-Bit BAR:** 0 = **BAR5** is disabled 1 = **BAR5** is enabled as a 32-bit BAR	Offset D8Ch[2:1] (*BAR4 Type*) = 00b	RW	Yes	0
	64-Bit BAR: 0 = **BAR4/5** is disabled, all **BAR4/5** bits read 0 1 = **BAR4/5** is enabled as a 64-bit BAR	Offset D8Ch[2:1] (*BAR4 Type*) = 10b	RW	Yes	0

14.15.2 NT Port Virtual Interface NT Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Addresses D94h – DB0h)

This section describes the NT Port Virtual Interface NT Bridging-Specific Requester ID Translation Lookup Table (LUT) Entry registers. The NT Port uses these registers for Requester ID translation when it forwards:

- Memory Requests from the NT Port Virtual Interface to the NT Port Link Interface, –or–
- Completion TLPs from the NT Port Link Interface to the NT Port Virtual Interface

If the application needs to send traffic through the NT Port Virtual Interface, program the registers listed in this group with the corresponding Requester's Requester ID, then Set the *LUT Entry_n Enable* bit (bit 31) of each register accordingly.

Table 14-18 defines the register and address locations, as they relate to Register 14-84.

Table 14-18. NT Port Virtual Interface NT Bridging-Specific Requester ID Translation Lookup Table Entry_*n* Register Locations

ADDR Location	Lookup Table Entry_*n*	ADDR Location	Lookup Table Entry_*n*
D94h	0	DA4h	4
D98h	1	DA8h	5
D9Ch	2	DACh	6
DA0h	3	DB0h	7

Register 14-84. D94h – DB0h NT Port Virtual Interface Requester ID Translation LUT Entry_*n* (where *n* = 0 through 7)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
2:0	**Requester ID on Virtual Side**	**Function Number** LUT Entry_*n* Requester Function Number.	RW	Yes	000b
7:3		**Device Number** LUT Entry_*n* Requester Device Number.	RW	Yes	0000_0b
15:8		**Bus Number** LUT Entry_*n* Requester Bus Number.	RW	Yes	00h
29:16	***Reserved***		RsvdP	No	0-0h
30	**LUT Entry_*n* No Snoop Enable** If Set, the NT Port Clears the TLP *No Snoop* attribute bit for the Memory Request, then goes from the NT Port Virtual Interface to the NT Port Link Interface, and re-calculates the ECRC. If the original TLP has an ECRC error, the NT Port corrupts the re-calculated ECRC before transmitting to the other Host domain. The NT Port sets the *No Snoop* attribute bit when it forwards the Completion TLP from the NT Port Link Interface to the NT Port Virtual Interface if this bit is Set for the corresponding Requester ID entry. This ECRC rule applies to Completion TLPs as well. 0 = Disables 1 = Enables		RW	Yes	0
31	**LUT Entry_*n* Enable** 0 = Disables 1 = Enables		RW	Yes	0

14.16 NT Port Virtual Interface Device-Specific Registers (Offsets F34h – F8Ch)

The registers detailed in Section 12.16, "Device-Specific Registers (Offsets 54Ch – F8Ch)" (for offsets F34h through F8Ch), are unique to the PEX 8624 and not referenced in the *PCI Express Base r2.0*. These registers are also applicable to the NT Port Virtual Interface, except as defined in Table 14-19 (register map) and Table 14-20, and Register 14-85 through Register 14-91.

Other NT Port Virtual Interface Device-Specific registers are detailed in:

- Section 14.14, "NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)"
- Section 14.18, "NT Port Virtual Interface Device-Specific Registers – Link Error (Offsets FE0h – FFCh)"

Note: It is recommended that these registers not be changed from their default values.

Table 14-19. NT Port Virtual Interface Device-Specific Register Map (Offsets F34h – F8Ch)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device-Specific Registers – Read Pacing (Offsets F34h – F3Ch)				F34h … F3Ch
Device-Specific Registers – Error Reporting (Offsets F40h – F4Ch)				F40h … F4Ch
NT Port Virtual Interface Device-Specific Registers – ARI Capability (Offsets F50h – F8Ch)				F50h … F8Ch

14.16.1 NT Port Virtual Interface Device-Specific Registers – ARI Capability (Offsets F50h – F8Ch)

The Alternative Routing ID (ARI) Capability registers detailed in Section 12.16.16, "Device-Specific Registers – ARI Capability (Offsets F50h – F8Ch)," are also applicable to the NT Port Virtual Interface, except as defined in Table 14-20 (register map), and Register 14-85 through Register 14-91.

Table 14-20. NT Port Virtual Interface Device-Specific ARI Capability Register Map (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device Control 2 for Port 0		Device Capability 2 for Port 0		F50h
Device Control 2 for Port 1		Device Capability 2 for Port 1		F54h
Factory Test Only				F58h – F5Ch
Device Control 2 for Port 4		Device Capability 2 for Port 4		F60h
Device Control 2 for Port 5		Device Capability 2 for Port 5		F64h
Device Control 2 for Port 6		Device Capability 2 for Port 6		F68h
Factory Test Only				F6Ch
Device Control 2 for Port 8		Device Capability 2 for Port 8		F70h
Device Control 2 for Port 9		Device Capability 2 for Port 9		F74h
Factory Test Only				F78h – F7Ch
Reserved				F80h – F8Ch

Register 14-85. F50h Device Capability and Control 2 for Port 0 (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 0					
4:0	***Reserved***		RsvdP	No	0-0h
5	**ARI Forwarding Supported** If the NT Port is Station 0, Port 0, the NT Port Virtual Interface holds the ARI forwarding supported, to a value of 1. Otherwise, the default value is 0. 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	NT Port is Station 0, Port 0	RO	Yes	1
		Otherwise	RO	Yes	0
15:6	***Reserved***		RsvdP	No	0-0h
Device Control 2 for Port 0					
20:16	***Reserved***		RsvdP	No	0-0h
21	**ARI Forwarding Enable** 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0		RW	Yes	0
31:22	***Reserved***		RsvdP	No	0-0h

Register 14-86. F54h Device Capability and Control 2 for Port 1 (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 1					
4:0	***Reserved***		RsvdP	No	0-0h
5	**ARI Forwarding Supported** If the NT Port is Station 0, Port 0, the NT Port Virtual Interface holds the ARI forwarding supported, to a value of 1. Otherwise, the default value is 0. 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	NT Port is Station 0, Port 0	RO	Yes	1
		Otherwise	RO	Yes	0
15:6	***Reserved***		RsvdP	No	0-0h
Device Control 2 for Port 1					
20:16	***Reserved***		RsvdP	No	0-0h
21	**ARI Forwarding Enable** 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0		RW	Yes	0
31:22	***Reserved***		RsvdP	No	0-0h

Register 14-87. F60h Device Capability and Control 2 for Port 4 (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 4					
4:0	***Reserved***		RsvdP	No	0-0h
5	**ARI Forwarding Supported** If the NT Port is Station 0, Port 0, the NT Port Virtual Interface holds the ARI forwarding supported, to a value of 1. Otherwise, the default value is 0. 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	NT Port is Station 0, Port 0	RO	Yes	1
		Otherwise	RO	Yes	0
15:6	***Reserved***		RsvdP	No	0-0h
Device Control 2 for Port 4					
20:16	***Reserved***		RsvdP	No	0-0h
21	**ARI Forwarding Enable** 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0		RW	Yes	0
31:22	***Reserved***		RsvdP	No	0-0h

Register 14-88. F64h Device Capability and Control 2 for Port 5 (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 5					
4:0	***Reserved***		RsvdP	No	0-0h
5	**ARI Forwarding Supported** If the NT Port is Station 0, Port 0, the NT Port Virtual Interface holds the ARI forwarding supported, to a value of 1. Otherwise, the default value is 0. 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	NT Port is Station 0, Port 0	RO	Yes	1
		Otherwise	RO	Yes	0
15:6	***Reserved***		RsvdP	No	0-0h
Device Control 2 for Port 5					
20:16	***Reserved***		RsvdP	No	0-0h
21	**ARI Forwarding Enable** 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0		RW	Yes	0
31:22	***Reserved***		RsvdP	No	0-0h

Register 14-89. F68h Device Capability and Control 2 for Port 6 (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 6					
4:0	***Reserved***		RsvdP	No	0-0h
5	**ARI Forwarding Supported** If the NT Port is Station 0, Port 0, the NT Port Virtual Interface holds the ARI forwarding supported, to a value of 1. Otherwise, the default value is 0. 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	NT Port is Station 0, Port 0	RO	Yes	1
		Otherwise	RO	Yes	0
15:6	***Reserved***		RsvdP	No	0-0h
Device Control 2 for Port 6					
20:16	***Reserved***		RsvdP	No	0-0h
21	**ARI Forwarding Enable** 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0		RW	Yes	0
31:22	***Reserved***		RsvdP	No	0-0h

Register 14-90. F70h Device Capability and Control 2 for Port 8 (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 8					
4:0	***Reserved***		RsvdP	No	0-0h
5	**ARI Forwarding Supported** If the NT Port is Station 0, Port 0, the NT Port Virtual Interface holds the ARI forwarding supported, to a value of 1. Otherwise, the default value is 0. 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	NT Port is Station 0, Port 0	RO	Yes	1
		Otherwise	RO	Yes	0
15:6	***Reserved***		RsvdP	No	0-0h
Device Control 2 for Port 8					
20:16	***Reserved***		RsvdP	No	0-0h
21	**ARI Forwarding Enable** 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0		RW	Yes	0
31:22	***Reserved***		RsvdP	No	0-0h

Register 14-91. F74h Device Capability and Control 2 for Port 9 (Only Ports 0, 4, and 8, except if Port 0 is the NT Port, then NT Port Virtual Interface (containing the Station 0 value), and Ports 4 and 8)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Device Capability 2 for Port 9					
4:0	***Reserved***		RsvdP	No	0-0h
5	**ARI Forwarding Supported** If the NT Port is Station 0, Port 0, the NT Port Virtual Interface holds the ARI forwarding supported, to a value of 1. Otherwise, the default value is 0. 0 = ARI forwarding is not supported 1 = ARI forwarding is supported when the **Device Capability 2** register *ARI Forwarding Supported* bit (offset 8Ch[5]) is Set for this Port	NT Port is Station 0, Port 0	RO	Yes	1
		Otherwise	RO	Yes	0
15:6	***Reserved***		RsvdP	No	0-0h
Device Control 2 for Port 9					
20:16	***Reserved***		RsvdP	No	0-0h
21	**ARI Forwarding Enable** 1 = Configuration Type 1-to-Type 0 occurs, even if the Device Number is not 0		RW	Yes	0
31:22	***Reserved***		RsvdP	No	0-0h

14.17 NT Port Virtual Interface Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)

The registers detailed in Section 12.17, "Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)," are also applicable to the NT Port Virtual Interface, except for the Next Capability Offset value, as defined in Table 14-21 (register map), and Register 14-92 through Register 14-97.

Table 14-21. NT Port Virtual Interface Advanced Error Reporting Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (148h)	Capability Version (1h) / PCI Express Extended Capability ID (0001h)	FB4h
Uncorrectable Error Status		FB8h
Uncorrectable Error Mask		FBCh
Uncorrectable Error Severity		FC0h
Correctable Error Status		FC4h
Correctable Error Mask		FC8h
Advanced Error Capabilities and Control		FCCh
Header Log 0		FD0h
Header Log 1		FD4h
Header Log 2		FD8h
Header Log 3		FDCh

Register 14-92. FB4h Advanced Error Reporting Extended Capability Header

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**PCI Express Extended Capability ID**	RO	Yes	0001h
19:16	**Capability Version**	RO	Yes	1h
31:20	**Next Capability Offset** Program to 148h, which addresses the **Virtual Channel Extended Capability** structure.	RO	Yes	148h

Register 14-93. FB8h Uncorrectable Error Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
The following PCI Express errors are not valid for the NT Port Virtual Interface: • Data Link Protocol error • Surprise Down error				
3:0	***Reserved***	RsvdP	No	0h
4	**Data Link Protocol Error Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
5	**Surprise Down Error Status** ***Reserved***	RsvdP	No	0
11:6	***Reserved***	RsvdP	No	0-0h
12	**Poisoned TLP Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
13	**Flow Control Protocol Error Status** ***Reserved/Not supported***	RsvdP	No	0
14	**Completion Timeout Status** ***Not applicable to switches.***	RsvdP	No	0
15	**Completer Abort Status**	RW1CS[a]	Yes	0
16	**Unexpected Completion Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
17	**Receiver Overflow Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
18	**Malformed TLP Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
19	**ECRC Error Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
20	**Unsupported Request Error Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
31:21	***Reserved***	RsvdP	No	0-0h

*a. When the **ECC Error Check Disable** register Software Force Error Enable bit (offset 1C8h[2]) is Set, Type changes from RW1CS to RW.*

Register 14-94. FBCh Uncorrectable Error Mask (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The following PCI Express errors are not valid for the NT Port Virtual Interface: • Data Link Protocol error • Surprise Down error				
3:0	***Reserved***	RsvdP	No	0h
4	**Data Link Protocol Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	RWS	Yes	0
5	**Surprise Down Error Mask** ***Reserved***	RsvdP	No	0
11:6	***Reserved***	RsvdP	No	0-0h
12	**Poisoned TLP Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	RWS	Yes	0
13	**Flow Control Protocol Error Mask** ***Reserved/Not supported***	RsvdP	No	0
14	**Completion Timeout Mask** ***Not applicable to switches.***	RsvdP	No	0
15	**Completer Abort Mask**	RWS	Yes	0
16	**Unexpected Completion Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	RWS	Yes	0
17	**Receiver Overflow Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	RWS	Yes	0
18	**Malformed TLP Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	RWS	Yes	0
19	**ECRC Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	RWS	Yes	0
20	**Unsupported Request Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	RWS	Yes	0
31:21	***Reserved***	RsvdP	No	0-0h

Register 14-95. FC0h Uncorrectable Error Severity (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
The following PCI Express errors are not valid for the NT Port Virtual Interface: • Data Link Protocol error • Surprise Down error				
3:0	***Reserved***	RsvdP	No	0h
4	**Data Link Protocol Error Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal	RWS	Yes	1
5	**Surprise Down Error Severity** ***Reserved***	RsvdP	No	1
11:6	***Reserved***	RsvdP	No	0-0h
12	**Poisoned TLP Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal	RWS	Yes	0
13	**Flow Control Protocol Error Severity** ***Reserved/Not supported***	RsvdP	No	1
14	**Completion Timeout Severity** ***Not applicable to switches.*** Because the Status and Mask are both ***reserved*** for this bit, Severity can be ignored.	RsvdP	No	0
15	**Completer Abort Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal	RWS	Yes	0
16	**Unexpected Completion Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal	RWS	Yes	0
17	**Receiver Overflow Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal	RWS	Yes	1
18	**Malformed TLP Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal	RWS	Yes	1
19	**ECRC Error Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal	RWS	Yes	0
20	**Unsupported Request Error Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal	RWS	Yes	0
31:21	***Reserved***	RsvdP	No	0-0h

Register 14-96. FC4h Correctable Error Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
The following PCI Express errors are not valid for the NT Port Virtual Interface: • Receiver error • Bad TLP error • Bad DLLP error • Replay Number Rollover error • Replay Timer Timeout error				
0	**Receiver Error Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
5:1	***Reserved***	RsvdP	No	0-0h
6	**Bad TLP Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
7	**Bad DLLP Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
8	**REPLAY NUM Rollover Status** Replay Number Rollover status. 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
11:9	***Reserved***	RsvdP	No	000b
12	**Replay Timer Timeout Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
13	**Advisory Non-Fatal Error Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
31:14	***Reserved***	RsvdP	No	0-0h

*a. When the **ECC Error Check Disable** register Software Force Error Enable bit (offset 1C8h[2]) is Set, Type changes from RW1CS to RW.*

Register 14-97. FC8h Correctable Error Mask (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The following PCI Express errors are not valid for the NT Port Virtual Interface: • Receiver error • Bad TLP error • Bad DLLP error • Replay Number Rollover error • Replay Timer Timeout error				
0	**Receiver Error Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
5:1	***Reserved***	RsvdP	No	0-0h
6	**Bad TLP Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
7	**Bad DLLP Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
8	**REPLAY NUM Rollover Mask** Replay Number Rollover mask. 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
11:9	***Reserved***	RsvdP	No	000b
12	**Replay Timer Timeout Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
13	**Advisory Non-Fatal Error Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	1
31:14	***Reserved***	RsvdP	No	0-0h

14.18 NT Port Virtual Interface Device-Specific Registers – Link Error (Offsets FE0h – FFCh)

This section details the NT Port Virtual Interface Device-Specific Link Error registers, located at offsets FE0h through FFCh. These Device-Specific registers are unique to the NT Port Virtual Interface and not referenced in the *PCI Express Base r2.0*. Table 14-22 defines the register map used by the NT Port Virtual Interface.

Other NT Port Virtual Interface Device-Specific registers are detailed in:

- Section 14.14, "NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)"
- Section 14.16, "NT Port Virtual Interface Device-Specific Registers (Offsets F34h – F8Ch)"

Note: It is recommended that these registers not be changed from their default values.

Table 14-22. NT Port Virtual Interface Device-Specific Register Map – Link Error (Offsets FE0h – FFCh) (Port 0, when Port 0 is NT Port, Virtual Interface Only)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Link Error Status Virtual		FE0h
Link Error Mask Virtual		FE4h
Reserved		FE8h – FFCh

Register 14-98. FE0h Link Error Status Virtual (Port 0, when Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be masked by their respective* ***Link Error Mask Virtual*** *register bits (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE4h).*				
0	**Link Side Correctable Error Status** 1 = NT Port Link Interface detected a Correctable TLP error, and signaled the interrupt to the Local Host	RW1CS	Yes	0
1	**Link Side Uncorrectable Error Status** 1 = NT Port Link Interface detected an Uncorrectable TLP error, and signaled the interrupt to the Local Host	RW1CS	Yes	0
2	**Link Side DL Active Change Status** 1 = NT Port Link Interface *DL_Active* state change occurred upon detection of an NT Port Link Interface *DL_Down* state rise edge and fall edge	RW1CS	Yes	0
3	**Link Side Uncorrectable Error Message Drop Status** 1 = NT Port Link Interface received an Uncorrectable Error Message, and signaled the interrupt to the Local Host	RW1CS	Yes	0
31:4	***Reserved***	RsvdP	No	0000_000h

Register 14-99. FE4h Link Error Mask Virtual (Port 0, when Port 0 is the NT Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be used to mask their respective* ***Link Error Status Virtual*** *register bits (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE0h).*				
0	**Link Side Correctable Error Mask** 0 = No effect on reporting activity 1 = *Link Side Correctable Error Status* bit is masked/disabled	RWS	Yes	1
1	**Link Side Uncorrectable Error Mask** 0 = No effect on reporting activity 1 = *Link Side Uncorrectable Error Status* bit is masked/disabled	RWS	Yes	1
2	**Link Side DL Active Change Mask** 0 = No effect on reporting activity 1 = *Link Side DL Active Change Status* bit is masked/disabled	RWS	Yes	1
3	**Link Side Uncorrectable Error Message Drop Mask** 0 = No effect on reporting activity 1 = *Link Side Uncorrectable Error Message Drop Status* bit is masked/disabled	RWS	Yes	1
31:4	***Reserved***	RsvdP	No	0000_000h

Chapter 15 NT Port Link Interface Registers – NT Mode Only

15.1 Introduction

Note: *Check the latest design guides, application notes and errata list for Non-Transparent (NT) usage.*

The NT Port includes two sets of Configuration, Capability, Control, and Status registers, to support the Link and Virtual Interfaces. This chapter defines the PEX 8624 NT Port Link Interface registers. Other registers are defined in:

- Chapter 12, "Transparent Port Registers"
- Chapter 14, "NT Port Virtual Interface Registers – NT Mode Only"

Note: *For Chip- and Station-specific registers (those that exist only in Port 0), if Port 0 is the NT Port, then those registers exist only in the NT Port Virtual Interface.*

All PEX 8624 registers can be accessed by Configuration or Memory Requests.

For further details regarding register names and descriptions, refer to the following specifications:

- *PCI r3.0*
- *PCI Power Mgmt. r1.2*
- *PCI Express Base r2.0*

15.2 NT Port Link Interface Type 0 Register Map

Table 15-1 defines the NT Port Link Interface Type 0 register mapping.

Table 15-1. NT Port Link Interface Type 0 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
NT Port Link Interface PCI-Compatible Type 0 Configuration Header Registers (Offsets 00h – 3Ch)		00h … 3Ch
	Capability Pointer (40h)	34h
	Next Capability Pointer (48h) / Capability ID (01h)	40h
NT Port Link Interface PCI Power Management Capability Registers (Offsets 40h – 44h)		44h
	Next Capability Pointer (68h) / Capability ID (05h)	48h
NT Port Link Interface MSI Capability Registers (Offsets 48h – 64h)		… 64h
	Next Capability Pointer (A4h) / Capability ID (10h)	68h
NT Port Link Interface PCI Express Capability Registers (Offsets 68h – A0h)		… A0h
	Next Capability Pointer (C8h) / SSID/SSVID Capability ID (0Dh)	A4h
NT Port Link Interface Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – C4h)		… C4h
	Next Capability Pointer 3 (00h) / Capability ID 3 (09h)	C8h
NT Port Link Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)		… FCh
Next Capability Offset (FB4h) / 1h	PCI Express Extended Capability ID (0003h)	100h
NT Port Link Interface Device Serial Number Extended Capability Registers (Offsets 100h – 134h)		… 134h
Next Capability Offset (148h) / 1h	PCI Express Extended Capability ID (0004h)	138h
NT Port Link Interface Power Budget Extended Capability Registers (Offsets 138h – 144h)		… 144h
Next Capability Offset (950h) / 1h	PCI Express Extended Capability ID (0002h)	148h
NT Port Link Interface Virtual Channel Extended Capability Registers (Offsets 148h – 1A4h)		… 1A4h
Reserved		1A8h – 1BCh

Table 15-1. NT Port Link Interface Type 0 Register Map *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
NT Port Link Interface Device-Specific Registers (Offsets 1C0h – C88h)		1C0h …
Next Capability Offset 2 (C34h) / 1h	PCI Express Extended Capability ID 2 (000Bh)	950h
NT Port Link Interface Device-Specific Registers (Offsets 1C0h – C88h)		…
Next Capability Offset 4 (000h) / 1h	PCI Express Extended Capability ID 4 (000Bh)	C34h
NT Port Link Interface Device-Specific Registers (Offsets 1C0h – C88h)		… C88h
NT Port Link Interface NT Bridging-Specific Registers (Offsets C8Ch – EFCh)		C8Ch … EFCh
NT Port Link Interface Device-Specific Registers – Source Queue Weight (Offsets F00h – F30h)		F00h … F30h
Reserved		F34h – FB0h
Next Capability Offset (138h) / 1h	PCI Express Extended Capability ID (0001h)	FB4h
NT Port Link Interface Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)		… FDCh
Reserved		FE0h – FFCh

15.3 Register Access

The PEX 8624 NT Port Link Interface implements a 4-KB Configuration Space. The lower 256 bytes (offsets 00h through FFh) comprise the PCI-compatible Configuration Space, and the upper 960 Dwords (offsets 100h through FFFh) comprise the PCI Express Extended Configuration Space. The PEX 8624 supports three mechanisms for accessing the NT Port Link Interface registers:

- PCI Express Base r2.0 Configuration Mechanism
- Device-Specific Memory-Mapped Configuration Mechanism
- Device-Specific Cursor Mechanism

15.3.1 *PCI Express Base r2.0* Configuration Mechanism

The *PCI Express Base r2.0* Configuration mechanism is divided into two mechanisms:

- **PCI r3.0-Compatible Configuration Mechanism** – Provides Conventional PCI access to the first 256 bytes (the bytes at offsets 00h through FFh) of the NT Port Link Interface Configuration Register space
- **PCI Express Enhanced Configuration Access Mechanism** – Provides access to the entire 4-KB Configuration Space

Both are described in the sections that follow.

The PEX 8624 decodes Type 0 Configuration transactions received on its NT Port Link Interface. The PEX 8624 reads from or writes to the NT Port Link Interface register, as specified in the original Type 0 Configuration access.

15.3.1.1 *PCI r3.0*-Compatible Configuration Mechanism

The *PCI r3.0*-Compatible Configuration Space consists of the first 256 bytes of the NT Port Link Interface Configuration Space. (Refer to Figure 15-1.) The *PCI r3.0*-Compatible Configuration mechanism provides standard access to the PEX 8624 NT Port Link Interface's first 256 bytes (the bytes at offsets 00h through FFh) of the PCI Express Configuration Space.

This mechanism uses the same Request format as the PCI Express Enhanced Configuration Access Mechanism. For PCI-compatible Configuration Requests, the Extended Register Address field must be all zeros (0).

Because the mechanism is limited to the first 256 bytes of the NT Port Link Interface Configuration Register space, one of the following must be used to access beyond Byte FFh:

- PCI Express Enhanced Configuration Access Mechanism
- Device-Specific Memory-Mapped Configuration Mechanism
- Device-Specific Cursor Mechanism

15.3.1.2 PCI Express Enhanced Configuration Access Mechanism

The PCI Express Enhanced Configuration Access mechanism uses a flat, Root Complex Memory-Mapped Address space to access the device Configuration registers. In this case, the Memory address determines the Configuration register accessed, and Memory data returns the addressed register contents. The Root Complex converts the Memory transaction into a Configuration transaction before transmitting this access to the downstream devices.

This mechanism is used to access the NT Port Link Interface Type 0 registers:

- NT Port Link Interface PCI-Compatible Type 0 Configuration Header Registers (Offsets 00h – 3Ch)
- NT Port Link Interface PCI Power Management Capability Registers (Offsets 40h – 44h)
- NT Port Link Interface MSI Capability Registers (Offsets 48h – 64h)
- NT Port Link Interface PCI Express Capability Registers (Offsets 68h – A0h)
- NT Port Link Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)
- NT Port Link Interface Device Serial Number Extended Capability Registers (Offsets 100h – 134h)
- NT Port Link Interface Power Budget Extended Capability Registers (Offsets 138h – 144h)
- NT Port Link Interface Virtual Channel Extended Capability Registers (Offsets 148h – 1A4h)
- NT Port Link Interface Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)
- NT Port Link Interface Device-Specific Registers – Vendor-Specific Extended Capability 4 (Offsets C34h – C88h)
- NT Port Link Interface Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)

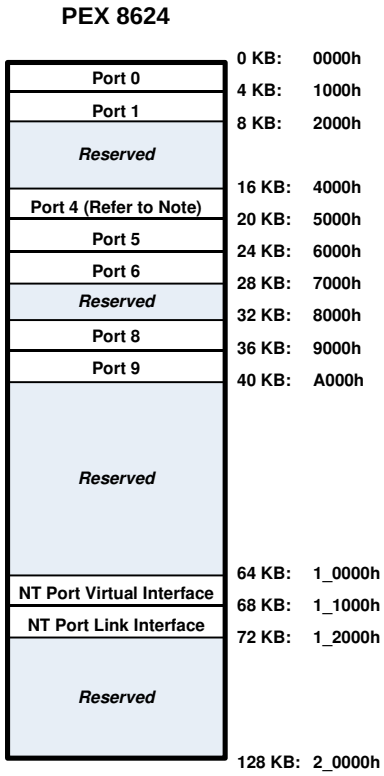
15.3.2 Device-Specific Memory-Mapped Configuration Mechanism

The Device-Specific Memory-Mapped Configuration mechanism provides a method to access the registers for all Ports within a single 128-KB Memory map, as illustrated in Figure 15-1. This Memory map is identical for Upstream Port **BAR0/1**, NT Port Virtual Interface **BAR0/1**, and NT Port Link Interface **BAR0/1**. The registers of each Port are located within a 4-KB range.

When the NT Port is enabled at Fundamental Reset, the NT Port Virtual and Link Interface registers use the *PCI r3.0* Type 0 Configuration Space Header.

To use this mechanism, use the PCI r3.0-Compatible Configuration Mechanism to program the PEX 8624 upstream Port **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively). After the PEX 8624 NT Port Link Interface Memory-Mapped register Base address is Set, the PEX 8624 Configuration Space registers are accessed, using Memory Reads and Writes to the 4-KB range, starting at offset 64 KB (1_0000h, Virtual Interface) and offset 68 KB (1_1000h, Link Interface).

Figure 15-1. NT Mode Configuration Register Mapping to Memory-Mapped BAR



Note: *Port 4 does not connect to a downstream device; therefore, no Memory nor I/O resources should be defined in Port 4 registers.*

15.3.3 Device-Specific Cursor Mechanism

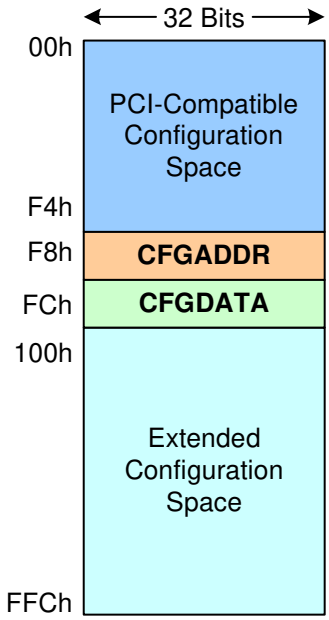
The Device-Specific Cursor mechanism is provided for use in development systems that can only generate *PCI r3.0* Configuration cycles (*that is*, the system cannot use either the Device-Specific Memory-Mapped Configuration Mechanism, nor generate Extended Configuration Requests to access the Extended Configuration Space).

In Figure 15-2, the software uses the **Configuration Address Window** (CFGADDR) register (offset F8h) to select the NT Port Link or Virtual Interface Configuration Space registers, including the PCI Express Extended Configuration Space registers (offsets 100h through FFFh).

Software uses the **Configuration Data Window** (CFGDATA) register (offset FCh) to write to or read from the selected Configuration Space registers.

Refer to Section 15.10, "NT Port Link Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)," for the register descriptions.

Figure 15-2. Configuration Space View



15.4 Register Descriptions

The remainder of this chapter details the PEX 8624 NT Port Link Interface registers, including:

- Bit/field names
- Description of register functions in the PEX 8624 NT Port Link and Virtual Interfaces
- Type (*such as* RW or HwInit; refer to Table 12-5, "Register Types, Grouped by User Accessibility," for Type descriptions)
- Whether the power-on/reset value can be modified, by way of the PEX 8624 serial EEPROM and/or I^2C Initialization feature
- Default power-on/reset value

15.5 NT Port Link Interface PCI-Compatible Type 0 Configuration Header Registers (Offsets 00h – 3Ch)

This section details the NT Port Link Interface PCI-Compatible Type 0 Configuration Header registers. Table 15-2 defines the register map.

Table 15-2. NT Port Link Interface PCI-Compatible Type 0 Configuration Header Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device ID		Vendor ID		00h
PCI Status		PCI Command		04h
PCI Class Code			PCI Revision ID	08h
PCI BIST ***(Not Supported)***	PCI Header Type	Master Latency Timer ***(Not Supported)***	Cache Line Size	0Ch
Base Address 0				10h
Base Address 1				14h
Base Address 2				18h
Base Address 3				1Ch
Base Address 4				20h
Base Address 5				24h
Reserved				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			Capability Pointer (40h)	34h
Reserved				38h
Max_Lat ***(Reserved)***	Min_Gnt ***(Reserved)***	PCI Interrupt Pin	PCI Interrupt Line	3Ch

Register 15-1. 00h PCI Configuration ID

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**Vendor ID** Identifies the device manufacturer. Defaults to the PCI-SIG-issued Vendor ID of PLX (10B5h), if not overwritten by serial EEPROM and/or I²C.	RO	Yes	10B5h
31:16	**Device ID** Identifies the particular device. Defaults to the PLX part number for the PEX 8624, if not overwritten by serial EEPROM and/or I²C.	RO	Yes	8624h

Register 15-2. 04h PCI Command/Status

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	PCI Command			
0	**I/O Access Enable** The NT Port Link Interface ignores the value of this register, because it does ***not support*** I/O resources.	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8624 ignores Memory Space Requests received on the NT Port Link Interface 1 = PEX 8624 accepts Memory Space Requests received on the NT Port Link Interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8624 forwarding of Memory Requests upstream. Does not affect Message forwarding nor Completions. 0 = PEX 8624 handles Memory Requests received on the NT Port Virtual Interface as Unsupported Requests (URs); for Non-Posted Requests, the PEX 8624 returns a Completion with UR Completion status 1 = PEX 8624 forwards Memory Requests from the NT Port Virtual Interface to the NT Port Link Interface	RW	Yes	0
3	**Special Cycle Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
4	**Memory Write and Invalidate Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
5	**VGA Palette Snoop** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
6	**Parity Error Response Enable** Controls bit 24 (*Master Data Parity Error Detected*).	RW	Yes	0
7	**IDSEL Stepping/Wait Cycle Control** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
8	**SERR# Enable** Controls bit 30 (*Signaled System Error*). 1 = Enables reporting of Fatal and Non-Fatal errors detected by the NT Port Link Interface to the Root Complex	RW	Yes	0
9	**Fast Back-to-Back Transactions Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
10	**Interrupt Disable** 0 = NT Port Link Interface is enabled to generate INT*x* Interrupt Messages 1 = NT Port Link Interface is prevented from generating INT*x* Interrupt Messages	RW	Yes	0
15:11	***Reserved***	RsvdP	No	00h

Register 15-2. 04h PCI Command/Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	PCI Status			
18:16	***Reserved***	RsvdP	No	000b
19	**Interrupt Status** 0 = No INT*x* interrupt is pending 1 = INT*x* interrupt is pending internally to the NT Port Link Interface –or– PEX_INTA# (if enabled) is asserted	RO	No	0
20	**Capability List** Capability function is supported. Set, as required by the *PCI Express Base r2.0*.	RO	Yes	1
21	**66 MHz Capable** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
22	***Reserved***	RsvdP	No	0
23	**Fast Back-to-Back Transactions Capable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
24	**Master Data Parity Error Detected** If bit 6 (*Parity Error Response Enable*) is Set, the NT Port Link Interface Sets this bit when the NT Port: • Forwards the poisoned Transaction Layer Packet (TLP) Write Request from the NT Port Virtual Interface to the NT Port Link Interface, –or– • Receives a Completion marked as poisoned on the NT Port Link Interface If the *Parity Error Response Enable* bit is Cleared, the PEX 8624 never Sets this bit. This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	**DEVSEL# Timing** ***Not supported*** Always Cleared.	RsvdP	No	00b
27	**Signaled Target Abort** The NT Port Link Interface Sets this bit if any of the following conditions exist: • NT Port Link Interface receives a Completion (from the Local Host) that has a Completion status of Completer Abort (CA), –or– • NT Port Link Interface receives a Memory Request targeting a PEX 8624 register, and the Payload Length (indicated within the Memory Request Header) is greater than 1 DWord • NT Port Link Interface receives a Memory Request targeting a PEX 8624 register address within a non-existent Port • NT Port Link Interface receives a Memory Write Request targeting enabled Expansion ROM Address space (Expansion ROM Base Address Register (BAR), offset 30h) ***Note:*** *When Set during a forwarded Completion, the* ***Uncorrectable Error Status*** *register Completer Abort Status bit (offset FB8h[15]) is not updated, because the NT Port does not log the corresponding Requests that it forwards.*	RW1C	Yes	0

Register 15-2. 04h PCI Command/Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
28	**Received Target Abort** Defaults to 0, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
29	**Received Master Abort** Defaults to 0, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
30	**Signaled System Error** If bit 8 (*SERR# Enable*) is Set, the NT Port Link Interface Sets this bit when transmitting an ERR_FATAL or ERR_NONFATAL Message to its upstream device. This error is natively reported by the **Device Status** register *Fatal Error Detected* and *Non-Fatal Error Detected* bits (offset 70h[18:17], respectively), which are mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
31	**Detected Parity Error** The NT Port Link Interface Sets this bit when receiving a Poisoned TLP, regardless of the bit 6 (*Parity Error Response Enable*) state. This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0

Register 15-3. 08h PCI Class Code and Revision ID

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	PCI Revision ID			
7:0	**Revision ID** Unless overwritten by the serial EEPROM, returns the Silicon Revision (AAh, ABh, or BBh), the PLX-assigned Revision ID for this version of the PEX 8624. The PEX 8624 Serial EEPROM register Initialization capability is used to replace the PLX Revision ID with another Revision ID.	RO	Yes	AAh, ABh, or BBh
	PCI Class Code			**068000h**
15:8	**Register-Level Programming Interface** Cleared, as required by the *PCI r3.0* for other bridge devices.	RO	Yes	00h
23:16	**Sub-Class Code** Other bridge devices.	RO	Yes	80h
31:24	**Base Class Code** Bridge devices.	RO	Yes	06h

Register 15-4. 0Ch Miscellaneous Control

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Cache Line Size				
7:0	**Cache Line Size** System Cache Line Size. Implemented as a RW field for Conventional PCI compatibility purposes and does not impact PEX 8624 functionality.	RW	Yes	00h
Master Latency Timer				
15:8	**Master Latency Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	00h
PCI Header Type				
22:16	**Configuration Layout Type** Type 0 Configuration Header for the NT Port.	RO	Yes	00h
23	**Multi-Function Device** 0 = Single-function device 1 = Indicates multiple (up to eight) functions (logical devices), each containing its own, individually addressable Configuration Space, 256 DWords in size	RO	Yes	0
PCI BIST				
31:24	**PCI BIST** ***Not supported*** Built-In Self-Test (BIST) Pass or Fail.	RsvdP	No	00h

Register 15-5. 10h Base Address 0 (NT Port Link Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *By default, NT Port Link Interface **BAR0** is enabled and **BAR1** is disabled, to provide a 32-bit **BAR0** for register access. **BAR1** can be enabled (by serial EEPROM or I²C), to provide a 64-bit **BAR0/1**, by programming the **NT Port Link Interface BAR0/1 Setup** register BAR0/1 Enable field (NT Port Link Interface, offset E4h[1:0]) to 11b (which enables both **BAR0** and **BAR1**).*				
0	**Memory Space Indicator** When enabled, the Base Address register maps PEX 8624 Port Configuration registers into Memory space. ***Note:*** *Hardwired to 0.*	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Base Address register maps the PEX 8624 Port Configuration registers into Non-Prefetchable Memory space	RO	Yes	0
16:4	***Reserved***	RsvdP	No	0-0h
31:17	**Base Address 0** 128-KB-aligned Base address used for Memory-Mapped access to the 128-KB block of all PEX 8624 registers (4 KB, per Port).	RW	Yes	0-0h

Register 15-6. 14h Base Address 1 (NT Port Link Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Upper 32-Bit Address for Memory-Mapped BAR** For 64-bit addressing (**BAR0/1**), Base Address 1 (**BAR1**) extends Base Address 0 (**BAR0**) to provide the upper 32 Address bits when the **Base Address 0** register *Memory Map Type* field (offset 10h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Read-Only when the **Base Address 0** (**BAR0**) register is not enabled as a 64-bit BAR (*Memory Map Type* field (offset 10h[2:1]) is not programmed to 10b).	RO	Yes	0000_0000h

Register 15-7. 18h Base Address 2 (NT Port Link Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Memory Space Indicator** 0 = Implemented as a Memory BAR	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
19:4	***Reserved***	RsvdP	No	0_000h
31:20	**Base Address 2**	RW	Yes	000h

Register 15-8. 1Ch Base Address 3 (NT Port Link Interface Memory Space)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *This register has RW privilege if* ***BAR2/3*** *is configured as a 64-bit BAR (**Base Address 2** register Memory Map Type field (NT Port Link Interface, offset 18h[2:1]), is programmed to 10b).*					
0	**Memory Space Indicator** **BAR3** can be used as an independent 32-bit only BAR, or as the upper 32 bits of 64-bit **BAR2/3**. 0 = Implemented as a Memory BAR in 32-Bit mode	Offset 18h[2:1]=00b	RsvdP	No	0
		Offset 18h[2:1]=10b	RW	Yes	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space All other encodings are ***reserved***.	Offset 18h[2:1]=00b	RsvdP	No	00b
		Offset 18h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset 18h[2:1]=00b	RsvdP	No	0
		Offset 18h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset 18h[2:1]=00b	RsvdP	No	0_000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset 18h[2:1]=10b	RW	Yes	0_000h
31:20	**Base Address 3**		RW	Yes	000h

Register 15-9. 20h Base Address 4 (NT Port Link Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Memory Space Indicator** 0 = Implemented as a Memory BAR; otherwise, ***reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
19:4	***Reserved***	RsvdP	No	0_000h
31:20	**Base Address 4**	RW	Yes	000h

Register 15-10. 24h Base Address 5 (NT Port Link Interface Memory Space)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *This register has RW privilege if* ***BAR4/5*** *is configured as a 64-bit BAR (****Base Address 4*** *register Memory Map Type field (NT Port Link Interface, offset 20h[2:1]), is programmed to 10b).*					
0	**Memory Space Indicator** **BAR5** can be used as an independent 32-bit only BAR, or as the upper 32 bits of 64-bit **BAR4/5**. 0 = Implemented as a Memory BAR in 32-Bit mode	Offset 20h[2:1]=00b	RsvdP	No	0
		Offset 20h[2:1]=10b	RW	Yes	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space All other encodings are ***reserved***.	Offset 20h[2:1]=00b	RsvdP	No	00b
		Offset 20h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset 20h[2:1]=00b	RsvdP	No	0
		Offset 20h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset 20h[2:1]=00b	RsvdP	No	0_000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset 20h[2:1]=10b	RW	Yes	0_000h
31:20	**Base Address 5**		RW	Yes	000h

Register 15-11. 2Ch Subsystem ID and Subsystem Vendor ID

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Subsystem Vendor ID				
15:0	**Subsystem Vendor ID** Identifies the device manufacturer. Defaults to the PCI-SIG-issued Vendor ID of PLX (10B5h), if not overwritten by serial EEPROM and/or I²C.	RO	Yes	10B5h
Subsystem ID				
31:16	**Subsystem ID** Identifies the particular device. Defaults to the PLX part number for the PEX 8624, if not overwritten by serial EEPROM and/or I²C.	RO	Yes	8624h

Register 15-12. 30h Expansion ROM Base Address

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *Expansion ROM can be enabled in either the NT Port Link or Virtual Interface, but not both simultaneously. Expansion ROM is enabled, by default, in the NT Port Link Interface (**Ingress Control** register Expansion ROM Virtual Side bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 660h[23]) is Cleared).*					
0	**Expansion ROM Enable** 0 = NT Port Link Interface Expansion ROM is disabled	NT Port Virtual Interface, offset 30h[0]=1	RsvdP	No	0
	1 = NT Port Link Interface Expansion ROM is enabled, and NT Port Virtual Interface Expansion ROM is disabled	NT Port Virtual Interface, offset 30h[0]=0	RO	Yes	0
		NT Port Virtual Interface, offset 30h[0]=1	RsvdP	No	0
13:1	***Reserved***		RsvdP	No	0-0h
31:14	**Expansion ROM Base Address** If the **Serial EEPROM Clock Frequency** register *Expansion ROM Size* bit (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 268h[16]) value is 0, the Expansion ROM size is 16 KB (default value is FFFF_C001h). Bit 14 is RW. If the *Expansion ROM Size* bit value is 1, the Expansion ROM size is 32 KB (default value is FFFF_8001h). Bit 14 is RO.	When Bit 0 = 0	RsvdP	No	0-0h
		When Bit 0 = 1	RW	Yes	0-0h

Register 15-13. 34h Capability Pointer

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Capability Pointer** Default 40h points to the **PCI Power Management Capability** structure.	RO	Yes	40h
31:8	***Reserved***	RsvdP	No	0000_00h

Register 15-14. 3Ch PCI Interrupt

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**PCI Interrupt Line** The Interrupt Line Routing Value communicates interrupt line routing information. Values in this register are programmed by system software and are system architecture-specific. The value is used by device drivers and operating systems.	RW	Yes	00h
15:8	**PCI Interrupt Pin** Identifies the Conventional PCI Interrupt Message(s) the device (or device function) uses. Only value 00h or 01h is allowed in the PEX 8624. 00h = Indicates that the device does not use Conventional PCI Interrupt Message(s) 01h, 02h, 03h, and 04h = Maps to Conventional PCI Interrupt Messages for INTA#, INTB#, INTC#, and INTD#, respectively	RO	Yes	01h
23:16	**Min_Gnt** Minimum Grant. ***Reserved*** Does not apply to PCI Express.	RsvdP	No	00h
31:24	**Max_Lat** Maximum Latency. ***Reserved*** Does not apply to PCI Express.	RsvdP	No	00h

15.6 NT Port Link Interface PCI Power Management Capability Registers (Offsets 40h – 44h)

This section details the NT Port Link Interface PCI Power Management Capability registers. Table 15-3 defines the register map.

Table 15-3. NT Port Link Interface PCI Power Management Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Power Management Capability		Next Capability Pointer (48h)	Capability ID (01h)	40h
PCI Power Management Data	PCI Power Management Control/Status Bridge Extensions ***(Reserved)***	PCI Power Management Status and Control		44h

Register 15-15. 40h PCI Power Management Capability

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Capability ID** Default = 01h – only value allowed.	RO	Yes	01h
15:8	**Next Capability Pointer** Default 48h points to the **MSI Capability** structure.	RO	Yes	48h
18:16	**Version** Default = 011b – only value allowed.	RO	Yes	011b
19	**PME Clock** Power Management Event (PME) clock. Does not apply to PCI Express. Returns 0.	RsvdP	No	0
20	***Reserved***	RsvdP	No	0
21	**Device-Specific Initialization** Default 0 indicates that Device-Specific Initialization is ***not*** required.	RO	Yes	0
24:22	**AUX Current** The PEX 8624 does ***not support*** PME generation from the D3cold Device Power Management (PM) state; therefore, the serial EEPROM value for this field should be 000b.	RO	Yes	000b
25	**D1 Support** ***Not supported*** Default value of 0 indicates that the PEX 8624 does ***not support*** the D1 Device PM state.	RsvdP	No	0
26	**D2 Support** ***Not supported*** Default value of 0 indicates that the PEX 8624 does ***not support*** the D2 Device PM state.	RsvdP	No	0
31:27	**PME Support** The default value is applied to bits [31, 30, and 27] only. PME Messages are disabled, by default.	RO	Yes	0000_0b

Register 15-16. 44h PCI Power Management Status and Control

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
PCI Power Management Status and Control				
1:0	**Power State** Used to determine the Port's current Device PM state, and to Set the Port into a new Device PM state. 00b = D0 01b = D1 – ***Not supported*** 10b = D2 – ***Not supported*** 11b = D3hot If software attempts to write an unsupported state to this field, the Write operation completes normally; however, the data is discarded and no state change occurs.	RW	Yes	00b
2	***Reserved***	RsvdP	No	0
3	**No Soft Reset** 1 = Devices transitioning from the D3hot to D0 Device PM state, because of Power State commands, do not perform an internal reset	RO	Yes	1
7:4	***Reserved***	RsvdP	No	0h
8	**PME Enable** Default value of 0 indicates that PME generation is disabled.	RsvdP	No	0
12:9	**Data Select** Initially writable by serial EEPROM and/or I^2C only[a]. This Configuration Space register (CSR) access privilege changes to RW after a Serial EEPROM or I^2C Write occurs to this register. Selects the **Data** and **Data Scale** registers (fields [31:24 and 14:13], respectively). 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated All other encodings are ***reserved***.	RO	Yes	0h
14:13	**Data Scale** Writable by serial EEPROM and/or I^2C only[a]. Indicates the scaling factor to be used when interpreting the **Data** register value. The value and meaning of this field varies, depending upon which data value is selected by field [12:9] (*Data Select*). There are four internal **Data Scale** registers (one each, per *Data Select* values 0h, 3h, 4h, and 7h). For other *Data Select* values, the **Data Scale** value returned is 0h.	RO	Yes	00b
15	**PME Status** 0 = PME is not being generated by the NT Port	RsvdP	No	0

Register 15-16. 44h PCI Power Management Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
PCI Power Management Control/Status Bridge Extensions				
21:16	***Reserved***	RsvdP	No	0-0h
22	**B2/B3 Support** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
23	**Bus Power/Clock Control Enable** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
PCI Power Management Data				
31:24	**Data** Writable by serial EEPROM and/or I²C only[a]. There are four supported *Data Select* values (0h, 3h, 4h, and 7h). For other *Data Select* values, the **Data Scale** value returned is 0h. Selected by field [12:9] (*Data Select*).	RO	Yes	00h

*a. With no serial EEPROM nor previous I²C programming, Reads return 00h for the **Data** and **Data Scale** registers (for all Data Selects).*

15.7 NT Port Link Interface MSI Capability Registers (Offsets 48h – 64h)

The registers detailed in Section 12.8, "MSI Capability Registers (Offsets 48h – 64h)," are also applicable to the NT Port Link Interface, except as defined in Table 15-4 (register map), and Register 15-17 through Register 15-19.

Table 15-4. NT Port Link Interface MSI Capability Register Map[a]

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
MSI Control		Next Capability Pointer (68h)	Capability ID (05h)	48h
MSI Address				4Ch
MSI Upper Address				50h
Reserved		MSI Data		54h
MSI Mask				58h
MSI Status				5Ch
Reserved				60h – 64h

*a. Offsets 54h, 58h, and 5Ch change to 50h, 54h, and 58h, respectively, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.*

Register 15-17. 48h MSI Capability

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
MSI Capability Header				
7:0	**Capability ID** Program to 05h, as required by the *PCI r3.0*.	RO	Yes	05h
15:8	**Next Capability Pointer** Program to 68h, to point to the **PCI Express Capability** structure.	RO	Yes	68h
MSI Control				
16	**MSI Enable** 0 = MSIs for the NT Port Link Interface are disabled 1 = MSIs for the NT Port Link Interface are enabled, and INT*x* Interrupt Messages and PEX_INTA# output assertion are disabled	RW	Yes	0
19:17	**Multiple Message Capable** 000b = NT Port Link Interface can request only one Vector 001b through 111b = NT Port Link Interface can request two Vectors	RO	Yes	001b
22:20	**Multiple Message Enable** 000b = NT Port Link Interface is allocated one Vector, by default 001b through 111b = NT Port Link Interface is allocated two Vectors ***Note:*** *This field should not be programmed with a value larger than that of field [19:17] (Multiple Message Capable). If the value of this field is larger than that of field [19:17], the Multiple Message Capable value takes effect.*	RW	Yes	000b
23	**MSI 64-Bit Address Capable** 0 = PEX 8624 is capable of generating MSI 32-bit addresses (**MSI Address** register, offset 4Ch, is the Message address) 1 = PEX 8624 is capable of generating MSI 64-bit addresses (**MSI Address** register, offset 4Ch, is the lower 32 bits of the Message address, and **MSI Upper Address** register, offset 50h, is the upper 32 bits of the Message address)	RO	Yes	1
24	**Per Vector Masking Capable** 0 = PEX 8624 does not have Per Vector Masking capability 1 = PEX 8624 has Per Vector Masking capability	RO	Yes	1
31:25	***Reserved***	RsvdP	No	0-0h

Register 15-18. 58h MSI Mask

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
The interrupt sources in the NT Port Link Interface are grouped into two categories – Power Management/Link State events and NT-Link Doorbell-generated interrupts. The number of allocated MSI Vectors is determined by the **MSI Control** register *Multiple Message Capable* and *Multiple Message Enable* fields (offset 48h[19:17 and 22:20], respectively). When the number of MSI Vectors that can be requested is: • **Two** – Both interrupt categories generate their own MSI Vector • **One** – Both interrupt categories generate the same MSI Vector ***Note:*** *The offset for this register changes from 58h, to 54h, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.* *The bits in this register can be used to mask their respective **MSI Status** register bits (offset 5Ch).*					
0	**MSI Mask for Link State Events** MSI mask for Power Management event- or Link State event-generated interrupts.	Offset 48h[22:20]≥001b	RW	Yes	0
	MSI Mask for Shared Interrupt Sources MSI mask for both interrupt sources when the **MSI Control** register *Multiple Message Enable* field indicates that the Host has allocated one Vector.	Offset 48h[22:20]=000b	RsvdP	No	0
2:1	***Reserved***		RsvdP	No	00b
3	**MSI Mask for NT-Link Doorbell-Generated Interrupts** Refer to the NT Port registers located at offsets C5Ch through C68h.	Offset 48h[22:20]≥001b	RW	Yes	0
	Reserved	Offset 48h[22:20]=000b	RsvdP	No	0
31:4	***Reserved***		RsvdP	No	0000_000h

Register 15-19. 5Ch MSI Status

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
The interrupt sources in the NT Port Link Interface are grouped into two categories – Power Management/Link State events and NT-Link Doorbell-generated interrupts. The number of allocated MSI Vectors is determined by the **MSI Control** register *Multiple Message Capable* and *Multiple Message Enable* fields (offset 48h[19:17 and 22:20], respectively). When the number of MSI Vectors that can be requested is: • **Two** – Both interrupt categories generate their own MSI Vector • **One** – Both interrupt categories generate the same MSI Vector ***Note:*** *The offset for this register changes from 58h, to 54h, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.* *The bits in this register can be masked by their respective **MSI Mask** register bits (offset 58h).*					
0	**MSI Pending Status for Link State Events** MSI pending status for Power Management event- or Link State event-generated interrupts.	Offset 48h[22:20]≥001b	RO	Yes	0
	MSI Pending Status for Shared Interrupt Sources MSI pending status for both interrupt sources when the **MSI Control** register *Multiple Message Enable* field indicates that the Host has allocated one Vector.	Offset 48h[22:20]=000b	RsvdP	No	0
2:1	***Reserved***		RsvdP	No	00b
3	**MSI Pending Status for NT-Link Doorbell-Generated Interrupts** Refer to the NT Port registers located at offsets C5Ch through C68h.	Offset 48h[22:20]≥001b	RO	Yes	0
	Reserved	Offset 48h[22:20]=000b	RsvdP	No	0
31:4	***Reserved***		RsvdP	No	0000_000h

15.8 NT Port Link Interface PCI Express Capability Registers (Offsets 68h – A0h)

The registers detailed in Section 12.9, "PCI Express Capability Registers (Offsets 68h – A0h)," are also applicable to the NT Port Link Interface, except as defined in Table 15-5 (register map; offsets 7Ch and 80h are ***reserved***), and Register 15-20 through Register 15-25.

Table 15-5. NT Port Link Interface PCI Express Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Express Capability		Next Capability Pointer (A4h)	Capability ID (10h)	68h
Device Capability				6Ch
Device Status		***Not Supported/Reserved***	Device Control	70h
Link Capability				74h
Link Status		***Reserved***	Link Control	78h
Reserved				7Ch – 88h
Device Capability 2				8Ch
Device Status 2 ***(Reserved)***		Device Control 2		90h
Reserved				94h
Link Status 2		Link Control 2		98h
Reserved				9Ch – A0h

Register 15-20. 68h PCI Express Capability List and Capability

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
PCI Express Capability List				
7:0	**Capability ID** Program to 10h, by default.	RO	Yes	10h
15:8	**Next Capability Pointer** Program to A4h, to point to the **Subsystem Capability** structure.	RO	Yes	A4h
PCI Express Capability				
19:16	**Capability Version** The PEX 8624 NT Port Link Interface programs this field to 2h, as required by the *PCI Express Base r2.0*.	RO	Yes	2h
23:20	**Device/Port Type** Default = PCI Express endpoint device.	RO	No	0h
24	**Slot Implemented** ***Not valid for PCI Express endpoint devices***	RsvdP	No	0
29:25	**Interrupt Message Number** The serial EEPROM writes 00_000b, because the Base Message and MSI Messages are the same.	RO	Yes	00_000b
31:30	***Reserved***	RsvdP	No	00b

Register 15-21. 6Ch Device Capability

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
2:0	**Maximum Payload Size Supported** The Maximum Payload Size for the NT Port Link Interface is 2,048 bytes. 000b = NT Port Link Interface supports a 128-byte maximum payload 001b = NT Port Link Interface supports a 256-byte maximum payload 010b = NT Port Link Interface supports a 512-byte maximum payload 011b = NT Port Link Interface supports a 1,024-byte maximum payload 100b = NT Port Link Interface supports a 2,048-byte maximum payload No other encodings are supported.	HwInit	Yes	100b
4:3	**Phantom Functions Supported** ***Not supported***	RO	Yes	00b
5	**Extended Tag Field Supported** 0 = Maximum *Tag* field is 5 bits 1 = Maximum *Tag* field is 8 bits	RO	Yes	0
8:6	**Endpoint L0s Acceptable Latency** 111b = No Limit	RO	Yes	111b
11:9	**Endpoint L1 Acceptable Latency** 111b = No Limit	RO	Yes	111b
14:12	***Reserved***	RsvdP	No	000b
15	**Role-Based Error Reporting**	RO	Yes	1
17:16	***Reserved***	RsvdP	No	00b
25:18	**Captured Slot Power Limit Value** For the NT Port Link Interface, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [27:26] (*Captured Slot Power Limit Scale*).	RO	Yes	00h
27:26	**Captured Slot Power Limit Scale** For the NT Port Link Interface, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [25:18] (*Captured Slot Power Limit Value*). 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001	RO	Yes	00b
31:28	***Reserved***	RsvdP	No	0h

Register 15-22. 70h Device Status and Control

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	Device Control			
0	**Correctable Error Reporting Enable** 0 = Disables 1 = Enables the NT Port Link Interface to report Correctable errors to the System Host	RW	Yes	0
1	**Non-Fatal Error Reporting Enable** 0 = Disables 1 = Enables the NT Port Link Interface to report Non-Fatal errors to the System Host	RW	Yes	0
2	**Fatal Error Reporting Enable** 0 = Disables 1 = Enables the NT Port Link Interface to report Fatal errors to the System Host	RW	Yes	0
3	**Unsupported Request Reporting Enable** 0 = Disables 1 = Enables the NT Port Link Interface to report UR errors as Error Messages with a programmed uncorrectable error severity	RW	Yes	0
4	**Enable Relaxed Ordering** ***Not supported***	RsvdP	No	0
7:5	**Maximum Payload Size** The NT Port Link Interface power-on/reset value is 000b, to support a Maximum Payload Size of 128 bytes. Software can change this field to configure the NT Port Link Interface to support other Payload sizes; however, software cannot change this field to a value larger than that indicated by the **Device Capability** register *Maximum Payload Size Supported* field (offset 6Ch[2:0]), for the NT Port Virtual and Link Interfaces. (Requester and Completer domains must possess the same Maximum Payload Size.) 000b = NT Port Link Interface supports a 128-byte maximum payload 001b = NT Port Link Interface supports a 256-byte maximum payload 010b = NT Port Link Interface supports a 512-byte maximum payload 011b = NT Port Link Interface supports a 1,024-byte maximum payload 100b = NT Port Link Interface supports a 2,048-byte maximum payload No other encodings are supported. ***Note:*** *Software must halt all transactions through the NT Port before changing this field.*	RW	Yes	000b
8	**Extended Tag Field Enable** ***Not supported***	RsvdP	No	0
9	**Phantom Functions Enable** ***Not supported***	RsvdP	No	0
10	**AUX Power PM Enable** ***Not supported***	RsvdP	No	0
11	**Enable No Snoop** ***Not supported***	RsvdP	No	0
14:12	**Maximum Read Request Size** ***Not supported***	RsvdP	No	000b
15	***Reserved***	RsvdP	No	0

Register 15-22. 70h Device Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	Device Status			
16	**Correctable Error Detected** Set when the NT Port Link Interface detects a Correctable error, regardless of the bit 0 (*Correctable Error Reporting Enable*) state. 0 = NT Port Link Interface did not detect a Correctable error 1 = NT Port Link Interface detected a Correctable error	RW1C	Yes	0
17	**Non-Fatal Error Detected** Set when the NT Port Link Interface detects a Non-Fatal error, regardless of the bit 1 (*Non-Fatal Error Reporting Enable*) state. 0 = NT Port Link Interface did not detect a Non-Fatal error 1 = NT Port Link Interface detected a Non-Fatal error	RW1C	Yes	0
18	**Fatal Error Detected** Set when the NT Port Link Interface detects a Fatal error, regardless of the bit 2 (*Fatal Error Reporting Enable*) state. 0 = NT Port Link Interface did not detect a Fatal error 1 = NT Port Link Interface detected a Fatal error	RW1C	Yes	0
19	**Unsupported Request Detected** Set when the NT Port Link Interface detects a UR, regardless of the bit 3 (*Unsupported Request Reporting Enable*) state. 0 = NT Port Link Interface did not detect a UR 1 = NT Port Link Interface detected a UR	RW1C	Yes	0
20	**AUX Power Detected** ***Not supported*** Initially Cleared.	RsvdP	No	0
21	**Transactions Pending** ***Not supported*** Because the PEX 8624 NT Port is a bridging device, it does not track Completion for the corresponding Non-Posted transactions. Therefore, the NT Port Link Interface does not implement Transactions Pending.	RsvdP	No	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 15-23. 74h Link Capability

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
3:0	**Supported Link Speeds** Indicates the NT Port Link Interface's supported Link speed. 0001b = 2.5 GT/s Link speed is supported 0010b = 5.0 GT/s and 2.5 GT/s Link speeds are supported All other encodings are ***reserved***.	RO	Yes	0010b (STRAP_RESERVED17#=H) 0001b (STRAP_RESERVED17#=L)
9:4	**Maximum Link Width** The PEX 8624 maximum Link width is x8 = 00_1000b. Actual maximum Link width is Set by the STRAP_STN*x*_PORTCFG*x* inputs. 00_0000b = ***Reserved*** 00_0001b = x1 00_0010b = x2 00_0100b = x4 00_1000b = x8 All other encodings are ***not supported***.	ROS	No	Set by STRAP_STN*x*_PORTCFG*x* input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station x* bits (Port 0, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 574h[5:0])
11:10	**Active State Power Management (ASPM) Support** Active State Link PM support. Indicates the level of ASPM supported by the Port. 01b = L0s Link PM state entry is supported All other encodings are ***reserved***.	RO	Yes	01b

Register 15-23. 74h Link Capability *(Cont.)*

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td>14:12</td><td>L0s Exit Latency
Indicates the L0s Link PM state exit latency for the given PCI Express Link. Value depends upon the Physical Layer Command and Status register N_FTS Value field (NT Port Virtual Interface, offset 220h[15:8]) value and Link speed. Exit latency is calculated, as follows:
• 2.5 GHz – Multiply N_FTS Value x 4 (4 symbol times in 1 N_FTS) x 4 ns (1 symbol time at 2.5 GT/s)
• 5.0 GHz – Multiply N_FTS Value x 4 (4 symbol times in 1 N_FTS) x 2 ns (1 symbol time at 5.0 GT/s)
100b = NT Port Link Interface L0s Link PM state Exit Latency is 512 ns to less than 1 s at 5.0 GT/s
101b = NT Port Link Interface L0s Link PM state Exit Latency is 1 s to less than 2 s at 2.5 GT/s
All other encodings are reserved.</td><td>RO</td><td>No</td><td>100b (5.0 GT/s)
101b (2.5 GT/s)</td></tr>
<tr><td>17:15</td><td>L1 Exit Latency
Indicates the L1 Link PM state exit latency for the given PCI Express Link. Value depends upon the Link speed.
001b = NT Port Link Interface L1 Link PM state Exit Latency is 1 s to less than 2 s at 5.0 GT/s
010b = NT Port Link Interface L1 Link PM state Exit Latency is 2 s to less than 4 s at 2.5 GT/s
All other encodings are reserved.</td><td>RO</td><td>Yes</td><td>001b (5.0 GT/s)
010b (2.5 GT/s)</td></tr>
<tr><td>18</td><td>Clock Power Management</td><td>RO</td><td>Yes</td><td>0</td></tr>
<tr><td>23:19</td><td>Reserved</td><td>RsvdP</td><td>No</td><td>0-0h</td></tr>
<tr><td>31:24</td><td>Port Number
The NT Port Number value is limited to the Station 0 Ports, and is selected by the STRAP_NT_UPSTRM_PORTSEL[1:0] Strapping inputs. All other encodings are reserved.
<table>
<tr><th>Register Value</th><th>Strapping Input Value</th><th>Port Number</th></tr>
<tr><td>00h</td><td>00b (LL)</td><td>0</td></tr>
<tr><td>01h</td><td>01b (LH)</td><td>1</td></tr>
</table></td><td>ROS</td><td>No</td><td>Set by STRAP_NT_UPSTRM_PORTSEL[1:0] input levels</td></tr>
</table>

Register 15-24. 78h Link Status and Control

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	Link Control			
1:0	**Active State Power Management (ASPM) Control** 00b = Disable[a] 01b = Enables only L0s Link PM state Entry 10b = Enables only L1 Link PM state Entry 11b = Enables both L0s and L1 Link PM state Entries	RW	Yes	00b
2	***Reserved***	RsvdP	No	0
3	**Read Request Return Parameter Control** Read Request Return Parameter "R" control. Read Completion Boundary (RCB). Cleared.	RO	Yes	0
4	**Link Disable** ***Reserved*** for the NT Port Link Interface.	RsvdP	No	0
5	**Retrain Link** ***Reserved*** for the NT Port Link Interface. Always read as 0.	RsvdP	No	0
6	**Common Clock Configuration** 0 = NT Port Link Interface and the device at the opposite end of the PCI Express Link use an asynchronous Reference Clock source 1 = NT Port Link Interface and the device at the opposite end of the PCI Express Link use a common (synchronous) Reference Clock source (constant phase relationship)	RW	Yes	0
7	**Extended Sync** 1 = Causes the NT Port Link Interface to transmit: • 4,096 FTS Ordered-Sets in the L0s Link PM state, • Followed by a single SKIP Ordered-Set prior to entering the L0 Link PM state, • Finally, transmission of 1,024 TS1 Ordered-Sets in the *Recovery* state.	RW	Yes	0
15:8	***Reserved***	RsvdP	No	00h

Register 15-24. 78h Link Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	Link Status			
19:16	**Current Link Speed** Indicates the negotiated Link speed of the Port's PCI Express Link. 0001b = 2.5 GT/s Link speed 0010b = 5.0 GT/s Link speed All other encodings are ***reserved***. The value in this field is undefined when the Link is not up.	RO	No	0001b
25:20	**Negotiated Link Width** Dependent upon the configuration of the physical Ports. Link width is determined by the negotiated value with the attached Lane/Port. 00_0000b = Link is down (default) 00_0001b = x1 or Port is in the *DL_Down* state 00_0010b = x2 00_0100b = x4 00_1000b = x8 All other encodings are ***not supported***.	RO	No	00_0000b
26	***Reserved***	RsvdP	No	0
27	**Link Training** ***Reserved*** for the NT Port Link Interface.	RsvdP	No	0
28	**Slot Clock Configuration** Set by the upstream Port or NT Port Link Interface, but not both. 0 = Indicates that the PEX 8624 uses an independent clock 1 = Indicates that the PEX 8624 uses the same physical Reference Clock that the platform provides on the connector	HwInit	Yes	0
31:29	***Reserved***	RsvdP	No	000b

a. The Port Receiver must be capable of entering the L0s Link PM state, regardless of whether the state is disabled.

Register 15-25. 98h Link Status and Control 2

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Link Control 2				
3:0	**Target Link Speed** 0001b = 2.5 GT/s Link speed supported 0010b = 5.0 GT/s Link speed supported All other encodings are ***reserved***.	RWS	Yes	0010b
4	**Enter Compliance**	RWS	Yes	0
5	**Hardware Autonomous Speed Disable** ***Reserved*** Initial transition to the highest supported common Link speed is not blocked by this bit.	RsvdP	No	0
6	**Selectable De-Emphasis** ***Reserved***	RsvdP	Yes	0
9:7	**Transmit Margin** Intended for debug and compliance testing only.	RWS	Yes	000b
10	**Enter Modified Compliance** Intended for debug and compliance testing only.	RWS	Yes	0
11	**Compliance SOS** 1 = Link Training and Status State Machine (LTSSM) must periodically send SKIP Ordered-Sets between sequences when sending the Compliance Pattern or Modified Compliance Pattern	RWS	Yes	0
12	**Compliance De-Emphasis** Sets the de-emphasis level in the *Polling.Compliance* state, if the entry occurred due to bit 4 (*Enter Compliance*) being Set.	RWS	Yes	0
15:13	***Reserved***	RsvdP	No	000b
Link Status 2				
16	**Current De-Emphasis Level** Reflects the de-emphasis level. 0 = -6 dB (Link is operating at 5.0 GT/s) 1 = -3.5 dB	RO	Yes	0 (5.0 GT/s) 1 (2.5 GT/s)
31:17	***Reserved***	RsvdP	No	0-0h

15.9 NT Port Link Interface Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – C4h)

The registers detailed in Section 12.10, "Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)," are also applicable to the NT Port, except as defined in Table 15-6 (register map) and Register 15-26.

Table 15-6. NT Port Link Interface Subsystem ID and Subsystem Vendor ID Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved	Next Capability Pointer (C8h) / SSID/SSVID Capability ID (0Dh)	A4h
Subsystem ID	Subsystem Vendor ID	A8h
Reserved	ACh –	C4h

Register 15-26. A4h Subsystem Capability

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**SSID/SSVID Capability ID** SSID/SSVID registers for the PCI-to-PCI bridge. Program to 0Dh, as required by the *PCI-to-PCI Bridge r1.2*.	RO	Yes	0Dh
15:8	**Next Capability Pointer** Program to C8h, to point to the **Vendor-Specific Capability 3** structure.	RO	Yes	C8h
31:16	***Reserved***	RsvdP	No	0000h

15.10 NT Port Link Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)

This section details the NT Port Link Interface Vendor-Specific Capability 3 registers. Table 15-7 defines the register map used by the NT Port Link Interface.

The Cursor Mechanism registers at offsets F8h and FCh provide a means for accessing PCI Express Extended Configuration Space registers (offsets 100h through FFFh) within the NT Port Link and Virtual Interfaces, when only standard PCI Configuration transactions (that do not support the *Extended Register Number* field within the Completion Request Header) are available.

Table 15-7. NT Port Link Interface Vendor-Specific Capability 3 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved / Vendor-Specific Capability 3	Next Capability Pointer 3 (00h) / Capability ID 3 (09h)	C8h
Vendor-Specific Header 3 ***(Reserved)***		CCh
Reserved		D0h – E0h
NT Port Link Interface BAR0/1 Setup		E4h
NT Port Link Interface Memory BAR2 Setup		E8h
NT Port Link Interface Memory BAR2/3 Setup		ECh
NT Port Link Interface Memory BAR4 Setup		F0h
NT Port Link Interface Memory BAR4/5 Setup		F4h
Configuration Address Window	***Reserved***	F8h
Configuration Data Window		FCh

Register 15-27. C8h Vendor-Specific Capability 3

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Capability ID 3**	RO	Yes	09h
15:8	**Next Capability Pointer 3** 00h = This capability is the last capability in the Linked List	RO	Yes	00h
23:16	**Length** Number of bytes in this Capability structure.	RO	Yes	38h
31:24	***Reserved***	RsvdP	Yes	00h

Register 15-28. CCh Vendor-Specific Header 3

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	***Reserved***	RO	Yes	0380_0002h

Register 15-29. E4h NT Port Link Interface BAR0/1 Setup

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
1:0	**BAR0/1 Enable** 00b = Disables Link Interface **BAR0** and **BAR1** 01b = ***Reserved*** 10b = Enables Link Interface **BAR0** and disables **BAR1** (**BAR0** is a 32-bit BAR) 11b = Enables Link Interface **BAR0** and **BAR1** (**BAR0/1** is a 64-bit BAR)	RW	No	10b
2	**BAR0 Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RW	No	0
31:3	***Reserved***	RsvdP	No	0-0h

Register 15-30. E8h NT Port Link Interface Memory BAR2 Setup

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
0	**Type Selector**		RsvdP	No	0
2:1	**BAR2 Type** 00b = **BAR2** is implemented as a 32-bit Memory BAR 10b = **BAR2/3** is implemented as a 64-bit Memory BAR No other encodings are allowed.		RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0-0h
30:20	**BAR2 Size** Specifies the Address Range size requested by **BAR2**. 0 = Corresponding **BAR2** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR2** bits are RW bits		RW	Yes	0-0h
31	**BAR2 Enable** 0 = **BAR2** is disabled, all **BAR2** bits read 0 1 = **BAR2** is enabled	Field [2:1] (*BAR2 Type*) = 00b	RW	Yes	0
	BAR2 Size Included with field [30:20] when this BAR is used as a 64-bit BAR.	Field [2:1] (*BAR2 Type*) = 10b	RW	Yes	0

Register 15-31. ECh NT Port Link Interface Memory BAR2/3 Setup

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *This register has RW privilege if **BAR2/3** is configured as a 64-bit BAR (**NT Port Link Interface Memory BAR2 Setup** register BAR2 Type field (NT Port Link Interface, offset E8h[2:1]), is programmed to 10b).*					
0	**Type Selector**	Offset E8h[2:1]=00b	RO	No	0
		Offset E8h[2:1]=10b	RW	Yes	0
2:1	**BAR3 Type** 00b = **BAR3** is implemented as a 32-bit Memory BAR No other encodings are allowed.	Offset E8h[2:1]=00b	RO	No	00b
		Offset E8h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset E8h[2:1]=00b	RO	No	0
		Offset E8h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset E8h[2:1]=00b	RO	No	0_000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset E8h[2:1]=10b	RW	Yes	0_000h
30:20	**BAR3 Size** Specifies the Address Range size requested by **BAR3**. 0 = Corresponding **BAR3** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR3** bits are RW bits		RW	Yes	0-0h
31	**BAR3 Enable** **32-Bit BAR:** 0 = **BAR3** is disabled 1 = **BAR3** is enabled as a 32-bit BAR	Offset E8h[2:1]=00b	RW	Yes	0
	64-Bit BAR: 0 = **BAR2/3** is disabled, all **BAR2/3** bits read 0 1 = **BAR2/3** is enabled as a 64-bit BAR	Offset E8h[2:1]=10b	RW	Yes	0

Register 15-32. F0h NT Port Link Interface Memory BAR4 Setup

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
0	**Type Selector**		RsvdP	No	0
2:1	**BAR4 Type** 00b = **BAR4** is implemented as a 32-bit Memory BAR (**BAR4**) 10b = **BAR4/5** is implemented as a 64-bit Memory BAR (**BAR4/5**) No other encodings are allowed.		RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0_000h
30:20	**BAR4 Size** Specifies the Address Range size requested by **BAR4**. 0 = Corresponding **BAR4** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR4** bits are RW bits		RW	Yes	0-0h
31	**BAR4 Enable** 0 = **BAR4** is disabled, all **BAR4** bits read 0 1 = **BAR4** is enabled	Field [2:1] (*BAR4 Type*) = 00b	RW	Yes	0
	BAR4 Size Included with field [30:20] when this BAR is used as a 64-bit BAR.	Field [2:1] (*BAR4 Type*) = 10b	RW	Yes	0

Register 15-33. F4h NT Port Link Interface Memory BAR4/5 Setup

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
Note: *This register has RW privilege if* ***BAR4/5*** *is configured as a 64-bit BAR (**NT Port Link Interface Memory BAR4 Setup** register BAR4 Type field (NT Port Link Interface, offset F0h[2:1]), is programmed to 10b).*					
0	**Type Selector**	Offset F0h[2:1]=00b	RO	No	0
		Offset F0h[2:1]=10b	RW	Yes	0
2:1	**BAR5 Type** 00b = **BAR5** is implemented as a 32-bit Memory BAR No other encodings are allowed.	Offset F0h[2:1]=00b	RO	No	00b
		Offset F0h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset F0h[2:1]=00b	RO	No	0
		Offset F0h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset F0h[2:1]=00b	RsvdP	No	0_000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset F0h[2:1]=10b	RW	Yes	0_000h
30:20	**BAR5 Size** Specifies the Address Range size requested by **BAR5**. 0 = Corresponding **BAR5** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR5** bits are RW bits		RW	Yes	0-0h
31	**BAR5 Enable** **32-Bit BAR:** 0 = **BAR5** is disabled 1 = **BAR5** is enabled as a 32-bit BAR	Offset F0h[2:1]=00b	RW	Yes	0
	64-Bit BAR: 0 = **BAR4/5** is disabled, all **BAR4/5** bits read 0 1 = **BAR4/5** is enabled as a 64-bit BAR	Offset F0h[2:1]=10b	RW	Yes	0

Register 15-34. F8h Configuration Address Window (Device-Specific Cursor Mechanism)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	***Reserved***	RsvdP	No	0000h
25:16	**Register Offset**	RW	Yes	0-0h
30:26	***Reserved***	RsvdP	No	0-0h
31	**Interface Select** 0 = Access is to the NT Port Link Interface Type 0 Configuration Space register 1 = Access is to the NT Port Virtual Interface Type 0 Configuration Space register	RW	Yes	0

Register 15-35. FCh Configuration Data Window (Device-Specific Cursor Mechanism)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Data Window** Software selects a register by writing into the NT Port Link Interface Configuration Address window, then reads from or writes to that register using this register.	RW	Yes	0000_0000h

15.11 NT Port Link Interface Device Serial Number Extended Capability Registers (Offsets 100h – 134h)

The registers detailed in Section 12.11, "Device Serial Number Extended Capability Registers (Offsets 100h – 134h)," are also applicable to the NT Port. Table 15-8 defines the register map used by all Ports.

Table 15-8. NT Port Link Interface Device Serial Number Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (FB4h)	Capability Version (1h) / PCI Express Extended Capability ID (0003h)	100h
Serial Number (Lower DW)		104h
Serial Number (Upper DW)		108h
Reserved	10Ch –	134h

15.12 NT Port Link Interface Power Budget Extended Capability Registers (Offsets 138h – 144h)

The registers detailed in Section 12.12, "Power Budget Extended Capability Registers (Offsets 138h – 144h)," are also applicable to the NT Port Link Interface. Table 15-9 defines the register map.

Table 15-9. NT Port Link Interface Power Budget Extended Capability Register Map (Only Upstream Port, and also NT Port Link Interface; *Reserved* (RsvdP) for All Other Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (148h)	Capability Version (1h) / PCI Express Extended Capability ID (0004h)	138h
Reserved	Data Select	13Ch
Power Budget Data		140h
Power Budget Capability		144h

15.13 NT Port Link Interface Virtual Channel Extended Capability Registers (Offsets 148h – 1A4h)

The registers detailed in Section 12.13, "Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)," are also applicable to the NT Port Link Interface, except as defined in Table 15-10 (register map), and Register 15-36 through Register 15-40.

Table 15-10. NT Port Link Interface Virtual Channel Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (950h) / Capability Version (1h)	PCI Express Extended Capability ID (0002h)	148h
Port VC Capability 1		14Ch
Port VC Capability 2		150h
Port VC Status ***(Reserved)***	Port VC Control	154h
VC0 Resource Capability		158h
VC0 Resource Control		15Ch
VC0 Resource Status	***Reserved***	160h
Reserved		164h – 1A4h

Register 15-36. 148h Virtual Channel Extended Capability Header

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**PCI Express Extended Capability ID** Program to 0002h, as required by the *PCI Express Base r2.0*.	RO	No	0002h
19:16	**Capability Version** Program to 1h, as required by the *PCI Express Base r2.0*.	RO	No	1h
31:20	**Next Capability Offset** Next extended capability is the **Vendor-Specific Extended Capability 2** structure, offset 950h.	RO	No	950h

Register 15-37. 14Ch Port VC Capability 1

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**Extended VC Counter** 0 = PEX 8624 Port supports only one Virtual Channel (VC0) 1 = ***Reserved***	RO	No	0
3:1	***Reserved***	RsvdP	No	000b
4	**Low-Priority Extended VC Counter** For Strict Priority arbitration, indicates the number of extended VCs (those in addition to VC0) that belong to the Low-Priority Virtual Channel group for this PEX 8624 Port. 0 = For this PEX 8624 Port, only VC0 belongs to the Low-Priority Virtual Channel group 1 = ***Reserved***, because the PEX 8624 supports only one VC	RO	No	0
7:5	***Reserved***	RsvdP	No	000b
9:8	**Reference Clock** Cleared.	RsvdP	No	00b
11:10	**Port Arbitration Table Entry Size**	RsvdP	No	00b
31:12	***Reserved***	RsvdP	No	0000_0h

Register 15-38. 158h VC0 Resource Capability

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
1:0	**Port Arbitration Capability** Bit 0 = 1 – Non-configurable Round-Robin (Hardware-Fixed) arbitration Bit 1 = 1 – Weighted Round-Robin (WRR) arbitration with 32 Phases	RO	No	01b
14:2	***Reserved***	RsvdP	No	0-0h
15	**Reject Snoop Transactions** Not a PCI Express switch feature; therefore, Cleared.	RsvdP	No	0
22:16	**Maximum Time Slots** ***Not supported***	RsvdP	No	000_0000b
23	***Reserved***	RsvdP	No	0
31:24	**Port Arbitration Table Offset** Offset of the Port Arbitration Table, as the number of DQWords from the Base address of the **Virtual Channel Extended Capability** structure. 00h = Port Arbitration Table is not present	RO	No	00h

Register 15-39. 15Ch VC0 Resource Control

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**TC/VC Map** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped into VC0. Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.	RO	No	1
7:1		RW	Yes	7Fh
15:8	***Reserved***	RsvdP	No	00h
16	**Load Port Arbitration Table** Hardware writable and software readable.	RW	Yes	0
19:17	**Port Arbitration Select** Selects the Port Arbitration type for the NT Port Link Interface. Indicates the bit number in the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[1:0]) that corresponds to the arbitration type. 0 = Round-Robin (Hardware-Fixed) arbitration scheme	RW	Yes	000b
23:20	***Reserved***	RsvdP	No	0h
24	**VC ID** Defines the NT Port Link Interface VC0 ID code. Cleared, because there is only one Virtual Channel.	RO	No	0
30:25	***Reserved***	RsvdP	No	0-0h
31	**VC Enable** 0 = Not allowed 1 = Enables the NT Port Link Interface VC0	RO	No	1

Register 15-40. 160h VC0 Resource Status

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	***Reserved***	RsvdP	No	0000h
16	**Port Arbitration Table Status** ***Not implemented***	RO	No	0
17	**VC0 Negotiation Pending** 0 = VC0 negotiation completed 1 = VC0 initialization is not complete for the NT Port Link Interface	RO	Yes	1
31:18	***Reserved***	RsvdP	No	0-0h

15.14 NT Port Link Interface Device-Specific Registers (Offsets 1C0h – C88h)

The registers detailed in Section 12.14, "Device-Specific Registers (Offsets 1C0h – 51Ch)," and Section 12.16, "Device-Specific Registers (Offsets 54Ch – F8Ch)" (for offsets A00h through C88h), are unique to the PEX 8624 and not referenced in the *PCI Express Base r2.0*. These registers are also applicable to the NT Port Link Interface, except as defined in Table 15-11 (register map; offsets 200h through 65Ch, 680h through 94Ch, and 960h through C30h are ***reserved***) through Table 15-15, and Register 15-41 through Register 15-48.

Another NT Port Link Interface Device-Specific register is detailed in Section 15.16, "NT Port Link Interface Device-Specific Registers – Source Queue Weight (Offsets F00h – F30h)."

Note: It is recommended that these registers not be changed from their default values.

Table 15-11. NT Port Link Interface Device-Specific Register Map (Offsets 1C0h – C88h)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
NT Port Link Interface Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)		1C0h … 1FCh
Reserved		200h – 65Ch
NT Port Link Interface Device-Specific Registers – Ingress Control and Port Enable (Offsets 660h – 67Ch)		660h … 67Ch
Reserved		680h – 94Ch
Next Capability Offset 2 (C34h)	1h / PCI Express Extended Capability ID 2 (000Bh)	950h
NT Port Link Interface Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)		… 95Ch
Reserved		960h – C30h
Next Capability Offset 4 (000h)	1h / PCI Express Extended Capability ID 4 (000Bh)	C34h
NT Port Link Interface Device-Specific Registers – Vendor-Specific Extended Capability 4 (Offsets C34h – C88h)		… C88h

15.14.1 NT Port Link Interface Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)

The registers detailed in Section 12.14.1, "Device-Specific Registers – Error Checking and Debug (Offsets 1C0h – 1FCh)," are also applicable to the NT Port Link Interface, except as defined in Table 15-12 (register map; offsets 1C0h, 1C4h, 1CCh through 1DCh, and 1F4h are ***reserved*** or ***Factory Test Only***), and Register 15-41 through Register 15-43.

Table 15-12. NT Port Link Interface Device-Specific Error Checking and Debug Register Map (Ports[a])

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				1C0h – 1C4h
ECC Error Check Disable				1C8h
Reserved				1CCh
Factory Test Only				1D0h
Reserved				1D4h – 1DCh
Power Management Hot Plug User Configuration				1E0h
Factory Test Only				1E4h
Bad TLP Counter				1E8h
Bad DLLP Counter				1ECh
Reserved				1F0h – 1F4h
ACK Transmission Latency Limit				1F8h
Factory Test Only				1FCh

a. Certain registers are Port-specific, others are Station-specific or Chip-specific; all are device-specific.

Register 15-41. 1C8h ECC Error Check Disable

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
1:0	***Reserved***	RsvdP	No	00b
2	**Software Force Error Enable** 1 = **Correctable Error Status** and **Uncorrectable Error Status** registers (offsets FC4h and FB8h, respectively) change from RW1CS to RW register	RWS	Yes	0
3	**Software Force Non-Posted Request** 1 = Enables handling of errors associated with Posted TLPs as if those errors are associated with Non-Posted TLPs	RWS	Yes	0
4	***Reserved***	RsvdP	No	0
5	**Enable PEX_INTA# Interrupt Output(s) for Device-Specific Error and Event-Triggered Interrupt** 0 = Device-Specific Error and Event Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = Device-Specific Error and Event Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)	RWS	Yes	0
6	**Enable PEX_INTA# Interrupt Output(s) for GPIO-Generated Interrupts** 0 = General-Purpose Input/Output (GPIO) Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = GPIO Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)	RWS	Yes	0
7	**Enable PEX_INTA# Interrupt Output(s) for NT-Link Doorbell-Generated Interrupts** 0 = NT Port Link Interface Doorbell Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = NT Port Link Interface Doorbell Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)	RWS	Yes	0
8	**Disable Sending MSI If MSI Is Enabled after Interrupt Status Set** 0 = Does not disable sending an MSI, if MSI is enabled after an *Interrupt Status* bit is Set 1 = Disables sending an MSI, if MSI is enabled after an *Interrupt Status* bit is Set ***Note:*** *This bit must remain Cleared, for compliance to specifications governing the MSI Capability.*	RWS	Yes	0
31:9	***Reserved***	RsvdP	No	0-0h

Register 15-42. 1E0h Power Management Hot Plug User Configuration

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**L0s Entry Idle Counter** Traffic Idle time to meet, to enter the L0s Link PM state. 0 = Idle condition must last 1 s 1 = Idle condition must last 4 s	RW	Yes	0
1	***Factory Test Only***	RW	Yes	0
2	**NT Virtual MPS CSR Select** NT Port Virtual Interface Maximum Payload Size register select. 0 = NT Port Virtual Interface uses the NT Port Link Interface's Maximum Payload Size (offset 70h[7:5]) 1 = NT Port Virtual Interface uses its own Maximum Payload Size (offset 70h[7:5])	RW	Yes	0
7:3	***Factory Test Only***	RW	Yes	0-0h
8	**DLLP Timeout Link Retrain Disable** Disable Link retraining when no Data Link Layer Packets (DLLPs) are received for more than 256 s. 0 = Enables Link retraining when no DLLPs are received for more than 256 s (default) 1 = DLLP Timeout is disabled	RW	Yes	0
9	***Factory Test Only***	RW	Yes	0
10	**L0s Entry Disable** 0 = Enables entry into the L0s Link PM state on a Port when the L0s idle conditions are met 1 = Disables entry into the L0s Link PM state on a Port when the L0s idle conditions are met	RW	Yes	0
31:11	***Reserved***	RsvdP	No	0-0h

Register 15-43. 1F8h ACK Transmission Latency Limit

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
The value of this register should be valid after Link negotiation.				
11:0	**ACK Transmission Latency Limit** Acknowledge Control Packet (ACK) Transmission Latency Limit.	RWS	Yes	237d
15:12	***Reserved***	RsvdP	No	0h
23:16	**Upper 8 Bits of the Replay Timer Limit** The value in this register is a multiplier of the default internal timer values that are compliant to the *PCI Express Base r2.0*. These bits should normally remain the default value, 00h.	RWS	Yes	00h
30:24	***Reserved***	RsvdP	No	0-0h
31	**ACK Transmission Latency Timer Status** Indicates the written status of field [11:0] (*ACK Transmission Latency Limit*). After the register is written, either by software and/or serial EEPROM, this bit is Set, and Cleared only by a Fundamental Reset.	RO	No	0

15.14.2 NT Port Link Interface Device-Specific Registers – Ingress Control and Port Enable (Offsets 660h – 67Ch)

The registers detailed in Section 12.16.3, "Device-Specific Registers – Ingress Control and Port Enable (Offsets 660h – 67Ch)," are also applicable to the NT Port Link Interface, except as defined in Table 15-13 (register map; offsets 660h, 664h, and 678h are ***reserved***).

Table 15-13. NT Port Link Interface Device-Specific Ingress Control and Port Enable Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				660h – 664h
Port Enable Status				668h
Negotiated Link Width for Ports 0, 1, 5, 6				66Ch
Reserved		***Factory Test Only***	Negotiated Link Width for Ports 8, 9	670h
Port Cut-Thru Enable Status				674h
Reserved				678h – 67Ch

15.14.3 NT Port Link Interface Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)

The registers detailed in Section 12.16.8, "Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets 950h – 95Ch)," are also applicable to the NT Port, except for the Next Capability Offset value, as defined in Table 15-14 (register map) and Register 15-44.

Table 15-14. NT Port Link Interface Device-Specific, Vendor-Specific Extended Capability 2 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset 2 (C34h)	Capability Version 2 (1h) / PCI Express Extended Capability ID 2 (000Bh)	950h
Vendor-Specific Header 2		954h
Hardwired Device ID	Hardwired Vendor ID	958h
Reserved	PLX Hardwired Revision ID	95Ch

Register 15-44. 950h Vendor-Specific Extended Capability 2

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**PCI Express Extended Capability ID 2** Program to 000Bh, indicating that the Capability structure is the **Vendor-Specific Extended Capability** structure.	RO	Yes	000Bh
19:16	**Capability Version 2**	RO	Yes	1h
31:20	**Next Capability Offset 2** Program to C34h, which addresses the **Vendor-Specific Extended Capability 4** structure.	RO	Yes	C34h

15.14.4 NT Port Link Interface Device-Specific Registers – Vendor-Specific Extended Capability 4 (Offsets C34h – C88h)

The registers detailed in Section 14.14.4, "NT Port Virtual Interface Device-Specific Registers – Vendor-Specific Extended Capability 4 (Offsets C34h – C88h)," are also applicable to the NT Port Link Interface, except as defined in Table 15-15 (register map), and Register 15-45 through Register 15-48.

Table 15-15. NT Port Link Interface Device-Specific, Vendor-Specific Extended Capability 4 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset 4 (000h)	Capability Version 4 (1h) / PCI Express Extended Capability ID 4 (000Bh)	C34h
Vendor-Specific Header 4		C38h
Memory BAR2 Address Translation Lower		C3Ch
Memory BAR3 Address Translation Upper		C40h
Memory BAR4 Address Translation Lower		C44h
Memory BAR5 Address Translation Upper		C48h
Reserved	Virtual Interface IRQ Set	C4Ch
Reserved	Virtual Interface IRQ Clear	C50h
Reserved	Virtual Interface IRQ Mask Set	C54h
Reserved	Virtual Interface IRQ Mask Clear	C58h
Reserved	Link Interface IRQ Set	C5Ch
Reserved	Link Interface IRQ Clear	C60h
Reserved	Link Interface IRQ Mask Set	C64h
Reserved	Link Interface IRQ Mask Clear	C68h
NT Port SCRATCH0		C6Ch
NT Port SCRATCH1		C70h
NT Port SCRATCH2		C74h
NT Port SCRATCH3		C78h
NT Port SCRATCH4		C7Ch
NT Port SCRATCH5		C80h
NT Port SCRATCH6		C84h
NT Port SCRATCH7		C88h

Register 15-45. C3Ch Memory BAR2 Address Translation Lower

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**NT Port Link-to-Virtual Interface BAR2 Base Translation Address** Base Translation address when **BAR2** is enabled (**NT Port Link Interface Memory BAR2 Setup** register *BAR2 Enable* bit, offset E8h[31], is Set).	RW	Yes	000h

Register 15-46. C40h Memory BAR3 Address Translation Upper

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	Offset ECh[31]=0	RsvdP	No	0_0000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:0]) are used as the upper 32 bits.	Offset ECh[31]=1	RW	Yes	0_0000h
31:20	**NT Port Link-to-Virtual Interface BAR3 Base Translation Address** Base Translation address when **BAR3** is enabled (**NT Port Link Interface Memory BAR2/3 Setup** register *BAR3 Enable* bit, offset ECh[31], is Set).		RW	Yes	000h

Register 15-47. C44h Memory BAR4 Address Translation Lower

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**NT Port Link-to-Virtual Interface BAR4 Base Translation Address** Base Translation address when **BAR4** is enabled (**NT Port Link Interface Memory BAR4 Setup** register *BAR4 Enable* bit, offset F0h[31], is Set).	RW	Yes	000h

Register 15-48. C48h Memory BAR5 Address Translation Upper

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
19:0	***Reserved***	Offset F4h[31]=0	RsvdP	No	0_0000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:0]) are used as the upper 32 bits.	Offset F4h[31]=1	RW	Yes	0_0000h
31:20	**NT Port Link-to-Virtual Interface BAR5 Base Translation Address** Base Translation address when **BAR5** is enabled (**NT Port Link Interface Memory BAR4/5 Setup** register *BAR5 Enable* bit, offset F4h[31], is Set).		RW	Yes	000h

15.15 NT Port Link Interface NT Bridging-Specific Registers (Offsets C8Ch – EFCh)

Table 15-16 defines the register map of the NT Port Link Interface NT Bridging-Specific registers.

Table 15-16. NT Port Link Interface NT Bridging-Specific Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				C8Ch – DB0h
NT Port Link Interface NT Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Addresses DB4h – DF0h)				DB4h … DF0h
Reserved				DF4h – EFCh

15.15.1 NT Port Link Interface NT Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Addresses DB4h – DF0h)

This section describes the NT Port Link Interface NT Bridging-Specific Requester ID Translation Lookup Table (LUT) Entry registers. The NT Port uses these registers for Requester ID translation when it forwards:

- Memory Requests from the NT Port Link Interface to the NT Port Virtual Interface, –or–
- Completion TLPs from the NT Port Virtual Interface to the NT Port Link Interface

If the application needs to send traffic through the NT Port Link Interface, program the registers listed in this group with the corresponding Requester's Requester ID, then Set the *LUT Entry_n Enable* and *LUT Entry_m Enable* bits (bits 0 and 16, respectively) for each LUT entry, as needed.

Table 15-17 defines the register and address locations, as they relate to Register 15-49.

Table 15-17. NT Port Link Interface NT Bridging-Specific Requester ID Translation LUT Entry_*n_m* Register Locations

ADDR Location	Lookup Table Entry_*n_m*	ADDR Location	Lookup Table Entry_*n_m*
DB4h	0_1	DD4h	16_17
DB8h	2_3	DD8h	18_19
DBCh	4_5	DDCh	20_21
DC0h	6_7	DE0h	22_23
DC4h	8_9	DE4h	24_25
DC8h	10_11	DE8h	26_27
DCCh	12_13	DECh	28_29
DD0h	14_15	DF0h	30_31

Register 15-49. DB4h – DF0h NT Port Link Interface Requester ID Translation LUT Entry_*n_m* (where *n_m* = 0_1 through 30_31)

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
0	**LUT Entry_*n* Enable** 0 = Disables 1 = Enables		RW	Yes	0
1	**LUT Entry_*n* No Snoop Enable** If Set, the NT Port Clears the TLP *No Snoop* attribute bit for the Memory Request, then goes from the NT Port Link Interface to the NT Port Virtual Interface, and re-calculates the End-to-end Cyclic Redundancy Check (ECRC). If the original TLP has an ECRC error, the NT Port corrupts the re-calculated ECRC before transmitting to the other Host domain. The NT Port sets the *No Snoop* attribute bit when it forwards the Completion TLP from the NT Port Virtual Interface to the NT Port Link Interface if this bit is Set for the corresponding Requester ID entry. This ECRC rule applies to Completion TLPs as well. 0 = Disables 1 = Enables		RW	Yes	0
2	***Reserved***		RsvdP	No	0
7:3	**Requester ID on Link Side**	**Device Number** LUT Entry_*n* Requester Device Number.	RW	Yes	0000_0b
15:8		**Bus Number** LUT Entry_*n* Requester Bus Number.	RW	Yes	00h
16	**LUT Entry_*m* Enable** 0 = Disables 1 = Enables		RW	Yes	0
17	**LUT Entry_*m* No Snoop Enable** If Set, the NT Port Clears the TLP *No Snoop* attribute bit for the Memory Request, then goes from the NT Port Link Interface to the NT Port Virtual Interface, and re-calculates the ECRC. If the original TLP has an ECRC error, the NT Port corrupts the re-calculated ECRC before transmitting to the other Host domain. The NT Port sets the *No Snoop* attribute bit when it forwards the Completion TLP from the NT Port Virtual Interface to the NT Link Virtual Interface if this bit is Set for the corresponding Requester ID entry. This ECRC rule applies to Completion TLPs as well. 0 = Disables 1 = Enables		RW	Yes	0
18	***Reserved***		RsvdP	No	0
23:19	**Requester ID on Link Side**	**Device Number** LUT Entry_*m* Requester Device Number.	RW	Yes	0000_0b
31:24		**Bus Number** LUT Entry_*m* Requester Bus Number.	RW	Yes	00h

15.16 NT Port Link Interface Device-Specific Registers – Source Queue Weight (Offsets F00h – F30h)

Register offset F10h, detailed in Section 12.16.13, "Device-Specific Registers – Source Queue Weight and Soft Error (Offsets F00h – F30h)," is also applicable to the NT Port Link Interface. The remaining registers within the register set are ***reserved*** in the NT Port Link Interface, as defined in the Table 15-18 register map.

Other NT Port Link Interface Device-Specific registers are detailed in Section 15.14, "NT Port Link Interface Device-Specific Registers (Offsets 1C0h – C88h)."

Table 15-18. NT Port Link Interface Device-Specific Source Queue Weight Register Map (Offsets F00h – F30h)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				F00h – F0Ch
Port Egress TLP Threshold				F10h
Reserved				F14h – F30h

15.17 NT Port Link Interface Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)

The registers detailed in Section 12.17, "Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)," are also applicable to the NT Port Link Interface, except for the Next Capability Offset value, as defined in Table 15-19 (register map) and Register 15-50.

Table 15-19. NT Port Link Interface Advanced Error Reporting Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (138h)	Capability Version (1h) / PCI Express Extended Capability ID (0001h)	FB4h
Uncorrectable Error Status		FB8h
Uncorrectable Error Mask		FBCh
Uncorrectable Error Severity		FC0h
Correctable Error Status		FC4h
Correctable Error Mask		FC8h
Advanced Error Capabilities and Control		FCCh
Header Log 0		FD0h
Header Log 1		FD4h
Header Log 2		FD8h
Header Log 3		FDCh

Register 15-50. FB4h Advanced Error Reporting Extended Capability Header

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**PCI Express Extended Capability ID**	RO	Yes	0001h
19:16	**Capability Version**	RO	Yes	1h
31:20	**Next Capability Offset** Program to 138h, which addresses the upstream Port/NT Port Link Interface **Power Budget Extended Capability** structure.	RO	Yes	138h

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Chapter 16 Test and Debug

16.1 Introduction

This chapter describes the following test- and debug-related information:

- Physical Layer Loopback Operation
- Using the SerDes Quad x Diagnostic Data Registers
- Pseudo-Random and Bit-Pattern Generation
- PHY Testability Features
- JTAG Interface
- Port Good Status LEDs

16.2 Physical Layer Loopback Operation

16.2.1 Overview

Physical Layer (PHY) Loopback functions are used to test the SerDes in the PEX 8624, connections between devices, and SerDes of external devices, as well as various PEX 8624 and external digital logic. The PEX 8624 supports four types of Loopback operations, as described in Table 16-1. Additional information regarding each type is provided in the sections that follow.

Table 16-1. Loopback Operations

Operation	Description
Analog Loopback Master Mode	Analog Loopback Master mode depends upon an external device or dumb connection (*such as* a cable) to loop back the transmitted data to the PEX 8624. If an external device is used, it must not include its Elastic buffer in the Loopback data path, because no SKIP Ordered-Sets are transmitted. Use the PRBS generator and checker to create and check the data pattern. The corresponding PEX 8624 Port enters Analog Loopback Master mode when a Port's **Physical Layer Port Command** register *Port x Loopback Command* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 230h[0, 4, or 8]) is Set.
Digital Loopback Master Mode	As with Analog Loopback Master mode, Digital Loopback Master mode depends upon an external device to loop back the transmitted data. This method is best used with an external device that includes at least its Elastic buffer in the Loopback data path. The PEX 8624 provides a programmable data pattern generator and checker that inserts the SKIP Ordered-Set at the proper intervals. The corresponding PEX 8624 Port enters Digital Loopback Master mode when a Port's **Physical Layer Port Command** register *Port x Loopback Command* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 230h[0, 4, or 8]) is Set.
Analog Loopback Slave Mode	The corresponding PEX 8624 Port enters Analog Loopback Slave mode when an external device transmits Training Sets with the *Loopback Training Control Bit* Set and the **Physical Layer Test** register *Analog Loopback Enable* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 228h[6]) is Set. The received data is looped back from the SerDes 10-bit Receive interface to the 10-bit Transmit interface.
Digital Loopback Slave Mode	The corresponding PEX 8624 Port Digital Loopback Slave mode when an external device transmits Training Sets with the *Loopback Training Control Bit* Set and the **Physical Layer Test** register *Analog Loopback Enable* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 228h[6]) is Cleared. In this mode, the data is looped back at an 8-bit level, which includes the PEX 8624's Elastic buffer, 8b/10b decoder, and 8b/10b encoder in the loopback data path.

16.2.2 Analog Loopback Master Mode

Analog Loopback Master mode is typically used for Analog Far-End testing, as illustrated in Figure 16-1.

The mode can also be used to re-create the previously described BIST, by looping back the data with a cable. Looping back with a cable includes the internal bond, external balls, board trace, and connectors in the test data path, as illustrated in Figure 16-2.

Figure 16-1. Analog Far-End Loopback

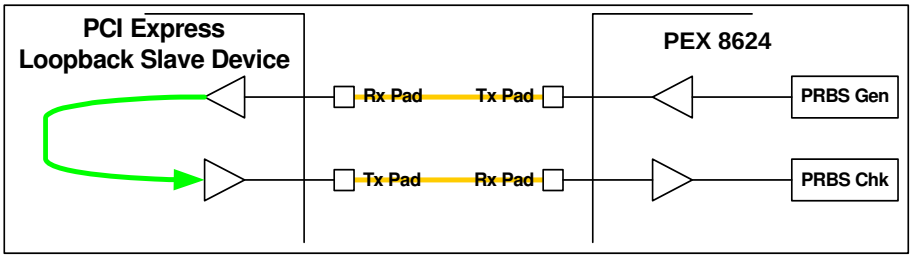
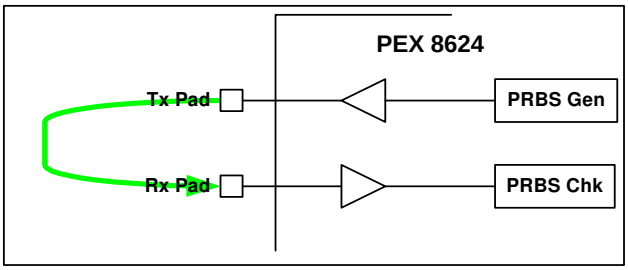


Figure 16-2. Cable Loopback



To cause a PEX 8624 Port to request to become a Loopback Master:

1. After the Link is up, a Configuration Write to the Port's **Physical Layer Port Command** register *Port x Loopback Command* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 230h[0, 4, or 8]) causes the Port to transition from the L0 Link PM state to Recovery, and then to the *Loopback* state:
   - If a cable is used for the loopback, the Port transitions from the *Configuration* state to the *Loopback* state. Connect the cable only after the upstream Link is up and Configuration Writes are possible.
   - If the cable is connected before the upstream device is able to Set the *Port x Loopback Command* bit, the Link with the cable may reach the L0 Link PM state and not go to the *Loopback* state. In this case, the Port must be forced to the *Recovery* state, by Setting the Port's **Link Control** register *Retrain Link* bit (offset 78h[5]).
   - Cable length is limited only by the PCI Express drivers and cable properties.
2. After the Port is in the *Loopback* state, the Port's **Physical Layer Port Command** register *Port x Ready as Loopback Master* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 230h[3, 7, or 11]) is Set:
   - At this time, the PRBS engine can be enabled by Setting the **Physical Layer Test** register *SerDes Quad x PRBS Enable* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 228h[18:16]) associated with the SerDes assigned to the Port being tested.
   - The PRBS checker checks the returned PRBS data. Any errors are logged in the **SerDes Quad *x* Diagnostic Data** register (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 238h through 244h) that corresponds to the SerDes quad being tested.

16.2.3 Digital Loopback Master Mode

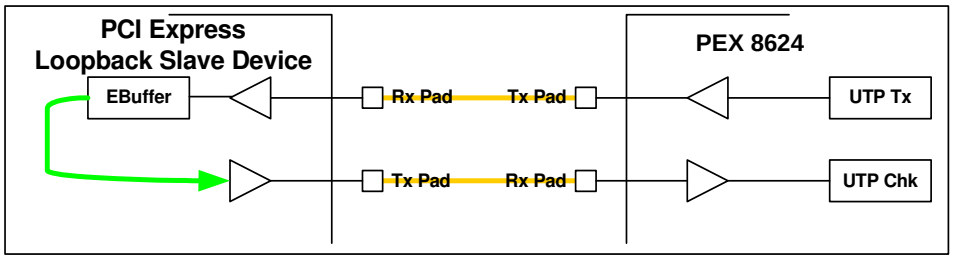
The only difference between Analog and Digital Loopback Master modes is that the external device is assumed to retain, to some extent, its digital logic in the loopback data path. Because this includes the Elastic buffer, SKIP Ordered-Sets must be included in the test pattern. For the PEX 8624, this precludes PRBS engine use, because the PRBS generator does not generate SKIP Ordered-Sets.

The PEX 8624 provides the programmable test pattern Transmitter for Digital Far-End Loopback testing, as illustrated in Figure 16-3. After Digital Loopback Master mode is established, Configuration Writes are used to fill the **Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 210h through 21Ch). The **Physical Layer Test** register *SerDes Quad x User Test Pattern Enable* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 228h[30:28]) associated with the SerDes assigned to the Port being tested, is Set, which starts the transmission of the test pattern on a bit per Lane basis. If one or more of the **Physical Layer Test** register *SerDes Quad x PRBS Enable* bits (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 228h[18:16]) are also Set, the test pattern is transmitted on all Lanes of the corresponding Port, regardless of the Port's width. However, if the *SerDes Quad x PRBS Enable* bit is Cleared, the test pattern is transmitted only on the corresponding SerDes quad Lanes.

SKIP Ordered-Sets are inserted at an interval determined by the **SKIP Ordered-Set Interval** register *SKIP Ordered-Set Interval* field (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 234h[11:0]) value (default is 1,180 symbol times), at the nearest data pattern boundary.

The Test Pattern checker ignores SKIP Ordered-Sets returned by the Loopback Slave, because the number of SKIP symbols received can differ from the number transmitted. All other data is compared to the transmitted data, and errors are logged in the **SerDes Quad *x* Diagnostic Data** register (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 238h through 244h), for the SerDes quad associated with that Port.

Figure 16-3. Digital Far-End Loopback



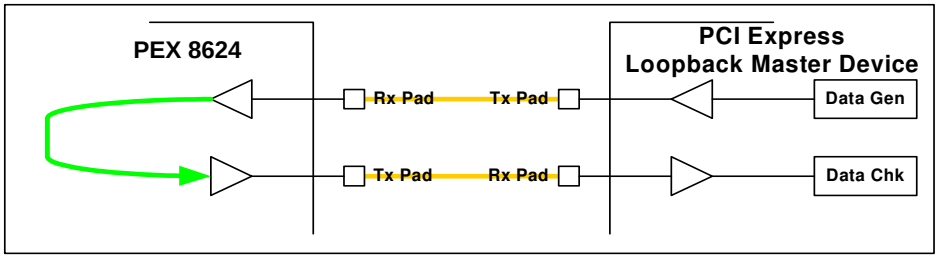
16.2.4 Analog Loopback Slave Mode

The PEX 8624 becomes an Analog Loopback Slave if it receives Training Sets with the *Loopback Training Control Bit* Set while the **Physical Layer Test** register *Analog Loopback Enable* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 228h[6]) is Set. While it is an Analog Loopback Slave, the PEX 8624 includes only the SerDes in the loopback data path. The Loopback Master must provide the test pattern and data pattern checking. It is unnecessary for the Loopback Master to include SKIP Ordered-Sets in the data pattern.

Figure 16-4 illustrates the loopback data path when Analog Loopback Slave mode is enabled.

Note: *There is no scrambling nor de-scrambling logic in the Slave analog loopback data path.*

Figure 16-4. Analog Loopback Slave Mode



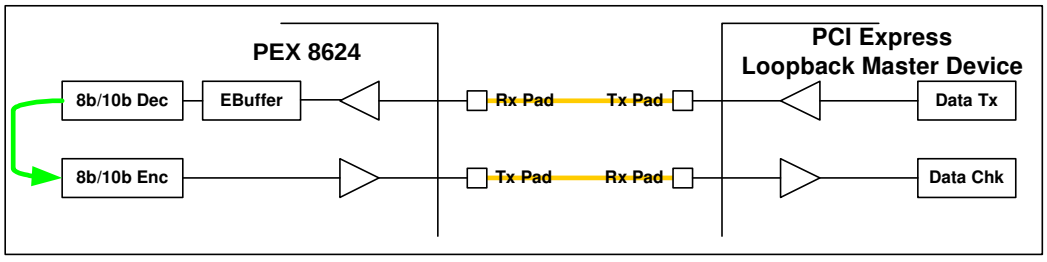
16.2.5 Digital Loopback Slave Mode

The PEX 8624 becomes a Digital Loopback Slave if it receives Training Sets with the *Loopback Training Control Bit* Set while the **Physical Layer Test** register *Analog Loopback Enable* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 228h[6]) is Cleared.

When a PEX 8624 Port is a Digital Loopback Slave, the Port includes the Elastic buffer and 8b/10b decoder and encoder in the loopback data path. The Loopback Master must provide the test pattern and data pattern checker. The Loopback Master must also transmit SKIP Ordered-Sets with the data pattern. Because the PEX 8624 can return more or fewer SKIP symbols than it receives, the data checker must make provisions for this possibility.

Note: *There is no scrambling nor de-scrambling logic in the Slave digital loopback data path.*

Figure 16-5. Digital Loopback Slave Mode



16.3 Using the SerDes Quad *x* Diagnostic Data Registers

Each SerDes quad has its own Diagnostic Data register, per Station. The **SerDes Quad *x* Diagnostic Data** register (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 238h through 244h) contents reflect the performance of the SerDes selected by the registers' *SerDes Diagnostic Data Select* field [25:24]. This control is specific to this register (which reports results of UTP and PRBS tests).

When field [25:24] is Cleared, the information in that Diagnostic Data register is for the first SerDes within that SerDes quad. When field [25:24] is programmed to 01b, the information in that Diagnostic Data register is for the second SerDes within that SerDes quad, as illustrated in Table 16-2. Following this pattern, a value of 10b indicates the third SerDes within that SerDes quad, and a value of 11b indicates the fourth SerDes within that SerDes quad. If a SerDes module does not exist in that position, the bits are "***Factory Test Only***," ***reserved*** (RsvdP), and not serial EEPROM nor I^2C writable.

Table 16-2. SerDes Quad *x* Diagnostic Data Register Contents When *SerDes Diagnostic Data Select* Field [25:24]=01b

Port 0, 4, or 8 Register Offset (For NT, Ports 4 and 8 are *Reserved*)	Register	Port 0	Port 4	Port 8
238h	**SerDes Quad 0 Diagnostic Data**	SerDes 1	***Factory Test Only***	SerDes 33
23Ch	**SerDes Quad 1 Diagnostic Data**	SerDes 5	***Factory Test Only***	SerDes 37
240h	**SerDes Quad 2 Diagnostic Data**	***Factory Test Only***	SerDes 25	***Factory Test Only***
244h	**SerDes Quad 3 Diagnostic Data**	***Factory Test Only***	SerDes 29	***Factory Test Only***

16.4 Pseudo-Random and Bit-Pattern Generation

Each SerDes quad has an associated PRBS generator and checker. The PRBS generator is based upon a 7-bit **Linear Feedback Shift** register (**LFSR**), which can generate up to ($2^7 - 1$) unique patterns. The PRBS logic is assigned to a SerDes in the quad, by manipulating the **SerDes Quad *x* Diagnostic Data** register *SerDes Diagnostic Data Select* bits (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 238h through 244h[25:24]), for the SerDes quad associated with that Port. The PRBS bit stream is used for Analog Far-End Loopback testing.

The PEX 8624 also provides a method of creating a repeating programmable bit pattern. Each of the four 32-bit **Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 210h through 21Ch) are loaded with a 32-bit data pattern. After a Port is established as a Loopback Master, Set the **Physical Layer Test** register *SerDes Quad x User Test Pattern Enable* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 228h[30:28]), for the SerDes quad associated with that Port. The PEX 8624 proceeds to transmit the data pattern on all Lanes, starting with Byte 0 of the **Physical Layer User Test Pattern, Bytes 0 through 3** register and continuing, in sequence, through Byte 3 of the **Physical Layer User Test Pattern, Bytes 12 through 15** register. SKIP Ordered-Sets are inserted at the proper intervals, which makes this method appropriate for Digital Far-End Loopback testing. The received pattern is compared to the transmitted pattern. Any errors are logged in one or more of the **SerDes Quad *x* Diagnostic Data** register RO bits (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 238h through 244h, bits [30 and 23:0]). The errors can be retrieved, by reading the appropriate bit.

To produce a pseudo-clock bitstream in Analog Loopback mode, Set the registers as follows:

1. In the Slave device, enable Analog Loopback by Setting the **Physical Layer Test** register *Analog Loopback Enable* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 228h[6]).
2. In the PEX 8624 Loopback Master device:
   a. Write the value 4A4A_4A4Ah into each of the **Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets 210h through 21Ch).
   b. Set the Port's **Physical Layer Port Command** register *Port x Loopback Command* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 230h[0, 4, or 8]).
   c. To check whether loopback is successful, read the Port's **Physical Layer Port Command** register *Port x Ready as Loopback Master* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 230h[3, 7, or 11]) in the same Nibble that was Set in step a. The Nibble value will be 9h if loopback is successful.
   d. Set the **Physical Layer Test** register *SerDes Quad x User Test Pattern Enable* bit (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 228h[30:28]) for the SerDes quad used by the Port selected in step b.
   e. The interval between SKIP Ordered-Sets can be programmed in the **SKIP Ordered-Set Interval** register *SKIP Ordered-Set Interval* field (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 234h[11:0]).

   Note: *A high value (such as FFFh) can cause the Link to fail.*

3. Exit Loopback mode, by Clearing the following registers, in the sequence listed:
   a. **Physical Layer Port Command** register (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 230h), for the Port selected in step b.
   b. **Physical Layer Test** register (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset 228h), for the SerDes quad used by the Port selected in step d.

   After the registers are Cleared, the Link will re-establish itself.

16.5 PHY Testability Features

The PEX 8624 includes several Configuration bits to ease PHY testability. Features include:

- Full support of the standard and modified compliance patterns
- Register controllability of the common block and Lane-specific inputs of the SerDes

Table 16-3 describes the Configuration bits.

Table 16-3. Configuration Bits to Ease PHY Testability

Register Bit(s)[a]	Description
SerDes x Mask Electrical Idle Detect **Physical Layer Electrical Idle Detect Mask** register (offset 204h[15:0])	When any one of these bits is Set, the Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.
SerDes x Mask Receiver Not Detected **Physical Layer Receiver Not Detected Mask** register (offset 204h[31:16])	When any one of these bits is Set, the PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.
Test Pattern x **Physical Layer User Test Pattern, Bytes *x* through *y*** registers (offsets 210h through 21Ch)	A 16-byte test pattern can be written to these four registers. When UTP transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 16.2.3 for further details.) Every byte of the UTP is a Control or Data character. Illegal Control characters can be specified.
Port x Scrambler Disable Command **Physical Layer Port Command** register (offset 230h[1, 5, or 9])	When Set, unconditionally disables the data scramblers on the Lanes of the corresponding Port and causes the *Scrambler Disable Training Control Bit* to be Set in transmitted Training Sets. There is one bit for each Port in the associated Station.
Disable Port x **Port Control** register (offset 234h[18:16])	When Set, unconditionally disables the corresponding Port. This is different from the Link Training and Status State Machine (LTSSM) *Disabled* state, in that the Port does not attempt to enter this state. If the Port is idle, it ceases attempting to detect a Receiver. If the Port is up, it immediately returns to the *Detect.Quiet* state and remains there. No Electrical Idle Ordered-Set (EIOS) is sent, which could force any connected device to the *Recovery* state, and then to the LTSSM *Detect* state. The Port remains disabled until its *Disable Port x* bit is Cleared. While the Port is disabled, Receiver termination is disabled and the SerDes that belong to the disabled Port are placed into the L1 Link PM state.
Port x Quiet **Port Control** register (offset 234h[22:20])	When Set, the LTSSM remains in the *Detect.Quiet* state if it is currently in, or returns to, that state. Unlike the *Disable Port x* bits (bits [18:16]), these bits do not force the LTSSM into the *Detect.Quiet* state. Once in the *Detect.Quiet* state, Receiver termination is enabled and the Transmitters are placed in the L0 Link PM state. This Port can now transmit test patterns (PRBS or UTP), with or without an attached device and without being in the *Loopback.Active* state.

Table 16-3. Configuration Bits to Ease PHY Testability *(Cont.)*

Register Bit(s)[a]	Description
Test Pattern x Rate **Port Control** register (offset 234h[27:24])	When Set along with a *Port x Quiet* bit (bits [22:20]), the selected test pattern is transmitted at 5.0 GT/s for the corresponding Port.
Port x Receiver Error Counter **Port Receiver Error Counter** register (offset 248h[23:0])	Contains four 8-bit fields that, when read, return the number of Receiver errors detected by the corresponding Port. The Error Counter saturates at 255. The Counter is Cleared with any Write to the corresponding byte in this register; otherwise, this register is RO.

a. All registers listed in this table are located, as follows:

Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port.

16.6 JTAG Interface

The PEX 8624 provides a Joint Test Action Group (JTAG) Boundary Scan interface, which is used to debug board connectivity for each ball.

16.6.1 *IEEE 1149.1* and *IEEE 1149.6* Test Access Port

The *IEEE Standard 1149.1* Test Access Port (TAP), commonly called the *JTAG Debug Port*, is an architectural standard described in the *IEEE Standard 1149.1-1990*. The *IEEE Standard 1149.6-2003* defines extensions to *1149.1* to support PCI Express SerDes testing. These standards describe methods for accessing internal device facilities, using a four- or five-signal interface.

The JTAG Debug Port, originally designed to support scan-based board testing, is enhanced to support the attachment of debug tools. The enhancements, which comply with the *IEEE Standard 1149.1-1994 Specifications for Vendor-Specific Extensions*, are compatible with standard JTAG hardware for boundary-scan system testing.

- **JTAG Signals** – JTAG Debug Port implements the four required JTAG signals – JTAG_TCK, JTAG_TDI, JTAG_TDO, JTAG_TMS – and optional JTAG_TRST# signal
- **Clock Requirements** – JTAG_TCK signal frequency ranges from 0 to 20 MHz
- **JTAG Reset Requirements** – Refer to Section 16.6.4

16.6.2 JTAG Instructions

The JTAG Debug Port provides the *IEEE Standard 1149.1-1990* BYPASS, EXTEST, SAMPLE, PRELOAD, CLAMP, and IDCODE instructions. *IEEE Standard 1149.6-2003* EXTEST_PULSE and EXTEST_TRAIN instructions are also supported. Table 16-4 lists the JTAG instructions, along with their input codes.

The PEX 8624 returns the JTAG IDCODE values listed in Table 16-5.

Table 16-4. JTAG Instructions

Instruction	Input Code	Comments
BYPASS	3FFF_FFFFh	*IEEE Standard 1149.1-1990*
EXTEST	3FFF_FFE8h	
SAMPLE	3FFF_FFF8h	
PRELOAD	3FFF_FFF8h	
EXTEST_PULSE	3FFB_FFE8h	*IEEE Standard 1149.6-2003*
EXTEST_TRAIN	3FE9_FFE8h	
CLAMP	3FFF_FFEFh	*IEEE Standard 1149.1-1990*
IDCODE	3FFF_FFFEh	

Table 16-5. JTAG IDCODE Values

Silicon Revision	Units	Version	Part Number	PLX Manufacturer Identity	Least Significant Bit
AA	Bits	0000b	1000_0110_0010_0100b	001_1100_1101b	1
	Hex	0h	8624h	1CDh	1h
	Decimal	0	34340	461	1
AB	Bits	0001b	1000_0110_0010_0100b	001_1100_1101b	1
	Hex	1h	8624h	1CDh	1h
	Decimal	1	34340	461	1
BB	Bits	0100b	1000_0110_0010_0100b	001_1100_1101b	1
	Hex	4h	8624h	1CDh	1h
	Decimal	4	34340	461	1

16.6.3 JTAG Boundary Scan

Boundary Scan Description Language (BSDL), IEEE Standard 1149.1-1994, is a supplement to the *IEEE Standard 1149.1-1990* and *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*. BSDL, a subset of the *IEEE 1076-1993 Standard VHSIC Hardware Description Language (VHDL)*, allows a rigorous description of testability features in components which comply with the standard. This standard is used by automated test pattern generation tools for package interconnect tests, and Electronic Design Automation (EDA) tools for synthesized test logic and verification. BSDL supports robust extensions that can be used for internal test generation and to write software for hardware debug and diagnostics.

The primary components of BSDL include the logical Port description, physical ball map, instruction set, and **Boundary** register description.

The logical Port description assigns symbolic names to the device's signal balls. Each ball includes a logical type of *in*, *out*, *in out*, *buffer*, or *linkage* that defines the logical direction of signal flow.

The physical ball map correlates the device's logical Ports to the physical balls of a specific package. A BSDL description can include several physical ball maps, and maps are provided with a unique name.

Instruction set statements describe the bit patterns that must be shifted into the **Instruction** register to place the device in the various test modes defined by the standard. Instruction set statements also support descriptions of instructions that are unique to the PEX 8624.

The **Boundary** register description lists each cell or shift stage of the **Boundary** register. Each cell has a unique number – the cell numbered 0 is the closest to the JTAG Test Data Output (JTAG_TDO), and the cell with the highest number is closest to the JTAG Test Data Input (JTAG_TDI). Each cell includes additional information, *such as*:

- Cell type
- Logical Port associated with the cell
- Logical function of the cell
- Safe value
- Control cell number
- Disable value
- Result value

16.6.4 JTAG Reset Input – JTAG_TRST#

The JTAG_TRST# input is the asynchronous JTAG logic reset. When JTAG_TRST# is Set Low, it causes the PEX 8624's JTAG TAP Controller to initialize. In addition, when the JTAG TAP Controller is initialized, it selects the PEX 8624 standard logic path (core-to-I/O). It is recommended to take the following into consideration when implementing the asynchronous JTAG logic reset on a board:

- If JTAG functionality is required, consider one of the following:
  - JTAG_TRST# input to use a Low-to-High transition once during PEX 8624 boot-up, along with the system PEX_PERST# signal
  - Hold JTAG_TMS input High while clocking the JTAG_TCK input five times
- If JTAG functionality is not required, the JTAG_TRST# input must be directly connected to VSS, to hold the JTAG TAP Controller inactive
- If the PEX 8624's JTAG TAP Controller is not intended to be used by the design, it is recommended that a 1.5KΩ pull-down resistor be connected to the JTAG_TRST# input, to hold the JTAG TAP Controller in the *Test-Logic-Reset* state, which enables standard logic operation

16.7 Port Good Status LEDs

The PEX 8624 provides Port Good outputs, PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]#, that can directly drive external common anode LED modules to provide visual indication that the PHY of that Port's Link is trained to at least x1 width. These outputs can:

- Default to the PORT_GOOD output function (when the STRAP_TESTMODE[3:0] inputs are asserted to 1011b or 1101b), –or–
- Be programmed as a general-purpose I/O, to assume the PORT_GOOD output function

Software can determine:

- Which Lanes have completed PHY linkup, by performing a Memory Read of the **Station *x* Lane Status** register *Lane Up Status* bits in Port 0:
  - Offset 1F4h[7:0] corresponds to Station 0 Ports (Lanes [7-0], respectively)
  - Offset 1F4h[31:24] corresponds to Station 1 Ports (Lanes [31-24], respectively)
  - Offset 270h[7:0] corresponds to Station 2 Ports (Lanes [39-32], respectively)
- Whether the Link for each Port has trained, by reading either the **Link Status** register *Data Link Layer Link Active* bit (offset 78h[29]), or **VC0 Resource Status** register *VC0 Negotiation Pending* bit (offset 160h[17]) in each Port. If the *Data Link Layer Link Active* bit is Set, or *VC0 Negotiation Pending* bit is Cleared, the Link has completed Flow Control (FC) initialization.

  The **Link Status** register can be read by either a PCI Express Configuration Request or Memory Read. The **VC0 Resource Status** register can be read by either a PCI Express Enhanced Configuration access or Memory Read.
- The negotiated Link width of each Port, by reading the **Link Status** register *Negotiated Link Width* field (offset 78h[25:20]) in each Port. This register can be read by either a Configuration Request or Memory Read.

Table 16-6 describes the LED On/Off patterns when connected to the PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]# signals.

Table 16-6. PEX_PORT_GOOD*x*# LED On/Off Patterns, by State

State	LED Pattern
Link is down	Off
Link is up, 5.0 GT/s, all Lanes are up	On
Link is up, 5.0 GT/s, reduced Lanes are up	Blinking, 0.5 seconds On, 0.5 seconds Off
Link is up, 2.5 GT/s, all Lanes are up	Blinking, 1.5 seconds On, 0.5 seconds Off
Link is up, 2.5 GT/s, reduced Lanes are up	Blinking, 0.5 seconds On, 1.5 seconds Off

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Chapter 17 Electrical Specifications

17.1 Introduction

This chapter provides the PEX 8624 electrical specifications.

17.2 Power-Up/Power-Down Sequence

The PEX 8624 does not have power sequencing requirements. The power rails can be powered up and powered down, in any sequence.

17.3 Absolute Maximum Ratings

Warning: ***Maximum limits indicate the temperatures and voltages above which permanent damage can occur. Proper operation at these conditions is not guaranteed, and continuous operation of the PEX 8624 at these limits is not recommended.***

17.4 Power Characteristics

Table 17-1. Absolute Maximum Rating (All Voltages Referenced to VSS System Ground)

Item	Symbol	Absolute Maximum Rating	Units
I/O Interface Supply Voltage	VDD25	-0.5 to +3.6	V
Phase-Locked Loop (PLL) Supply Voltage	VDD25A	-0.5 to +3.6	V
Core (Logic) Supply Voltage	VDD10	-0.3 to +1.5	V
SerDes Analog Supply Voltage	VDD10A	-0.3 to +1.5	V
Input Voltage (2.5V Interface)	V_I	-0.3 to +3.6	V
Operating Ambient Temperature (Commercial)	T_A	0 to +70	°C
Operating Ambient Temperature Commercial Industrial	T_A	 0 to +70 -40 to +85	 °C °C
Storage Temperature	T_{STG}	-65 to +150	°C

Table 17-2. Operating Condition Power Supply Rails

Symbol	Parameter	Min	Typ	Max	Units
VDD10	Digital Core Supply {1.0V ±5%}	0.95	1.0	1.05	V
VDD10A	Analog SerDes Supply {1.0V ±5%}	0.95	1.0	1.05	V
VDD25	I/O Supply {2.5V ±10%}	2.25	2.50	2.75	V
VDD25A	Phase-Locked Loop (PLL) Supply {2.5V ±10%}	2.25	2.50	2.75	V

17.5 Power Consumption Estimates

Table 17-3. Power Consumption Estimates (Watts)

VDD10 (1.0V Digital)		VDD10A (1.0V Digital)		VDD25A (2.5V Digital)		VDD25 (2.5V Digital)		Total	
Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ[a]	Max[b c]
1.86	3.51	0.66	1.77	0.09	0.12	0.01	0.03	2.62	5.43

a. *Typical power based upon 35% traffic, idle Lanes in active L0s Power Management (PM) state, typical power rails (1.0V/2.50V).*

b. *Maximum power based upon 85% traffic, idle Lanes in active L0s Link PM state, maximum power rails (1.05V/2.75V).*

c. *Maximum power is at high temperature and Fast/Fast (FF) process corner silicon.*

17.6 I/O Interface Signal Groupings

Table 17-4. Signal Group PCI Express Analog Interface

Signal Group	Signal Type	Signals	Notes
(a)	PCI Express Output (Transmit)	PEX_PETn*x*, PEX_PETp*x*	Refer to Table 17-6 and Table 17-7
(b)	PCI Express Input (Receive)	PEX_PERn*x*, PEX_PERp*x*	Refer to Table 17-6 and Table 17-8
(c)	PCI Express Differential Clock Input	PEX_REFCLKn, PEX_REFCLKp	Refer to Table 17-6 and Table 17-9
(d)	SerDes External Resistor	REXT_A[4, 3, 0], REXT_B[4, 3, 0]	1.43KΩ ±1%, and refer to Table 17-6

Table 17-5. Signal Group Digital Interface

Signal Group	Signal Type	Signals	Note
(e1)	Digital Input[a]	JTAG_TCK, JTAG_TDI, JTAG_TMS, JTAG_TRST#, STRAP_DEBUG_SEL[1:0], STRAP_FAST_BRINGUP#, STRAP_NT_ENABLE#, STRAP_NT_UPSTRM_PORTSEL[1:0], STRAP_PLL_BYPASS#, STRAP_PROBE_MODE#, STRAP_RESERVED[16, 8, 7, 4:0], STRAP_RESERVED17#, STRAP_SERDES_MODE_EN#, STRAP_STN0_PORTCFG1, STRAP_STN1_PORTCFG0, STRAP_STN2_PORTCFG1, STRAP_TESTMODE[3:0], STRAP_UPSTRM_PORTSEL[3:0]	Refer to Table 17-6
(e2)	Digital Input[a]	HP_MRL_B#, I2C_ADDR[2:0], SHPC_INT#	
(f)	Digital Input with Internal Pull-down Resistor	HP_PWR_GOOD_[C, B, A]	
(g)	Digital Tri-State Output (8 mA)	EE_DI, FATAL_ERR#, JTAG_TDO, PEX_NT_RESET#	
(h)	Bidirectional with Internal Pull-up Resistor (8 mA Drive)	EE_CS#, EE_DO, EE_SK, HP_ATNLED_[C, B, A]#, HP_BUTTON_[C, B, A]#, HP_CLKEN_[C, B, A]#, HP_MRL_[C, A]#, HP_PERST_[C, B, A]#, HP_PRSNT_[C, B, A]#, HP_PWREN_[C, B, A], HP_PWRFLT_[C, B, A]#, HP_PWRLED_[C, B, A]#, GPIO[19:12], GPIO[11, 10, 7, 4:2], PEX_PERST#, PEX_PORT_GOOD[9, 8, 6, 5, 1, 0]#, SPARE[4:0]	
(i)	Bidirectional (Open Drain) with Internal Pull-up Resistor	PEX_INTA#	
(j)	Bidirectional (Open Drain) Schmitt Trigger Input	I2C_SCL0, I2C_SCL1, I2C_SDA0, I2C_SDA1	

a. These signals must be pulled or tied High to VDD25 or Low to VSS (GND), per the instructions provided in Section 3.4, "Signal Ball Descriptions."

Table 17-6. Analog and Digital Interfaces (All Signal Groups) – DC Electrical Characteristics

Symbol	Signal Group	Parameter	Min	Typ	Max	Unit	Conditions
I_{OL}	(g) (h) (i) (j)	Output Low Current	13	22	32	mA	V_{OLmax} = 0.7V
I_{OH}	(g) (h)	Output High Current	8	16	27	mA	V_{OHmin} = 1.7V
V_{IL}	(e1) (e2) (f) (h) (i) (j)	Input Low Voltage	-0.3		0.7	V	
V_{IH}	(e1) (e2) (f) (h) (i) (j)	Input High Voltage	1.7		2.8	V	Refer to Note 1.
V_T	(e1) (e2) (f) (h) (i)	Threshold Point	0.97	1.05	1.14	V	
C_{PIN}	(a) (b) (c) (d) (e1) (e2) (f) (g) (h) (i) (j)	Ball Capacitance			5	pF	
$I_{LEAKAGE}$	(g)	Tri-State Leakage			±10	µA	
	(e1)	Input Leakage			±10	µA	
	(e2)	Input Leakage	-22.6		-47.5	µA	
	(h) (i)	Pull-Up Leakage	-22.6		-47.5	µA	
	(f)	Pull-Down Leakage	22.6		54.4	µA	
R_{PU}	(h) (i)	Pull-Up Impedance	74K	111K	178K	Ω	
R_{PD}	(f)	Pull-Down Impedance	62K	99K	179K	Ω	
V_T	(j)	Schmitt Trigger Rising Threshold	1.2	1.3	1.4	V	
		Schmitt Trigger Falling Threshold	0.84	0.93	1.01	V	
V_{HYS}	(j)	Input Hysteresis	360	370	390	mV	

Note:

1. *The specified maximum V_{IH} is for recommended operating conditions. Because these I/O buffers are 3.3V tolerant, a maximum V_{IH} of 3.6V can safely be applied to these signal balls.*

Table 17-7. 2.5 and 5.0 GT/s PCI Express Transmitter (Signal Group a) – AC and DC Characteristics

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps	The specified UI is equivalent to a tolerance of ±300 ppm. UI does not account for variations caused by Spread-Spectrum Clock (SSC). Refer to Note 1.
$V_{TX-DIFF-PP}$	Differential Peak-to-Peak Output Voltage	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	Measured with compliance test load. $V_{TX-DIFF-PP} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$
$V_{TX-DIFF-PP-LOW}$	Low Power Differential Peak-to-Peak Output Voltage	0.4 (min) 1.2 (max)	0.4 (min) 1.2 (max)	V	Measured with compliance test load. $V_{TX-DIFF-PP-LOW} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ Must be implemented with no de-emphasis.
$V_{TX-DE-RATIO-3.5dB}$	Tx De-Emphasis Level Ratio	3.0 (min) 4.0 (max)	3.0 (min) 4.0 (max)	dB	Ratio of the $V_{TX-DIFF-PP}$ of the 2nd and following bits after a transition, divided by the $V_{TX-DIFF-PP}$ of the 1st bit after a transition. Refer to Note 2.
$V_{TX-DE-RATIO-6dB}$	Tx De-Emphasis Level Ratio	N/A	5.5 (min) 6.5 (max)	dB	Ratio of the $V_{TX-DIFF-PP}$ of the 2nd and following bits after a transition, divided by the $V_{TX-DIFF-PP}$ of the 1st bit after a transition. Refer to Note 2.
$T_{MIN-PULSE}$	Instantaneous Pulse Width (including all jitter sources)	Not specified	0.9 (min)	UI	Measured relative to rising/falling pulse. Refer to Note 3.
T_{TX-EYE}	Minimum Tx Eye Width	0.75 (min)	0.75 (min)	UI	Does not include SSC nor REFCLK jitter. Includes Rj at 10^{-12}. Refer to Notes 3 and 4.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time between the Jitter Median and Maximum Deviation from the Median	0.125 (max)	Not specified	UI	Measured differentially at zero crossing points, after applying the 2.5 GT/s Clock Recovery function. Refer to Note 3.
$T_{TX-HF-DJ-DD}$	Tx Deterministic Jitter > 1.5 MHz	Not specified	0.15 (max)	UI	Deterministic jitter only. Refer to Note 3.
$T_{TX-LF-RMS}$	Tx RMS Jitter < 1.5 MHz	Not specified	3.0	ps RMS	Total energy measured over a 10-kHz to 1.5-MHz range.
$T_{TX-RISE-FALL}$	Tx Rise and Fall Time	0.125 (min)	0.15 (min)	UI	Measured differentially from 20 to 80% of swing. Refer to Note 3.
$T_{RF-MISMATCH}$	Tx Rise/Fall Mismatch	Not specified	0.1 (max)	UI	Measured from 20 to 80% differentially. Refer to Note 3.
BW_{TX-PLL}	Maximum Tx PLL Bandwidth	22 (max)	16 (max)	MHz	Second Order PLL Jitter Transfer Bounding function. Refer to Note 5.

Table 17-7. 2.5 and 5.0 GT/s PCI Express Transmitter (Signal Group a) – AC and DC Characteristics *(Cont.)*

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$BW_{TX-PLL-LO-3DB}$	Minimum Tx PLL Bandwidth for 3-dB Peaking	1.5 (min)	8 (min)	MHz	Second Order PLL Jitter Transfer Bounding function. Refer to Notes 5 and 7.
$BW_{TX-PLL-LO-1DB}$	Minimum Tx PLL Bandwidth for 1-dB Peaking	Not specified	5 (min)	MHz	
$PKG_{TX-PLL1}$	TX PLL Peaking with 8-MHz Minimum Bandwidth	Not specified	3.0 (max)	dB	
$PKG_{TX-PLL2}$	TX PLL peaking with 5-MHz Minimum Bandwidth	Not specified	1.0 (max)	dB	Refer to Note 7.
$RL_{TX-DIFF}$	TX Differential Return Loss (Package + Silicon)	10 (min)	10 (min) for 0.05 to 1.25 GHz 8 (min) for 1.25 to 2.5 GHz	dB	
RL_{TX-CM}	TX Common Mode Return Loss (Package + Silicon)	6 (min)	6 (min)	dB	S_{11} parameter. 2.5 GT/s – Measured over 0.05- to 1.25-GHz range. 5.0 GT/s – Measured over 0.05- to 2.5-GHz range.
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	80 (min) 120 (max)	120 (max)	Ω	Tx DC Differential mode low impedance. Parameter is captured for 5.0 GHz by $RL_{TX-DIFF}$.
$V_{TX-CM-AC-PP}$	Tx AC Common Mode Voltage (5.0 GT/s)	Not specified	100 (max)	mVPP	Refer to Note 6.
$V_{TX-CM-AC-P}$	Tx AC Common Mode Voltage (2.5 GT/s)	20 (max)	Not specified	mVPP	Refer to Note 6.
$I_{TX-SHORT}$	Tx Short Circuit Current Limit	90 (max)	90 (max)	mA	Total current the Transmitter can provide when shorted to its Ground.
$V_{TX-DC-CM}$	Tx DC Common Mode Voltage	0 (min) 3.6 (max)	0 (min) 3.6 (max)	V	Allowed DC common mode voltage, under any conditions.
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage during L0 Link PM state and Electrical Idle	0 (min) 100 (max)	0 (min) 100 (max)	mV	$\lvert V_{TX-CM-DC}$ [during L0] - $V_{TX-CM-Idle-DC}$ [during Electrical Idle]$\rvert \leq$ 100 mV $V_{TX-CM-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} + V_{TX-D-}\rvert$ / 2 [L0] $V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} + V_{TX-D-}\rvert$ / 2 [Electrical Idle]

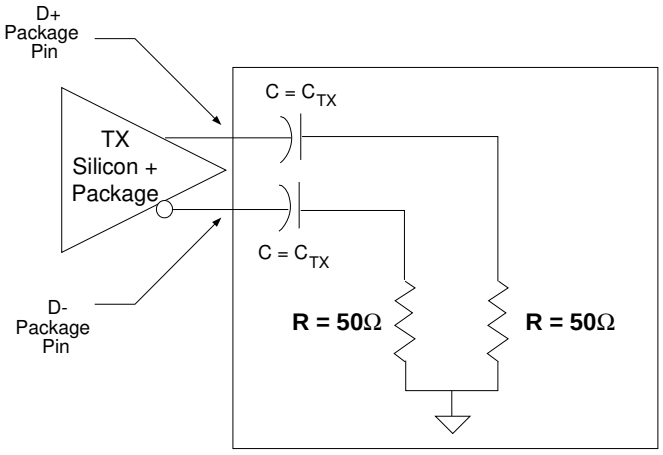
Table 17-7. 2.5 and 5.0 GT/s PCI Express Transmitter (Signal Group a) – AC and DC Characteristics *(Cont.)*

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0 (min) 25 (max)	0 (min) 25 (max)	mV	$\lvert V_{TX\text{-}CM\text{-}DC\text{-}D+} - V_{TX\text{-}CM\text{-}DC\text{-}D-} \rvert \leq 25$ mV $V_{TX\text{-}CM\text{-}DC\text{-}D+} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D+} \rvert$ $V_{TX\text{-}CM\text{-}DC\text{-}D-} = DC_{(avg)}$ of $\lvert V_{TX\text{-}D-} \rvert$
$V_{TX\text{-}IDLE\text{-}DIFF\text{-}AC\text{-}p}$	Electrical Idle Differential Peak Output Voltage	0 (min) 20 (max)	0 (min) 20 (max)	mV	$V_{TX\text{-}IDLE\text{-}DIFFp} = \lvert V_{TX\text{-}Idle\text{-}D+} - V_{TX\text{-}Idle\text{-}D-} \rvert \leq 20$ mV Voltage must be high-pass filtered, to remove any DC component.
$V_{TX\text{-}IDLE\text{-}DIFF\text{-}DC}$	DC Electrical Idle Differential Peak Output Voltage	Not specified	0 (min) 5 (max)	mV	$V_{TX\text{-}IDLE\text{-}DIFF\text{-}DC} = \lvert V_{TX\text{-}Idle\text{-}D+} - V_{TX\text{-}Idle\text{-}D-} \rvert \leq 5$ mV Voltage must be high-pass filtered, to remove any AC component.
$V_{TX\text{-}RCV\text{-}DETECT}$	Amount of Voltage Change Allowed during Receiver Detection	600 (max)	600 (max)	mV	Total amount of voltage change that a Transmitter can apply, to sense whether a low-impedance Receiver is present.
$T_{TX\text{-}IDLE\text{-}MIN}$	Minimum Time Spent in Electrical Idle	20 (min)	20 (min)	ns	Minimum time a Transmitter must be in Electrical Idle. Used by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle Ordered-Set (EIOS).
$T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$	Maximum Time to Transition to a Valid Electrical Idle after Sending an Electrical Idle Ordered-Set	8 (max)	8 (max)	ns	After sending the required EIOS, the Transmitter must meet all Electrical Idle specifications within this time. This is measured from the end of the last UI of the last EIOS to the Tx in Electrical Idle.
$T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$	Maximum Time to Transition to Valid Differential Signaling after Leaving Electrical Idle	8 (max)	8 (max)	ns	Maximum time to transition to valid differential signaling, after leaving Electrical Idle. This is considered a de-bounce time to the Tx.
$T_{CROSSLINK}$	Cross-Link Random Timeout	1.0 (max)	1.0 (max)	ms	Random timeout that helps resolve potential conflicts in the cross-link configuration.
$L_{TX\text{-}SKEW}$	Lane-to-Lane Output Skew	500 ps + 2 UI (max)	500 ps + 4 UI (max)	ps	Static skew between any two Lanes within a single Transmitter.
C_{TX}	AC-Coupling Capacitor	75 (min) 200 (max)	75 (min) 200 (max)	nF	All Transmitters shall be AC-coupled. The AC coupling is required either within the media, or within the transmitting component itself.

Notes:

1. *SSC permits a +0, -5,000 ppm modulation of the clock frequency, at a modulation rate not to exceed 33 kHz.*
2. *Specified at the measurement point into a timing and voltage compliance test load, as illustrated in Figure 17-1.*

Figure 17-1. Compliance Test/Measurement Load



3. *Measurements at 5.0 GT/s require an oscilloscope with a bandwidth of ≥12.5 GHz, or equivalent, while measurements made at 2.5 GT/s require a scope with at least 6.2 GHz bandwidth. Measurements at 5.0 GT/s must de-convolve effects of the compliance test board, to yield an effective measurement at the Tx balls. 2.5 GT/s can be measured within 200 mils of the Tx device's balls; however, de-convolution is recommended. At least 10^6 UI of data must be acquired.*
4. *Transmitter jitter is measured by driving the Tx under test with a low jitter "ideal" clock and connecting the device under test (DUT) to a reference load.*
5. *The Tx PLL bandwidth must lie between the minimum and maximum ranges listed in Table 17-7. PLL peaking must lie below the values listed in Table 17-7.*

   The PLL bandwidth extends from zero (0) up to the value(s) specified in Table 17-7.
6. *Measurement is made over at least 10^6 UI.*
7. *A single combination of PLL bandwidth and peaking is specified for 2.5 GT/s implementations. For 5.0 GT/s, two 20 combinations of PLL bandwidth and peaking are specified to permit designers to make a tradeoff between the two parameters. If the PLL's minimum bandwidth is ≥8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's minimum bandwidth is relaxed to ≥5.0 MHz, then a tighter peaking value of 1.0 dB must be met. In both cases, the maximum PLL bandwidth is 16 MHz.*

Table 17-8. 2.5 and 5.0 GT/s PCI Express Receiver (Signal Group b) – AC and DC Characteristics

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps	UI does not account for variations caused by SSC.
$V_{RX-DIFF-PP-CC}$	Differential Rx Peak-to-Peak Voltage for Common REFCLK Rx Architecture	0.175 (min) 1.2 (max)	0.120 (min) 1.2 (max)	V	$V_{RX-DIFF-PP} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$
T_{RX-EYE}	Receiver Eye Time Opening	0.40 (min)	N/A	UI	Minimum eye time at Rx pins to yield a 10^{-12} Bit Error Rate. Receiver eye margins are defined into a 2 x 50Ω reference load.
$T_{RX-TJ-CC}$	Maximum Rx Inherent Timing Error	N/A	0.40 (max)	UI	Maximum Rx inherent total timing error for common REFCLK Rx architecture. Refer to Note 1.
$T_{RX-DJ-DD-CC}$	Maximum Rx Inherent Deterministic Timing Error	N/A	0.30 (max)	UI	Maximum Rx inherent deterministic timing error for common REFCLK Rx architecture. Refer to Note 1.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time Delta between the Median and Deviation from the Median	0.3 (max)	Not specified	UI	
$T_{RX-MIN-PULSE}$	Minimum Width Pulse at Rx	Not specified	0.6 (min)	UI	Measured to account for worst Tj at 10^{-12} Bit Error Rate.
$V_{RX-MAX-MIN-RATIO}$	Minimum/ Maximum Pulse Voltage on Consecutive UI	Not specified	5 (max)	Ratio	Rx eye must simultaneously meet V_{RX-EYE} limits.
$BW_{RX-PLL-HI}$	Maximum Rx PLL Bandwidth	22 (max)	16 (max)	MHz	Second Order PLL Jitter Transfer Bounding function. Refer to Note 2.
$BW_{RX-PLL-LO-3DB}$	Minimum Rx PLL Bandwidth for 3-dB Peaking	1.5 min	8 (min)	MHz	
$BW_{RX-PLL-LO-1DB}$	Minimum Rx PLL Bandwidth for 1-dB Peaking	Not specified	5 (min)	MHz	
$PKG_{RX-PLL1}$	Rx PLL Peaking with 8-MHz Minimum Bandwidth	Not specified	3.0	dB	
$PKG_{RX-PLL2}$	Rx PLL Peaking with 5-MHz Minimum Bandwidth	Not specified	1.0	dB	

Table 17-8. 2.5 and 5.0 GT/s PCI Express Receiver (Signal Group b) – AC and DC Characteristics *(Cont.)*

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$RL_{RX-DIFF}$	Rx Differential Return Loss (Package + Silicon)	10 (min)	10 (min) for 0.05 to 1.25 GHz 8 (min) for 1.25 to 2.5 GHz	dB	Refer to Note 3.
RL_{RX-CM}	Common Mode Return Loss	6 (min)	6 (min)	dB	Refer to Note 3.
Z_{RX-DC}	Rx DC Single-Ended Impedance	40 (min) 60 (max)	40 (min) 60 (max)	Ω	Required Rx D+ and D- DC impedance (50Ω ±20% tolerance). Refer to Note 4.
$Z_{RX-DIFF-DC}$	DC Differential Rx Impedance	80 (min) 120 (max)	Not specified	Ω	Rx DC Differential mode impedance. Parameter is captured for 5.0 GHz by $RL_{RX-DIFF}$. Refer to Note 4.
$V_{RX-CM-AC-P}$	Rx AC Common Mode Voltage	150 (max)	150 (max)	mVP	Measured at Rx pins, into a pair of 50Ω terminations into Ground. Refer to Note 5.
$Z_{RX-HIGH-IMP-DC-POS}$	DC Input Common Mode Input Impedance for Voltage >0 during Reset or Power-Down	50K (min)	50K (min)	Ω	Rx DC common mode impedance with the Rx terminations not powered, measured over the range 0 to 200 mV (with respect to Ground). Refer to Note 6.
$Z_{RX-HIGH-IMP-DC-NEG}$	DC Input Common Mode Input Impedance for Voltage <0 during Reset or Power-Down	1.0K (min)	1.0K (min)	Ω	Rx DC common mode impedance with the Rx terminations not powered, measured over the range -150 to 0 mV (with respect to Ground). Refer to Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65 (min) 175 (max)	65 (min) 175 (max)	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the Receiver's package pins.
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Idle Detect Threshold Integration Time	10 (max)	10 (max)	ms	An un-expected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ to signal an unexpected idle condition.
$L_{RX-SKEW}$	Total Lane-to-Lane Skew	20 (max)	8 (max)	ns	Across all Lanes on a Port. Includes variation in the length of a SKIP Ordered-Set at the Rx, as well as any delay differences arising from the interconnect itself. Refer to Note 7.

Notes:

1. *The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing.*

2. *Two combinations of PLL bandwidth and peaking are specified at 5.0 GT/s, to permit designers to make trade-offs between the two parameters. If the PLL's minimum bandwidth is ≥8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's minimum bandwidth is relaxed to ≥5.0 MHz, then a tighter peaking value of 1.0 dB must be met.*

   A PLL bandwidth extends from zero up to the value(s) defined as the minimum or maximum in Table 17-8. For 2.5 GT/s, a single PLL bandwidth and peaking value of 1.5 to 22 MHz and 3.0 dB are defined.

3. *Measurements must be made for both common mode and differential return loss. In both cases, the DUT must be powered up and DC-isolated, and its D+/D- inputs must be in the low-Z state.*

4. *The Rx DC Single-Ended Impedance must be present when the Receiver terminations are first enabled, to ensure that the Receiver Detect occurs properly. Compensation of this impedance can start immediately, and the Rx Single-Ended Impedance (constrained by RL_{RX-CM} to 50Ω ±20%) must be within the specified range by the time Detect is entered.*

5. *Common mode peak voltage is defined by the expression:*

   $max\{|(Vd+ - Vd-) - V\text{-}CMDC|\}$

6. *$Z_{RX-HIGH-IMP-DC-NEG}$ and $Z_{RX-HIGH-IMP-DC-POS}$ are defined, respectively, for negative and positive voltages at the input of the Receiver. Transmitter designers must comprehend the large difference between >0 and <0 Rx impedances when designing Receiver detect circuits.*

7. *The $L_{RX-SKEW}$ parameter exists to handle repeaters that re-generate REFCLK and introduce differing numbers of skips on different Lanes.*

Table 17-9. PCI Express Differential Clock (Signal Group c) – AC and DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
F_{REFCLK}	Reference Clock Frequency		100		MHz	1
$T_{REFCLK-HF-RMS}$	High frequency jitter -> 1.5 MHz to Nyquist RMS jitter after applying filter functions, per the *PCI Express Base r2.0*			3.1	ps RMS	
$T_{REFCLK-LF-RMS}$	Low frequency jitter – 10 kHz to 1.5 MHz jitter after applying filter functions, per the *PCI Express Base r2.0*			3.0	ps RMS	
$T_{REFCLK-SSC-RES}$	SSC residual after applying filter functions, per the *PCI Express Base r2.0*			75	ps	
V_{SW}	Differential Voltage Swing (0-to-peak)	125	200	800	mV	
	Differential Voltage Swing (peak-to-peak)	250	400	1,600	mV	
T_R/T_F	Clock Input Rise/Fall Time	0.6		4.0	V/ns	2
DC_{REFCLK}	Input Clock Duty Cycle	45	50	55	%	
R_{TERM}	Input Parallel Termination (Single-ended)		50		Ω	
	Input Parallel Termination (Differential)		100		Ω	
PPM	Reference Clock Tolerance	-300		+300	ppm	

Notes:

1. *PEX_REFCLKn/p must be AC-coupled. Use a 0.01 to 0.1 µF capacitor.*
2. *Specified at 20 to 80% points at the package balls. Measured differentially in the region of +150 mV and -150 mV.*

17.7 Transmit Drive Characteristics

The Drive Current and Transmit Equalization functions are programmable, to allow for optimization of different backplane lengths and materials.

The Transmit Drive Level is programmable (5-bit, per SerDes/Lane), to provide differential swing within the range listed in Table 17-10. The **SerDes Drive Level *x*** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets B84h through B90h) provide access to all 24 Lanes for Drive Level programmability.

The Transmitter also incorporates programmable (5-bit, per SerDes/Lane) de-emphasis, to provide equalization to compensate for FR4 channel effects within the range listed in Table 17-10. The **Post-Cursor Emphasis Level *x*** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets B94h through BA0h) provide access to all 24 Lanes for de-emphasis programmability.

The Transmit_Drive_Level[4:0] and Post-Cursor_Emphasis_Level[4:0] bits are used together, to program the differential swing, as well as the dB loss for optimum Tx drive across the intended backplane.

Table 17-10 lists all possible combinations of Tx DRV_LVL[4:0] and POST_CURSOR[4:0], to achieve minimum 800 mV transition amplitude and the resulting de-emphasis (in decibels, dB). Of these, only certain combinations yield the specified 3 to 4 dB or 5.5 to 6.5 dB de-emphasis, per the *PCI Express Base r2.0* (**highlighted in bold**). All combinations are listed, however, to provide maximum flexibility for fine-tuning the Tx drive characteristics to a specific backplane.

Table 17-10. Tx Programmable Drive and De-Emphasis Levels

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
01h	11h	820	789	0.34	
	12h	849	818	0.33	
	13h	876	845	0.31	
02h	10h	799	742	0.65	
	11h	830	773	0.61	
	12h	858	802	0.58	
	13h	884	829	0.56	
03h	10h	809	727	0.93	
	11h	839	758	0.88	
	12h	867	787	0.84	
	13h	893	814	0.80	
04h	10h	818	712	1.22	
	11h	848	743	1.15	
	12h	876	772	1.09	
	13h	901	799	1.04	

Table 17-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
05h	0Fh	797	664	1.59	
	10h	828	697	1.50	
	11h	857	728	1.41	
	12h	884	758	1.34	
	13h	909	785	1.27	
	1Fh	796	663	1.59	
06h	0Fh	806	649	1.88	
	10h	837	682	1.77	
	11h	866	714	1.68	
	12h	892	743	1.59	
	13h	916	770	1.51	
	1Fh	806	649	1.88	
07h	0Fh	816	635	2.18	
	10h	846	668	2.05	
	11h	874	700	1.94	
	12h	900	729	1.83	
	13h	924	756	1.74	
	1Fh	816	635	2.18	
08h	0Fh	825	620	2.48	
	10h	855	654	2.33	
	11h	883	685	2.20	
	12h	908	715	2.08	
	13h	931	742	1.98	
	1Fh	825	620	2.47	
09h	0Eh	802	571	2.95	
	0Fh	834	607	2.77	
	10h	863	640	2.60	
	11h	891	671	2.46	
	12h	916	701	2.33	
	13h	938	728	2.21	
	1Eh	802	571	2.96	
	1Fh	834	606	2.77	

Table 17-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
0Ah	0Eh	811	557	3.27	
	0Fh	843	593	3.06	
	10h	872	626	2.88	
	11h	899	658	2.71	
	12h	923	687	2.57	
	13h	945	714	2.43	
	1Eh	811	557	**3.27**	
	1Fh	843	593	**3.06**	
0Bh	0Eh	821	543	**3.58**	
	0Fh	851	579	**3.35**	
	10h	880	612	**3.15**	
	11h	906	644	2.97	
	12h	930	673	2.81	
	13h	951	700	2.66	
	1Eh	820	543	**3.58**	
	1Fh	851	579	**3.35**	
0Ch	0Dh	797	492	4.19	
	0Eh	829	530	**3.89**	
	0Fh	860	566	**3.64**	
	10h	888	599	**3.42**	
	11h	914	630	**3.22**	
	12h	937	660	**3.05**	
	13h	958	687	2.89	
	1Dh	797	492	4.19	
	1Eh	829	530	**3.89**	
	1Fh	860	565	**3.64**	
0Dh	0Dh	806	479	4.52	
	0Eh	838	517	4.20	
	0Fh	868	552	**3.93**	-3.5 dB default for PEX 8624
	10h	896	586	**3.69**	
	11h	921	617	**3.48**	
	12h	944	646	**3.29**	
	13h	964	673	**3.11**	
	1Dh	806	479	4.52	
	1Eh	838	516	4.20	
	1Fh	868	552	**3.93**	

Table 17-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
0Eh	0Dh	815	466	4.86	
	0Eh	847	503	4.51	
	0Fh	876	539	4.22	
	10h	903	572	**3.96**	
	11h	928	604	**3.73**	
	12h	950	633	**3.53**	
	13h	970	660	**3.34**	
	1Dh	815	466	4.86	
	1Eh	846	503	4.52	
	1Fh	876	539	4.22	
0Fh	0Dh	824	453	5.20	
	0Eh	855	490	4.83	
	0Fh	884	526	4.51	
	10h	911	559	4.23	
	11h	935	591	**3.98**	
	12h	957	620	**3.76**	
	13h	975	647	**3.56**	
	1Dh	823	453	5.20	
	1Eh	855	490	4.83	
	1Fh	884	526	4.51	
10h	0Ch	799	399	**6.02**	
	0Dh	832	439	**5.55**	
	0Eh	863	477	5.15	
	0Fh	892	513	4.81	
	10h	918	546	4.51	
	11h	942	578	4.25	
	12h	963	607	4.01	
	13h	981	634	3.79	
	1Ch	799	399	**6.02**	
	1Dh	832	439	**5.55**	
	1Eh	863	477	5.15	
	1Fh	892	513	4.81	

Table 17-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
11h	0Ch	808	387	**6.40**	
	0Dh	841	427	**5.89**	
	0Eh	871	464	5.46	
	0Fh	899	500	5.10	
	10h	925	533	4.78	
	11h	948	565	4.50	
	12h	969	594	4.24	
	13h	986	621	4.02	
	1Ch	808	387	**6.40**	
	1Dh	840	427	**5.89**	
	1Eh	871	464	5.46	
	1Fh	899	500	5.10	
12h	0Ch	816	374	6.77	
	0Dh	849	414	**6.23**	
	0Eh	879	452	**5.78**	
	0Fh	906	487	5.39	
	10h	932	521	5.05	
	11h	954	552	4.75	
	12h	974	582	4.48	
	13h	991	609	4.24	
	1Ch	816	374	6.78	
	1Dh	849	414	6.23	
	1Eh	879	452	5.78	
	1Fh	906	487	5.39	
13h	0Ch	825	362	7.16	
	0Dh	857	402	6.58	
	0Eh	886	439	6.09	
	0Fh	913	475	5.68	
	10h	938	509	5.32	
	11h	960	540	5.00	
	12h	980	569	4.72	
	13h	996	596	4.46	
	1Bh	795	326	7.76	
	1Ch	825	362	7.16	
	1Dh	856	402	6.58	
	1Eh	886	439	**6.09**	
	1Fh	913	475	**5.68**	

Table 17-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
14h	0Bh	799	308	8.29	
	0Ch	833	350	7.54	
	0Dh	864	389	6.93	
	0Eh	893	427	**6.41**	
	0Fh	920	463	**5.97**	
	10h	944	496	**5.59**	
	11h	966	528	5.25	
	12h	985	557	4.95	
	13h	1,001	584	4.68	
	1Bh	804	313	8.19	
	1Ch	833	349	7.54	
	1Dh	864	389	6.93	
	1Eh	893	427	**6.41**	
	1Fh	920	463	**5.97**	
15h	0Bh	808	296	8.73	
	0Ch	841	337	7.93	
	0Dh	872	377	7.28	-6 dB default for PEX 8624-AA
	0Eh	901	415	6.73	-6 dB default for PEX 8624-AB, BB
	0Fh	927	451	**6.26**	
	10h	950	484	**5.86**	
	11h	972	516	**5.50**	
	12h	990	545	5.19	
	13h	1,006	572	4.90	
	1Bh	812	301	8.62	
	1Ch	841	337	7.93	
	1Dh	872	377	7.28	
	1Eh	900	415	6.73	
	1Fh	927	451	**6.62**	

Table 17-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
16h	0Bh	816	284	9.18	
	0Ch	849	326	8.32	
	0Dh	879	365	7.63	
	0Eh	907	403	7.05	
	0Fh	933	439	6.56	
	10h	956	472	**6.13**	
	11h	977	504	**5.76**	
	12h	995	533	5.42	
	13h	1,010	560	5.12	
	1Bh	820	289	9.05	
	1Ch	849	325	8.33	
	1Dh	879	365	7.63	
	1Eh	907	403	7.05	
	1Fh	933	439	6.56	
17h	0Bh	824	272	9.63	
	0Ch	856	314	8.72	
	0Dh	886	354	7.98	
	0Eh	914	391	7.37	
	0Fh	939	427	6.85	
	10h	962	460	**6.40**	
	11h	982	492	**6.01**	
	12h	999	521	**5.65**	
	13h	1,014	548	5.34	
	1Bh	828	277	9.50	
	1Ch	856	314	8.72	
	1Dh	886	353	7.99	
	1Eh	914	391	7.37	
	1Fh	939	427	6.85	

Table 17-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
18h	0Ah	798	216	11.35	
	0Bh	832	260	10.10	
	0Ch	864	302	9.13	
	0Dh	893	342	8.35	
	0Eh	921	380	7.70	
	0Fh	945	415	7.15	
	10h	968	449	6.68	
	11h	987	480	**6.26**	
	12h	1,004	509	**5.89**	
	13h	1,018	537	**5.56**	
	1Ah	802	222	11.16	
	1Bh	836	266	9.96	
	1Ch	864	302	9.13	
	1Dh	893	342	8.35	
	1Eh	921	379	7.70	
	1Fh	945	415	7.15	
19h	0Ah	806	204	11.91	
	0Bh	840	249	10.57	
	0Ch	871	290	9.54	
	0Dh	900	330	8.71	
	0Eh	927	368	8.02	
	0Fh	951	404	7.45	
	10h	973	437	6.95	
	11h	992	469	6.51	
	12h	1,008	498	**6.12**	
	13h	1,021	525	**5.78**	
	1Ah	810	210	11.71	
	1Bh	844	254	10.42	
	1Ch	871	290	9.54	
	1Dh	900	330	8.71	
	1Eh	927	368	8.03	
	1Fh	951	404	7.45	

Table 17-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
1Ah	0Ah	814	193	12.49	
	0Bh	847	237	11.05	
	0Ch	878	279	9.95	
	0Dh	907	319	9.08	
	0Eh	933	357	8.35	
	0Fh	957	392	7.74	
	10h	978	426	7.22	
	11h	996	457	6.76	
	12h	1,012	487	**6.36**	
	13h	1,025	514	**6.00**	
	1Ah	818	199	12.28	
	1Bh	851	243	10.89	
	1Ch	878	279	9.96	
	1Dh	907	319	9.08	
	1Eh	933	357	8.35	
	1Fh	957	392	7.74	
1Bh	0Ah	821	182	13.09	
	0Bh	854	226	11.55	
	0Ch	885	268	10.38	
	0Dh	913	308	9.45	
	0Eh	939	346	8.68	
	0Fh	962	381	8.04	
	10h	983	415	7.50	
	11h	1,000	446	7.01	
	12h	1,016	475	6.59	
	13h	1,028	503	**6.22**	
	1Ah	826	188	12.86	
	1Bh	858	232	11.38	
	1Ch	885	268	10.38	
	1Dh	913	308	9.45	
	1Eh	939	345	8.69	
	1Fh	962	381	8.04	

Table 17-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
1Ch	0Ah	829	171	13.71	
	0Bh	861	215	12.06	
	0Ch	892	257	10.81	
	0Dh	919	297	9.82	
	0Eh	945	334	9.02	
	0Fh	967	370	8.35	
	10h	987	404	7.77	
	11h	1,004	435	7.27	
	12h	1,019	464	6.83	
	13h	1,031	491	**6.44**	
	19h	799	131	15.71	
	1Ah	833	177	13.46	
	1Bh	865	221	11.87	
	1Ch	891	257	10.81	
	1Dh	919	297	9.83	
	1Eh	944	334	9.02	
	1Fh	967	370	8.35	
1Dh	09h	802	114	16.95	
	0Ah	836	160	14.36	
	0Bh	868	204	12.58	
	0Ch	898	246	11.25	
	0Dh	925	286	10.20	
	0Eh	950	324	9.36	
	0Fh	972	359	8.65	
	10h	992	393	8.05	
	11h	1,008	424	7.52	
	12h	1,022	454	7.06	
	13h	1,034	481	6.65	
	19h	806	120	16.55	
	1Ah	841	166	14.09	
	1Bh	872	210	12.38	
	1Ch	898	246	11.25	
	1Dh	925	286	10.21	
	1Eh	950	323	9.36	
	1Fh	972	359	8.65	

Table 17-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
1Eh	09h	809	103	17.90	
	0Ah	843	149	15.04	
	0Bh	875	193	13.11	
	0Ch	904	235	11.69	
	0Dh	931	275	10.59	
	0Eh	955	313	9.69	
	0Fh	977	349	8.95	
	10h	996	382	8.32	
	11h	1,012	413	7.77	
	12h	1,025	443	7.29	
	13h	1,037	470	6.87	
	19h	814	109	17.44	
	1Ah	848	155	14.74	
	1Bh	879	199	12.90	
	1Ch	904	235	11.70	
	1Dh	931	275	10.59	
	1Eh	955	313	9.70	
	1Fh	977	348	8.95	
1Fh	09h	817	93	18.91	
	0Ah	850	139	15.75	
	0Bh	881	183	13.66	
	0Ch	910	225	12.15	
	0Dh	936	265	10.98	
	0Eh	960	302	10.04	
	0Fh	981	338	9.26	
	10h	999	371	8.60	
	11h	1,015	403	8.03	
	12h	1,028	432	7.53	
	13h	1,039	459	7.09	
	19h	821	99	18.40	
	1Ah	854	145	15.43	
	1Bh	885	188	13.44	
	1Ch	910	225	12.15	
	1Dh	936	264	10.98	
	1Eh	960	302	10.04	
	1Fh	981	338	9.26	

17.7.1 Default Transmit Settings

Table 17-11 lists the default values of the Transmit Drive and Post-Cursor De-Emphasis levels (**SerDes Drive Level *x*** and **Post-Cursor Emphasis Level *x*** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets B84h through B90h and B94h through BA0h, respectively)).

Table 17-11. Default Transmit Settings

Silicon Revision	Mode (dB)	Link Speed (GT/s)	DRV_LVL [4:0]	POST_CURSOR [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	Equalization[a] (dB)
All	-3.5	2.5	0Fh	0Dh	868	552	-3.93
AA	-6	5.0	0Dh	15h	872	377	-7.28
AB, BB	-6	5.0	0Eh	15h	901	415	-6.73[b]

a. dB Equalization formula:

```
20 x log[(Non-Transition Amplitude) / (Transition Amplitude)]
```

b. The -6 dB Setting is slightly larger than the maximum -6.5 dB specification, to better compensate for FR4 loss characteristics across a typical backplane application.

17.8 Receive Characteristics

The Receiver circuit includes programmable equalization, to further compensate for the low-pass FR4 loss characteristics of the channel.

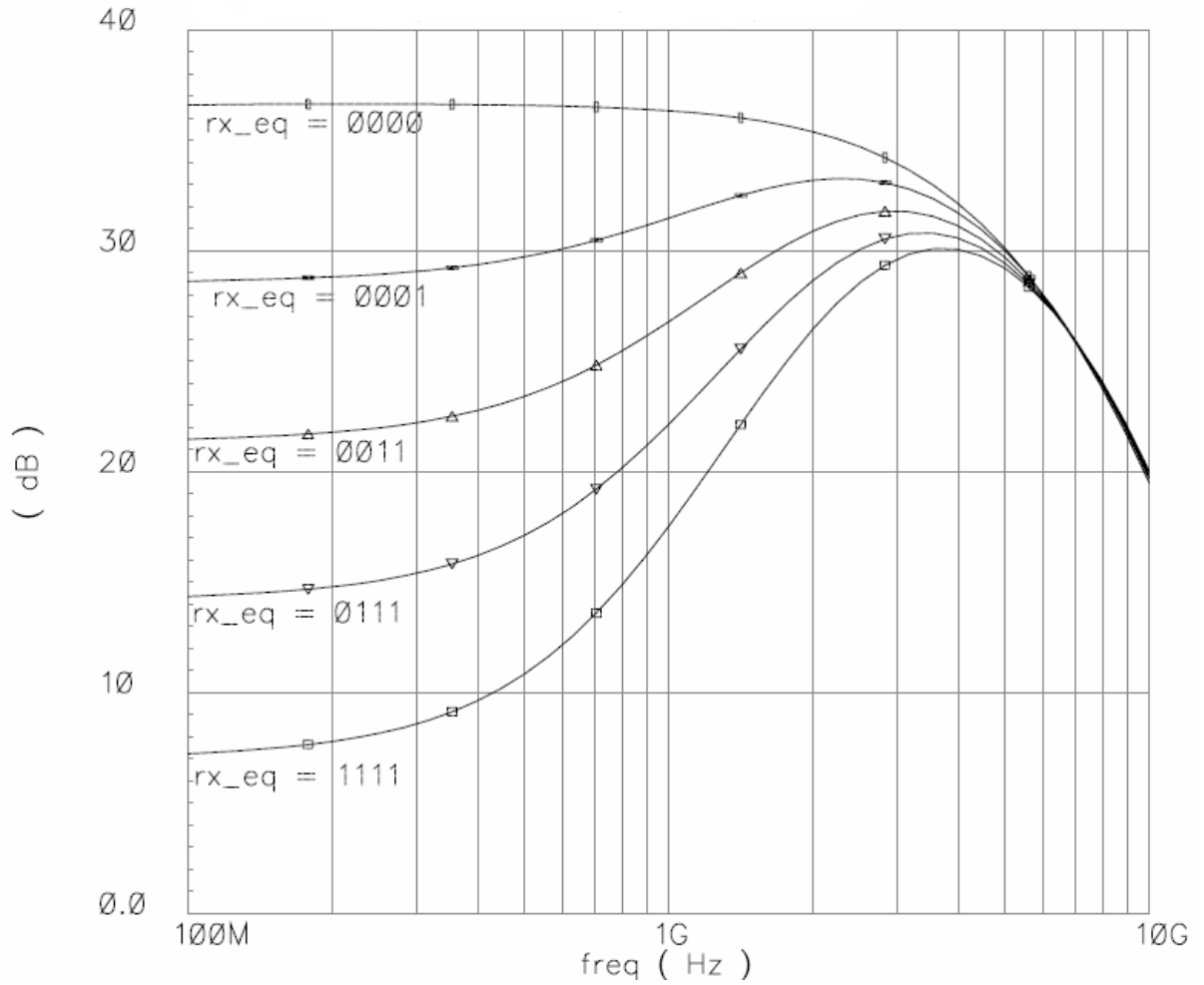
17.8.1 Receive Equalization

Table 17-12 lists the programmable bits used for controlling the Receiver circuit's electrical characteristics, to mitigate the effects of signal loss and distortion across the PCB channel. The **Receiver Equalization Level *x*** registers (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offsets BA4h and BA8h) provide access to all 24 Lanes for Rx Equalization programmability. Figure 17-2 illustrates the Rx Equalization frequency characteristics.

Table 17-12. Receiver Equalization Settings

Rx Equalization[3:0]	Equalization
0h (default)	Off
1h	Minimum
2h to 3h	Low
4h to 6h	Low to Medium
7h to 9h	Medium
Ah to Dh	High to Medium
Eh to Fh	Maximum

Figure 17-2. Rx Equalization Frequency Characteristics



17.8.2 Receiver Electrical Idle

The Receiver circuit contains a signal detect circuit that is used to detect signal idling at the input. The threshold to detect the idle level is programmable, using the **Signal Detect Level** register (Port 0, 4, or 8, and also NT Port Virtual Interface if Port 0 is the NT Port, offset BACh). A value of 00b provides the lowest signal voltage level detection threshold.

Chapter 18 Thermal and Mechanical Specifications

18.1 Thermal Characteristics

The PEX 8624 does not include a heat sink. The information described in this section is based upon sample thermal performance when a heat sink is used with the PEX 8624, and is provided for reference only.

18.1.1 Sample Thermal Data

Table 18-1 lists the sample thermal data for the PEX 8624, with and without a heat sink, at various temperatures.

Table 18-1. Thermal Resistance Matrix (19 x 19 mm^2 FCBGA Package, with Heat Spreader)[a b c g]

Maximum Power (W)	Θ_{JC} (°C/W)	Heat Sink and Heat Sink Size (mm)	Ambient Temperature (°C)	Maximum Θ_{JA} (°C/W)	Air Flow (m/s)	Θ_{JA} 4-Layer Jedec Board (°C/W)	Θ_{JA} 8-Layer Board (°C/W)	4-Layer Board Minimum Ambient Temperature (°C)	8-Layer Board Minimum Ambient Temperature (°C)
5.40	0.43	No	70	7.41	0.00	13.49	8.66	-19.97	**-12.82**
					1.00	9.98	7.46	-14.77	-11.04
					2.00	8.63	7.02	-12.77	-10.39
			75	6.48	0.00	13.49	8.66	-19.97	-12.82
					1.00	9.98	7.46	-14.77	**-11.04**
					2.00	8.63	7.02	-12.77	-10.39
			80	5.56	0.00	13.49	8.66	-19.97	-12.82
					1.00	9.98	7.46	-14.77	-11.04
					2.00	8.63	7.02	-12.77	-10.39
			85	4.63	0.00	13.49	8.66	-19.97	-12.82
					1.00	9.98	7.46	-14.77	-11.04
					2.00	8.63	7.02	-12.77	-10.39
		Yes[d] 21.6 x 21.6 x 13.21	70	7.41	0.00	11.05	9.65	-16.35	-14.28
					1.00	5.92	5.20	**-8.76**	-7.70
					2.00	4.72	4.20	-6.99	-6.22
			75	6.48	0.00	11.05	9.65	-16.35	-14.28
					1.00	5.92	5.20	**-8.76**	-7.70
					2.00	4.72	4.20	-6.99	-6.22
			80	5.56	0.00	11.05	9.65	-16.35	-14.28
					1.00	5.92	5.20	**-8.76**	-7.70
					2.00	4.72	4.20	-6.99	-6.22
			85	4.63	0.00	11.05	9.65	-15.25	-13.32
					1.00	5.92	5.20	-8.17	**-7.18**
					2.00	4.72	4.20	-6.51	-5.80
		Yes[e] 19 x 19 x 10	70	7.41	0.00	12.05	7.78	-17.83	**-11.51**
					1.00	7.21	5.54	-10.67	-8.20
					2.00	5.84	4.95	-8.64	-7.33
			75	6.48	0.00	12.05	7.78	-17.83	-11.51
					1.00	7.21	5.54	**-10.67**	-8.20
					2.00	5.84	4.95	-8.64	-7.33
			80	5.56	0.00	12.05	7.78	-17.83	-11.51
					1.00	7.21	5.54	-10.67	-8.20
					2.00	5.84	4.95	**-8.64**	-7.33
			85	4.63	0.00	12.05	7.78	-17.83	-11.51
					1.00	7.21	5.54	-10.67	-8.20
					2.00	5.84	4.95	-8.64	**-7.33**
		Yes[f] 19 x 19 x 15	70	7.41	0.00	10.78	7.48	-15.95	**-11.07**
					1.00	6.21	5.01	-9.19	-7.41
					2.00	5.18	4.34	-7.67	-6.42
			75	6.48	0.00	10.78	7.48	-15.95	**-11.07**
					1.00	6.21	5.01	-9.19	-7.41
					2.00	5.18	4.34	-7.67	-6.42
			80	5.56	0.00	10.78	7.48	-15.95	-11.07
					1.00	6.21	5.01	**-9.19**	-7.41
					2.00	5.18	4.34	-7.67	-6.42
			85	4.63	0.00	10.78	7.48	-15.95	-11.07
					1.00	6.21	5.01	-9.19	-7.41
					2.00	5.18	4.34	**-7.67**	-6.42

Notes:

a. The highlighted cells indicate that the thermal solution meets the Minimal Thermal Solution Requirement for the given Ambient Temperature.

b. Data provided in Table 18-1 reflects values for Silicon Revision BB only.

c. Maximum Junction Temperature (Tj) for Reliability is 125°C.

d. 21.6 x 21.6 x 13.21 mm^3 heat sink (80600B00850) from Aavid Thermalloy, LLC. TIM of 0.13-mm thick and 1W/mK Thermal conductivity.

e. 19 x 19 x 10 mm^3 heat sink S1519-10W from Alpha Novatech, Inc.

f. 19 x 19 x 15 mm^3 heat sink S1519-15W from Alpha Novatech, Inc.

*g. The PEX 8624 has been qualified to support an Extended Operating Temperature range of -10 to 85°C. For high-temperature environments (70 to 85°C), a heat sink and/or air flow might be required. Refer to Table 18-1 to select the appropriate thermal solution for your system. For low-temp environments (0 to -10°C), cold starts are **not supported**. Be sure to allow the PEX 8624 to self-heat (hold in reset) for 10 seconds, before starting standard switch operation.*

18.2 General Package Specifications

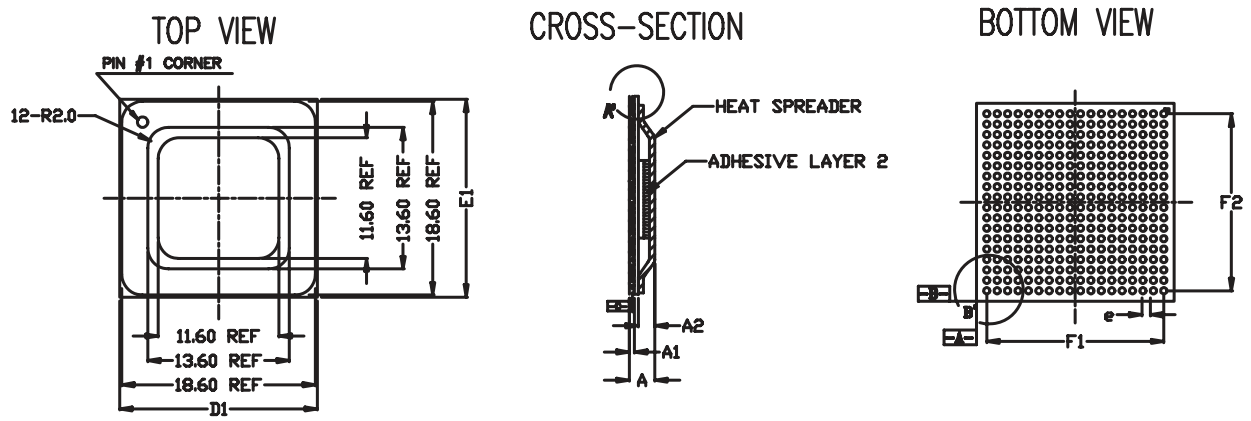
Table 18-2 lists general package specifications. For a more complete list, refer to Figure 18-1.

Table 18-2. General Package Specifications

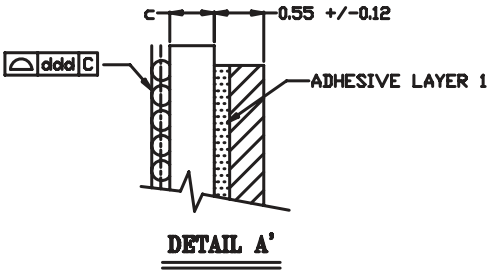
Parameter	Specification
Package Type	Flip-Chip Ball Grid Array (FCBGA) with Heat Spreader
Number of Balls	324
Package Dimensions	19 x 19 mm^2 (approximately 2.28 ±0.20-mm high)
Ball Matrix Pattern	18 x 18
Ball Pitch	1.0 mm
Ball Diameter	0.60 ±0.1 mm
Ball Spacing	0.40 mm

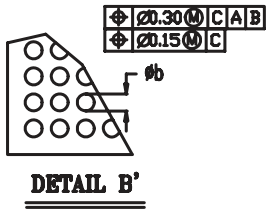
18.3 Mechanical Dimensions

Figure 18-1. Package Mechanical Dimensions (19 x 19 mm^2 FCBGA Package with Heat Spreader)

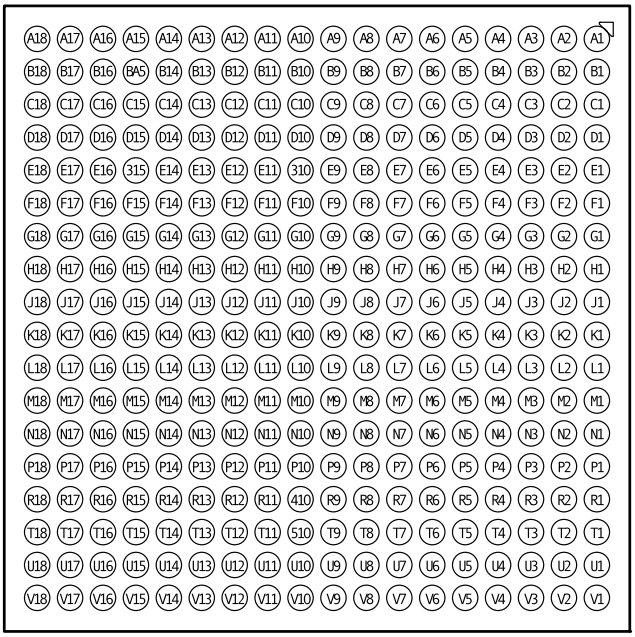


Symbol	UNITS IN MILLIMETER		
	MIN	NOM	MAX
c	0.48	0.58	0.68
A	2.08	2.28	2.48
A1	0.40	0.50	0.60
A2	1.08	1.20	1.32
øb	0.50	0.60	0.70
D1	18.80	19.00	19.20
E1	18.80	19.00	19.20
F1	—	17.00	—
F2	—	17.00	—
e	—	1.00	—
ddd	—	—	0.15





BALL NAMES (BOTTOM VIEW)



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Appendix A General Information

A.1 Product Ordering Information

Contact your local PLX Sales Representative for ordering information.

Table A-1. Product Ordering Information

Part Numbers	Description
PEX8624-BB50RBC F	PEX 8624 24-Lane/6-Port PCI Express Gen 2 Switch FCBGA Lead-Free Package (19 x 19 mm^2, 324-ball) with Heat Spreader, Commercial Temperature
PEX8624-BB50BI F	PEX 8624 24-Lane/6-Port PCI Express Gen 2 Switch FCBGA Lead-Free Package (19 x 19 mm^2, 324-ball) with Heat Spreader, Industrial Temperature
where	PEX – PCI Express Product Family 8624 – Part Number BB – Silicon Revision 50 – Signaling Rate (5.0 GT/s) R – REXT fix for Enhanced Noise Immunity B – Flip-Chip Ball Grid Array C – Commercial Temperature I – Industrial Temperature F – Lead-free 2nd Level Interconnect (2LI) Solder bump First Level Interconnect (FLI) contains lead per RoHS exemption for Flip-Chip
PEX 8624-BB RDK	PEX 8624 Rapid Development Kit with x8 Edge Connector
x1 Adapter	PCI Express x8 to x1 Adapter
x4 Adapter	PCI Express x8 to x4 Adapter

A.2 United States and International Representatives and Distributors

PLX Technology, Inc., representatives and distributors are listed at www.plxtech.com.

A.3 Technical Support

PLX Technology, Inc., technical support information is listed at www.plxtech.com/support, or call 800 759-3735 (domestic only) or 408 774-9060.