

# SN54HC00, SN74HC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

SCLS181B – DECEMBER 1982 – REVISED MAY 1997

- Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

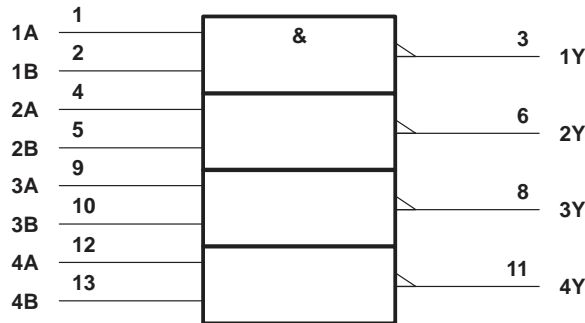
These devices contain four independent 2-input NAND gates. They perform the Boolean function  $Y = A \cdot B$  or  $Y = \overline{A + B}$  in positive logic.

The SN54HC00 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HC00 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE  
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

## logic symbol†

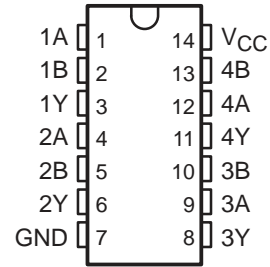


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, J, N, PW, and W packages.

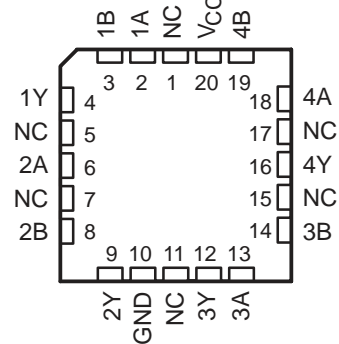
## logic diagram (positive logic)



SN54HC00 . . . J OR W PACKAGE  
SN74HC00 . . . D, N, OR PW PACKAGE  
(TOP VIEW)



SN54HC00 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection



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# SN54HC00, SN74HC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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## absolute maximum ratings over operating free-air temperature†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	127°C/W
N package	78°C/W
PW package	170°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions

		SN54HC00			SN74HC00			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V		1.5	1.5		V	
		$V_{CC} = 4.5$ V		3.15	3.15			
		$V_{CC} = 6$ V		4.2	4.2			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V		0	0.5	0	0.5	V
		$V_{CC} = 4.5$ V		0	1.35	0	1.35	
		$V_{CC} = 6$ V		0	1.8	0	1.8	
$V_I$	Input voltage	0	$V_{CC}$		0	$V_{CC}$		V
$V_O$	Output voltage	0	$V_{CC}$		0	$V_{CC}$		V
$t_t$	Input transition (rise and fall) time	$V_{CC} = 2$ V		0	1000	0	1000	ns
		$V_{CC} = 4.5$ V		0	500	0	500	
		$V_{CC} = 6$ V		0	400	0	400	
$T_A$	Operating free-air temperature	-55	125		-40	85		°C



# SN54HC00, SN74HC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC00		SN74HC00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.8		5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I <sub>OL</sub> = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I <sub>OL</sub> = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1	±100		±1000		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V			2		40		20	μA
C <sub>i</sub>			2 V to 6 V		3	10		10		10	pF

**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC00		SN74HC00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	2 V		45	90		135		115	ns
			4.5 V		9	18		27		23	
			6 V		8	15		23		20	
t <sub>t</sub>		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

**operating characteristics, T<sub>A</sub> = 25°C**

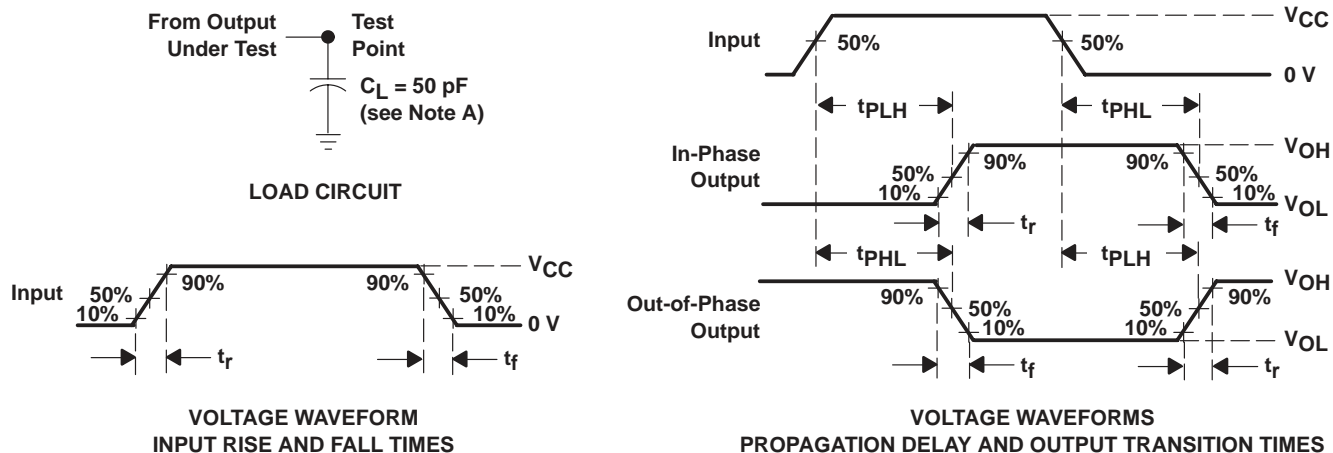
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per gate	No load	20	pF



# SN54HC00, SN74HC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATES

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - C. The outputs are measured one at a time with one input transition per measurement.
  - D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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## SN54HC00, Quadruple 2-Input Positive-NAND Gates

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54HC00
Voltage Nodes (V)	6, 5, 2
Vcc range (V)	2.0 to 6.0
Input Level	CMOS
Output Level	CMOS
No. of Gates	4

### FEATURES

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- Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

### DESCRIPTION

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These devices contain four independent 2-input NAND gates. They perform the Boolean function  $Y = A \cdot B$  or  $Y = A + B$  in positive logic.

The SN54HC00 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HC00 is characterized for operation from -40°C to 85°C.

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<u>ORDERABLE DEVICE</u>	<u>PACKAGE</u>	<u>PINS</u>	<u>TEMP (°C)</u>	<u>STATUS</u>	<u>BUDGETARY PRICE US\$/UNIT QTY= 1000+</u>	<u>PACK QTY</u>	<u>DSCC NUMBER</u>	<u>PRICING/AVAILABILITY</u>
84037012A	<u>FK</u>	20	-55 TO 125	ACTIVE	6.71	1		<u>Check stock or order</u>
8403701DA	<u>W</u>	14	-55 TO 125	ACTIVE	8.29	1		<u>Check stock or order</u>
JM38510/65001B2A	<u>FK</u>	20	-55 TO 125	ACTIVE	7.65	1		<u>Check stock or order</u>
JM38510/65001BCA	<u>J</u>	14	-55 TO 125	ACTIVE	3.93	1		<u>Check stock or order</u>
JM38510/65001BDA	<u>W</u>	14	-55 TO 125	ACTIVE	9.30	1		<u>Check stock or order</u>
SN54HC00J	<u>J</u>	14	-55 TO 125	ACTIVE	0.87	1		<u>Check stock or order</u>
SNJ54HC00FK	<u>FK</u>	20	-55 TO 125	ACTIVE	6.71	1	84037012A	<u>Check stock or order</u>
SNJ54HC00J	<u>J</u>	14	-55 TO 125	ACTIVE	1.03	1		<u>Check stock or order</u>
			-55					

SNJ54HC00W	<u>W</u>	14	TO 125	ACTIVE	8.29	1	8403701DA	<u>Check stock or order</u>
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## SN74HC00, Quadruple 2-Input Positive-NAND Gates

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74HC00
Voltage Nodes (V)	6, 5, 2
Vcc range (V)	2.0 to 6.0
Input Level	CMOS
Output Level	CMOS
Output Drive (mA)	-4/4
No. of Gates	4
Static Current	0.02
tpd(max) (ns)	20

### FEATURES

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SN74HC00ADBLE	<u>DB</u>	14	-40 TO 85	OBSOLETE			
SN74HC00ADBR	<u>DB</u>	14	-40 TO 85	NRND	0.33	2000	<a href="#">Check stock or order</a>
SN74HC00D	<u>D</u>	14	-40 TO 85	ACTIVE	0.25	50	<a href="#">Check stock or order</a>
SN74HC00DR	<u>D</u>	14	-40 TO 85	ACTIVE	0.28	2500	<a href="#">Check stock or order</a>
SN74HC00N	<u>N</u>	14	-40 TO 85	ACTIVE	0.23	25	<a href="#">Check stock or order</a>
SN74HC00N3	<u>N</u>	14	-40 TO 85	OBSOLETE			
SN74HC00NSR	<u>NS</u>	14	-40 TO 85	ACTIVE	0.33	2000	<a href="#">Check stock or order</a>
SN74HC00PWLE	<u>PW</u>	14	-40 TO 85	OBSOLETE			
SN74HC00PWR	<u>PW</u>	14	-40 TO 85	ACTIVE	0.25	2000	<a href="#">Check stock or order</a>

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