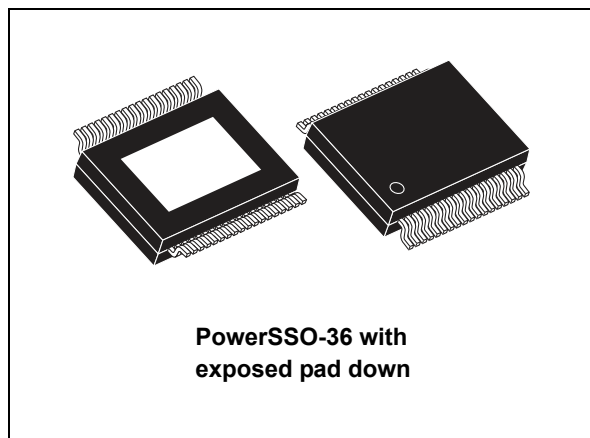


50 W mono BTL class-D audio amplifier

Datasheet - production data



Description

The TDA7492MV is a mono BTL class-D audio amplifier with single power supply designed for home systems and docking stations.

Thanks to the high efficiency and an exposed-pad-down (EPD) package no heatsink is required.

Features

- 50 W continuous output power: $R_L = 6 \Omega$, THD = 10% at $V_{CC} = 25 \text{ V}$
- 40 W continuous output power: $R_L = 8 \Omega$, THD = 10% at $V_{CC} = 25 \text{ V}$
- Wide range single supply operation (10 - 26 V)
- High efficiency ($\eta = 90\%$)
- Four selectable, fixed gain settings of nominally 21.6 dB, 27.6 dB, 31.1 dB and 33.6 dB
- Differential inputs minimize common-mode noise
- Standby and mute features
- Short-circuit protection
- Thermal-overload protection
- Externally synchronizable

Table 1. Device summary

| Order code | Operating temp. range | Package | Packaging |
|---------------|-----------------------|-----------------|---------------|
| TDA7492MV13TR | 0 to 70 °C | PowerSSO-36 EPD | Tape and reel |

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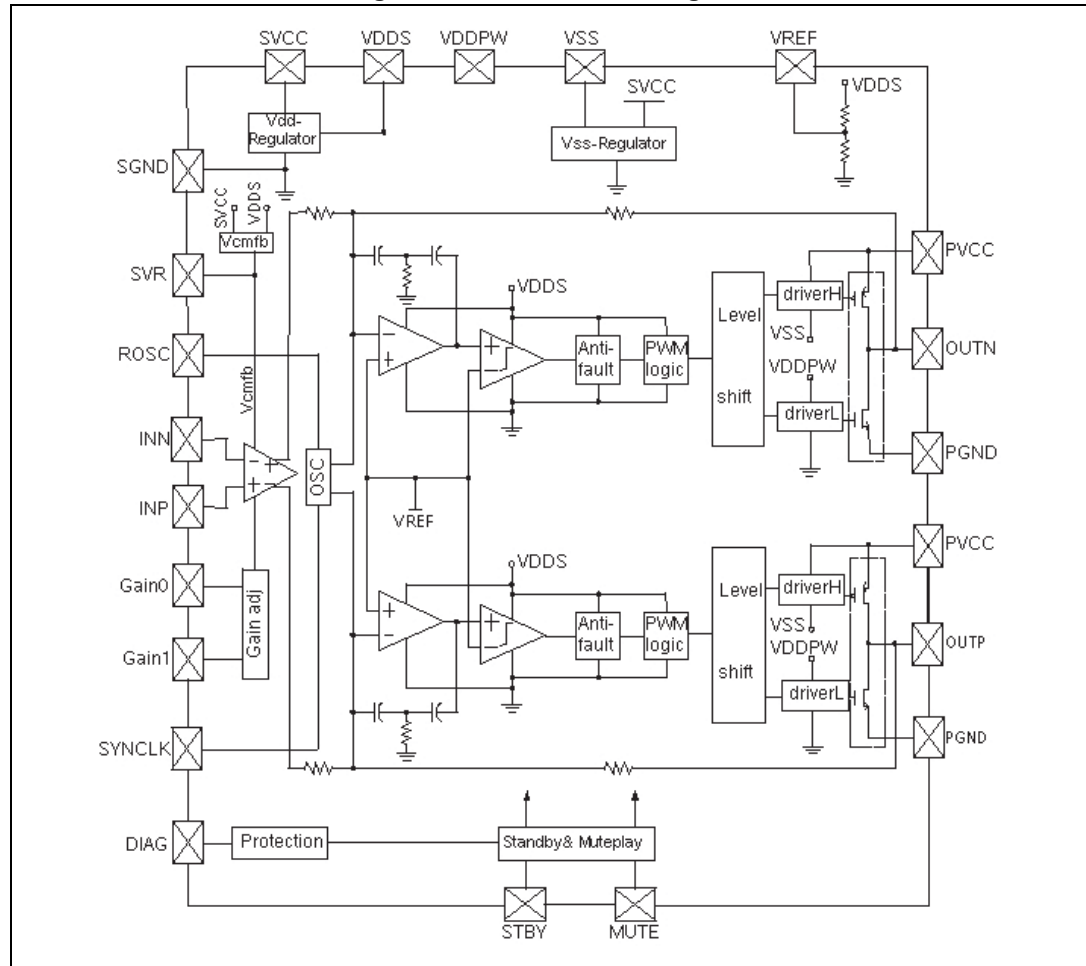
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1 Device block diagram

Figure 1 shows the block diagram of the TDA7492MV.

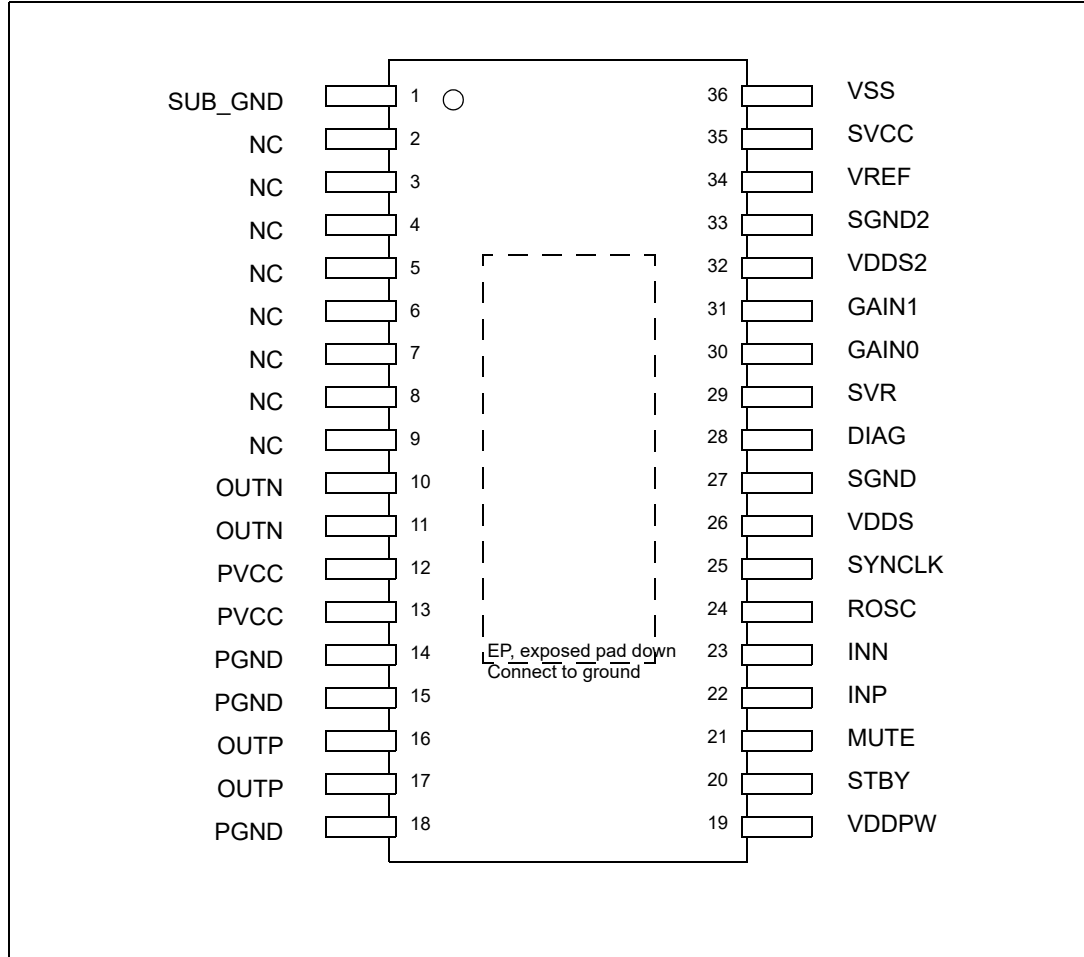
Figure 1. Internal block diagram



2 Pin description

2.1 Pin out

Figure 2. Pin connection (top view, PCB view)



2.2 Pin list

Table 2. Pin description list

| Pin n° | Name | Type | Description |
|--------|---------|--------|---|
| 1 | SUB_GND | POWER | Connect to the frame |
| 2,3 | NC | - | No internal connection |
| 4,5 | NC | - | No internal connection |
| 6,7 | NC | - | No internal connection |
| 8,9 | NC | - | No internal connection |
| 10,11 | OUTN | OUT | Negative PWM output |
| 12,13 | PVCC | POWER | Power supply for output channel |
| 14,15 | PGND | POWER | Power ground for output channel |
| 16,17 | OUTP | OUT | Positive PWM output |
| 18 | PGND | POWER | Power supply ground |
| 19 | VDDPW | OUT | 3.3-V (nominal) regulator output referred to ground for power stage |
| 20 | STBY | INPUT | Standby mode control |
| 21 | MUTE | INPUT | Mute mode control |
| 22 | INP | INPUT | Positive differential input |
| 23 | INN | INPUT | Negative differential input |
| 24 | ROSC | OUT | Master oscillator frequency-setting pin |
| 25 | SYNCLK | IN/OUT | Clock in/out for external oscillator |
| 26 | VDDS | OUT | 3.3-V (nominal) regulator output referred to ground for signal blocks |
| 27 | SGND | POWER | Signal ground |
| 28 | DIAG | OUT | Open-drain diagnostic output |
| 29 | SVR | OUT | Supply voltage rejection |
| 30 | GAIN0 | INPUT | Gain setting input 1 |
| 31 | GAIN1 | INPUT | Gain setting input 2 |
| 32 | VDDS2 | INPUT | To be connected to VDDS (pin 26) |
| 33 | SGND2 | INPUT | To be connected to SGND (pin 27) |
| 34 | VREF | OUT | Half VDDS (nominal) referred to ground |
| 35 | SVCC | POWER | Signal power supply |
| 36 | VSS | OUT | 3.3-V (nominal) regulator output referred to power supply |
| - | EP | - | Exposed pad for ground-plane heatsink, to be connected to ground |

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-----------|---|------------|------|
| V_{CC} | DC supply voltage for pins PVCC, SVCC | 30 | V |
| V_I | Voltage limits for input pins STBY, MUTE, INN, INP, GAIN0, GAIN1 | -0.3 - 3.6 | V |
| T_{op} | Operating temperature | 0 to 70 | °C |
| T_j | Junction temperature | -40 to 150 | °C |
| T_{stg} | Storage temperature | -40 to 150 | °C |

3.2 Thermal data

Table 4. Thermal data

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------|--------------------------------------|-----|-----|-----|------|
| $R_{th\ j-case}$ | Thermal resistance, junction to case | - | 2 | 3 | °C/W |

3.3 Electrical specifications

Unless otherwise stated, the results in [Table 5](#) below are given for the conditions:
 $V_{CC} = 25\text{ V}$, R_L (load) = $8\ \Omega$, $R_{OSC} = R3 = 39\text{ k}\Omega$, $C8 = 100\text{ nF}$, $f = 1\text{ kHz}$, $G_V = 21.6\text{ dB}$ and
 $T_{amb} = 25\text{ °C}$.

Table 5. Electrical specifications

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|-------------|---|--------------------|------|-----|-----|------------------|
| V_{CC} | Supply voltage for pins PVCCA, PVCCB, SVCC | - | 10 | - | 26 | V |
| I_q | Total quiescent current | Without LC | - | 26 | 35 | mA |
| I_{qSTBY} | Quiescent current in standby | - | - | 2.5 | 5.0 | μA |
| V_{OS} | Output offset voltage | Play mode | -100 | - | 100 | mV |
| | | Mute mode | -60 | - | 60 | |
| I_{OCP} | Overcurrent protection threshold | $R_L = 0\ \Omega$ | 4.8 | 6.0 | - | A |
| T_j | Junction temperature at thermal shutdown | - | - | 150 | - | °C |
| R_i | Input resistance | Differential input | 48 | 60 | - | $\text{k}\Omega$ |
| V_{OVP} | Overvoltage protection threshold | - | 28 | 29 | - | V |
| V_{UVP} | Undervoltage protection threshold | - | - | - | 7 | V |

Table 5. Electrical specifications (continued)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---------------------------------|----------------------------------|--|------|------|------|------|
| R _{dsON} | Power transistor on resistance | High side | - | 0.2 | - | Ω |
| | | Low side | - | 0.2 | - | |
| P _o | Output power | THD = 10% | - | 40 | - | W |
| | | THD = 1% | - | 32 | - | |
| P _o | Output power | R _L = 6 Ω, THD = 10%, V _{CC} = 25V | - | 50 | - | W |
| | | R _L = 6 Ω, THD = 1% V _{CC} = 25V | - | 40 | - | |
| P _D | Dissipated power | P _o = 40W, THD = 10% | - | 4.0 | - | W |
| η | Efficiency | P _o = 40 W | 80 | 90 | - | % |
| THD | Total harmonic distortion | P _o = 1 W | - | 0.1 | 0.4 | % |
| G _V | Closed-loop gain | GAIN0 = L, GAIN1 = L | 20.6 | 21.6 | 22.6 | dB |
| | | GAIN0 = L, GAIN1 = H | 26.6 | 27.6 | 28.6 | |
| | | GAIN0 = H, GAIN1 = L | 30.1 | 31.1 | 32.1 | |
| | | GAIN0 = H, GAIN1 = H | 32.6 | 33.6 | 34.6 | |
| ΔG _V | Gain matching | - | -1 | - | 1 | dB |
| eN | Total input noise | A Curve, G _V = 20 dB | - | 20 | - | μV |
| | | f = 22 Hz to 22 kHz | - | 25 | 35 | |
| SVRR | Supply voltage rejection ratio | f _r = 100 Hz, V _r = 0.5 V, C _{SVR} = 10 μF | 40 | 50 | - | dB |
| T _r , T _f | Rise and fall times | - | - | 50 | - | ns |
| f _{SW} | Switching frequency | Internal oscillator | 290 | 310 | 330 | kHz |
| f _{SWR} | Output switching frequency range | With internal oscillator ⁽¹⁾ | 250 | - | 400 | kHz |
| | | With external oscillator ⁽²⁾ | 250 | - | 400 | |
| V _{inH} | Digital input high (H) | - | 2.3 | - | - | V |
| V _{inL} | Digital input low (L) | | - | - | 0.8 | |
| A _{MUTE} | Mute attenuation | V _{MUTE} = 1 V | 60 | 80 | - | dB |

1. $f_{SW} = 10^6 / ((16 * R_{OSC} + 182) * 4)$ kHz, $f_{SYNCLK} = 2 * f_{SW}$ with R3 = 39 kΩ (see [Figure 20](#)).

2. $f_{SW} = f_{SYNCLK} / 2$ with the frequency of the external oscillator.

4 Characterization curves

The following characterization curves were made using the TDA7492MV exposed-pad-down test board with $V_{CC} = 25\text{ V}$, a signal frequency of 1 kHz and an output power of 1 W unless otherwise specified.

The LC filter for the 8- Ω load uses components of 33 μH and 220 nF and for the 6- Ω load 22 μH and 220 nF.

4.1 For 6 Ω load

Figure 3. Output power vs supply voltage

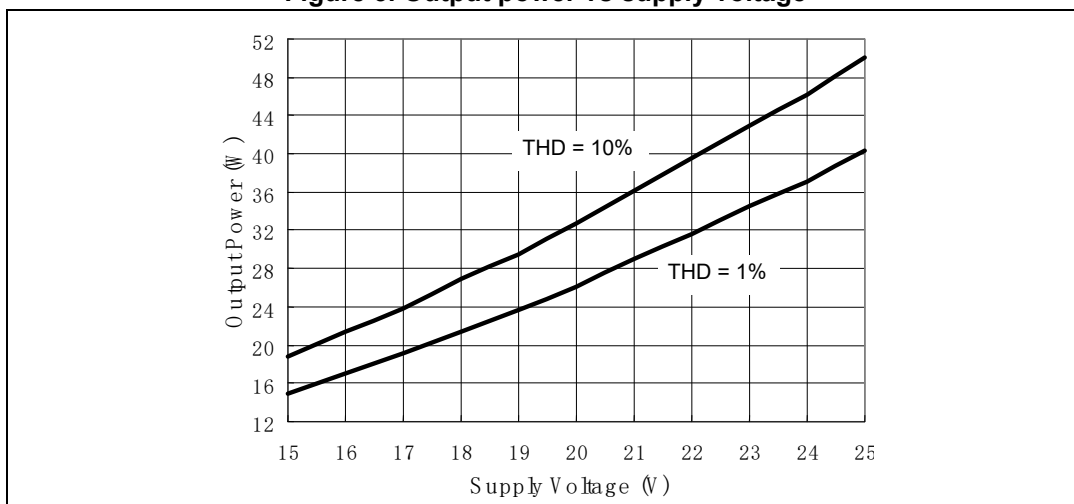


Figure 4. THD vs output power (1 kHz)

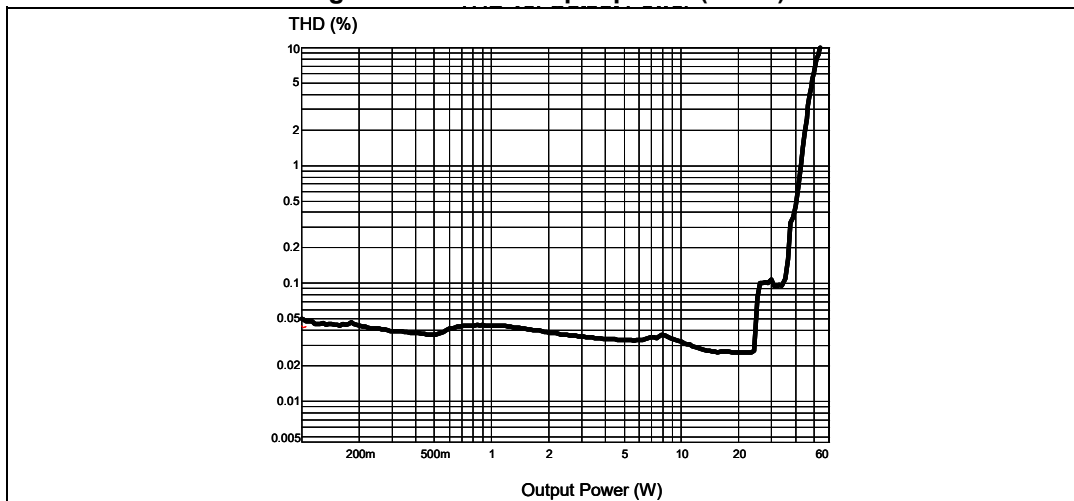


Figure 5. THD vs output power (100 Hz)

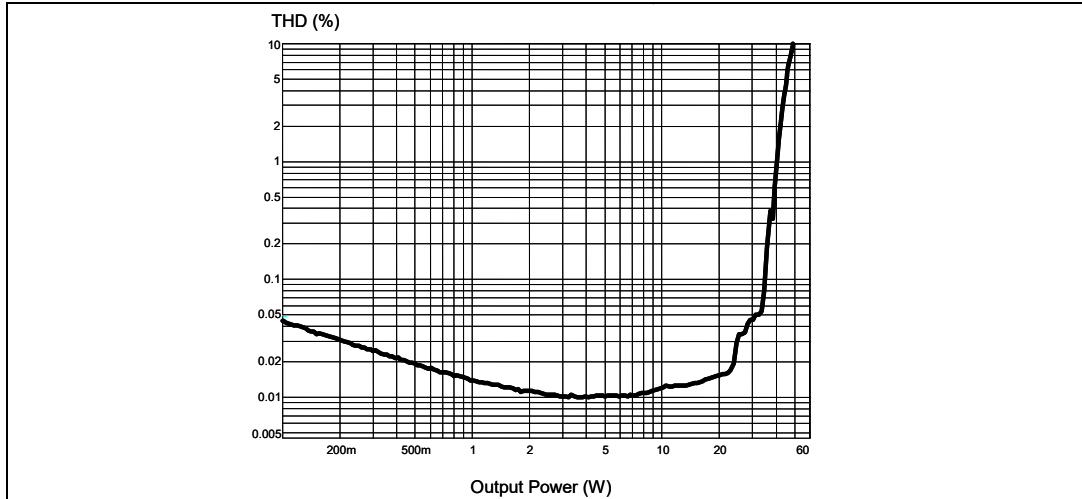


Figure 6. THD vs frequency (100 mW)

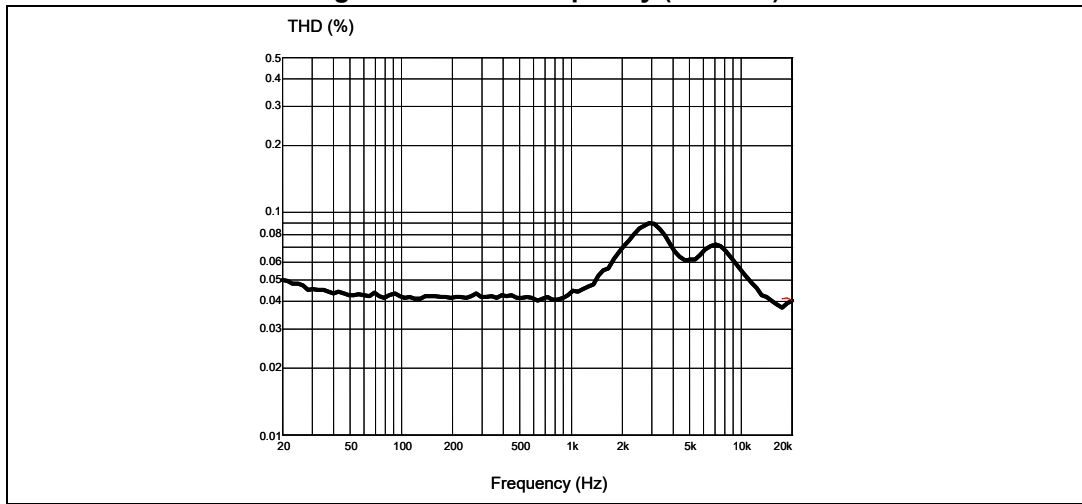


Figure 7. THD vs frequency

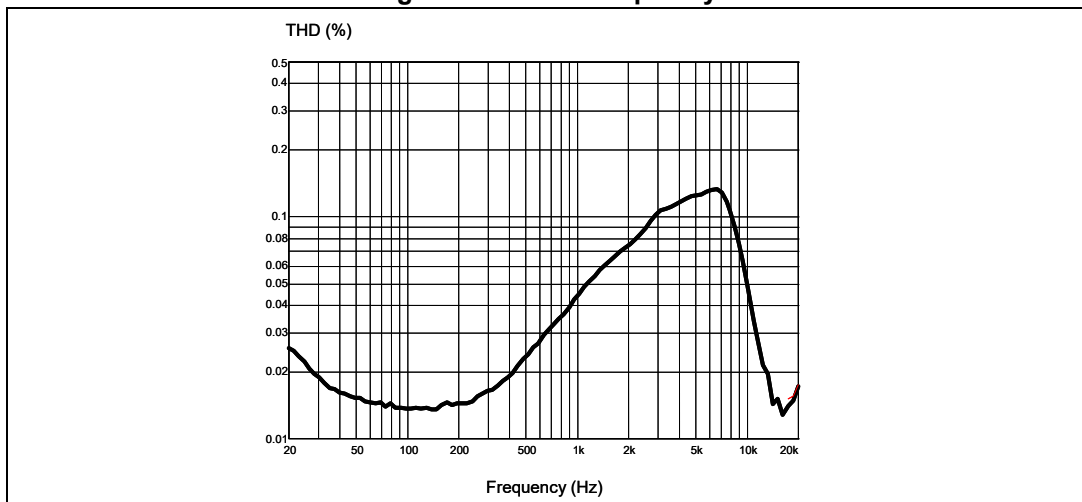


Figure 8. Frequency response

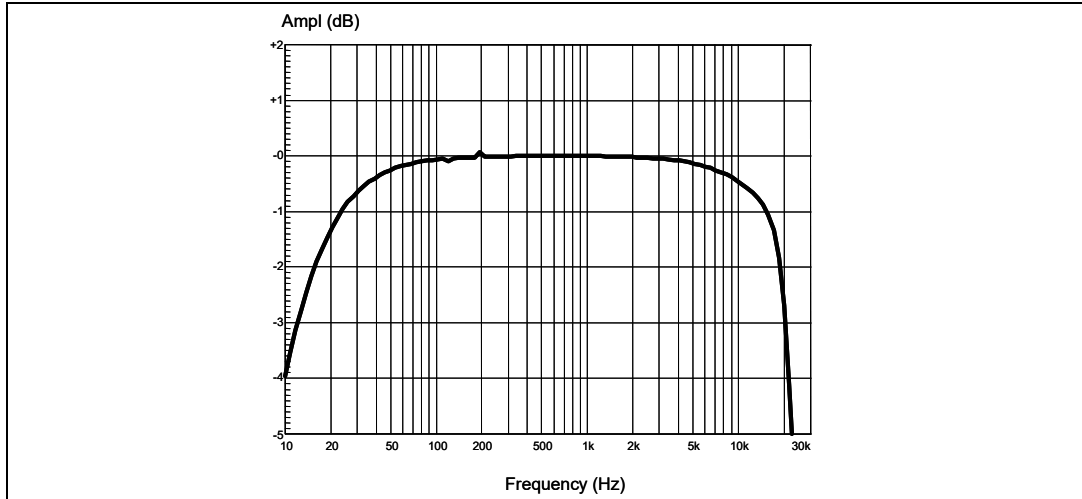


Figure 9. FFT (0 dB)

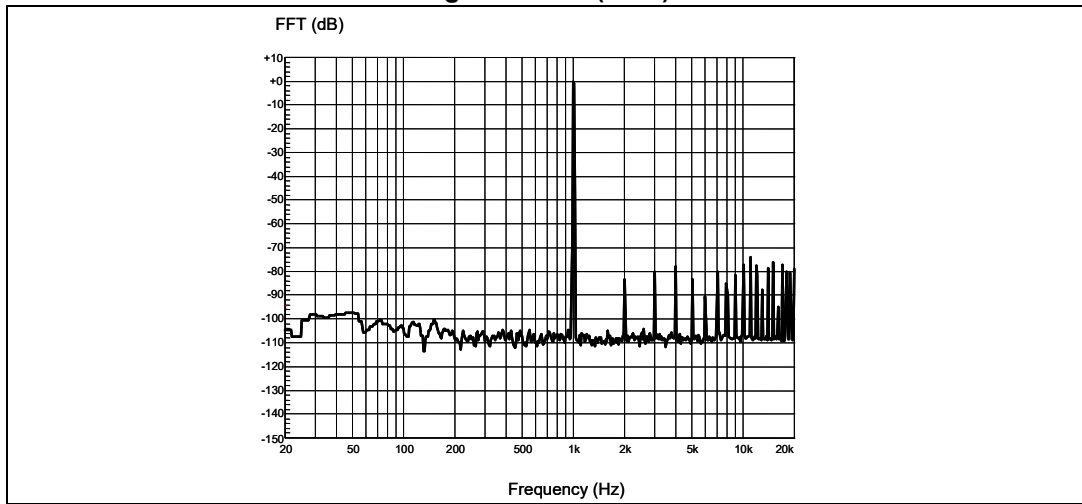
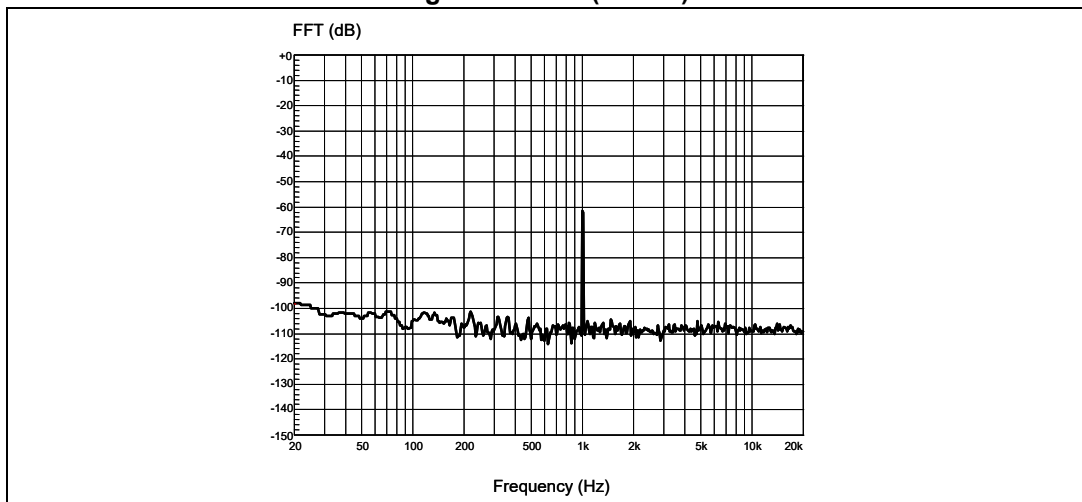


Figure 10. FFT (-60 dB)



4.2 For 8 Ω load

Figure 11. Output power vs supply voltage

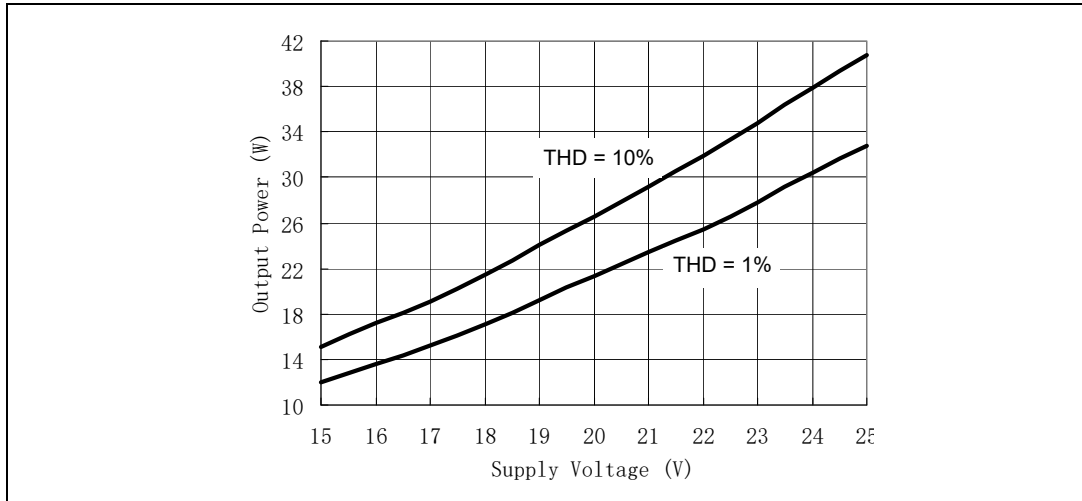


Figure 12. THD vs output power (1 kHz)

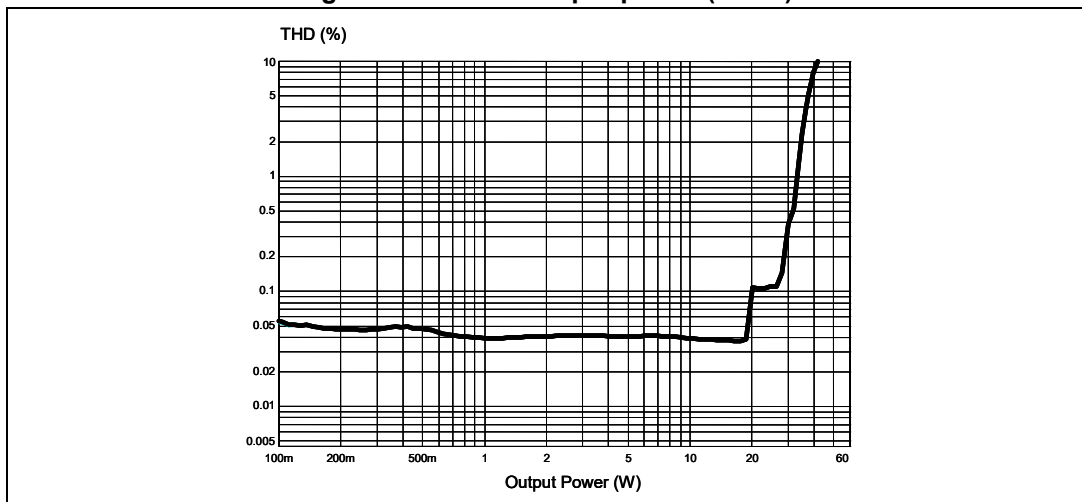


Figure 13. THD vs output power (100 Hz)

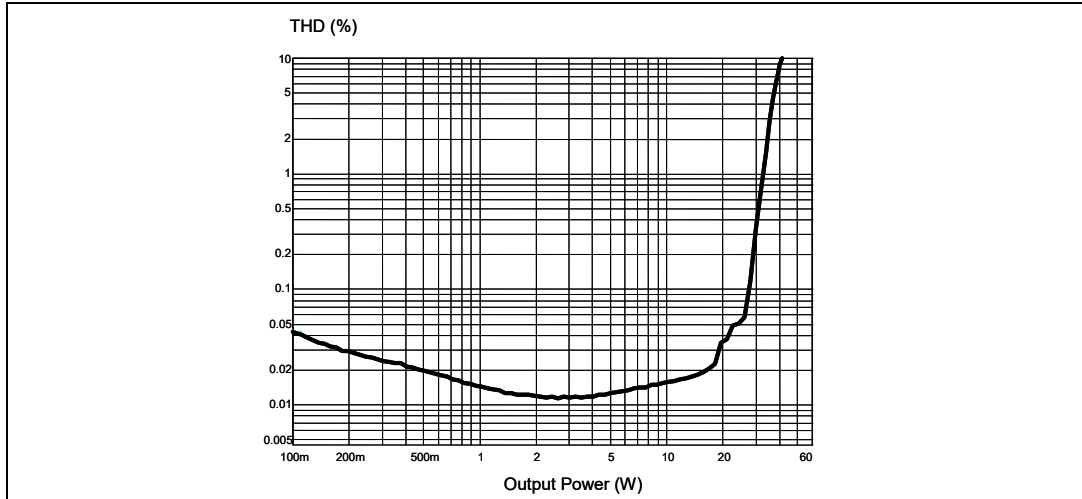


Figure 14. THD vs frequency (100 mW)

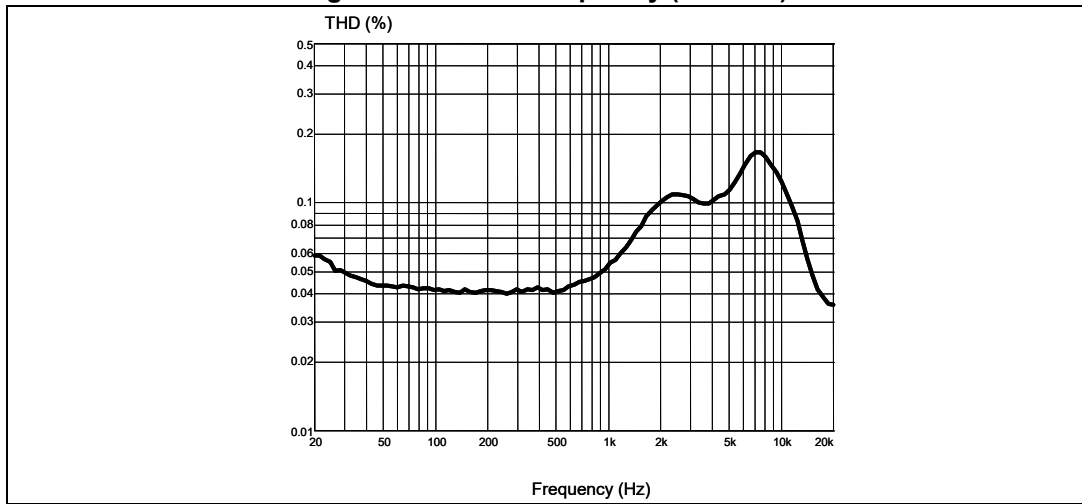


Figure 15. THD vs frequency

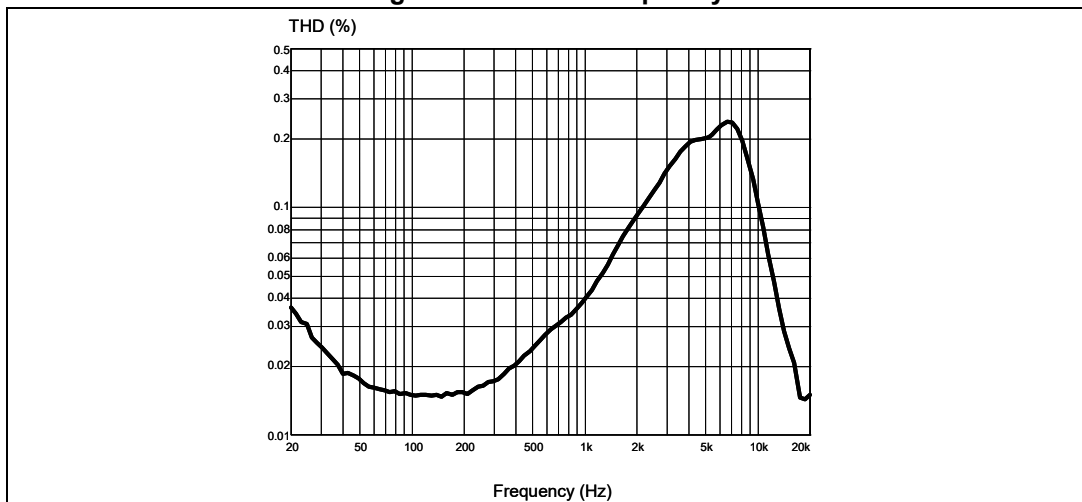


Figure 16. Frequency response

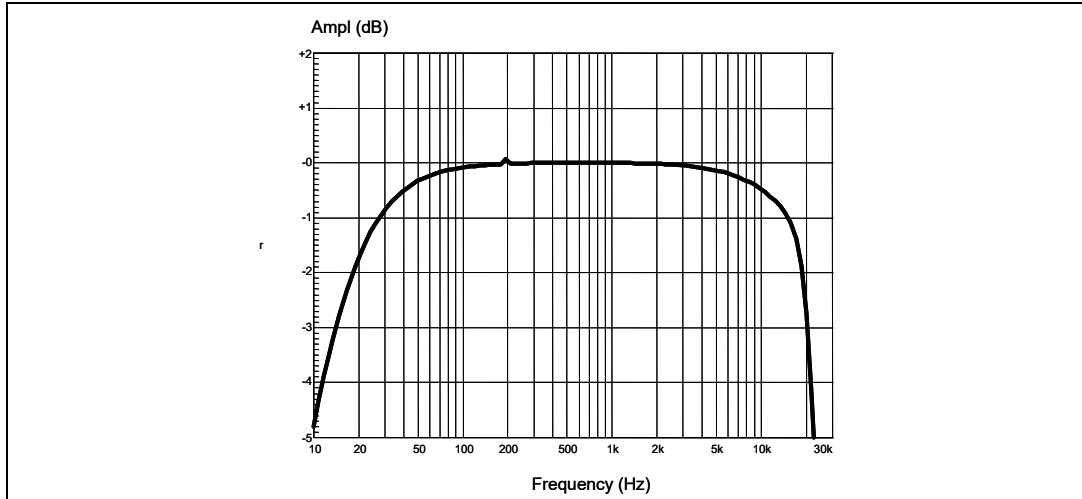


Figure 17. FFT (0 dB)

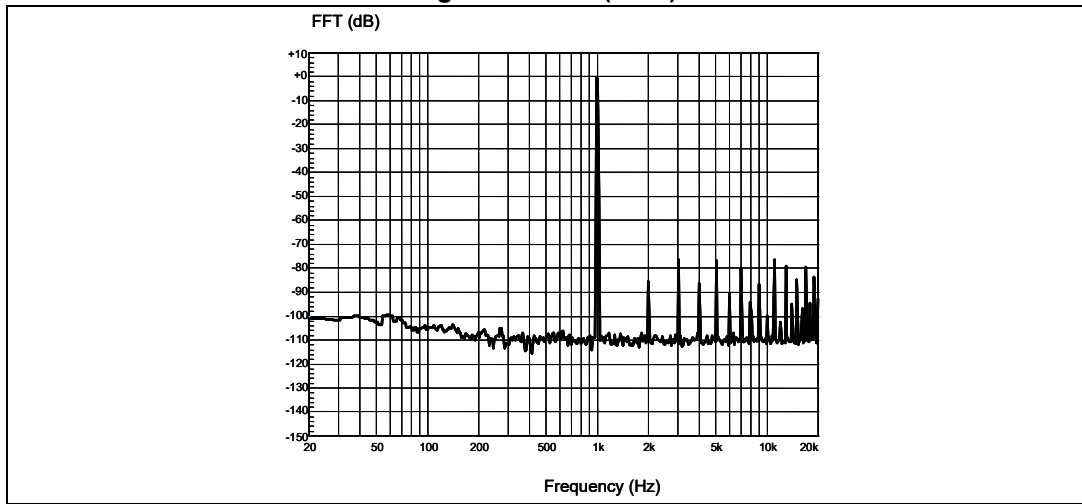
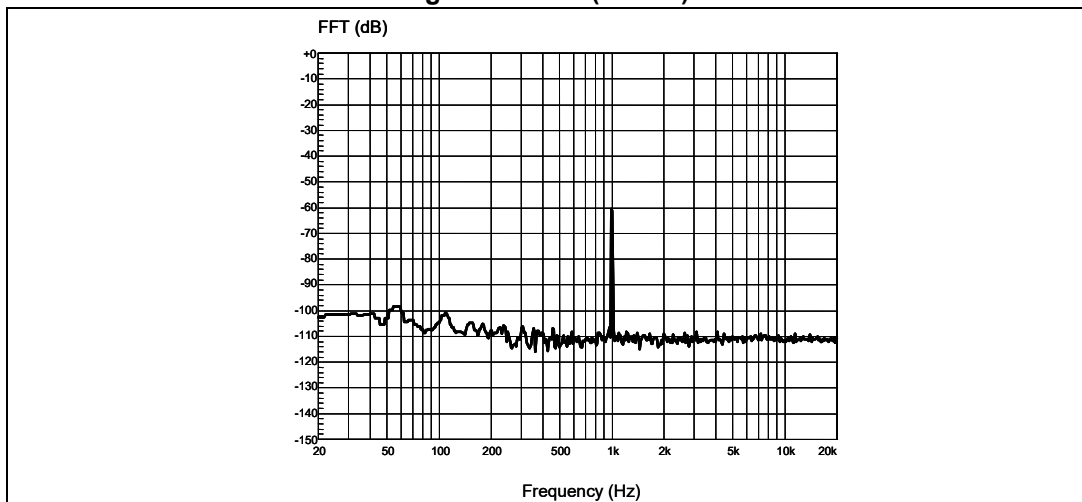
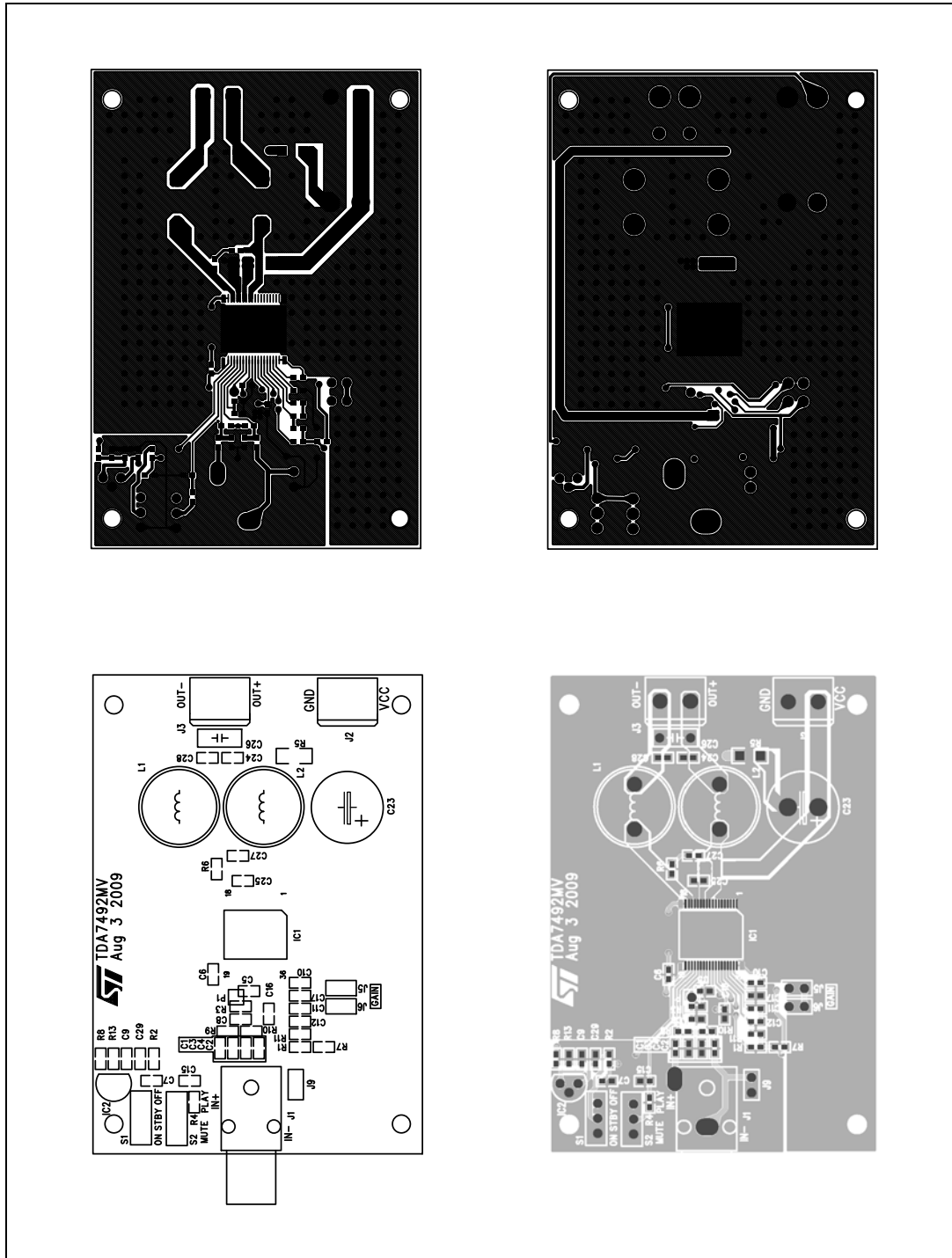


Figure 18. FFT (-60 dB)



4.3 Test board

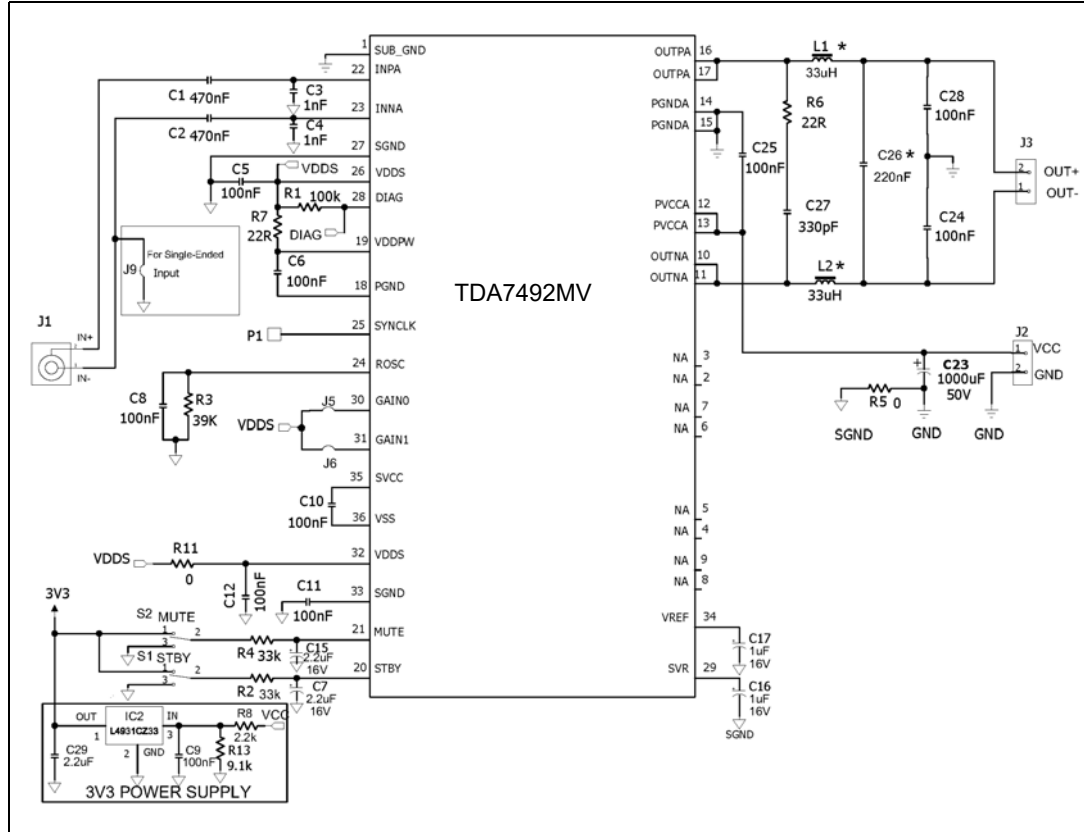
Figure 19. Test board layout



5 Applications information

5.1 Applications circuit

Figure 20. Applications circuit for class-D amplifier



5.2 Mode selection

The three operating modes of the TDA7492MV are set by the two inputs STBY (pin 20) and MUTE (pin 21).

- Standby mode: all circuits are turned off, very low current consumption.
- Mute mode: inputs are connected to ground and the positive and negative PWM outputs are at 50% duty cycle.
- Play mode: the amplifiers are active.

The protection functions of the TDA7492MV are realized by pulling down the voltages of the STBY and MUTE inputs shown in [Figure 21](#). The input current of the corresponding pins must be limited to 200 μ A.

Table 6. Mode settings

| Mode Selection | STBY | MUTE |
|----------------|------------------|----------------|
| Standby | L ⁽¹⁾ | X (don't care) |
| Mute | H ⁽¹⁾ | L |
| Play | H | H |

1. Drive levels defined in [Table 5: Electrical specifications on page 8](#)

Figure 21. Standby and mute circuits

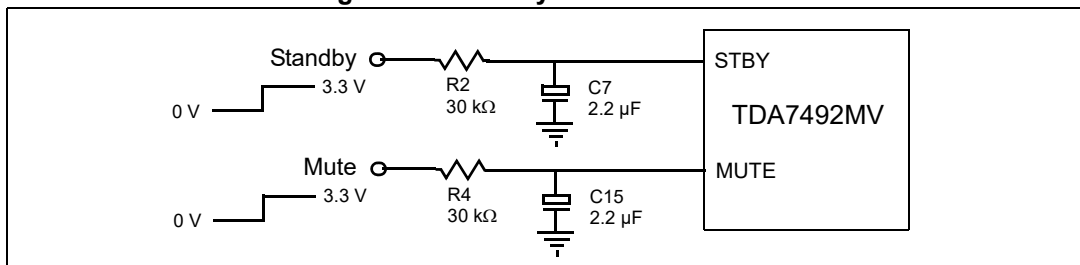
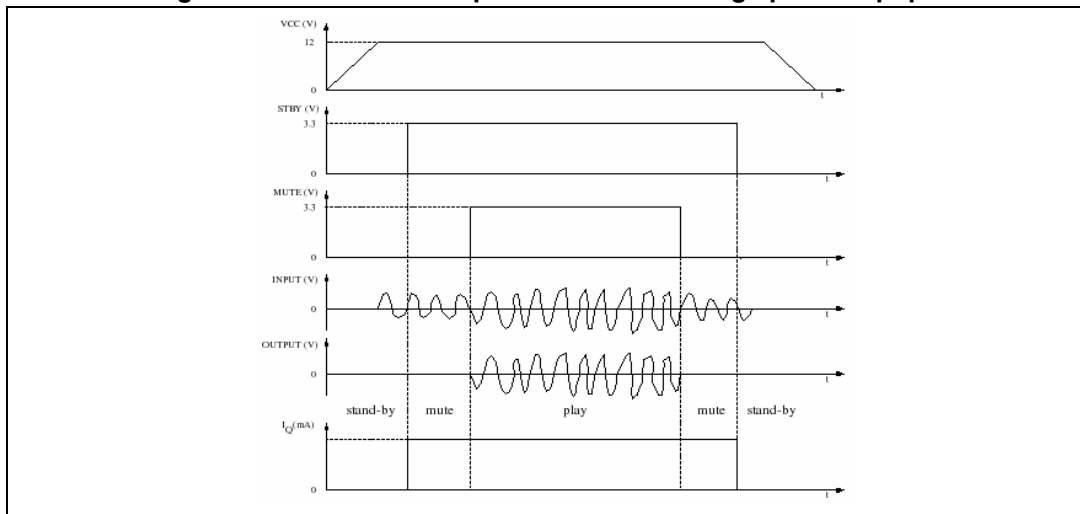


Figure 22. Turn-on/off sequence for minimizing speaker “pop”



5.3 Gain setting

The gain of the TDA7492MV is set by the two inputs, GAIN0 (pin 30) and GAIN1 (pin 31). Internally, the gain is set by changing the feedback resistors of the amplifier.

Table 7. Gain settings

| GAIN0 | GAIN1 | Nominal gain, G_v (dB) |
|-------|-------|--------------------------|
| L | L | 21.6 |
| L | H | 27.6 |
| H | L | 31.1 |
| H | H | 33.6 |

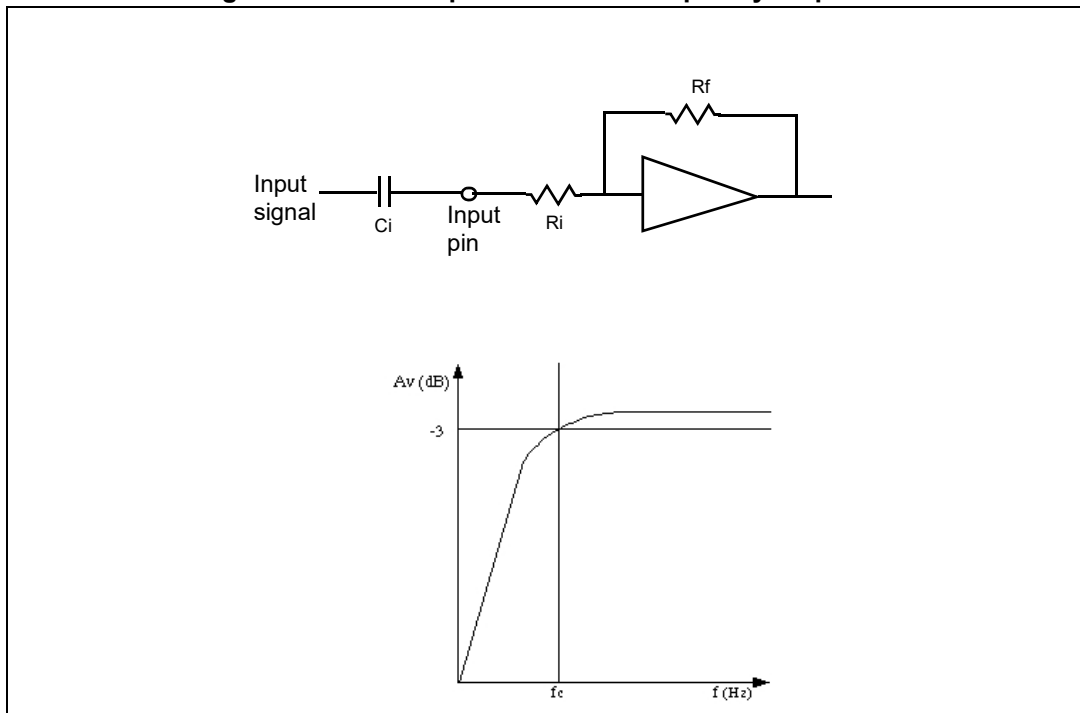
5.4 Input resistance and capacitance

The input impedance is set by an internal resistor $R_i = 60 \text{ k}\Omega$ (typical). An input capacitor (C_i) is required to couple the AC input signal.

The equivalent circuit and frequency response of the input components are shown in [Figure 23](#). For $C_i = 470 \text{ nF}$ the high-pass filter cut-off frequency is below 20 Hz:

$$f_c = 1 / (2 * \pi * R_i * C_i)$$

Figure 23. Device input circuit and frequency response



5.5 Internal and external clocks

The clock of the class-D amplifier can be generated internally or can be driven by an external source.

If two or more class-D amplifiers are used in the same system, it is recommended that all devices operate at the same clock frequency. This can be implemented by using one TDA7492MV as master clock, while the other devices are in slave mode (that is, externally clocked). The clock interconnect is via pin SYNCLK of each device. As explained below, SYNCLK is an output in master mode and an input in slave mode.

5.5.1 Master mode (internal clock)

Using the internal oscillator, the output switching frequency, f_{SW} , is controlled by the resistor, R_{OSC} , connected to pin ROSC:

$$f_{SW} = 10^6 / ((16 * R_{OSC} + 182) * 4) \text{ kHz}$$

where R_{OSC} is in $k\Omega$.

In master mode, pin SYNCLK is used as a clock output pin, whose frequency is:

$$f_{SYNCLK} = 2 * f_{SW}$$

For master mode to operate correctly then resistor R_{OSC} must be less than 60 $k\Omega$ as given below in [Table 8](#).

5.5.2 Slave mode (external clock)

In order to accept an external clock input the pin ROSC must be left open, that is, floating. This forces pin SYNCLK to be internally configured as an input as given in [Table 8](#).

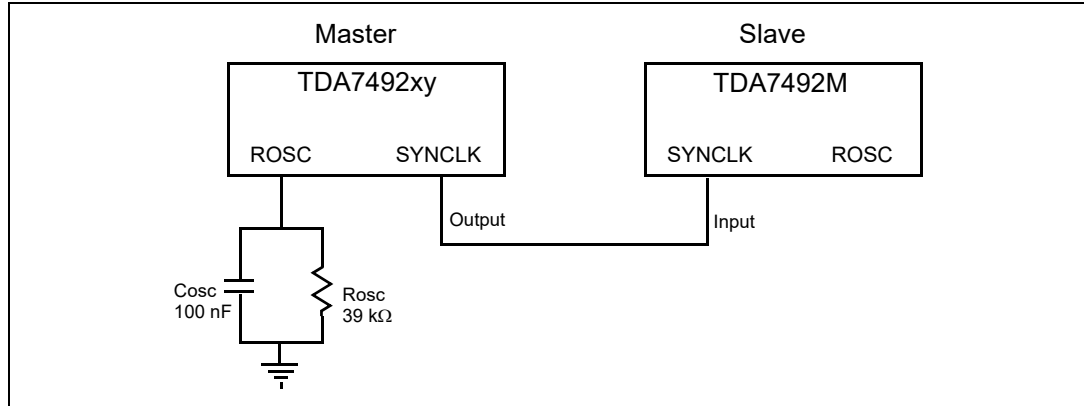
The output switching frequency of the slave devices is:

$$f_{SW} = f_{SYNCLK} / 2$$

Table 8. How to set up SYNCLK

| Mode | ROSC | SYNCLK |
|--------|--------------------------------|--------|
| Master | $R_{OSC} < 60 \text{ k}\Omega$ | Output |
| Slave | Floating (not connected) | Input |

Figure 24. Master and slave connection



5.6 Output low-pass filter

To avoid EMI problems, it may be necessary to use a low-pass filter before the speaker. The cutoff frequency should be larger than 22 kHz and much lower than the output switching frequency. It is necessary to choose the L-C component values depending on the loud speaker impedance. Some typical values, which give a cut-off frequency of 27 kHz, are shown in [Figure 25](#) and [Figure 26](#) below.

Figure 25. Typical LC filter for a 8 Ω speaker

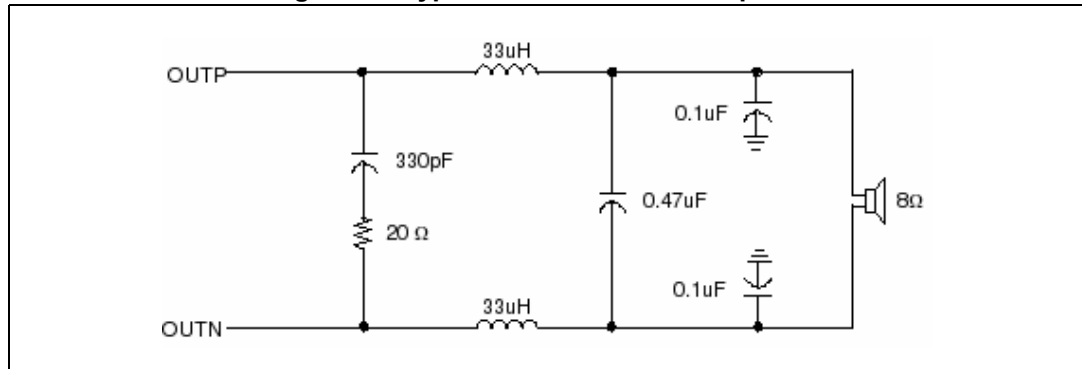
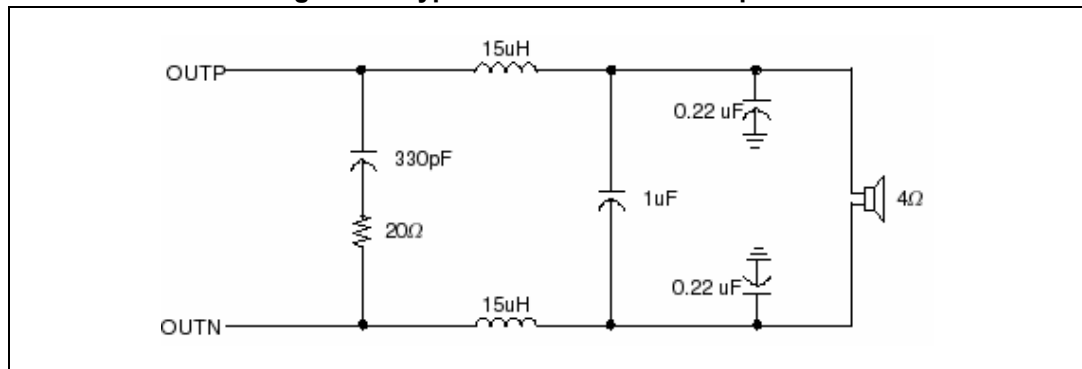


Figure 26. Typical LC filter for a 4 Ω speaker



5.7 Protection function

The TDA7492MV is fully protected against overvoltage, undervoltage, overcurrent and thermal overloads as explained here.

Overvoltage protection (OVP)

If the supply voltage exceeds the value for V_{OVP} given in [Table 5: Electrical specifications on page 8](#) the overvoltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage falls back to within the operating range the device restarts.

Undervoltage protection (UVP)

If the supply voltage drops below the value for V_{UVP} given in [Table 5: Electrical specifications on page 8](#) the undervoltage protection is activated which forces the outputs to the high-impedance state. When the supply voltage recovers to within the operating range the device restarts.

Overcurrent protection (OCP)

If the output current exceeds the value for I_{OCP} given in [Table 5: Electrical specifications on page 8](#) the overcurrent protection is activated which forces the outputs to the high-impedance state. Periodically, the device attempts to restart. If the overcurrent condition is still present then the OCP remains active. The restart time, T_{OC} , is determined by the R-C components connected to pin STBY.

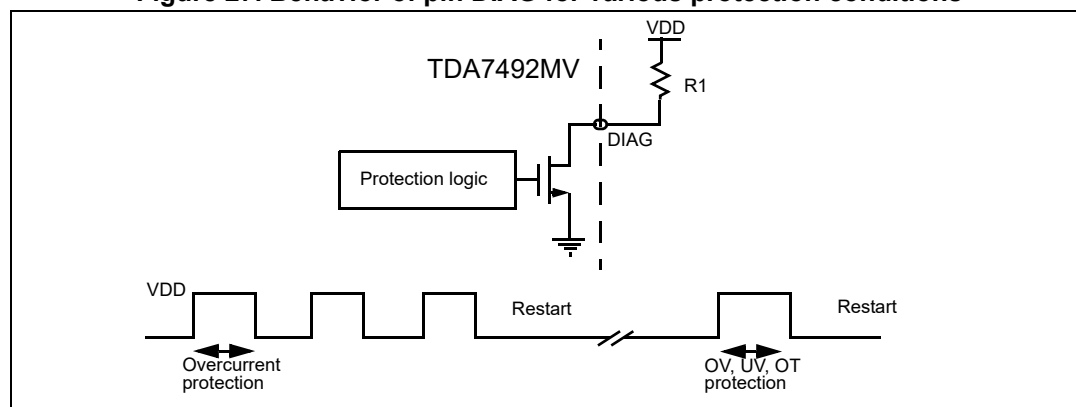
Thermal protection (OTP)

If the junction temperature, T_j , reaches 145 °C (nominal), the device goes to mute mode and the positive and negative PWM outputs are forced to 50% duty cycle. If the junction temperature exceeds the value for T_j given in [Table 5: Electrical specifications on page 8](#) the device shuts down and the output is forced to the high impedance state. When the device cools sufficiently the device restarts.

5.8 Diagnostic output

The output pin DIAG is an open drain transistor. When the protection is activated it is in the high-impedance state. The pin can be connected to a power supply (< 26 V) by a pull-up resistor whose value is limited by the maximum sinking current (200 μ A) of the pin.

Figure 27. Behavior of pin DIAG for various protection conditions



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 PowerSSO-36 EPD package mechanical data

The TDA7492MV comes in a 36-pin PowerSSO package with exposed pad down.

Figure 28 below shows the package outline and Table 9 gives the dimensions.

Figure 28. PowerSSO-36 EPD outline drawing

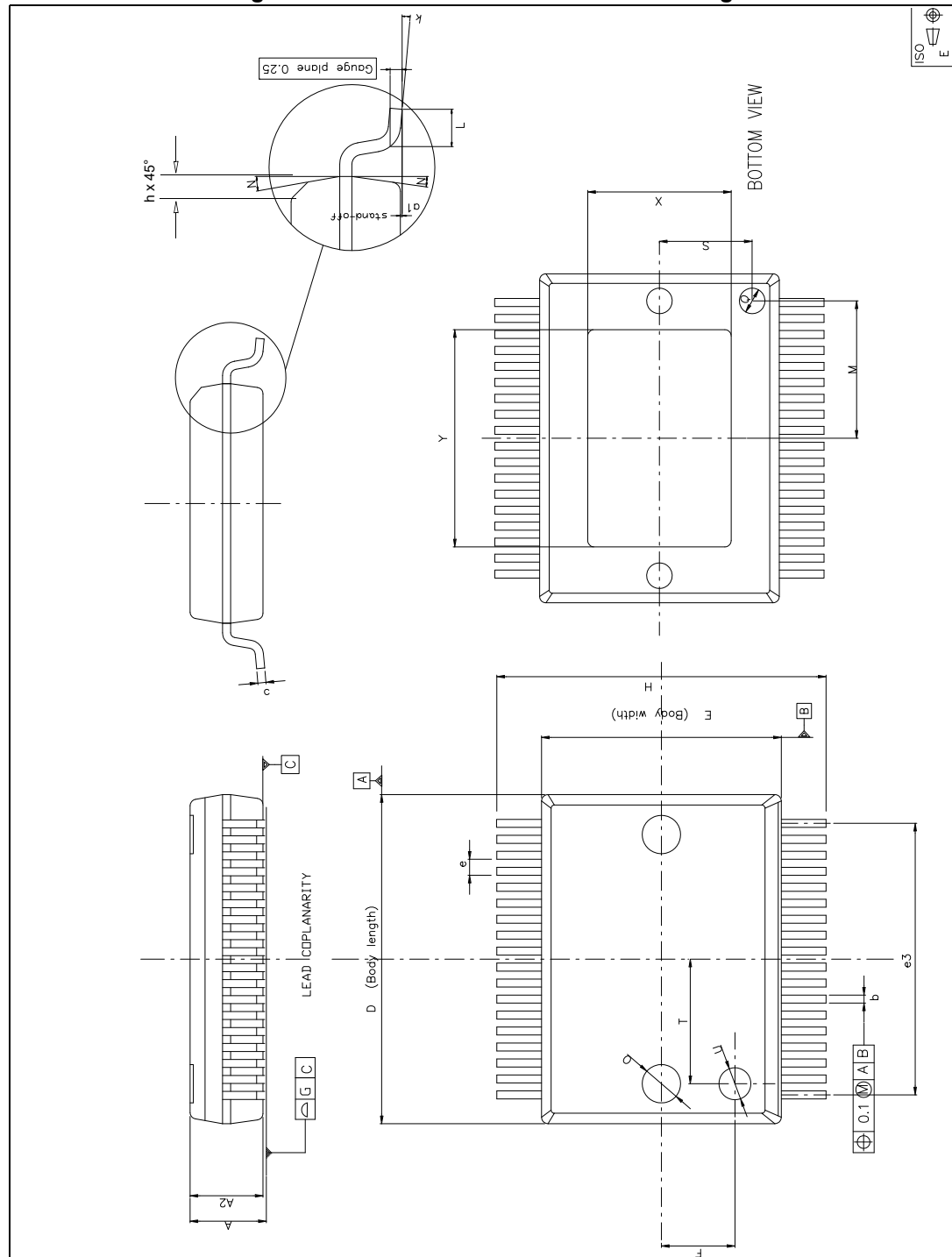


Table 9. PowerSSO-36 EPD dimensions

| Symbol | Dimensions in mm | | | Dimensions in inches | | |
|--------|------------------|------|------------|----------------------|-------|------------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 2.15 | - | 2.47 | 0.085 | - | 0.097 |
| A2 | 2.15 | - | 2.40 | 0.085 | - | 0.094 |
| a1 | 0.00 | - | 0.10 | 0.000 | - | 0.004 |
| b | 0.18 | - | 0.36 | 0.007 | - | 0.014 |
| c | 0.23 | - | 0.32 | 0.009 | - | 0.013 |
| D | 10.10 | - | 10.50 | 0.398 | - | 0.413 |
| E | 7.40 | - | 7.60 | 0.291 | - | 0.299 |
| e | - | 0.5 | - | - | 0.020 | - |
| e3 | - | 8.5 | - | - | 0.335 | - |
| F | - | 2.3 | - | - | 0.091 | - |
| G | - | - | 0.10 | - | - | 0.004 |
| H | 10.10 | - | 10.50 | 0.398 | - | 0.413 |
| h | - | - | 0.40 | - | - | 0.016 |
| k | 0 | - | 8 degrees | 0 | - | 8 degrees |
| L | 0.60 | - | 1.00 | 0.024 | - | 0.039 |
| M | - | 4.30 | - | - | 0.169 | - |
| N | - | - | 10 degrees | - | - | 10 degrees |
| O | - | 1.20 | - | - | 0.047 | - |
| Q | - | 0.80 | - | - | 0.031 | - |
| S | - | 2.90 | - | - | 0.114 | - |
| T | - | 3.65 | - | - | 0.144 | - |
| U | - | 1.00 | - | - | 0.039 | - |
| X | 4.10 | - | 4.70 | 0.161 | - | 0.185 |
| Y | 6.50 | - | 7.10 | 0.256 | - | 0.280 |

7 Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 20-Oct-2009 | 1 | Initial release |
| 20-Feb-2014 | 2 | Updated order code Table 1 on page 1 |
| 11-May-2020 | 3 | Updated Y dimensions in Table 9 |

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