T-46-07-11

National Semiconductor

74FCT564A
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'FCT564A is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The 'FCT564A device is functionally identical to the 'FCT574A, but with inverted outputs.

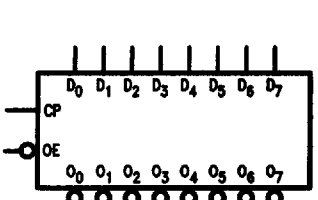
FACT™ FCTA features undershoot correction and split ground bus for superior performance.

Features

- I_{CC} and I_{OZ} reduced to 40.0 μA and ±2.5 μA respectively
- TRI-STATE outputs for bus-oriented applications
- Useful as input or output port for microprocessors
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA
- CMOS power levels
- 4 kV minimum ESD immunity

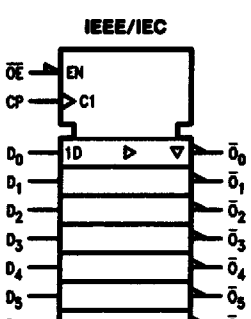
Ordering Code: See Section 8

Logic Symbols



TL/F/10640–1

IEEE/IEC



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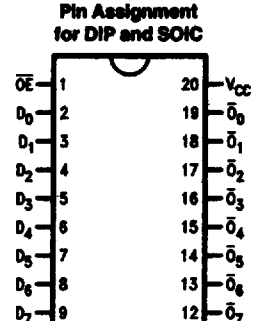
Connection Diagram

Pin Assignment for DIP and SOIC



TL/F/10640–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	TRI-STATE Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with respect to GND (V_{TERM})
74FCTA −0.5 to 7.0V

Temperature Under Bias (T_{BIAS})
74FCTA −55°C to +125°C

Storage Temperature (T_{STG})
74FCTA −55°C to +125°C

DC Output Current (I_{OUT}) 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ FCT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
74FCTA 4.75V to 5.25V

Input Voltage 0V to V_{CC}

Output Voltage 0V to V_{CC}

Operating Temperature (T_A)
74FCTA 0°C to +70°C

Junction Temperature (T_J)
PDIP 140°C

Note: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} 5.0V ±5%, T_A = 0°C to +70°; $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	74FCTA Min	74FCTA Typ	74FCTA Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			2.5 2.5 −2.5 −2.5	μA	V_{CC} = Max	$V_O = V_{CC}$ V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4	V_{CC} 4.3			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA I_{OH} = −15 mA
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3	0.2 0.50		V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = 300 μA I_{OL} = 48 mA

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; V_{HC} = V_{CC} − 0.2V.

Symbol	Parameter	74FCTA Min	74FCTA Typ	74FCTA Max	Units	Conditions	
I_{CC}	Maximum Quiescent Supply Current		1.0	40.0	µA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_i = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.40	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open $\overline{OE}$ = GND f_{CP} = 10 MHZ 50% Duty Cycle f_i = 5 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	7.8		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}$ = GND f_{CP} = 10 MHz 50% Duty Cycle f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	16.8			V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	74FCTA $T_A = +25°C$, $V_{CC} = 5.0V$	74FCTA $T_A, V_{CC} = Com$, $R_L = 500\Omega$, $C_L = 50\ pF$			Units	Fig. No.
		Typ	Min	(Note)	Max		
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_n$	4.5	2.0		6.5	ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	5.5	1.5		6.5	ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	4.0	1.5		5.5	ns	2-11
t_S	Set-Up Time High or Low D_n to CP	1.0	2.0			ns	2-10
t_H	HOLD Time High or Low D_n to CP	1.0	1.5			ns	2-10
t_W	CP Pulse Width High or Low	4.0	5.0			ns	2-9

Note: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance ($T_A = +25°C$, f = 1.0 MHz)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note: This parameter is measured at characterization but not tested.