- **Members of the Texas Instruments Widebus™ Family**
- **Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **High-Impedance State During Power Up and Power Down**
- **Typical V_{OLP} (Output Ground Bounce) <1 V at V_{CC} = 5 V, T_A = 25°C**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

SN54ABT162827A . . . WD PACKAGE
SN74ABT162827A . . . DGG OR DL PACKAGE
(TOP VIEW)

1$\overline{OE1}$	1	56	1$\overline{OE2}$
1Y1	2	55	1A1
1Y2	3	54	1A2
GND	4	53	GND
1Y3	5	52	1A3
1Y4	6	51	1A4
V_{CC}	7	50	V_{CC}
1Y5	8	49	1A5
1Y6	9	48	1A6
1Y7	10	47	1A7
GND	11	46	GND
1Y8	12	45	1A8
1Y9	13	44	1A9
1Y10	14	43	1A10
2Y1	15	42	2A1
2Y2	16	41	2A2
2Y3	17	40	2A3
GND	18	39	GND
2Y4	19	38	2A4
2Y5	20	37	2A5
2Y6	21	36	2A6
V_{CC}	22	35	V_{CC}
2Y7	23	34	2A7
2Y8	24	33	2A8
GND	25	32	GND
2Y9	26	31	2A9
2Y10	27	30	2A10
2$\overline{OE1}$	28	29	2$\overline{OE2}$
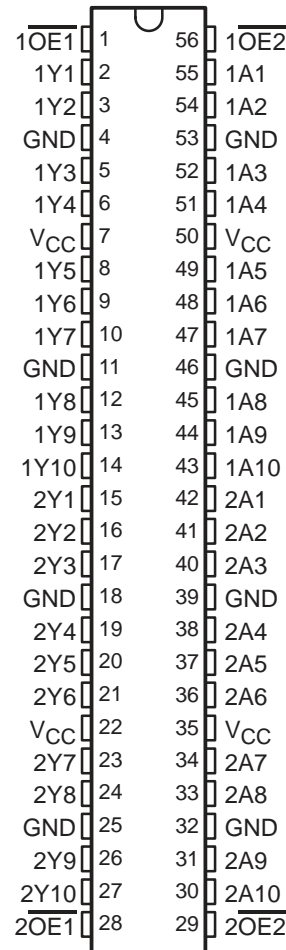
description/ordering information

The 'ABT162827A devices are noninverting 20-bit buffers composed of two 10-bit buffers with separate output-enable signals. For either 10-bit buffer, the two output-enable (1$\overline{OE1}$ and 1$\overline{OE2}$, or 2$\overline{OE1}$ and 2$\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP – DL	Tube	SN74ABT162827ADL	ABT162827A
		Tape and reel	SN74ABT162827ADLR	
	TSSOP – DGG	Tape and reel	SN74ABT162827ADGGR	ABT162827A
−55°C to 125°C	CFP – WD	Tube	SNJ54ABT162827AWD	SNJ54ABT162827AWD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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## description/ordering information (continued)

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ shall be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each 10-bit buffer)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic diagram (positive logic)
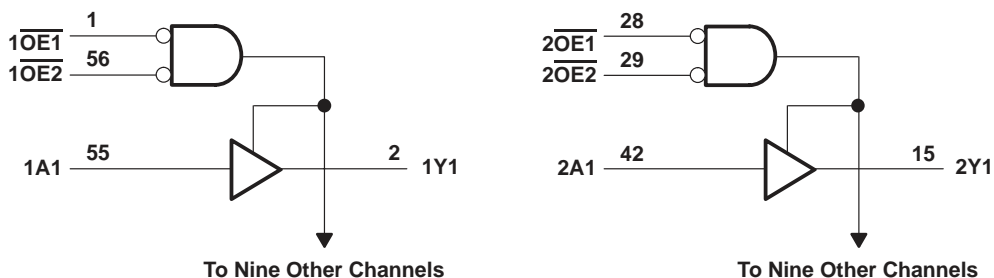
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V

Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V

Voltage range applied to any output in the high or power-off state, V_O .... −0.5 V to 5.5 V

Current into any output in the low state, I_O .... 30 mA

Input clamp current, I_{IK} ($V_I < 0$) .... −18 mA

Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA

Package thermal impedance, θ_{JA} (see Note 2): DGG package .... 64°C/W

DL package .... 56°C/W

Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

		SN54ABT162827A		SN74ABT162827A		UNIT
		MIN	**MAX**	**MIN**	**MAX**	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		−3		−12	mA
I_{OL}	Low-level output current		8		12	mA
$\Delta t/\Delta V$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		µs/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 3:   All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TEXAS INSTRUMENTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$T_A = 25°C$			SN54ABT162827A		SN74ABT162827A		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			−1.2		−1.2		−1.2	V
V_{OH}		$V_{CC} = 4.5$ V,	$I_{OH} = -1$ mA	3.35			3.35		3.35		V
		$V_{CC} = 5$ V,	$I_{OH} = -1$ mA	3.85			3.85		3.85		
		$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA	3.1			3.1		3.1		
			$I_{OH} = -12$ mA	2.6*					2.6		
V_{OL}		$V_{CC} = 4.5$ V	$I_{OL} = 8$ mA		0.4			0.8		0.65	V
			$I_{OL} = 12$ mA			0.8*				0.8	
V_{hys}					100						mV
I_I		$V_{CC} = 0$ to 5.5 V, $V_I = V_{CC}$ or GND				±1		±1		±1	µA
I_{OZPU}		$V_{CC} = 0$ to 2.1 V, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$				±50		±50		±50	µA
I_{OZPD}		$V_{CC} = 2.1$ V to 0, $V_O = 0.5$ V to 2.7 V, $\overline{OE} = X$				±50		±50		±50	µA
I_{OZH}‡		$V_{CC} = 2.1$ V to 5.5 V, $V_O = 2.7$ V, $\overline{OE} \geq 2$ V				10		10		10	µA
I_{OZL}‡		$V_{CC} = 2.1$ V to 5.5 V, $V_O = 0.5$ V, $\overline{OE} \geq 2$ V				−10		−10		−10	µA
I_{off}		$V_{CC} = 0$, V_I or $V_O \leq 4.5$ V				±100				±100	µA
I_{CEX}		$V_{CC} = 5.5$ V, $V_O = 5.5$ V	Outputs high			50		50		50	µA
I_O§		$V_{CC} = 5.5$ V,	$V_O = 2.5$ V	−25	−75	−100	−25	−100	−25	−100	mA
I_{CC}		$V_{CC} = 5.5$ V, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high			2		2		2	mA
			Outputs low			32		32		32	
			Outputs disabled			2		2		2	
ΔI_{CC}¶	Data inputs	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled			1		1.5		1	mA
			Outputs disabled			0.05		1		0.05	
	Control inputs	$V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	
C_i		$V_I = 2.5$ V or 0.5 V			4						pF
C_O		$V_O = 2.5$ V or 0.5 V			7						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at $V_{CC} = 5$ V.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT162827A		SN74ABT162827A		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.1	3.6	1	4.1	1	3.9	ns
t_{PHL}			1.1	2.8	4.2	1.1	5	1.1	4.7	
t_{PZH}	$\overline{OE}$	Y	1.5	3.4	6.3	1.5	7.2	1.5	6.9	ns
t_{PZL}			1.6	3.5	5.3	1.6	6.6	1.6	6.3	
t_{PHZ}	$\overline{OE}$	Y	2.1	4.1	6.5	2.1	6.8	2.1	6.6	ns
t_{PLZ}			1.5	3.5	5.9	1.5	7.3	1.5	6.3	

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PARAMETER MEASUREMENT INFORMATION
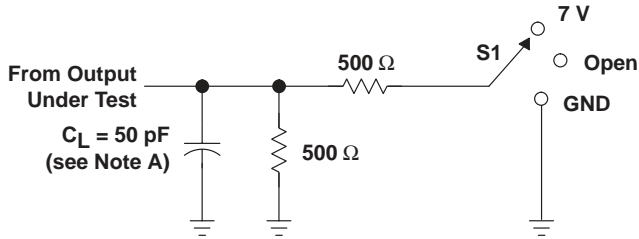
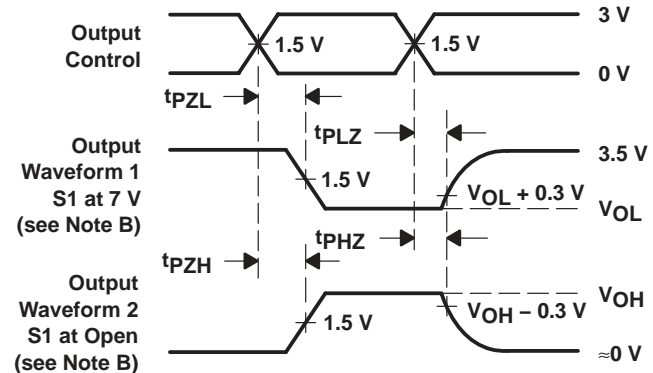| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT
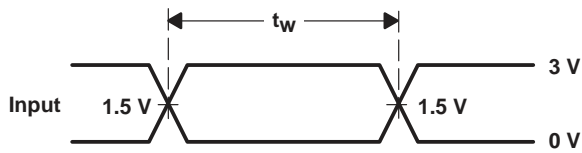
VOLTAGE WAVEFORMS
PULSE DURATION
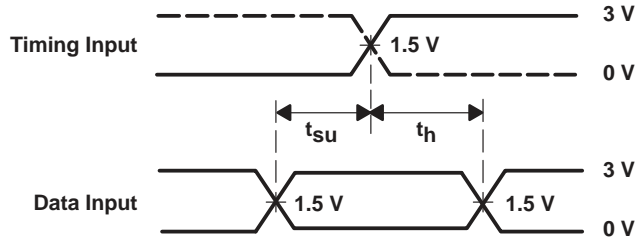
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
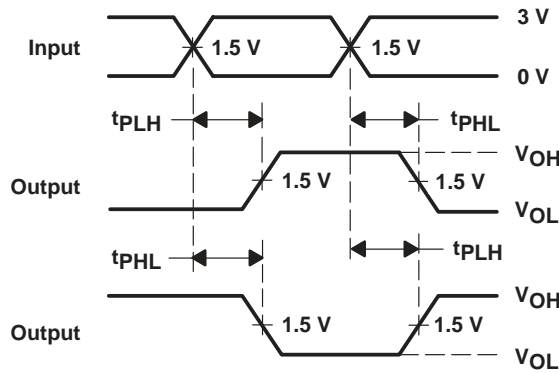
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
      B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
         Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
      C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
      D. The outputs are measured one at a time, with one transition per measurement.
      E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABT162827ADGGR	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162827A	Samples
SN74ABT162827ADL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162827A	Samples
SN74ABT162827ADLR	ACTIVE	SSOP	DL	56	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT162827A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
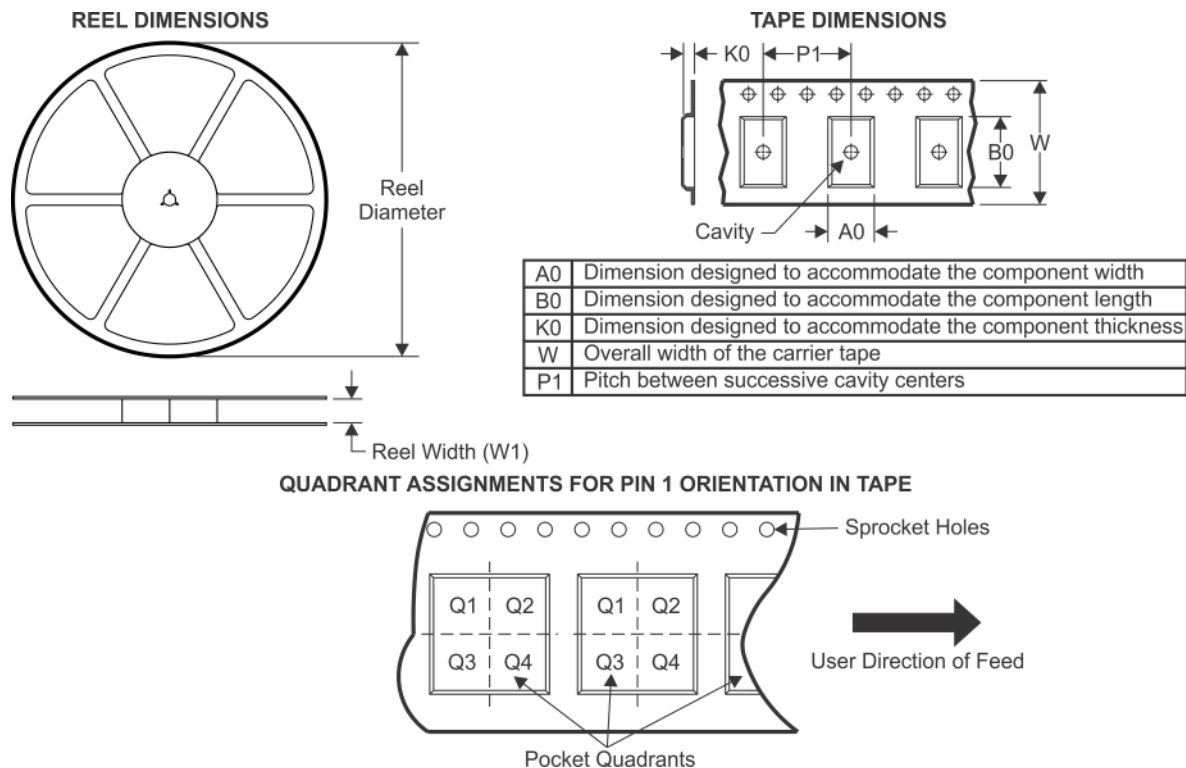
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT162827ADGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74ABT162827ADLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT162827ADGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74ABT162827ADLR	SSOP	DL	56	1000	367.0	367.0	55.0

PACKAGE MATERIALS INFORMATION

TUBE
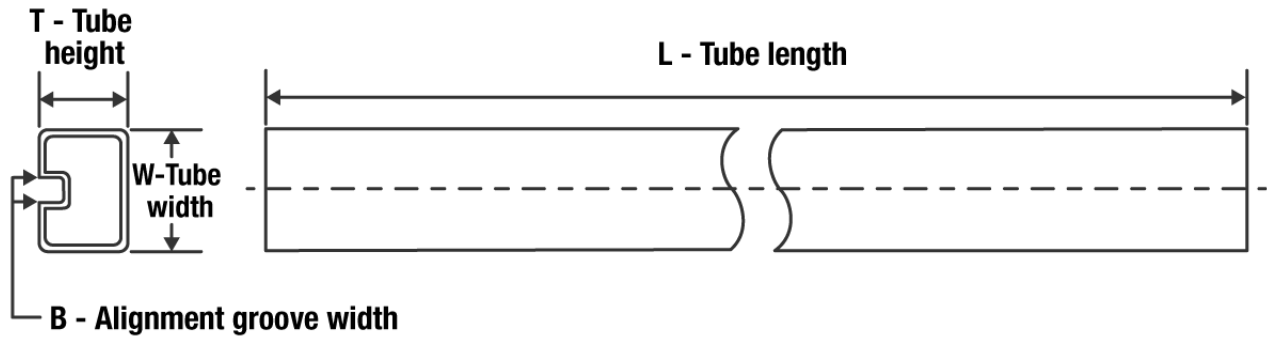
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ABT162827ADL	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R−PDSO−G56)   PLASTIC SMALL−OUTLINE PACKAGE

0.025 (0,635)

0.0135 (0,343)
0.008 (0,203)

⊕ 0.005 (0,13) Ⓜ

56   29

0.420 (10,67)
0.395 (10,03)

0.010 (0,25)
0.005 (0,13)

0.299 (7,59)
0.291 (7,39)

Gage Plane

0.010 (0,25)

1   28

0°−8°

0.730 (18,54)
0.720 (18,29)

0.040 (1,02)
0.020 (0,51)

0.110 (2,79) MAX

0.008 (0,20) MIN

Seating Plane

△ 0.004 (0,10)

4040048−4/F 05/13
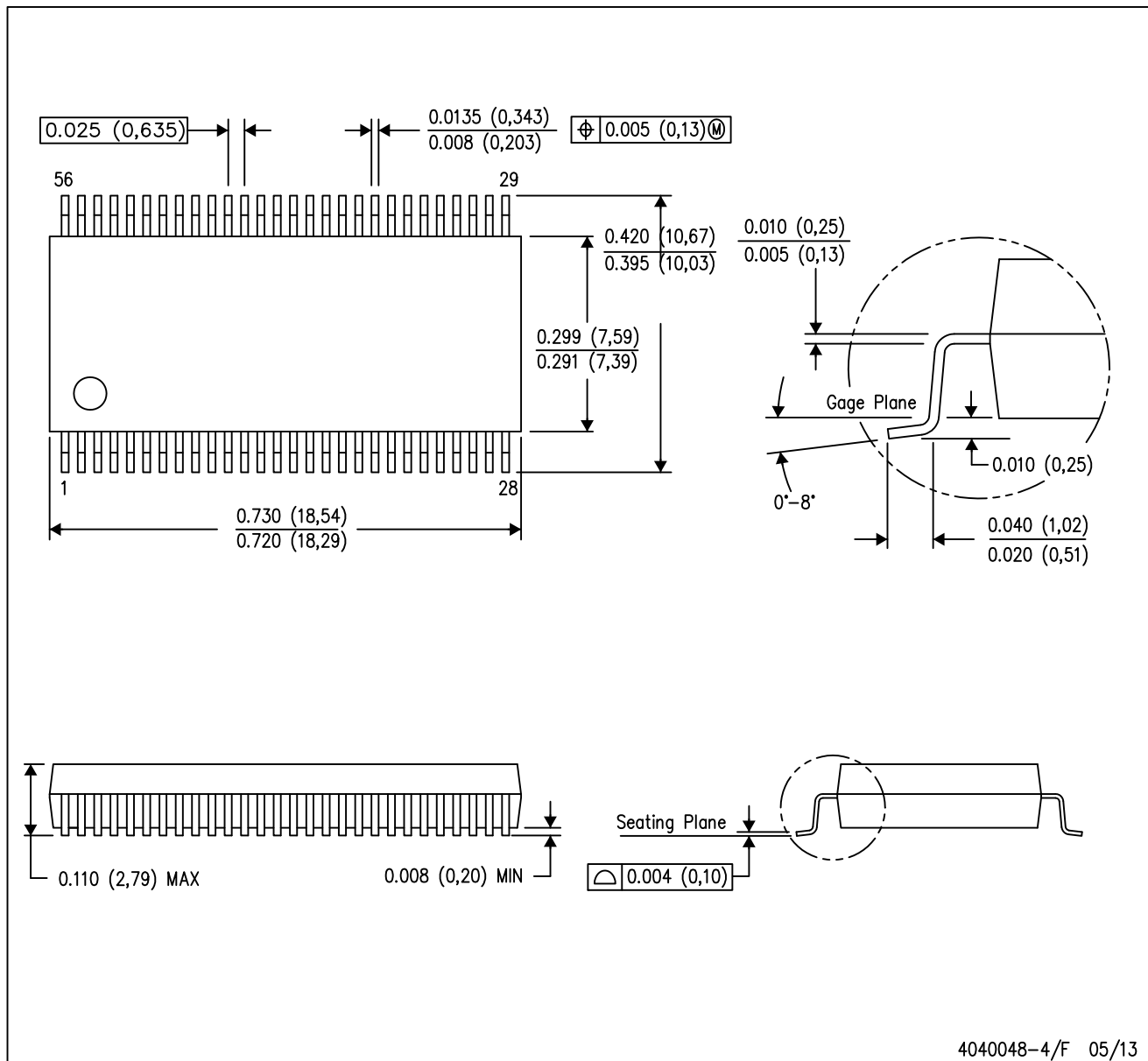
NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MO−118

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8.3
7.9 TYP

A

PIN 1 ID
AREA

1

54X 0.5

56

14.1
13.9
NOTE 3

2X
13.5

28

29

6.2
6.0

B

56X 0.27
0.17

⊕ 0.08 Ⓜ C AⓈ BⓈ

C

SEATING PLANE

⌒ 0.1 C

1.2 MAX

(0.15) TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

0.75
0.50

0.15
0.05
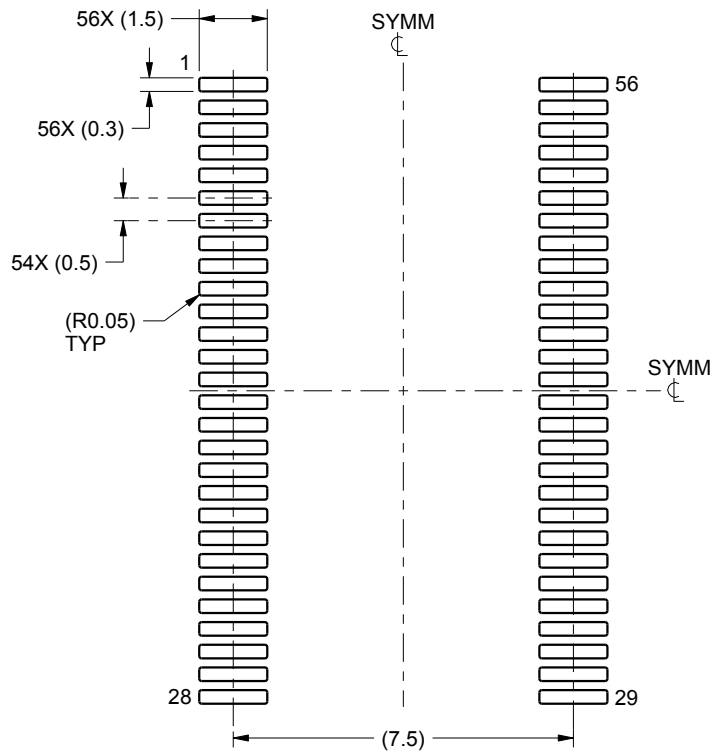
DETAIL A
TYPICAL
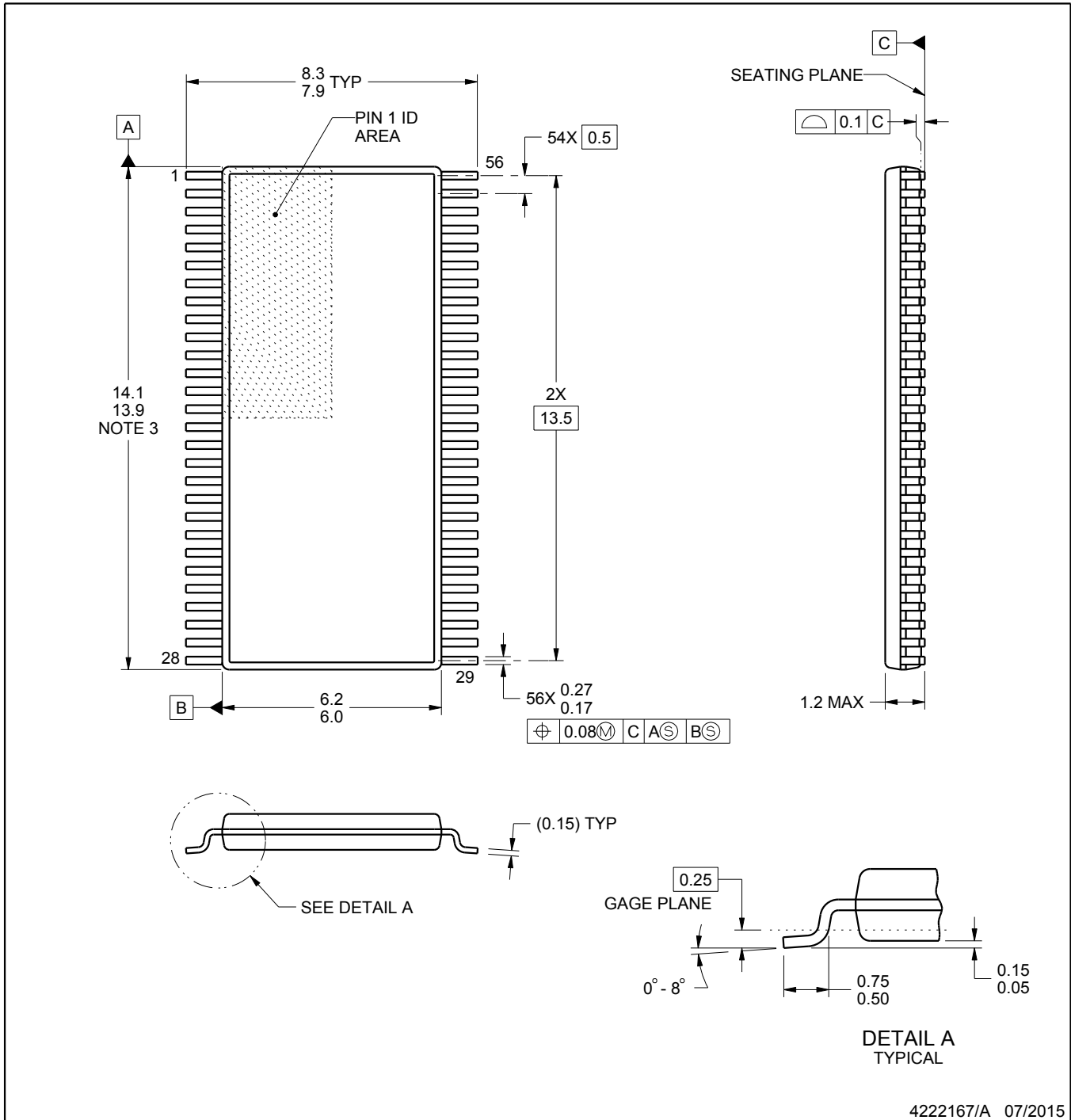
4222167/A   07/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
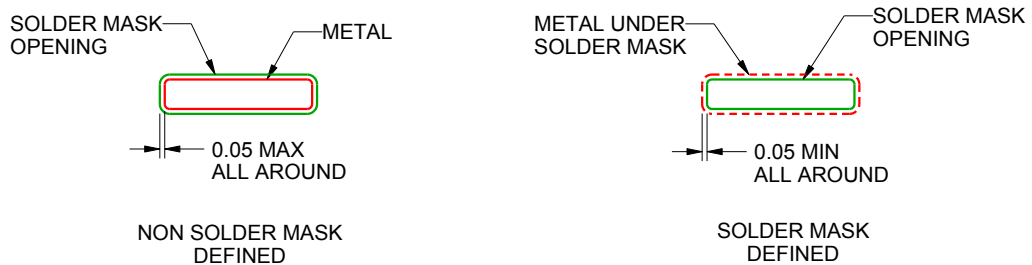4. Reference JEDEC registration MO-153.

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DGG0056A

56X (1.5)

1

56X (0.3)

56

54X (0.5)

(R0.05)
TYP

SYMM

SYMM

28

29

(7.5)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

**NON SOLDER MASK
DEFINED**

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

**SOLDER MASK
DEFINED**

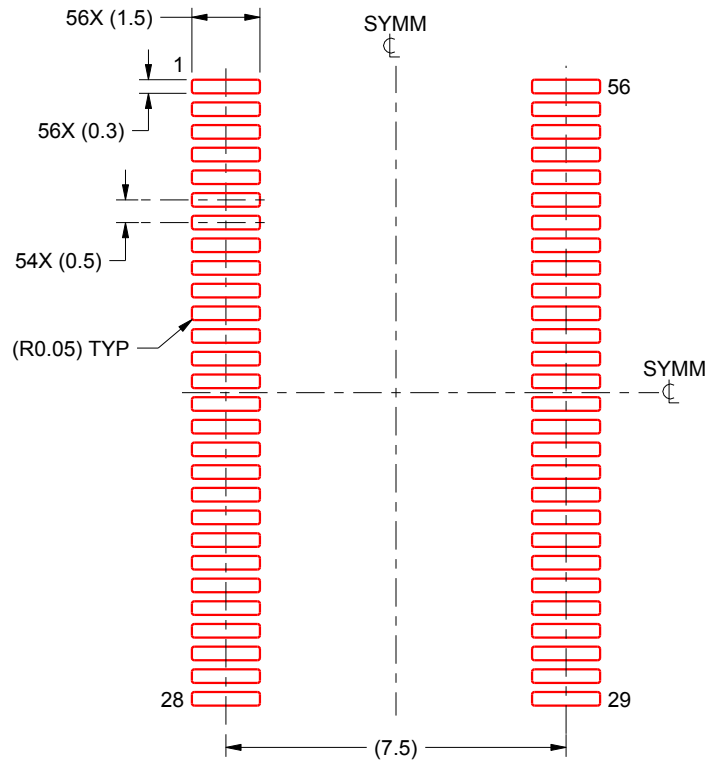**SOLDER MASK DETAILS**

4222167/A   07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

56X (1.5)

SYMM

1

56

56X (0.3)

54X (0.5)

(R0.05) TYP

SYMM

28

29

(7.5)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A   07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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