EVLVIPER25L-10WSB: 5 V/10 W, quasi-resonant isolated flyback
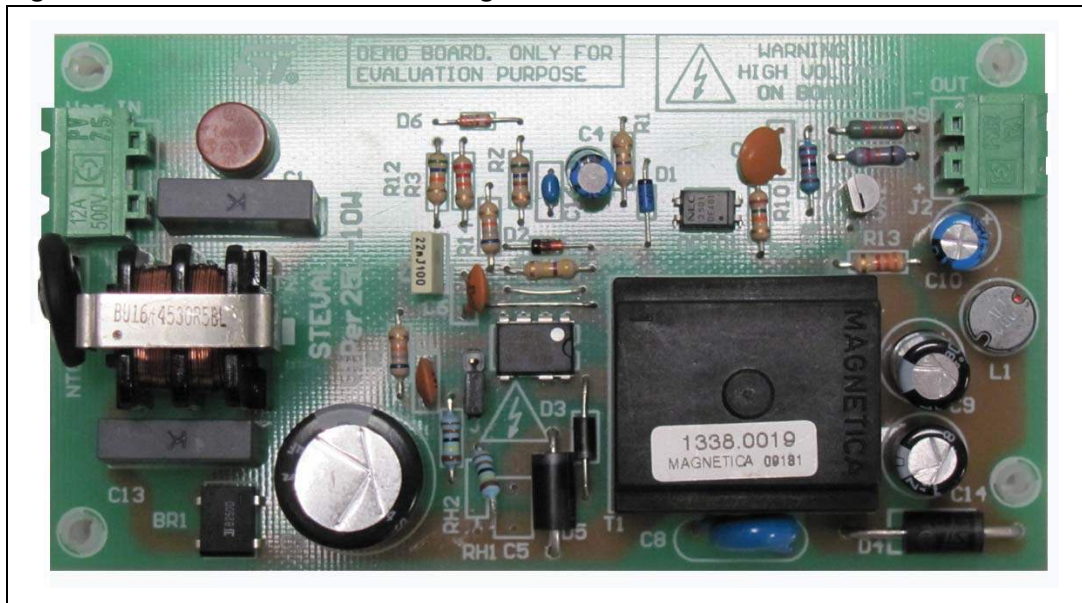
Introduction

This document describes a 5 V - 2 A SMPS using VIPer25, a current-mode offline converter, specifically designed to build quasi-resonant flyback converters. Quasi-resonant operation, in conjunction with other features of the device (very low quiescent currents; valley skipping operation at light load; burst mode operation at very low or disconnected load) helps to reach very good requirements both in terms of efficiency and in terms of consumption from the mains at light load, allowing to meet the most modern SMPS standards.

The other features of the device are: 800 V avalanche rugged power section, limiting current with adjustable set point, onboard soft-start, safe auto-restart after a fault condition, and feed-forward correction.

The available protections are: adjustable and accurate overvoltage protection, thermal shutdown with hysteresis, and delayed overload protection.

Figure 1.   Demonstration board image

Contents

List of tables

List of figures

1 Adapter features

Table 1 lists the electrical specifications of the demonstration board.

Table 1. Electrical specifications

Parameter	Symbol	Value
Input voltage range	V_{IN_AC}	[90 V_{AC} - 265 V_{AC}]
Output voltage	V_{OUT}	5 V
Max. output current	I_{OUTmax}	2 A
Precision of output regulation	$\triangle_{VOUT\_LF}$	±5%
High frequency output voltage ripple	$\triangle_{VOUT\_HF}$	50 mV
Max. ambient operating temperature	T_A	60 °C

1.1 Circuit description

The power supply is set in a flyback topology and its schematic is shown in Figure 2. The input section includes protection elements (fuse and NTC for inrush current limiting), a filter for EMC suppression (C1, T2, C13), a diode bridge (BR1), and an electrolytic bulk capacitor (C3) as the front-end AC-DC converter. The transformer uses a standard E25 ferrite core. A Transil™ clamp network is used for leakage inductance demagnetization.
At power-up the DRAIN pin supplies the internal HV startup current generator which charges the C4 capacitor up to V_{DDon}. At this point the power MOSFET starts switching, the generator is turned off, and the IC is powered by the energy stored in C4, until the auxiliary winding voltage becomes high enough to sustain the operation through D1 and R1. The value of the resistor R3 between the ZCD and GND pins defines the VIPer25 current limit and, in conjunction with D2 and R14, also realizes the overvoltage protection function. The ZCD pin is also responsible for the quasi-resonant operation, being a transformer demagnetization sensing input triggering the MOSFET turn-on.
Converter power capability variations with the mains voltage, inherent in quasi-resonant operation, are compensated by the R3-R15 voltage divider, which implements the line voltage feed-forward correction function. At very light or disconnected load the device enters burst mode, allowing to keep low the consumption from the mains in such conditions (< 50 mW at 265 V_{AC}). The output rectifier D4 has been selected according to the calculated maximum reverse voltage, forward voltage drop, and power dissipation, and is a power Schottky type. The output voltage regulation is performed by secondary feedback with a TS431 driving an optocoupler, in this case, a PC817, ensuring the required insulation between primary and secondary. The optotransistor drives directly the FB pin of the VIPer25, which is connected to the compensation network made up of C6, C7, and R12. A small LC network has been added at the output in order to filter the high frequency ripple without increasing the output capacitor size and a 100 nF capacitor has been placed very close to the output connector solder points, to limit the spike amplitude. Through jumper J, the BR pin can be either connected to a voltage divider sensing the mains rectified voltage in order to realize a brownout protection, or to GND. In the latter case, the RH1-RH2-RL branch can be disconnected from the mains in order to reach minimum standby consumption.

Figure 2. Application schematic
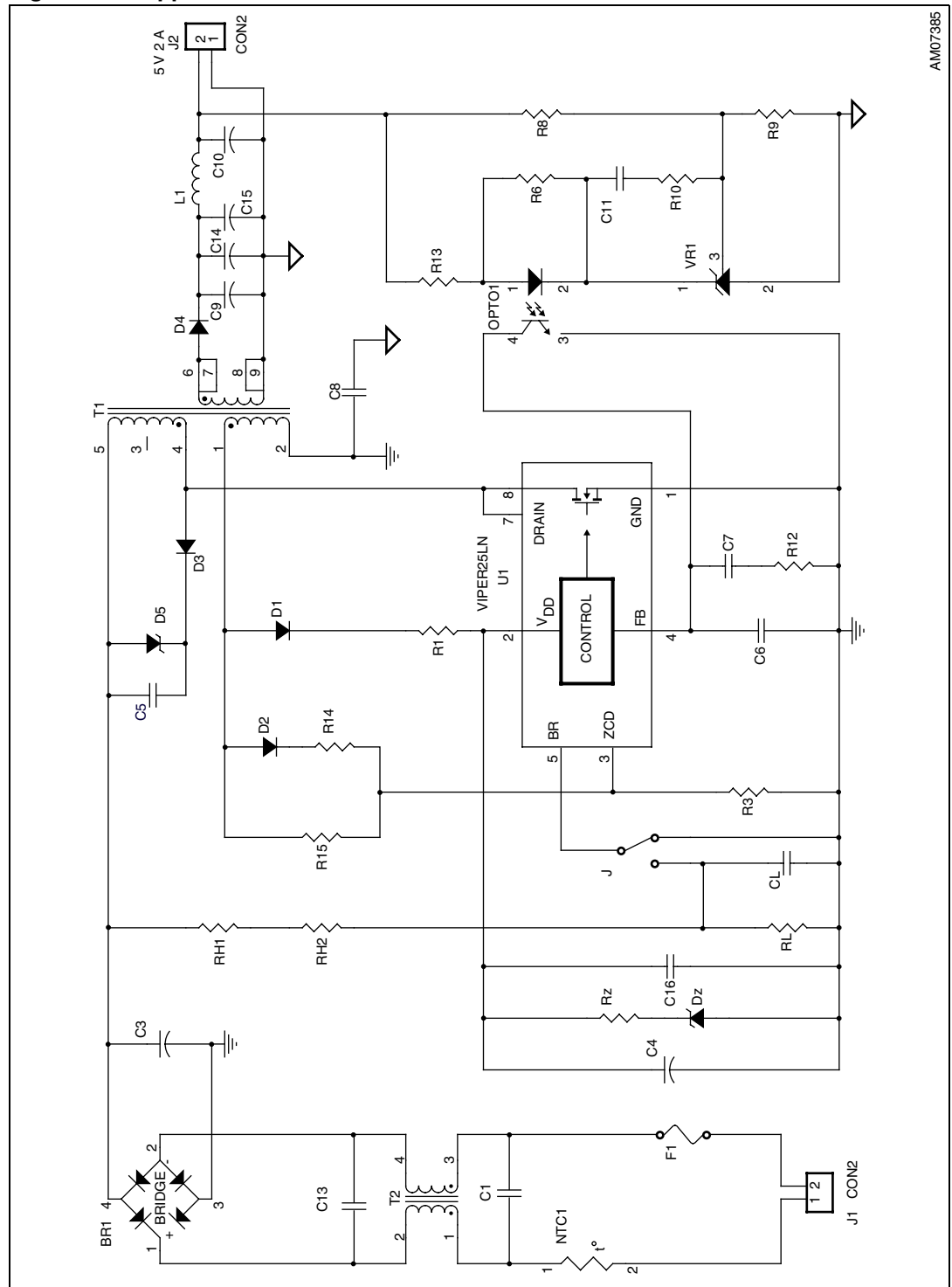
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Table 2. **Bill of material**

Reference	Part	Description	Manufacturer
BR1	DF06	Diode bridge	VISHAY®
C3	22 µF, 450 V	Electrolytic capacitor	
C4	22 µF, 35 V	Electrolytic capacitor	
C1, C13	100 nF	X2 capacitor	
C5	N.C.	Polypropylene capacitor	
C6	2.2 nF, 50 V	Ceramic capacitor	
C7	22 nF, 50 V	Polypropylene capacitor	
C8	2.2 nF	Y1 capacitor	
C9	N.C.	Electrolytic capacitor	
C10	100 µF, 25 V	Electrolytic capacitor	
C14, C15	680 µF, 16 V	Ultra-low ESR electrolytic capacitor, MCZ series	Rubycon
C11	27 nF, 50 V	Ceramic capacitor	
C16	100 nF, 50 V	Ceramic capacitor	
CL	10 nF, 50 V	Ceramic capacitor	
D1	BAT46	Small signal diode	STMicroelectronics™
D2	1N4148	Small signal diode	
D3	STTH1L06	Clamp diode	STMicroelectronics
D4	STPS5L60	Power diode	STMicroelectronics
D5	1.5KE250	Transil	STMicroelectronics
Dz		18 V Zener diode	
F1		Fuse 1.6 A 250 V	
NTC1	2.2 Ω	Thermistor	EPCOS
R1	4.7 Ω	1/4 W resistor	
R3	22 kΩ	1/4 W resistor	
R6	15 kΩ	1/4 W resistor	
R8	82 kΩ	1/4 W resistor, 1%	
R9	27 kΩ	1/4 W resistor, 1%	
R10	120 kΩ	1/4 W resistor	
R12	56 kΩ	1/4 W resistor	
R13	3.3 kΩ	1/4 W resistor	
R14	68 kΩ	1/4 W resistor	
R15	560 kΩ	1/4 W resistor	
Rz	560 Ω	1/4 W resistor	
RH1	1.1 MΩ	1/4 W resistor	

Table 2.   **Bill of material (continued)**

Reference	Part	Description	Manufacturer
RH2	1.1 MΩ	1/4 W resistor	
RL	12 kΩ	1/4 W resistor	
VR1	TS431	Voltage reference	STMicroelectronics
OPTO1	PC817	Optocoupler	
T1	1338.0019	Transformer	Magnetica®
T2	4530R4B	Common mode choke	TDK
L1	2.2 µH	RFB0807-2R2L	Coilcraft
J		3-pin jumper	
IC	VIPer25	PWM controller	STMicroelectronics

1.2   Transformer

The transformer's electrical characteristics are listed in *Table 3*.

Table 3.   **1338.0019 transformer characteristics**

Properties	Value	Test condition
Primary inductance	1.5 mH ±15%	Measured at 1 kHz
Leakage inductance	0.8% nom.	Measured at 10 kHz
Primary to secondary turn ratio (4 - 5)/(6, 7 - 10, 9)	12.85 ±5%	Measured at 10 kHz
Primary to auxiliary turn ratio (4 - 5)/(1 - 2)	5.29 ±5%	Measured at 10 kHz
Nominal operating frequency	60 kHz	VIPer25 demonstration board
Nominal/peak power	10 W/15 W	
Saturation current	1 A	B_{SAT} = 0.32T
Insulation	4 kV	Primary to secondary

The size, the pinout, and the mechanical characteristics are given in *Figure 3* and *4*:

Figure 3.   Transformer size and pin diagram

(a) Bottom view (pin side)   (b) Electrical diagram
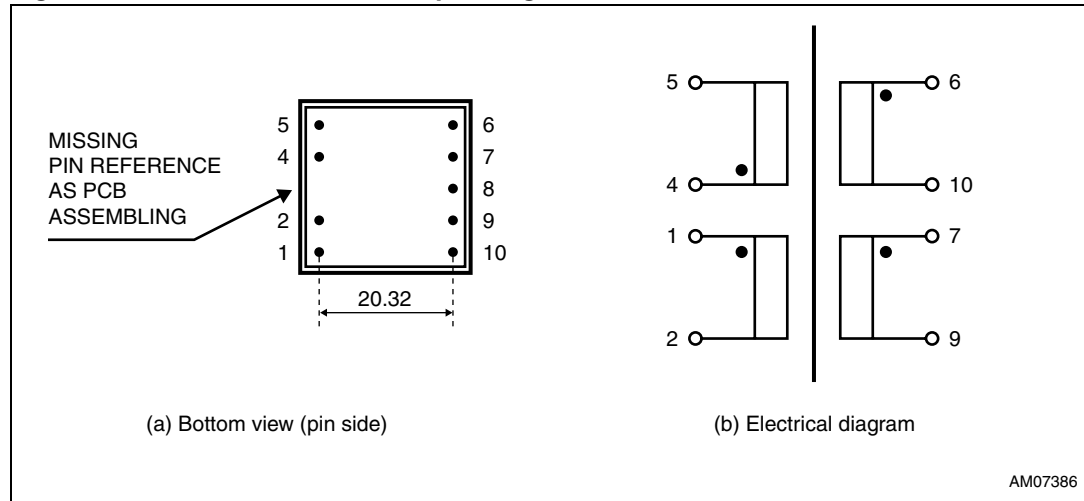
Figure 4.   Transformer size

(a) Side view 1   (a) Side view 2
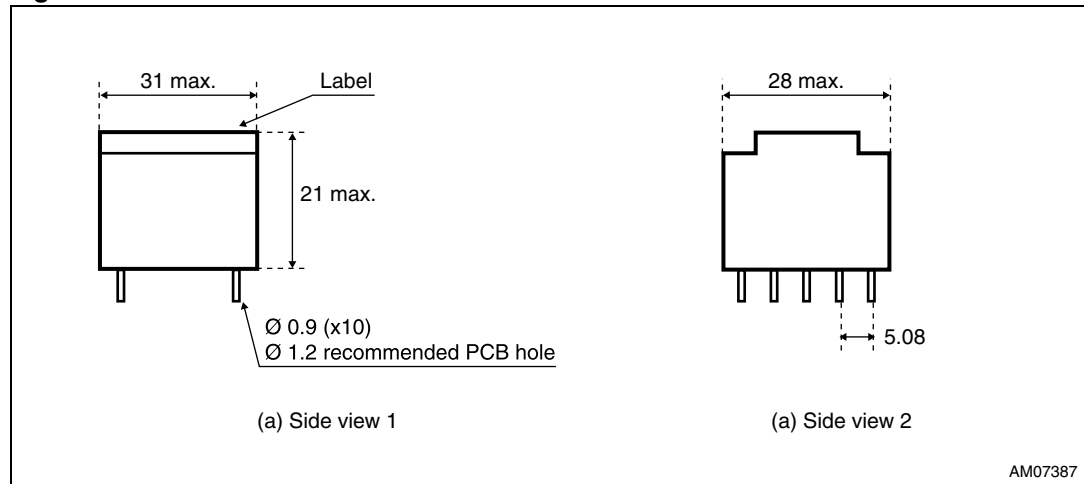
Table 4.   Transformer pin description

Pin	Description	Pin	Description
5	Primary, to the DC input voltage (400 V)	6	Secondary output 5 V 2 A (3 Apk)
4	Primary, to the drain of the MOSFET	7	
3	Removed	8	N. C.
2	Auxiliary GND	9	Secondary GND
1	Auxiliary output	10	

2 Testing the board

2.1 Typical board waveforms

The VIPer25 is operated in quasi-resonant mode. The ZCD (zero current detect) pin is able to sense the transformer demagnetization and switch on the MOSFET on the valley of the drain voltage ringing that follows the transformer demagnetization.
The converter has been designed so that in full load condition the MOSFET is always switched on, on the first valley of the transformer demagnetization, within the entire input voltage range. This operation mode is referred to as "quasi-resonant", or "boundary" between discontinuous conduction mode (DCM) and continuous conduction mode (CCM). *Figure 5* and *6* show drain current and voltage waveforms at nominal input voltages (115 V_{AC} and 230 V_{AC}) and maximum load (2 A). *Figure 7* and *8* show the same waveforms in the same load condition, but at minimum and maximum input voltage respectively.

Figure 5.	Drain current and voltage at max. load 115 V_{AC}	Figure 6.	Drain current and voltage at max. load 230 V_{AC}
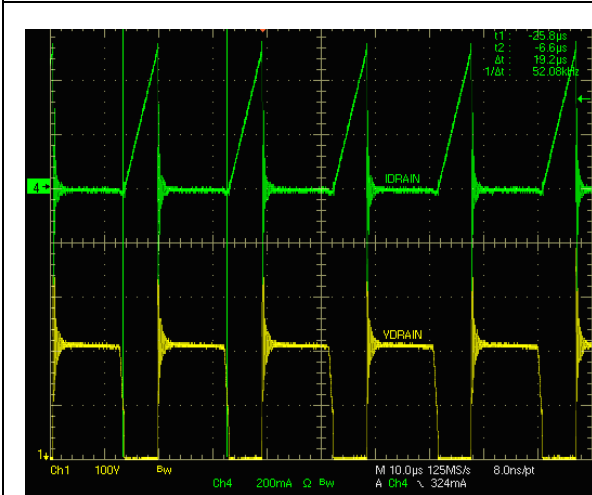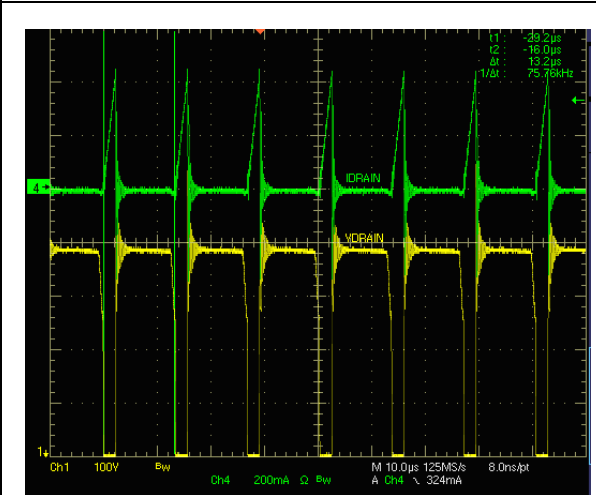
Figure 7. Drain current and voltage at max. load 90 V$_{AC}$	Figure 8. Drain current and voltage at max. load 265 V$_{AC}$
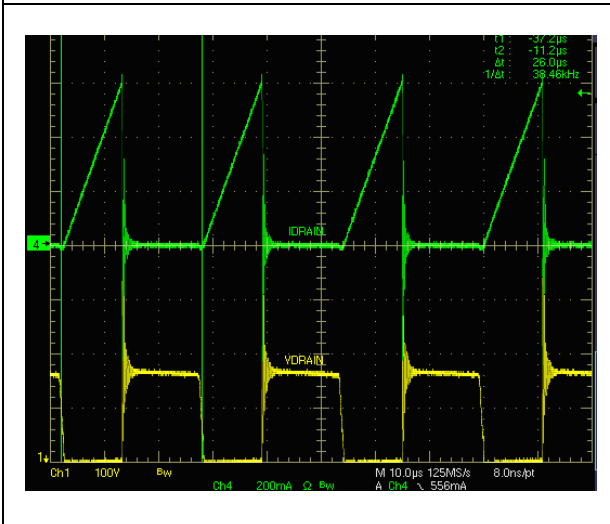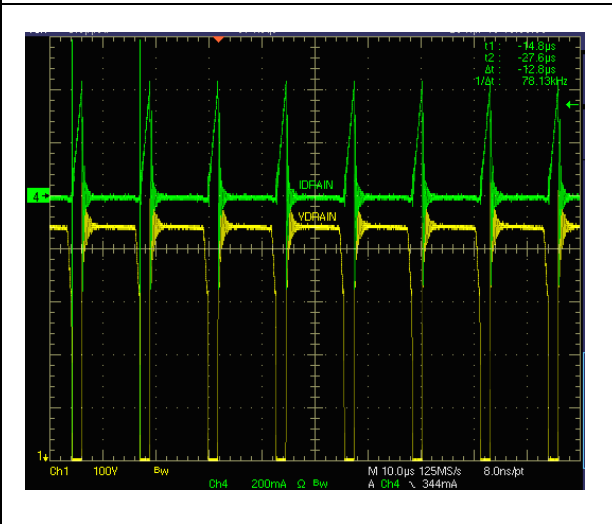
In quasi-resonant operation the switching frequency depends on the input/output conditions, increasing with increasing mains voltage and with decreasing output load. In fact, as the input voltage increases, the ON time is reduced and so the switching frequency increases; as the load decreases, the drain peak current (then also the needed ON time and the demagnetization time) decreases, therefore, the switching frequency increases.

In order to avoid the frequency increasing too much at medium/light load (which would result in an increase of all the frequency-related losses), the device is provided with a frequency fold-back function with an internal limit of 136 kHz (typ.); as the converter switching frequency approaches the limit, this function acts by inhibiting the MOSFET switch-on, on the first valley, and allowing it on the second, or the third and so on, depending on the working condition, as shown in *Figure 9* and *10* below. This mode of operation is referred to as "valley skipping mode".

In *Figure 9*, one ringing cycle of the drain voltage is always skipped. In this figure, what should be the switching frequency without the frequency fold-back function (f_{QR}), the MOSFET turn-on inhibit time ($1/f_{FF}$), and the actual converter switching frequency ($f_{Valley\_Skipping}$), is highlighted.

Figure 9. Drain current and voltage at 230 V$_{AC}$ 0.7 A (valley skip.)	Figure 10. Drain current and voltage at 115 V$_{AC}$ 0.6 A (uneven cycles)
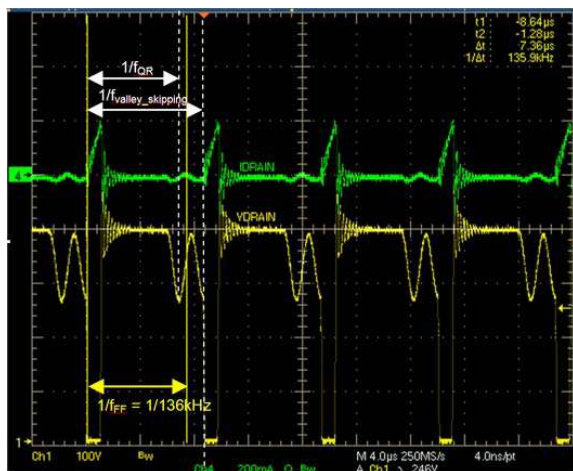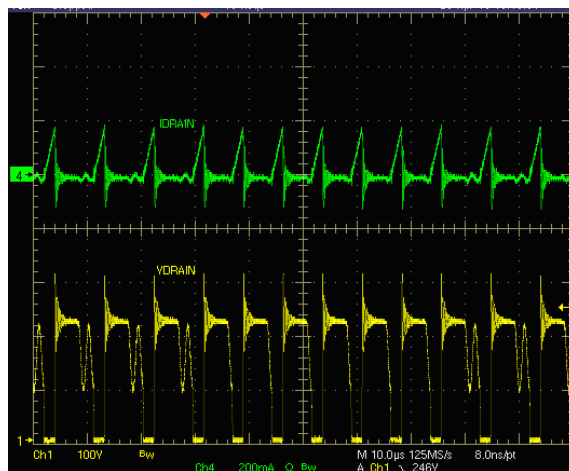
While the frequency fold-back is active, uneven switching cycles may be observed, due to the fact that the OFF time of the MOSFET is allowed to change with discrete steps (MOSFET is switched on always in the valley) while the OFF time needed for cycle-by-cycle energy balance may fall in between. One or more longer switching cycles is then compensated by one or more shorter ones, and vice versa.

This phenomenon (shown in *Figure 10*) is completely normal and there is no appreciable effect on the performance of the converter and its output voltage.

Figure 11 shows the changes of the switching frequency vs. the transformer input power (almost proportional to the output power) for two different input voltages.

Figure 11.   Switching frequency vs. transformer input power
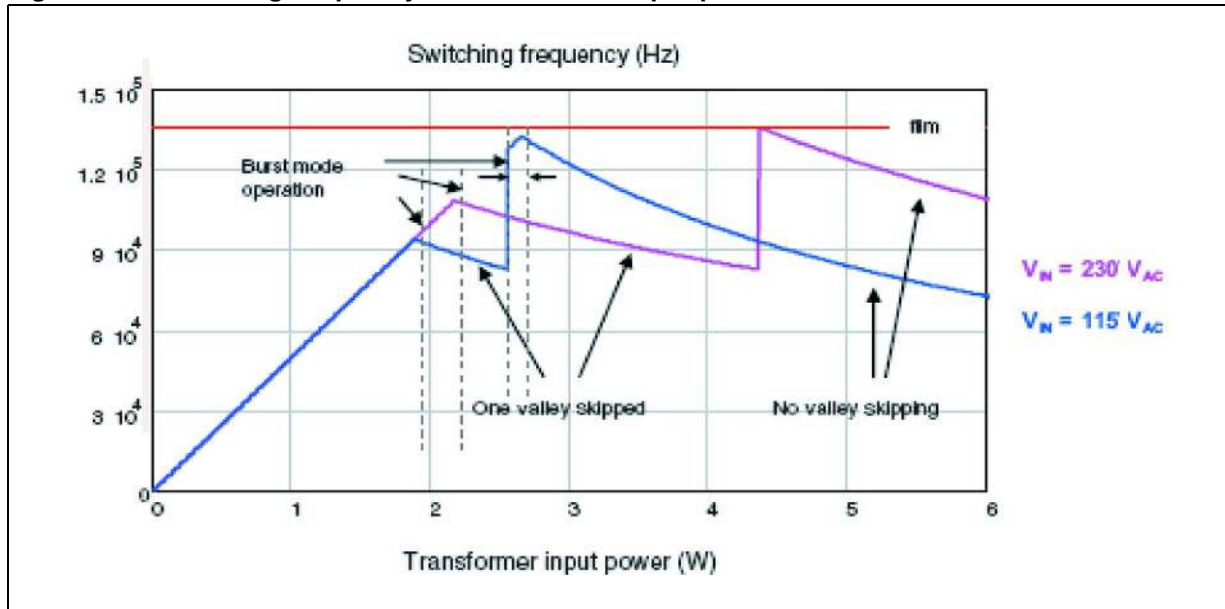
2.2 Regulation precision and output voltage ripple

The output voltage of the board and the V_{DD} pin voltage (rectified auxiliary output) have been measured in different line and load conditions. The results are given in *Table 5*. The output voltage practically is not affected by the line condition.

The V_{DD} voltage increases with the load on the regulated output; in order to avoid it exceeding its operating range an external clamp has been used (Dz, Rz).

Table 5.   Output voltage and V_{DD} line-load regulation

V_{IN} (VAC)	No load		Half load		Full load	
	V_{OUT} (V)	V_{DD} (V)	V_{OUT} (V)	V_{DD} (V)	V_{OUT} (V)	V_{DD} (V)
90	5.02	8.4	4.98	18.5	4.98	20.2
115	5.02	8.3	4.97	18.5	4.97	20.2
230	5.02	8.2	4.97	18.2	4.97	20.5
265	5.03	8.1	4.96	18.1	4.96	20.5

The ripple at the switching frequency superimposed at the output voltage has also been measured and the results are reported in *Table 6*.

Table 6.   Output voltage ripple

V_{IN} (VAC)	1/10 load	Half load	Full load
	V_{OUT} (mV)	V_{OUT} (mV)	V_{OUT} (mV)
90	45	19	50
115	46	16	38
230	48	22	28
265	48	25	27

Figure 12. Output voltage ripple at 115 V_{AC} - full load	**Figure 13.** Output voltage ripple at 230 V_{AC} - full load
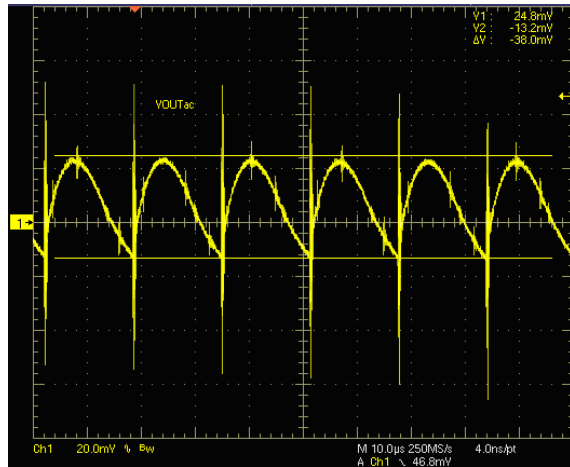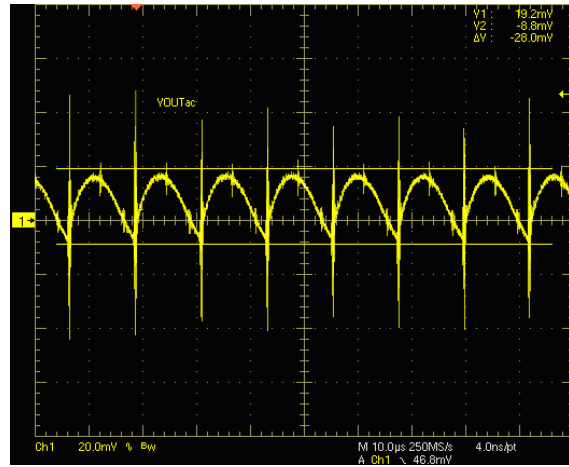
2.3 Burst mode and output voltage ripple

When the load is so low that the voltage at the FB pin falls below the V_{FBbm} internal threshold (0.6 V typical), the VIPer25 is disabled. At this point, the feedback reaction to the stop of the energy delivery makes the FB pin voltage increase again, and when it goes 100 mV above the V_{FBbm} threshold, the device restarts switching.
This results in a controlled on/off operation which is referred to as "burst mode" and is shown in the figures below, which report the output voltage ripple, the FB pin voltage, and the drain peak current when the converter is not or only lightly loaded and supplied with 115 V_{AC} and 230 V_{AC} respectively. During burst mode, the peak drain current value is I_{D_BM}, whose typical value is 160 mA, as shown in *Figure 15*. This mode of operation keeps the frequency-related losses low when the load is very light or disconnected and makes it easier to comply with energy saving regulations.

Figure 14. Output voltage ripple at 115 V_{AC} - no load
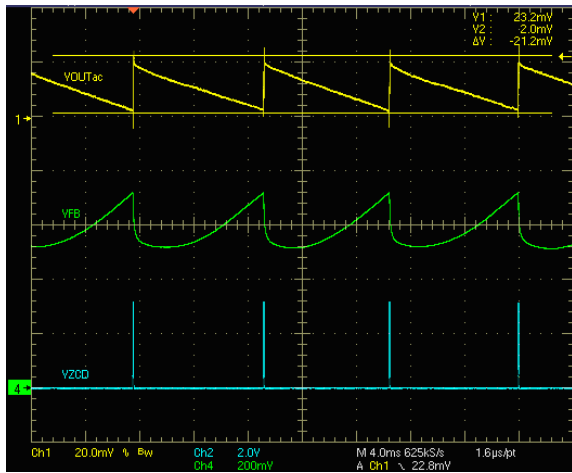
Figure 15. V_{FBbm}, $V_{FBbmhys}$ at 115 V_{AC} - no load
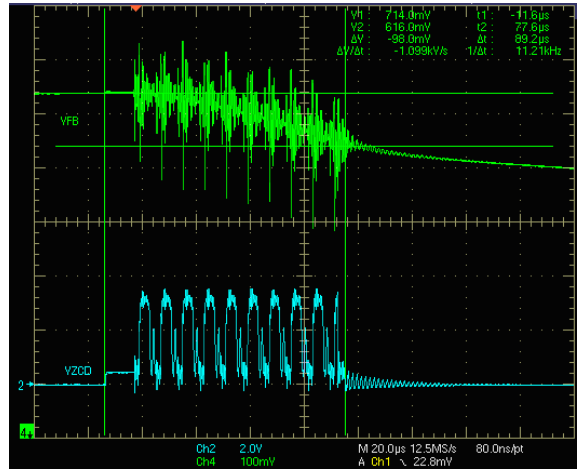
Figure 16. Output voltage ripple at 115 V_{AC} - 50 mA
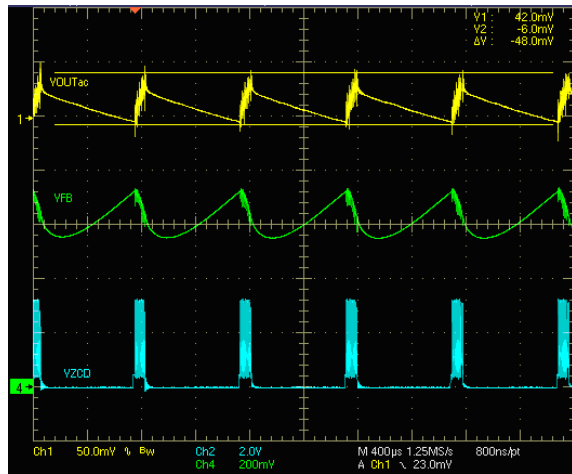
Figure 17. Output voltage ripple at 230 V_{AC} - 50 mA
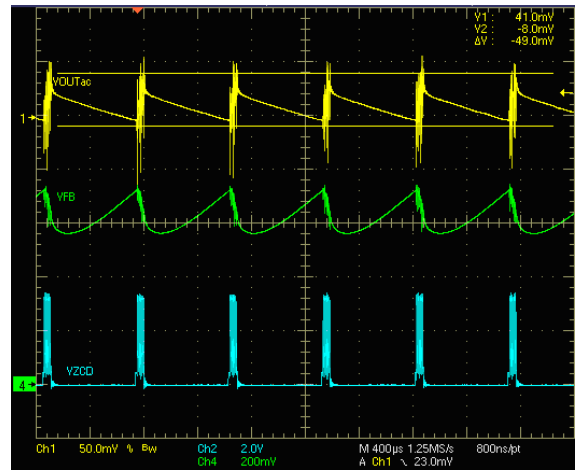
Table 7 shows the measured value of the burst mode frequency ripple measured in different operating conditions. The ripple in burst mode operation is very low and always below 50 mV.

Table 7.   Burst mode related output voltage ripple

V_{IN} (VAC)	No load (mV)	25 mA load (mV)	50 mA load (mV)
90	24	34	38
115	23	33	37
230	22	32	38
265	21	35	39

2.4   Efficiency

This section and the following section report the results of efficiency and light load measurements.
Appendix A at the end of this document provides some details on the settings of the power measurement equipment.
According to the ENERGY STAR® average active mode efficiency testing method, the efficiency measurements have been done at full load and at 75%, 50%, and 25% of full load for different input voltages. The results are reported in *Table 8*.

Table 8.   Efficiency

V_{IN} (VAC)	Efficiency (%)			
	Full load (2 A)	75% load (1.5 A)	50% load (1 A)	25% load (0.5 A)
90	78.00	80.60	81.33	82.83
115	80.42	82.40	82.37	82.83
150	81.95	83.16	82.46	82.34
180	82.49	83.33	82.15	81.62
230	82.63	83.00	81.17	80.33
265	82.25	82.29	80.00	79.28

For better visibility, the results have also been plotted in the diagrams below. *Figure 18* plots the efficiency vs. V_{IN} for the four different load values. *Figure 19* reports the efficiency as a function of the load for different input voltage values.

Figure 18. Efficiency vs. V$_{IN\_AC}$
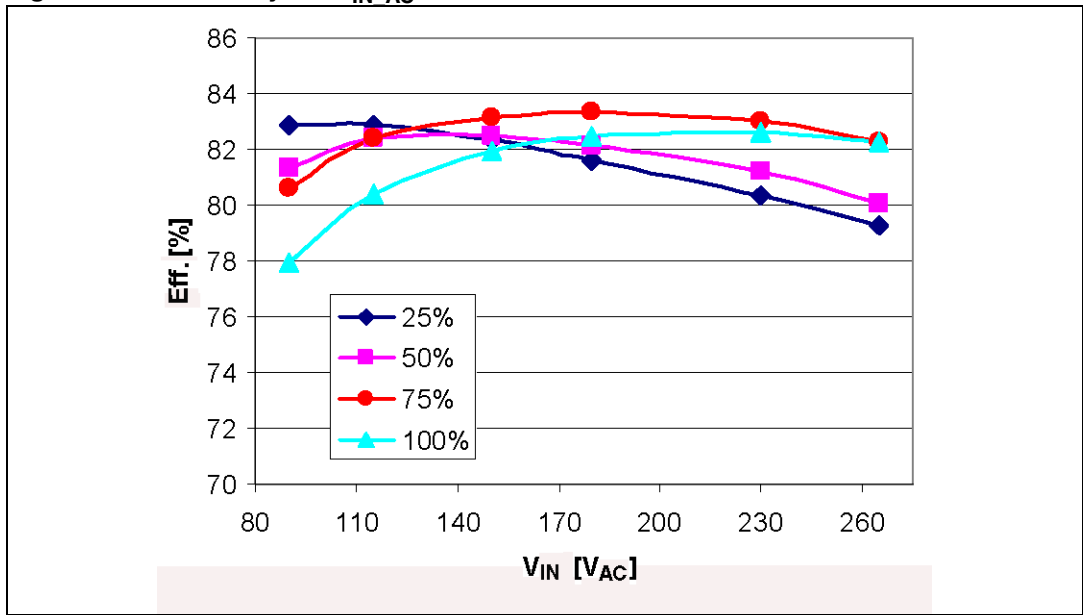
Figure 19. Efficiency vs. load
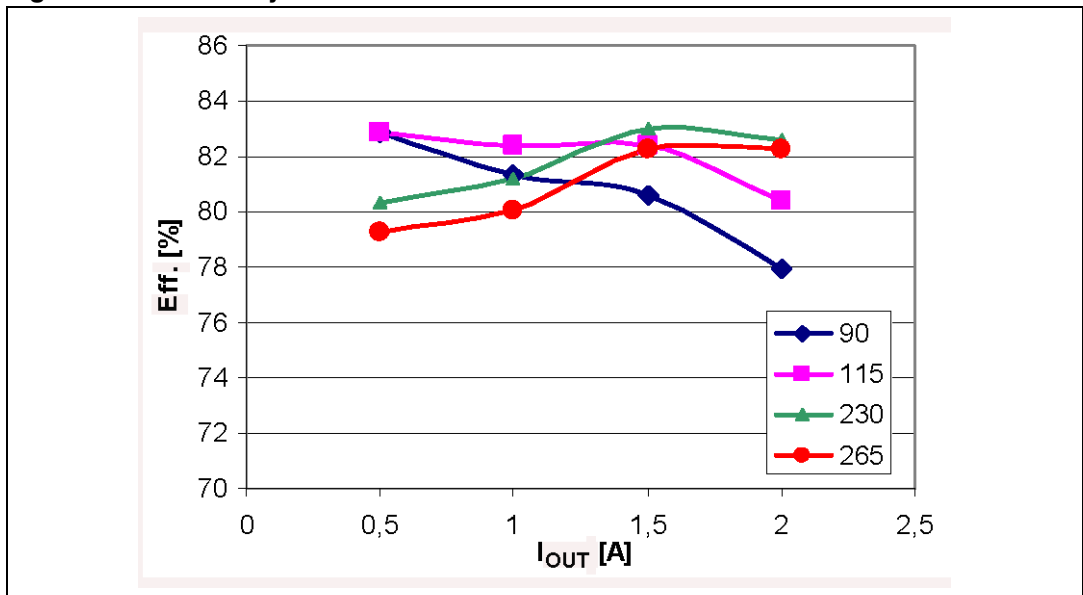
The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, and 75% of maximum load and at maximum load itself. *Table 9* reports the active mode efficiency calculated from the values in *Table 8*. For better visibility, *Table 9* values are plotted in *Figure 20*.

Table 9.   Active mode efficiencies

Active mode efficiency	
V_{IN} (VAC)	Efficiency (%)
90	80.67
115	82.00
150	82.48
180	82.40
230	81.78
265	80.97

Figure 20.   Active mode efficiency vs. V_{IN_AC}
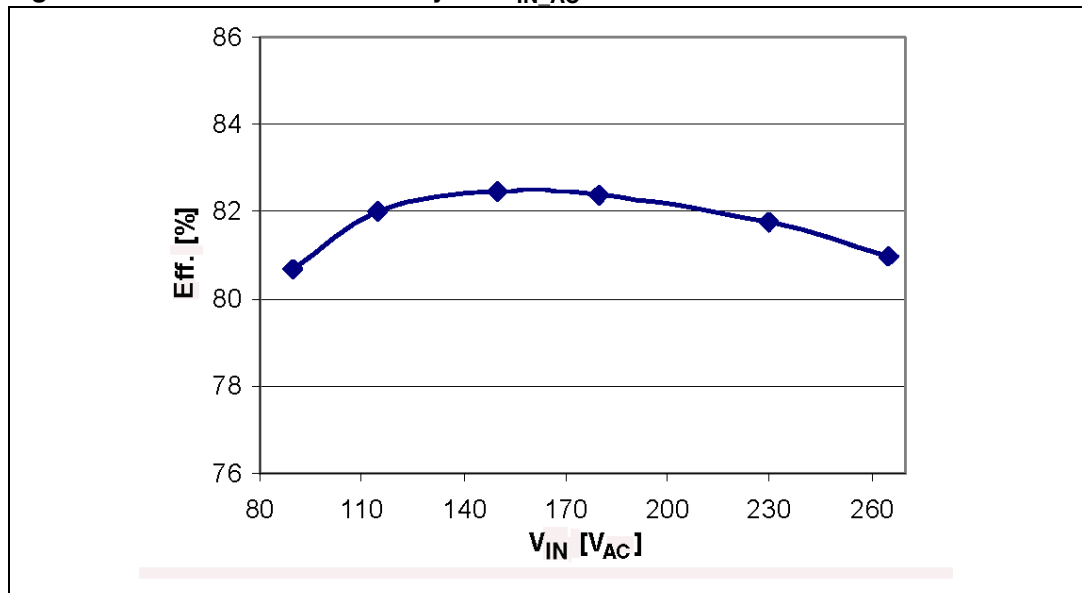
In *Table 10* and *Figure 21* the averaged value of the efficiency versus load are reported (average has been done considering the efficiency at different values of the input voltage).

Table 10.   Line voltage averaged efficiency vs. load

Load (% of full load)	Efficiency (%)
100	80.93
75	81.28
50	81.02
25	82.06

Figure 21. Input voltage averaged efficiency vs. load
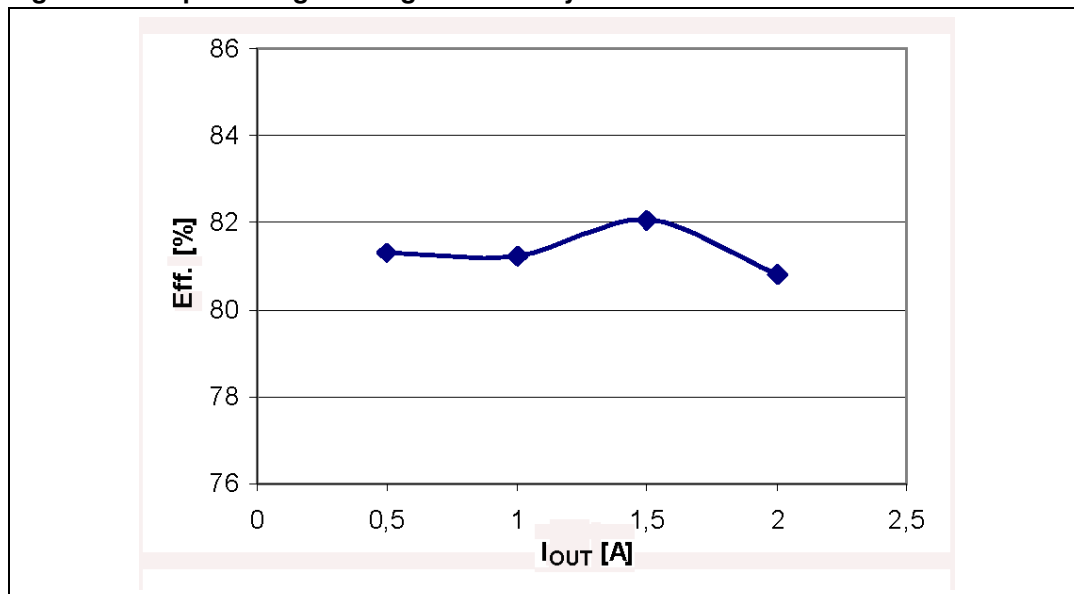
In version 2.0 of the ENERGY STAR program requirements for single voltage external AC-DC and AC-AC power supplies (1.), the power supplies are divided into two categories: low voltage power supplies and standard power supplies, with respect to the nameplate output voltage and current. To be considered a low-voltage power supply, an external power supply must have a nameplate output voltage of less than 6 V and a nameplate output current of more than or equal to 550 mA.

The following tables report the EPA energy efficiency criteria for AC-DC power supplies in active mode for standard models and low voltage models respectively.

Table 11.   Energy efficiency criteria for standard models

Nameplate output power (P_{no})	Minimum average efficiency in active mode (expressed as a decimal)
0 to ≤ 1 watt	$\geq 0.48 * P_{no} + 0.140$
> 1 to ≤ 49 watts	$\geq [0.0626 * \ln (P_{no})] + 0.622$
> 49 watts	≥ 0.870

Table 12.   Energy efficiency criteria for low voltage models

Nameplate output power (P_{no})	Minimum average efficiency in active mode (expressed as a decimal)
0 to ≤ 1 watt	$\geq 0.497 * P_{no} + 0.067$
> 1 to ≤ 49 watts	$\geq [0.075 * \ln (P_{no})] + 0.561$
> 49 watts	≥ 0.860

The criteria are plotted in *Figure 22*, where the red line depicts the criteria for the standard model and the blue line the criteria for the low voltage model. The PNO axis uses a logarithmic scale.

Figure 22.   ENERGY STAR efficiency criteria
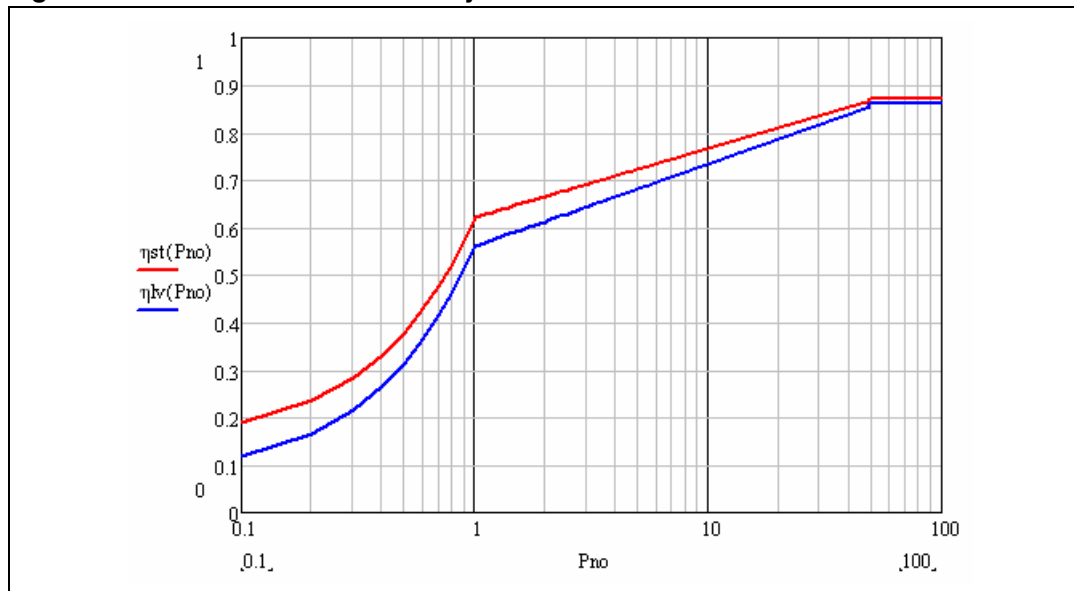
The presented power supply belongs to the low-voltage power supply category and, in order to be compliant with ENERGY STAR requirements, needs to have an efficiency higher than 73.37%. For all the considered input voltages, the efficiency results (see *Table 8*) are higher than the recommended value.

2.5   Light load performances

The input power of the converter was measured in no load conditions for different input voltages. The results are given in *Table 13*.

Table 13.   No load input power

V_{IN} (VAC)	P_{IN} (mW)
90	15
115	17
150	20
180	23
230	28
265	33

Version 2.0 of the ENERGY STAR program also takes into consideration the power consumption of the power supply when it is not loaded. The criteria to be compliant with are reported in *Table 14*.

Table 14. Energy consumption criteria for no load

Nameplate output power (P_{no})	Maximum power in no load for AC-DC EPS
0 to ≤ 50 watts	< 0.3 watts
> 50 watts < 250 watts	< 0.5 watts

The performance of the presented board is much better than required; the power consumption is about ten times lower than the ENERGY STAR limit. Even if the performance seems to be unproportionally better than required it is worth noting that often AC-DC adapter or battery charger manufacturers have very strict requirements about no load consumption, and if the converter is used as an auxiliary power supply, the line filter is often the big line filter of the entire power supply which significantly increases consumption in standby mode.

Even if the ENERGY STAR program does not have other requirements regarding light load performance, in order to provide complete information the input power and efficiency of the demonstration board, also in two other light load cases, is reported. *Table 15* and *16* show the board performances when the output load is 25 mW and 50 mW respectively.

Table 15. Light load performance P_{OUT} = 25 mW

V_{IN} (VAC)	P_{OUT} (mW)	P_{IN} (mW)	Eff. (%)	$P_{IN} - P_{OUT}$ (mW)
90	25	46	54.35	21
115	25	48	52.08	22
150	25	51	49.01	26
180	25	53	47.17	28
230	25	60	41.67	35
265	25	66	37.88	38

Table 16. Light load performance. P_{OUT} = 50 mW

V_{IN} (VAC)	P_{OUT} (mW)	P_{IN} (mW)	Eff. (%)	$P_{IN} - P_{OUT}$ (mW)
90	50	76.5	65.40	27
115	50	78	64.10	28
150	50	81	61.73	31
180	50	85	58.82	35
230	50	92	54.34	42
265	50	98	51.02	48

Figure 23 shows the input power vs. input voltage for no load and light load conditions.

Figure 23.   Input power vs. input voltage for no load and light load conditions
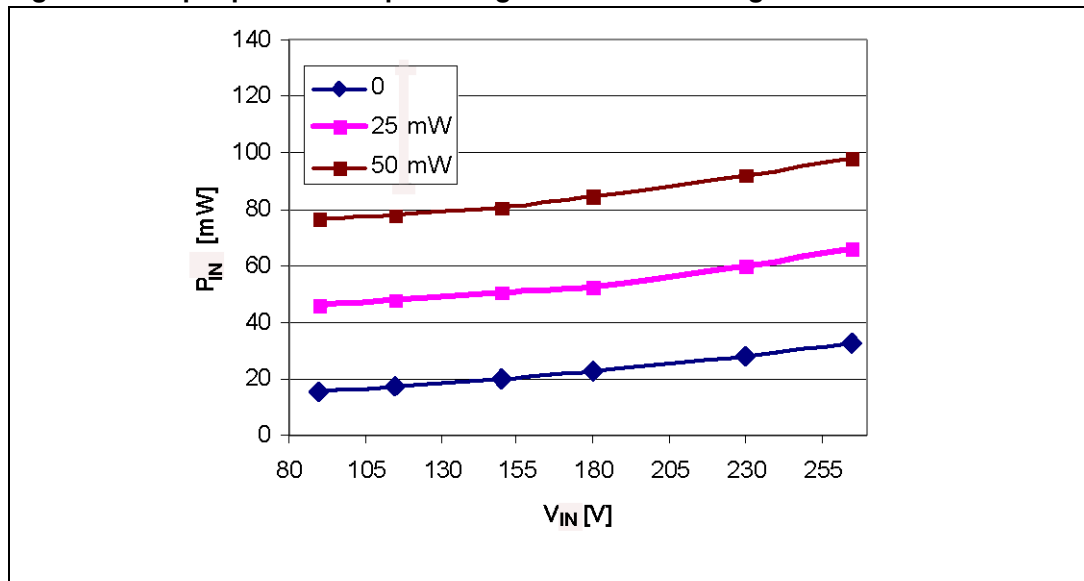
Depending on the equipment supplied, there are several criteria to measure the standby or light load performance of a converter. One of these is the measurement of the output power when the input power is equal to one watt. *Table 17* shows the output power needed to obtain 1 W of input power in different line conditions. *Figure 24* shows the results of this measurement.

Table 17.   Converter efficiency when the input power is 1 W

V_{IN} (VAC)	P_{IN} (W)	Eff. (%)
90	1	82.21
115	1	81.54
150	1	80.63
180	1	79.66
230	1	78.10
265	1	76.82

Figure 24. Converter efficiency when the input power is 1 W
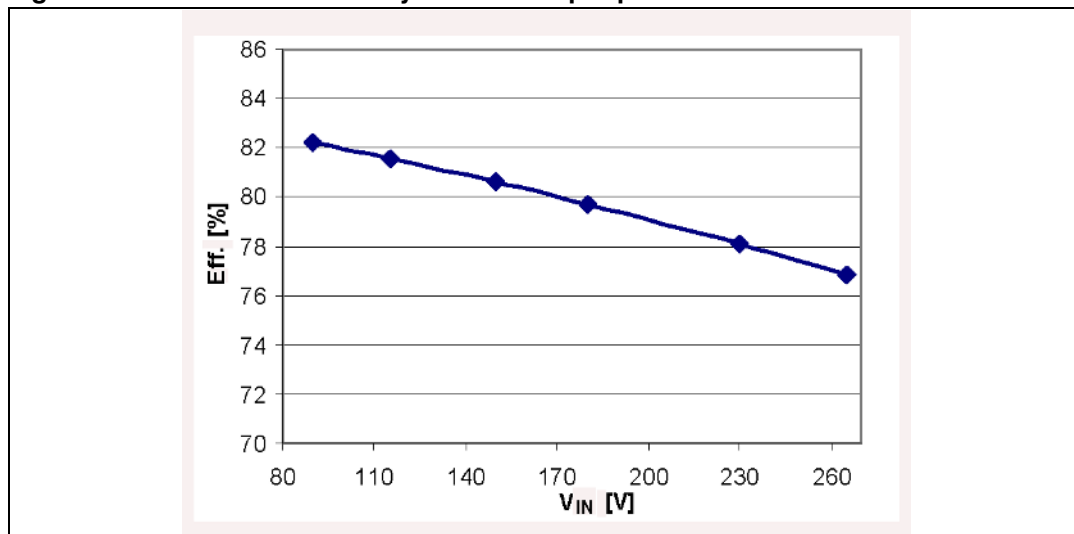
With the demonstration board presented here it is possible to have or to not have brownout protection. All the efficiency and light load performances have been measured with brownout protection disabled (series RH1, RH2, and RL in *Figure 2* disconnected). If brownout protection is required, for the same load condition, the input power increases, because the brownout network is connected in parallel with the bulk capacitor (C3 in the schematic) and dissipates some power according to the following formula:

Equation 1

$$P_{BR\_LOSS} = \frac{V_{BULK\_RMS}^2}{RH1 + RH2 + RL}$$

In light load condition the voltage across the bulk capacitor can be considered constant and equal to the peak of the AC input voltage. Considering the worst case of maximum input voltage the dissipation across the brownout network is:

Equation 2

$$P_{BR\_LOSS} = \frac{V_{ACMAX\_PK}^2}{RH1 + RH2 + RL} = \frac{(265 \cdot \sqrt{2})^2}{2.268 \cdot 10^6} = 64mW$$

which is negligible when measuring the efficiency in not too light load condition but becomes quite important when measuring the standby or light load performance.

2.6 Overload protection

The VIPer25 is a current mode converter. This means that the regulation of the output voltage is made by increasing or decreasing the primary peak current on a cycle-by-cycle basis as a consequence of the increase or decrease of the output power demand.
The peak current is internally sensed and converted into a voltage which is compared with the FB pin voltage. The device is shut down as soon as the two voltages are equal.
When the FB pin voltage reaches V_{FBlin} (3.3 V typical), the drain peak current reaches its maximum value, I_{DLIM} (which is 0.7 A typical or a lower value according to the value of the resistor if connected between the ZCD and GND pins).

If the load power demand exceeds the converter power capability, the FB pin voltage exceeds V_{FBlin}, the internal pull-up of the pin is disconnected and the pin starts sourcing a 3 µA current that charges the capacitor C7 of the schematic in *Figure 2*.

As the voltage across the FB pin reaches the V_{FB_olp} threshold (4.8 V typical), the VIPer25 stops switching (see *Figure 26*) and is not allowed to switch again until the V_{DD} voltage has fallen below $V_{DD\_RESTART}$ (4.5 V typical) and risen again up to V_{DD_ON} (14 V typical, see *Figure 25*). Therefore the value of C7 defines the maximum duration of an overload event without shutting down the IC.

If the overload (or short-circuit) is not removed, the protection is tripped again and the system works in auto-restart mode (see *Figure 25*, *27*, and *29*).

If the overload disappears, the converter resumes normal working mode at the first V_{DD} recycling, as shown in *Figure 29* and *30*.

C7 is needed because usually the value of the C6 capacitor, coming from the loop stability calculations, is too small to ensure an OLP delay time long enough to bypass the initial output voltage transient at startup. The value of C7 can be chosen high enough to provide the needed delay, and the value of R12 chosen so that the R12-C7 pole does not affect the stability of the loop.

During an overload the converter is operated at a very low duty cycle, being the MOSFET kept in the OFF state for most of the time. This results in a very low average power throughput, which is safe for the power elements in this condition.

Figure 25. OLP: output short and protection tripping	Figure 26. OLP: output short and protection tripping - zoom
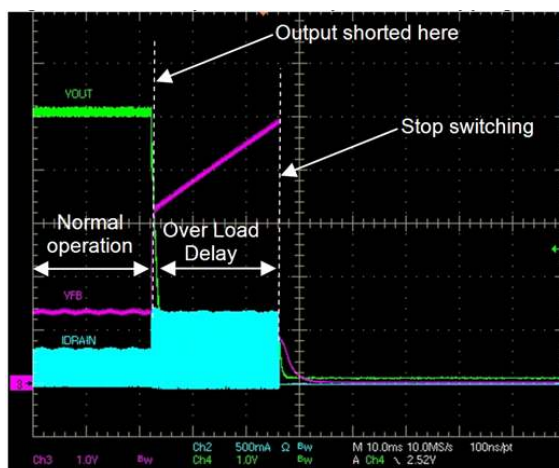
Figure 27. OLP: steady-state (auto-restart mode)	Figure 28. OLP: steady-state (auto-restart mode) - zoom

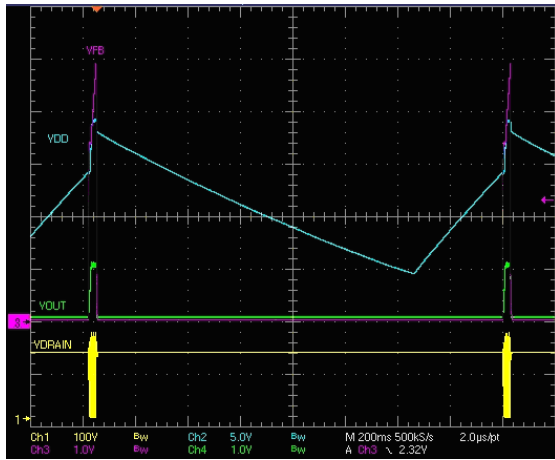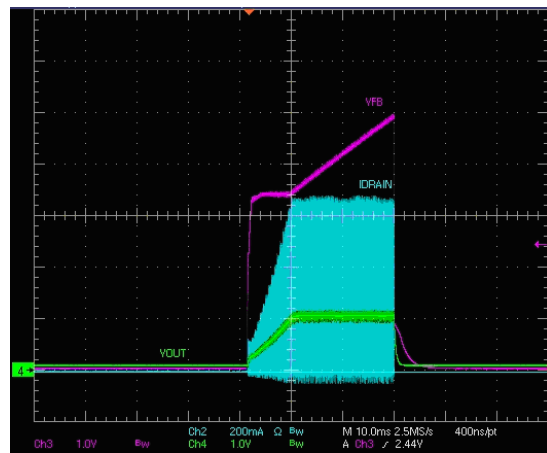| Figure 29. OLP: short removal and restart	Figure 30. OLP: short removal and restart - zoom
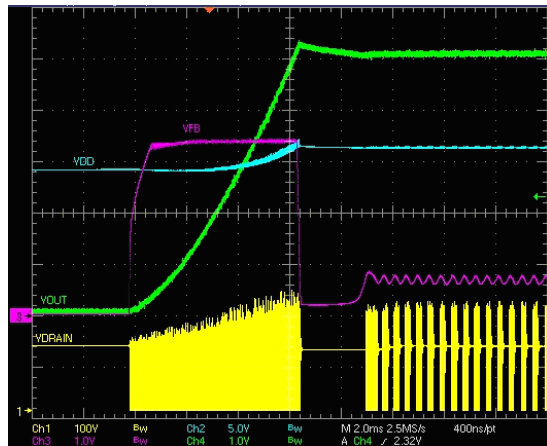
2.7   2nd OCP protection

The VIPer25 is provided with a first adjustable level of primary overcurrent limitation that switches off the power MOSFET if this level is exceeded. This limitation acts cycle-by-cycle, and its main purpose is to limit the maximum deliverable output power. A second level of primary overcurrent protection is also present, which is not adjustable but fixed to 1.2 A (typical value), to provide protection against short-circuit of the secondary rectifier, short - circuit on the secondary winding, or a hard-saturation of the flyback transformer. If the drain peak current exceeds this second overcurrent protection threshold, the device enters a warning state. If, during the next ON time of the power MOSFET, the second level of overcurrent protection is exceeded again, the device assumes that a secondary winding

short-circuit or a hard-saturation of the transformer is occurring and stops the PWM activity. To re-enable the operation, the V_{DD} pin voltage must be recycled, which means that V_{DD} must go down to $V_{DD(RESTART)}$), then rise up to V_{DDon}. At this point the MOSFET restarts switching. If the cause of activation of the second overcurrent protection is still present, the protection is tripped again and the system works in auto-restart mode, resuming normal operation as soon as the cause of the fault is removed and the V_{DD} recycled.

This protection has been tested in different operating conditions, short-circuiting the output diode. The following figures show the behavior of the system during these tests.

With faults such as those described, the 2nd OCP protection of the VIPer25 stops the operation after two switching cycles, therefore avoiding high currents in the primary as in the secondary windings and through the power section of the VIPer25 itself. *Figure 32* shows the operation when a permanent short-circuit is applied on the secondary winding. Most of the time the power section of VIPer25 is off, eliminating any risk of overheating.

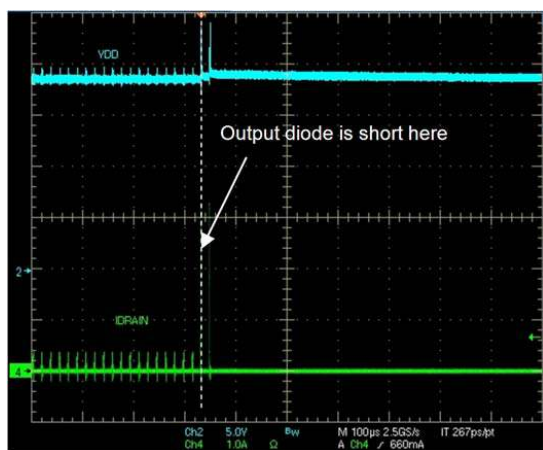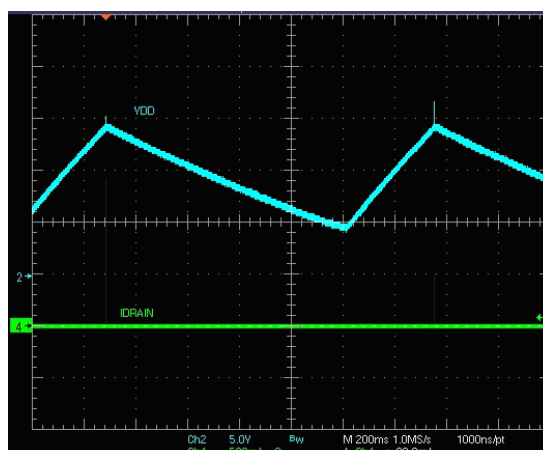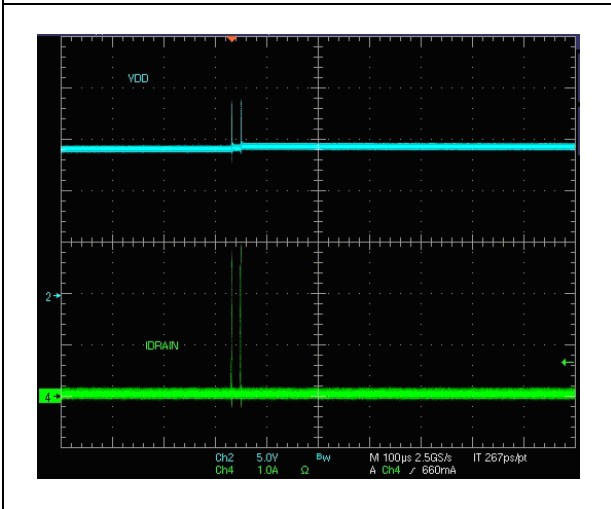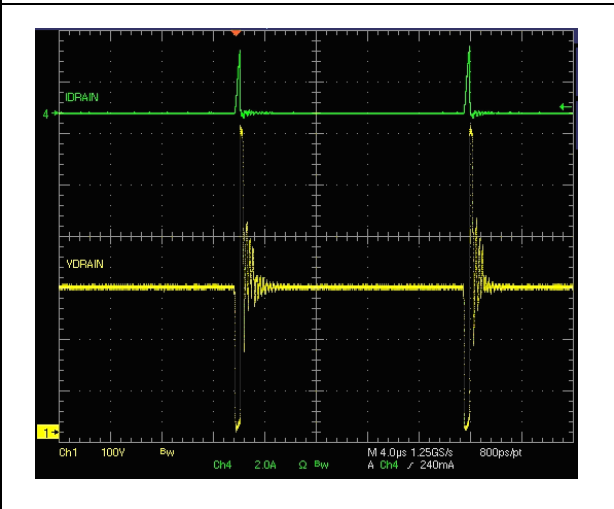| Figure 31. 2nd OCP protection tripping	Figure 32. Operating with secondary winding shorted - restart mode

Figure 33. Operating with secondary winding shorted - restart mode – zoom1	Figure 34. Operating with secondary winding shorted - restart mode – zoom2

2.8 Voltage feed-forward function

As briefly explained in *Section 2.1*, in a quasi-resonant converter the switching frequency increases with the input voltage.
According with *Equation 3*, for a fixed value of the maximum peak primary current, I_{PK_MAX}, the maximum deliverable output power is proportional to the switching frequency.

Equation 3

$$P_{IN\_TRAFO\_MAX} = \frac{1}{2} \cdot L_P \cdot I_{PK\_MAX^2} \cdot f_{sw}$$

If a power supply is designed in order to deliver a certain maximum output power at minimum input voltage, its power capability at maximum input voltage can be twice or more due to the increase of the switching frequency.
The system may not be able to detect an overload at high line because the load power demand does not exceed the converter power capability, therefore leading to overheating of the transformer, power MOSFET, and output diode.
In order to resolve this issue, the VIPer25 is provided with a voltage feed-forward function, which acts by lowering the maximum drain current as the input voltage increases.
This is realized by connecting a resistor between the auxiliary winding of the transformer and the ZCD pin (R_{FF} resistor in *Figure 35*). In fact, during the ON time of the MOSFET, the auxiliary winding voltage is negative and proportional to the flyback input voltage, therefore, through the R_{FF} resistor a current almost proportional to the input voltage is sunk by the ZCD pin. Thanks to the adjustable current limitation VIPer25 function, the maximum peak drain current is reduced proportionally to the increase of the input voltage value.

Figure 35. Implementing input voltage feed-forward function
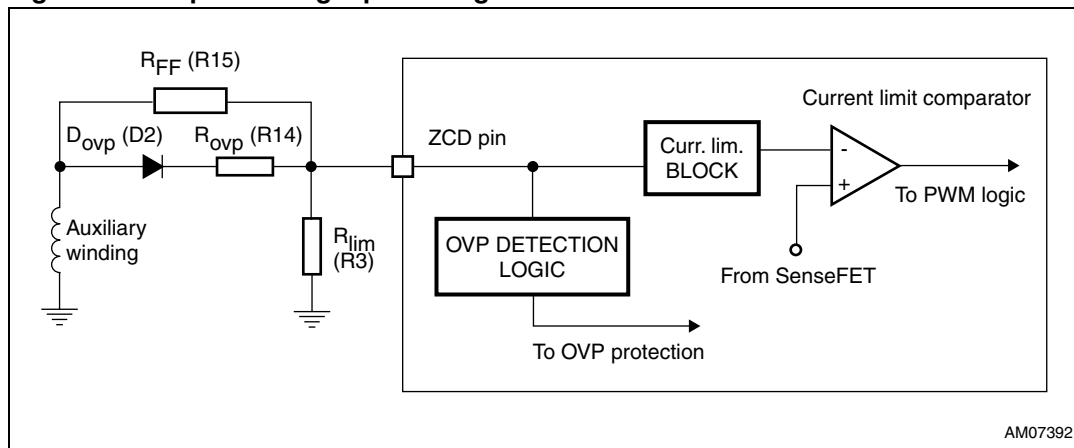
Figure 36 and *Table 18* show the output current when the overload protection is tripped (I_{OLP}, blue line), while the I_{OUT_REST} is the output current value at which the converter starts working again once the overload protection has been tripped and the output load gradually reduced.

Table 18. I_{OUT_OLP} and I_{OUT_REST} values

V_{IN} (VAC)	I_{OUT_OLP} [A]	I_{OUT_REST} [A]
90	2.12	1.88
115	2.26	1.97
230	2.37	1.96
265	2.31	1.88

Figure 36. I_{OUT_OLP} and I_{OUT_REST} vs. V_{IN_AC} diagram
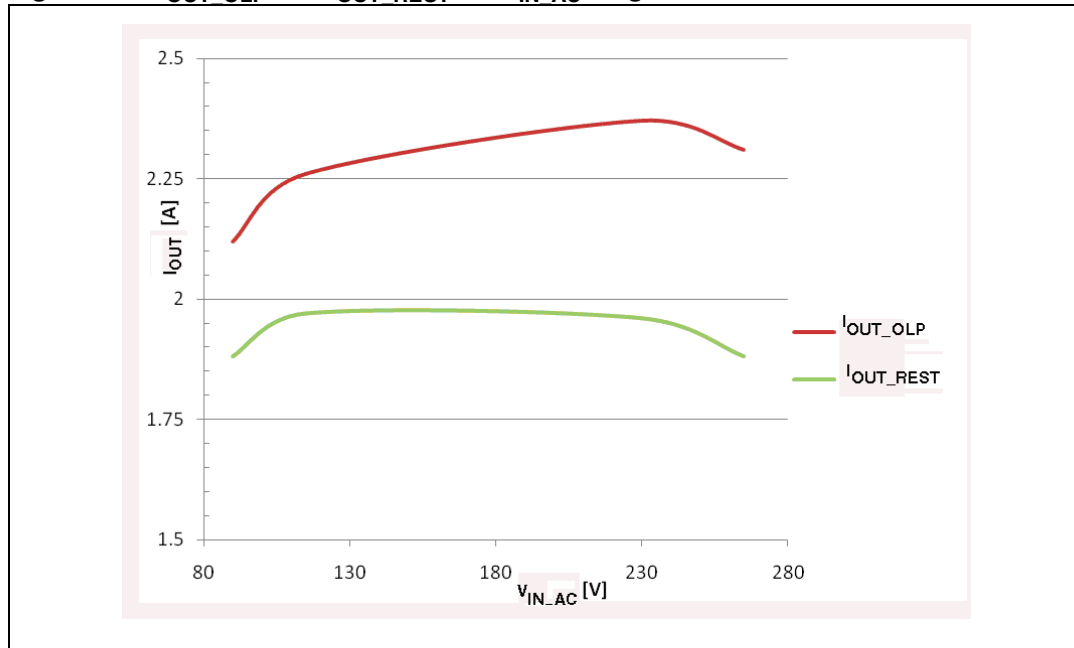
2.9 Output overvoltage protection

During the power MOSFET OFF time the voltage generated by the auxiliary winding tracks the converter's output voltage, through the transformer's auxiliary-to-secondary turn ratio. The diode D2 is forward biased, and the voltage divider made up of R14 and R3 (see *Figure 2* and *Figure 35*) between the auxiliary winding and the ZCD pin performs an output voltage monitor function; if the voltage applied to the ZCD pin exceeds the internal V_{OVP} threshold (4.2 V typical) for four consecutive switching cycles, the controller recognizes an overvoltage condition and shuts down the converter. This is done to provide high noise immunity and avoid spikes erroneously tripping the protection. To re-enable operation the V_{DD} voltage must be recycled.

As the value of R3 has already been selected as a consequence of the maximum output power that the converter must deliver, R14 can be chosen according to the following formula to reach the desired output overvoltage threshold, V_{OUT_OVP}:
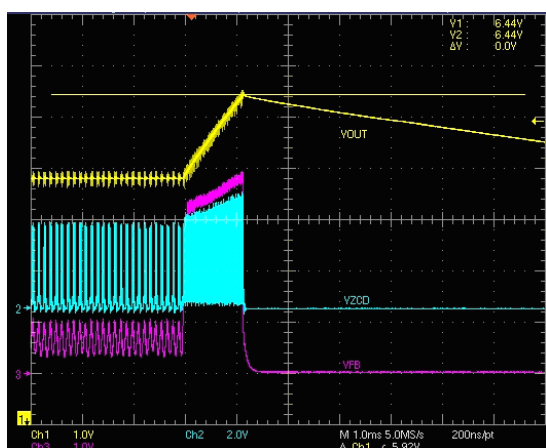
Equation 4

$$R_{OVP\_(R14)} = \frac{1}{\dfrac{V_{OVP}}{R_{LIM\_(R3)}} - I_{ZCD}} \cdot \frac{N_{AUX}}{N_{SEC}} \cdot (V_{OUT\_OVP} + V_{\gamma D4} - V_{\gamma D2}) - V_{OVP}$$

where $V_{\gamma D2}$ and $V_{\gamma D4}$ are the forward drop of the diodes D2 and D4 respectively, N_{AUX} and N_{SEC} are the auxiliary and secondary turns numbers respectively, and I_{ZCD} is the pull-up current exiting the ZCD pin.

The above formula, solved for V_{OUT_OVP}, gives about 6.5 V for the setting of the presented board.

This value has been verified experimentally, short-circuiting the lower resistor (R9) of the output voltage divider and therefore producing an output overvoltage, as shown in the figures below. In *Figure 37* it is possible to see that, as V_{OUT} reaches the value of about 6.5 V, the converter stops switching. In the same figure the ZCD pin voltage and the FB pin voltage are given. The crest value of the ZCD pin voltage during the MOSFET OFF time tracks the output voltage. The converter is shut down as the ZCD pin voltage reaches the V_{OVP} threshold (4 V, within the tolerance), as shown in *Figure 38*.

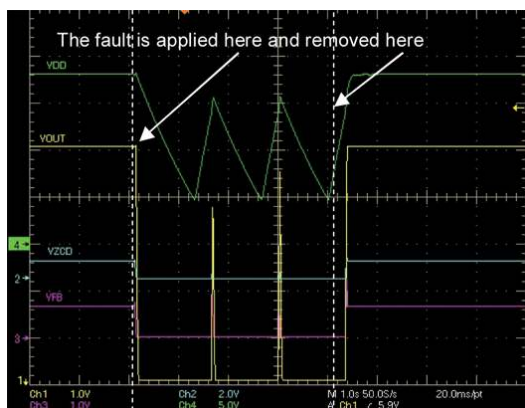| Figure 37. Output overvoltage protection at 115 V_{AC} 0.2 A	Figure 38. Output overvoltage protection at 115 V_{AC} 0.2 A - zoom
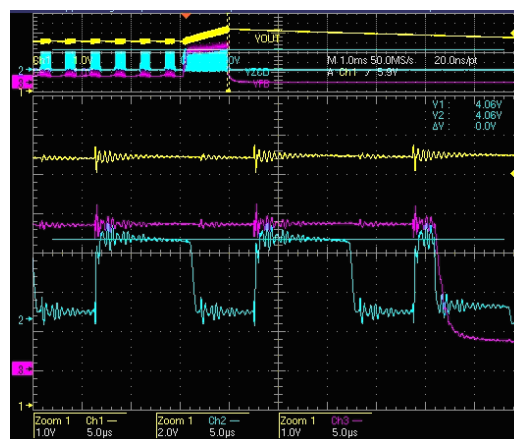
The OVP protection is in auto-restart mode; after the shutdown for the protection tripping, the V_{DD} recycles and, if the overvoltage is still present, the protection is tripped again, indefinitely, until the cause of the fault is removed, at which point the converter resumes normal operation, as shown in *Figure 39*.

| Figure 39. Auto-restart mode of the overvoltage protection	Figure 40. Auto-restart mode of the overvoltage protection - zoom
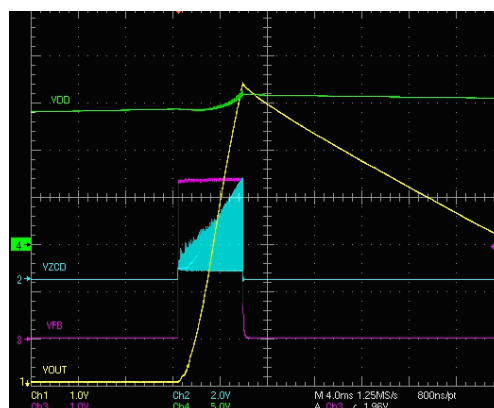
2.10   Brownout protection

Brownout protection is basically a not-latched device shutdown function activated when the mains voltage falls below the minimum specification of normal operation. There are several reasons why it may be desirable to shut down a converter during a brownout condition. Firstly, to avoid overheating of the primary power section due to an excess of RMS current. Secondly, to avoid spurious restarts during converter power-down, which may cause the output voltage to not decay to zero monotonically. A typical example of this happens when the mains is unplugged in a converter designed for the European range (230 V_{AC}). The converter is shut down due to the overload protection (due to the low input voltage the converter is not able to supply the full power) but the voltage on the bulk capacitor is still higher than $V_{DRAIN\ RESTART}$, so the device starts again and the output voltage rises again. This situation may be dangerous for some loads and in many applications it is advisable to avoid it.

If this protection is required, the BR pin of VIPer25 must be connected to the DC HV bus through a voltage divider. Otherwise the pin is to be connected to GND (the function is disabled until V_{BR} is lower than V_{DIS}, which is 50 mV typ., as shown in *Figure 41*). In the presented converter both settings are possible acting on the jumper J (see schematic in *Figure 2*).

The BR pin is the inverting input of a comparator whose non-inverting input is internally referenced to V_{BRth} (0.45 V typ.). The PWM is disabled if the voltage applied at the BR pin is below V_{BRth}, and is enabled when the BR pin voltage is above $V_{BRth} + V_{BRhyst}$, where V_{BRhyst} is a voltage hysteresis (50 mV, typ. value) that ensures noise immunity.

The brownout comparator is also provided with current hysteresis; an internal current generator, I_{BRhyst} (9.5 µA typ.), is ON as long as the voltage applied at the brownout pin is below V_{BRth} and is OFF if the voltage is above $V_{BRth} + V_{BRhyst}$.

Figure 41. Brownout function block diagram
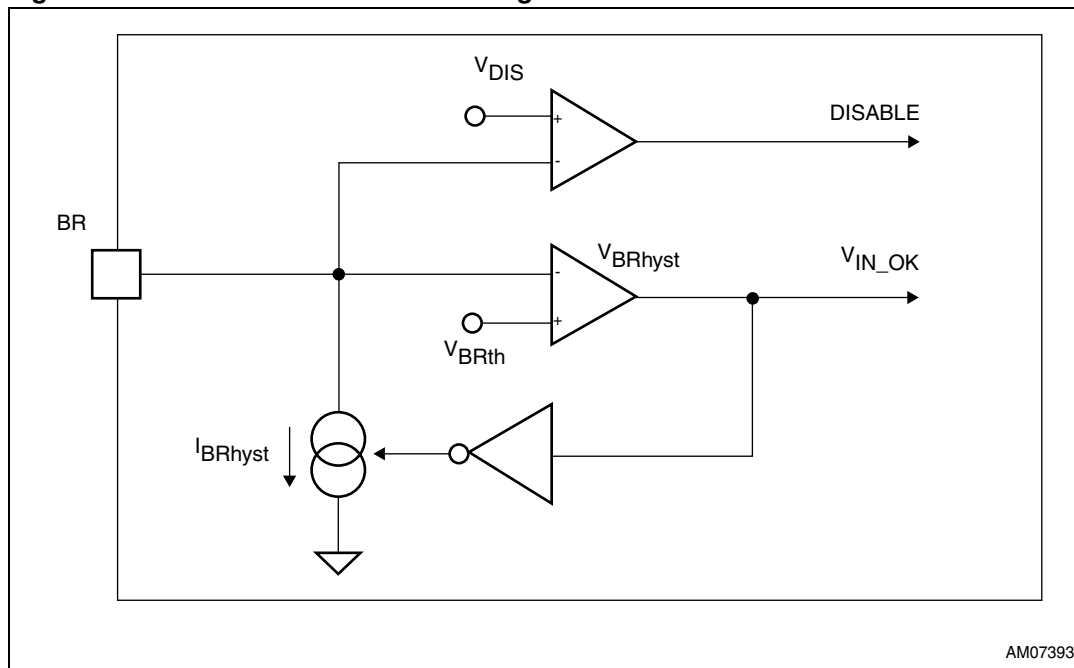
The current hysteresis provides an additional degree of freedom, allowing the designer to set the ON and OFF thresholds of the input voltage separately from each other, by properly choosing the values of the resistors of the voltage divider on the BR pin. The following relationships can be established:

Equation 5

$$V_{IN\_OFF} = V_{BRth} \cdot \left(\frac{R_H + R_L}{R_L}\right)$$

Equation 6

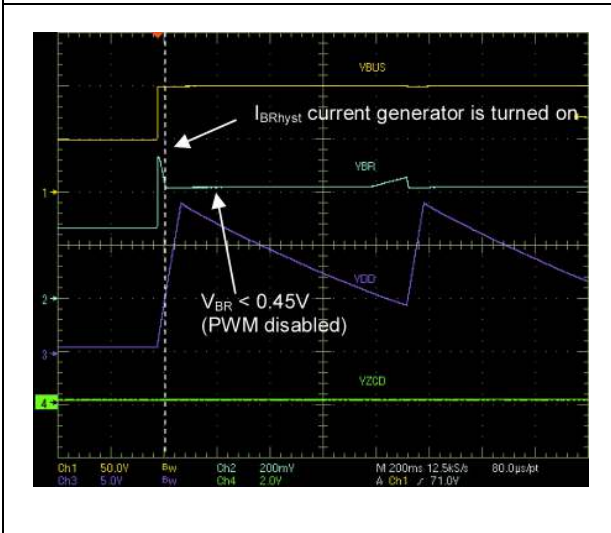$$V_{IN\_ON} = (V_{BRth} + V_{BRhyst}) \cdot \left(\frac{R_H + R_L}{R_L}\right) + R_H \cdot I_{BRhyst}$$

resulting in V_{IN_OFF} = 83 V and V_{IN_ON} = 114 V for the setting of the board. This can be verified in the figures below, showing how brownout protection works in the VIPer25. For a better understanding, DC input voltage has been applied.

At mains plug-in, the I_{BRhyst} current generator is activated as soon as the drain voltage exceeds V_{DRAIN_START}, pulling down the BR pin voltage. If $V_{IN} < V_{IN\_ON}$, V_{BR} is lower than 0.45 V and the PWM is not activated, as shown in *Figure 42*. If $V_{IN} > V_{IN\_ON}$, the BR pin voltage is higher than 0.45 V, the PWM is enabled and the switching starts as the V_{DD} voltage reaches V_{DDon} (*Figure 43*).

As the input voltage decreases, the IC continues switching until $V_{IN} > V_{IN\_OFF}$, which means $V_{BR} > 0.45$ V (*Figure 44*). When V_{IN} falls below V_{IN_OFF}, the I_{BRhyst} current generator is turned on, therefore pulling the BR pin voltage below 0.45 V and shutting down the system. The load is no longer supplied, and the output voltage decays monotonically to zero (*Figure 44*).
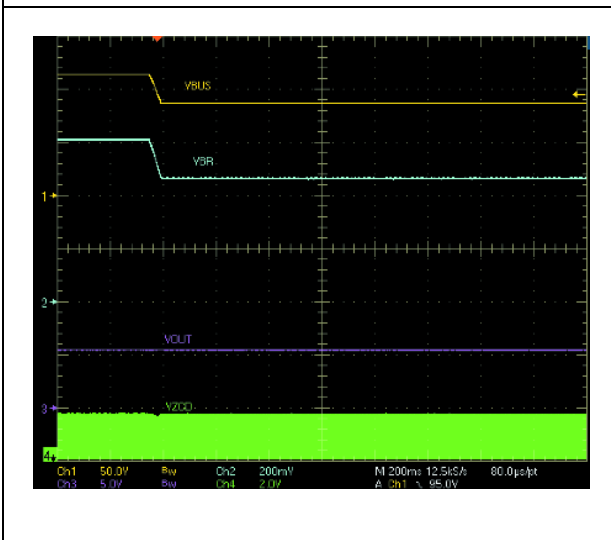
Figure 42. Input voltage steps from 60 V$_{DC}$ to 100 V$_{DC}$ - no turn-on	**Figure 43.** Input voltage steps from 60 V$_{DC}$ to 115 V$_{DC}$ - turn-on
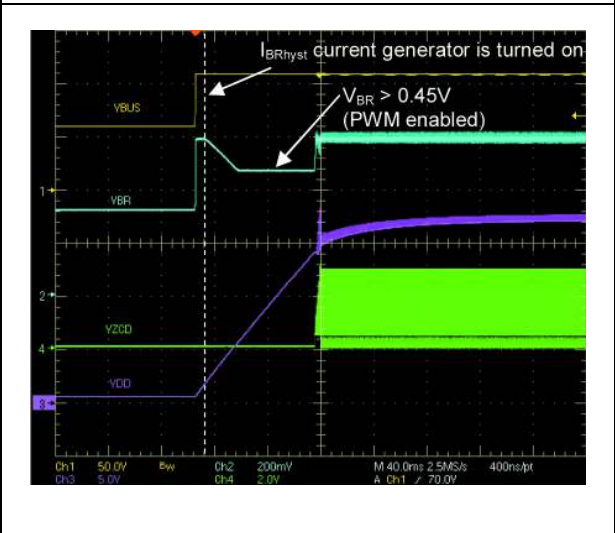
Figure 44. Input voltage steps from 115 V$_{DC}$ to 88 V$_{DC}$ - no turn-off	**Figure 45.** Input voltage steps from 115 V$_{DC}$ to 80 V$_{DC}$ - turn-off

2.11 EMI measurements

Pre-compliance tests to the EN55022 (Class B) European normative have been performed using an EMC analyzer and an LISN.

The quasi-peak and average EMC measurements at 230 V$_{AC}$ full load have been performed and the results are shown in *Figure 46* and *47* respectively.

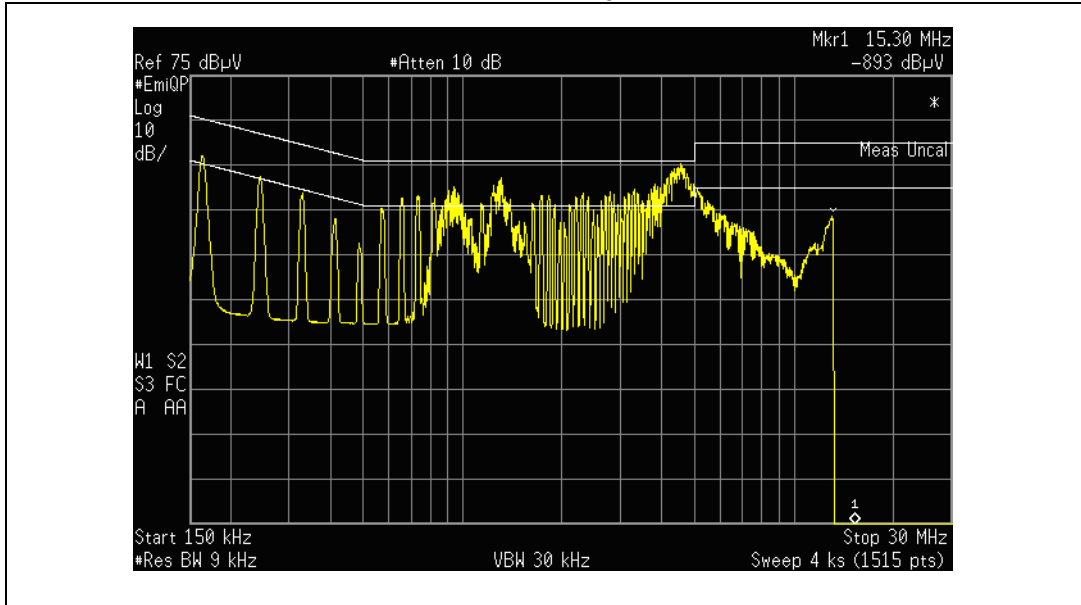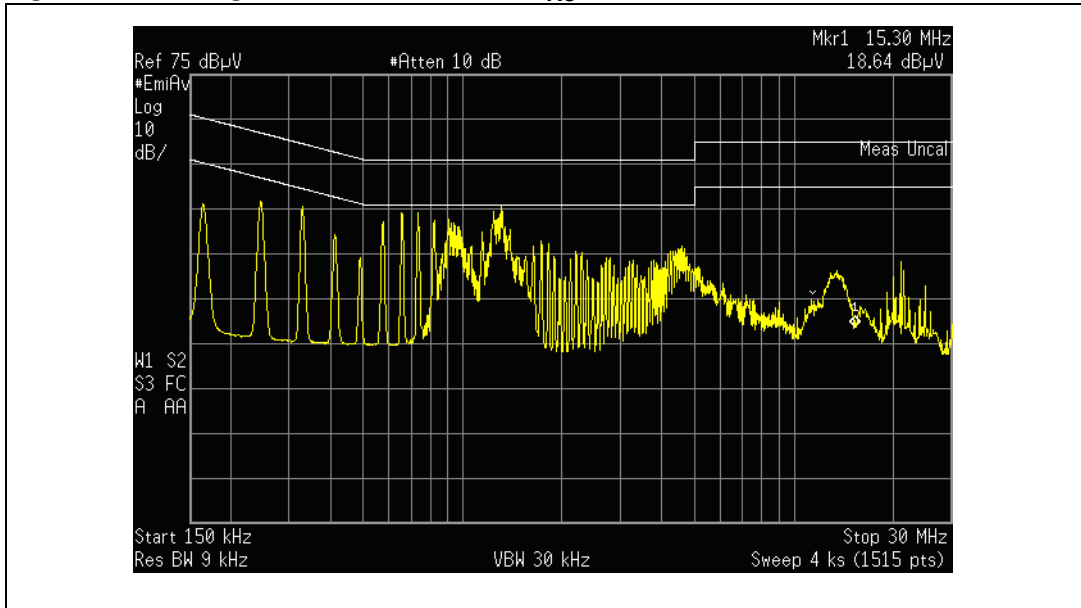**Figure 46. Quasi-peak measurement at 230 V_{AC} - full load**

Figure 47. Average measurement at 230 V_{AC} - full load

2.12 Board layout

Figure 48. Complete layout
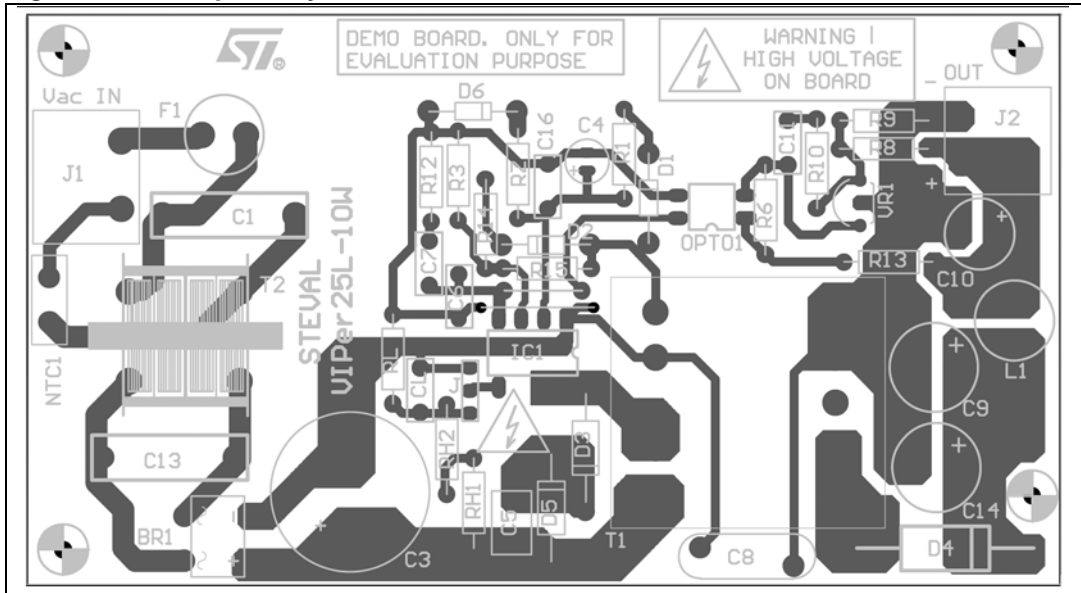
Figure 49. Top overlay
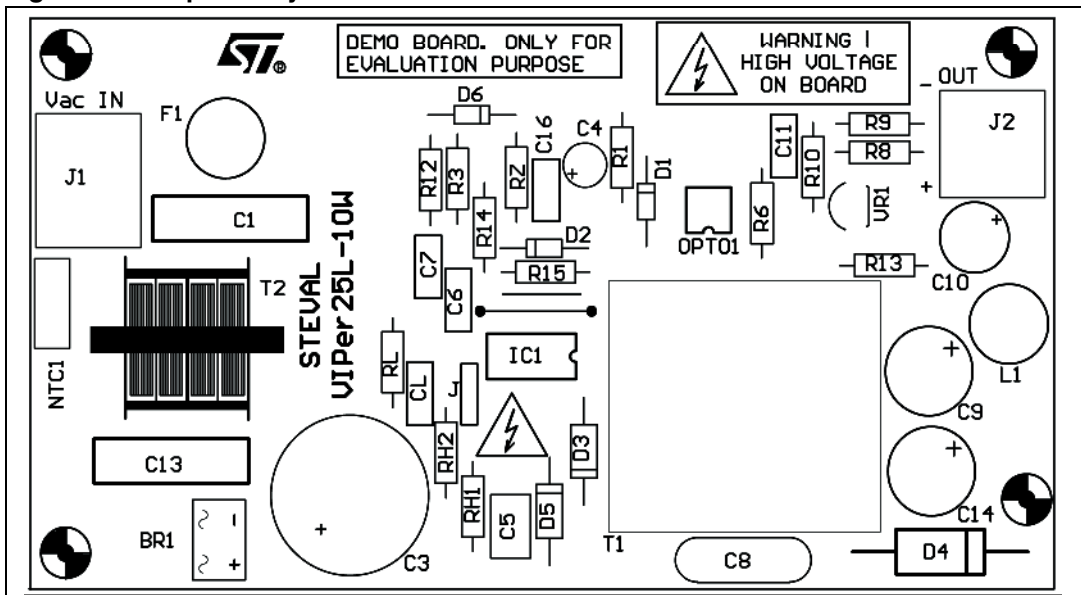
Figure 50. Bottom layer
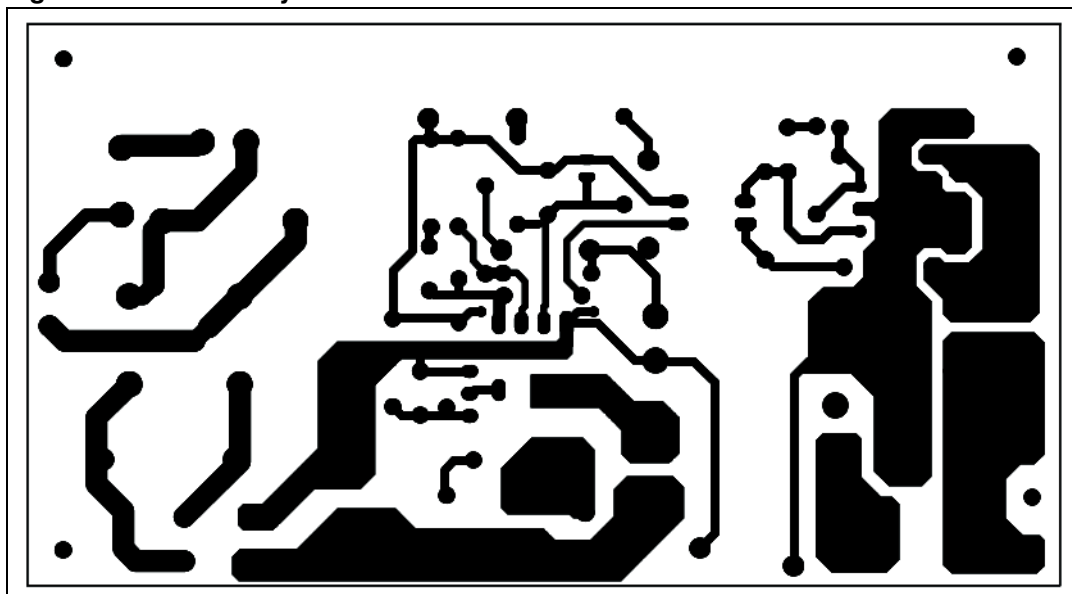
3 Conclusions

The presented flyback converter is suitable for different applications. It can be used as an external adapter or as an auxiliary power supply in consumer equipment. Special attention was dedicated to light load performance and the bench results are good with very low input power in light load conditions. The efficiency performances were compared with requirements of the ENERGY STAR program (Version 2.0) for an external AC-DC adapter with very good results; the measured active mode efficiency is always higher in respect to the minimum required.

Appendix A   Test equipment and measurement of efficiency and light load performance

The converter input power has been measured using a wattmeter. The wattmeter simultaneously measures the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The wattmeter is a digital instrument, so it samples the current and voltage and converts them into digital forms. The digital samples are then multiplied, yielding the instantaneous measured power. The sampling frequency is in the range of 20 kHz (or higher, depending on the instrument used). The display provides the average measured power, averaging the instantaneous measured power in a short period of time (1 s typ.).

Figure 51 shows how the wattmeter is connected to the UUT (unit under test) and to the AC source, as well as the wattmeter's internal block diagram.

An electronic load has been connected to the output of the power converter (UUT), enabling the user to set and measure the converter load current, while the output voltage has been measured by a voltmeter. The output power is the product of the load current vs. output voltage.

The ratio between the output power, calculated as previously mentioned, and the input power, measured by the wattmeter, is the converter's efficiency. It has been measured in different input/output conditions acting on the AC source and on the electronic load.

Notes on input power measurement

This section shows two possible connections between the wattmeter and the unit under test (UUT) for power measurements, each represented in *Figure 51* by the connection of the switch either in position 1 or in position 2.

Figure 51.   Connection of the UUT to the wattmeter for power measurements
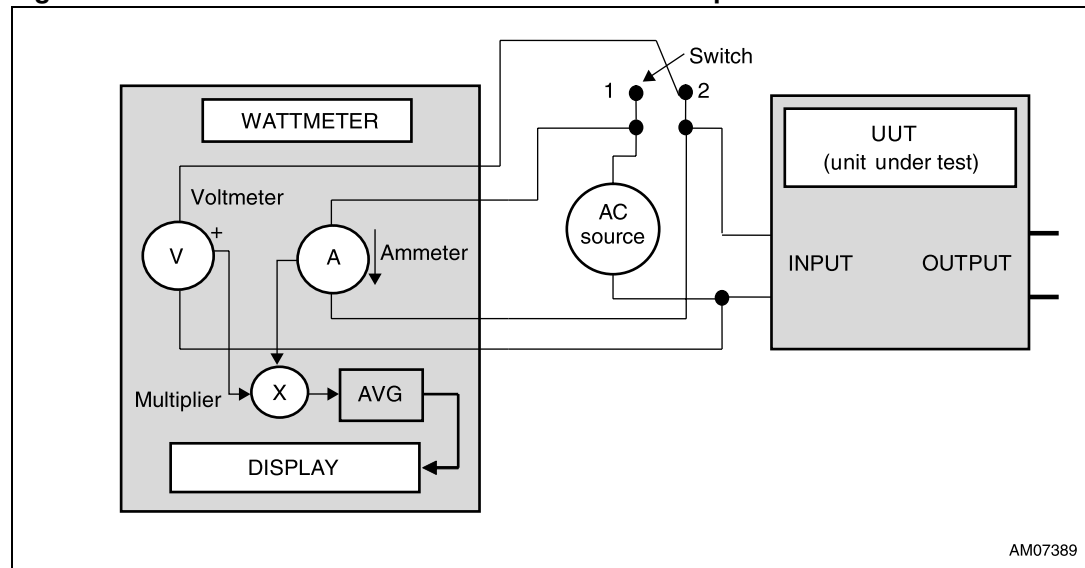
If the switch shown in *Figure 51* is in position 1 (see also the simplified scheme in *Figure 52*), the ammeter's internal shunt resistance (which is higher than zero) must be taken into account. This resistance produces a voltage drop (then an input measured voltage) higher than the input voltage at the UUT's input. This voltage drop is generally negligible if the UUT's input current is low (for example, when measuring the input power of

the UUT at light load conditions), but at heavy load conditions, when the UUT input current increases, the error introduced in the measurement with this setting can be relevant.

Figure 52. Suggested connection for low power measurements (switch in position 1)
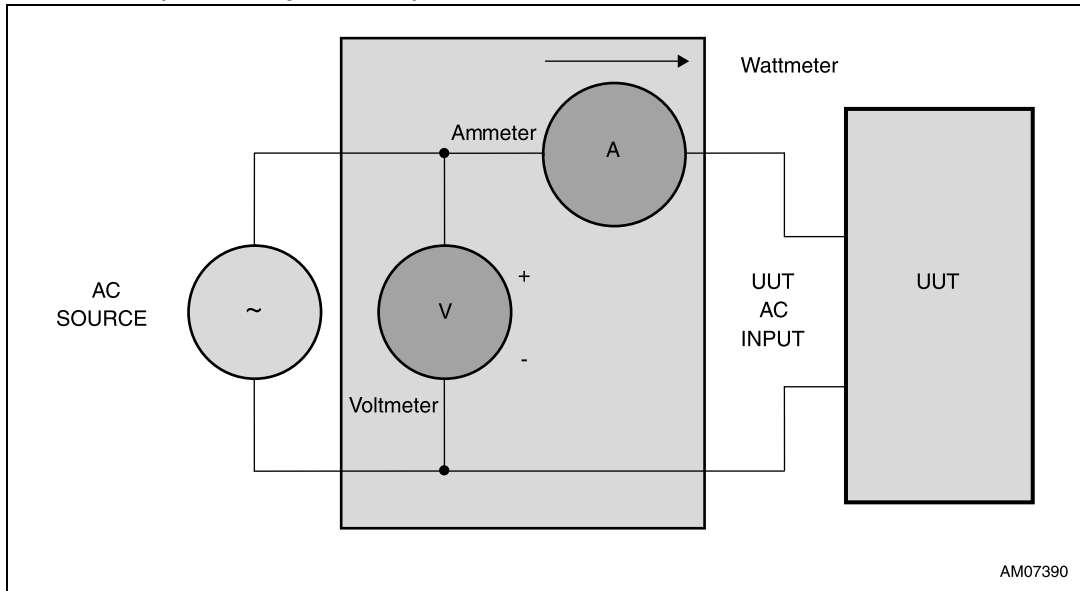
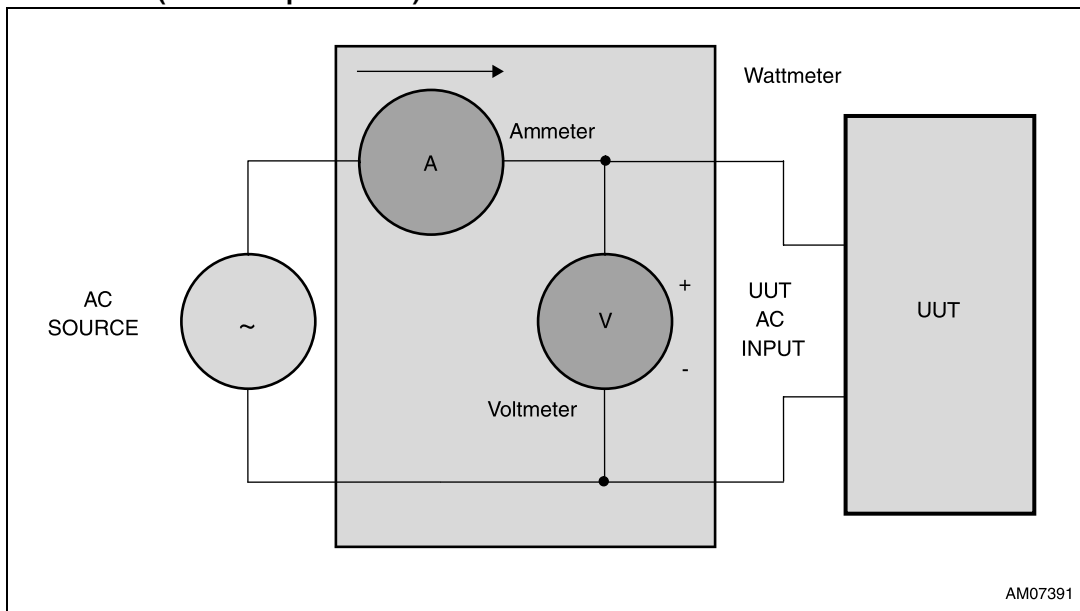In this case, it is advisable to connect the switch shown in *Figure 51* to position 2 (see simplified scheme in *Figure 52*); the UUT's input voltage is measured directly to the UUT's input terminal and the input current does not affect the measured input voltage.

Figure 53. Suggested connection for high power measurements (switch in position 2)

With this setting, the measurement error is introduced by the shunt resistance of the voltmeter, which is not infinite, that then causes a leakage current inside the voltmeter itself. This current is measured by the ammeter together with the UUT's input current, but the error

is negligible at heavy loads, when the UUT's input current is much higher than the voltmeter's leakage current.

On the other hand, at light load conditions, when the UUT's input current decreases and approaches the voltmeter's leakage current, the measurement error introduced with this setting becomes significant.

To conclude, it is possible to say that the setting shown in *Figure 52* should be used for light loads and standby measurements, while the setting in *Figure 53* for heavy loads and efficiency measurements. If it is not clear which measurement scheme has the least effect on the results, you can try with both and register the input power's lower value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT should be operated at 100% of the nameplate output current output for at least 30 minutes (warm-up period) immediately prior to conducting efficiency measurements. After this warm-up period, the AC input power should be monitored for a period of five minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value observed, the UUT can be considered stable and the measurements can be recorded at the end of the five minute period.

If the AC input power is not stable over a five minute period, the average power or accumulated energy should be measured over time for both the AC input and DC output. Some wattmeter models allow integrating the measured input power in a time range and then measuring the energy absorbed by the UUT during the integration time. The average input power is calculated by dividing the measured energy by the integration time itself.

References

1. ENERGY STAR® Program Requirements for Single Voltage External Ac-Dc and Ac-Ac Power Supplies (version 2.0)
2. VIPer25 datasheet

Revision history

Table 19.   Document revision history

Date	Revision	Changes
26-Aug-2011	1	Initial release.

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