



# STW56NM60N

N-channel 600 V, 0.05  $\Omega$ , 45 A TO-247  
MDmesh™ II Power MOSFET

Preliminary data

## Features

Order code	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>
STW56NM60N	600 V	< 0.06 $\Omega$	45 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

## Applications

- Switching applications

## Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

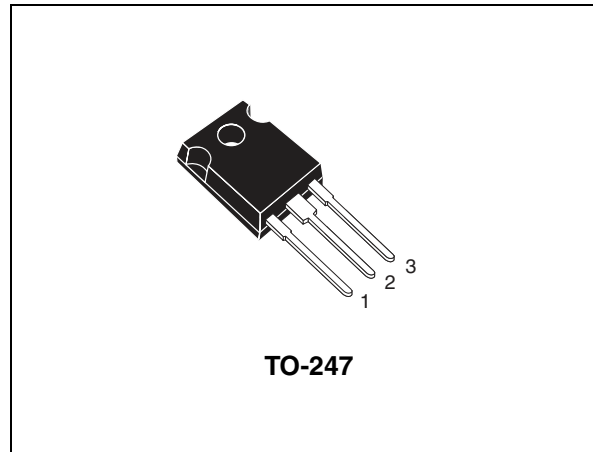


Figure 1. Internal schematic diagram

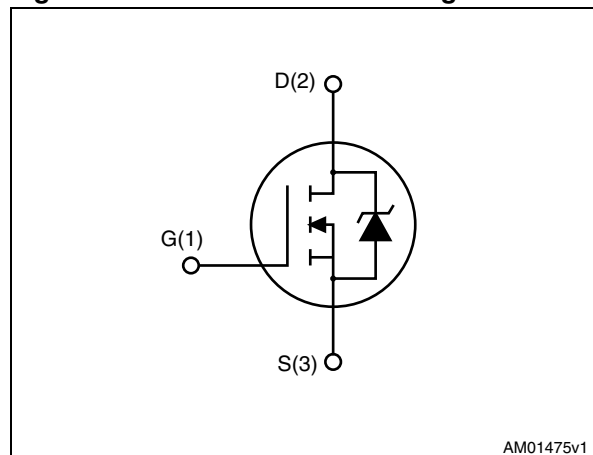


Table 1. Device summary

Order code	Marking	Package	Packaging
STW56NM60N	56NM60N	TO-247	Tube

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	600	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	45	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ °C}$	28	A
$I_{DM}^{(1)}$	Drain current (pulsed)	180	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ °C}$	300	W
$I_{AS}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	TBD	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j=25\text{ °C}$ , $I_D=I_{AS}$ , $V_{DD}=50\text{ V}$ )	TBD	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	°C
$T_j$	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 11\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS\text{ peak}} \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.42	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	°C/W
$T_l$	Maximum lead temperature for soldering purpose	300	°C

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ( $V_{GS} = 0$ )	$I_D = 1\text{ mA}$ ,	600			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 22.5\text{ A}$		0.05	0.06	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	4800	-	pF
$C_{oss}$	Output capacitance			320		pF
$C_{rss}$	Reverse transfer capacitance			4.5		pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }480\text{ V}$	-	TBD	-	pF
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 45\text{ A}$ , $V_{GS} = 10\text{ V}$ , (see Figure 3)	-	150	-	nC
$Q_{gs}$	Gate-source charge			TBD		nC
$Q_{gd}$	Gate-drain charge			TBD		nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 22\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 2)	-	TBD	-	ns
$t_r$	Rise time			TBD		ns
$t_{d(off)}$	Turn-off delay time			TBD		ns
$t_f$	Fall time			TBD		ns

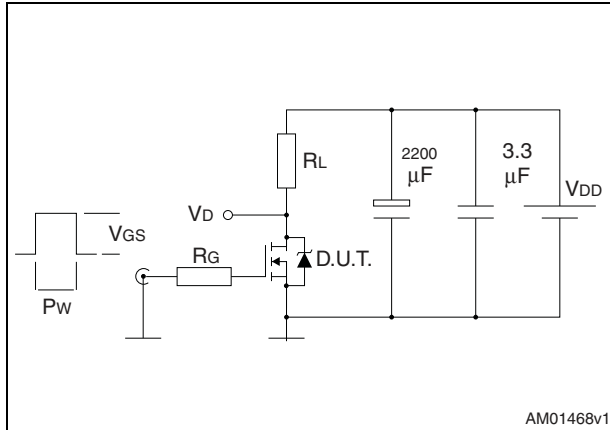
**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		45	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				180	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 45\text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 45\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see Figure 4)	-	TBD		ns
$Q_{rr}$	Reverse recovery charge			TBD		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			TBD		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 45\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see Figure 4)	-	TBD		ns
$Q_{rr}$	Reverse recovery charge			TBD		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			TBD		A

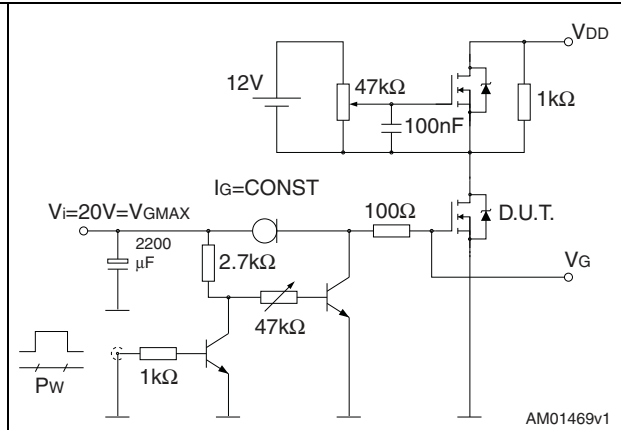
1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

### 3 Test circuits

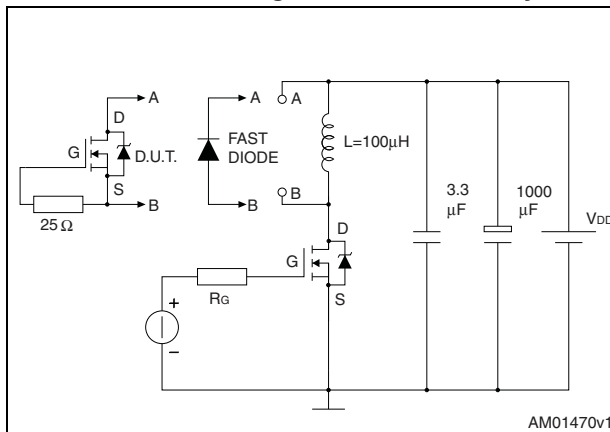
**Figure 2. Switching times test circuit for resistive load**



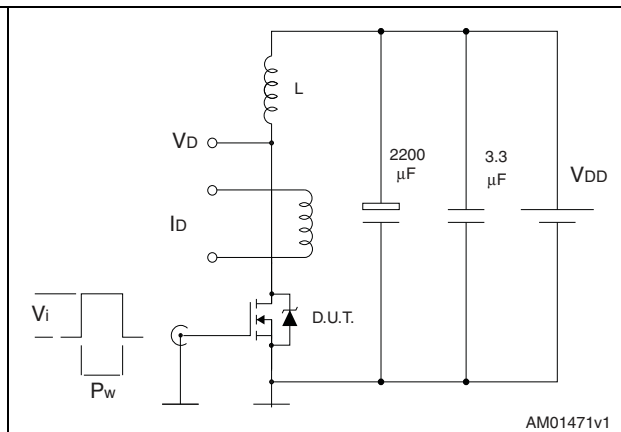
**Figure 3. Gate charge test circuit**



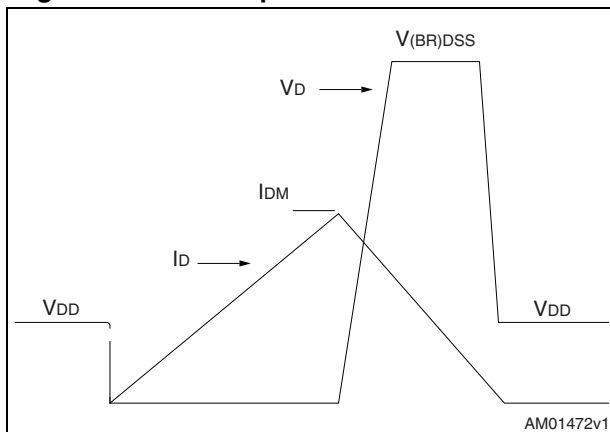
**Figure 4. Test circuit for inductive load switching and diode recovery times**



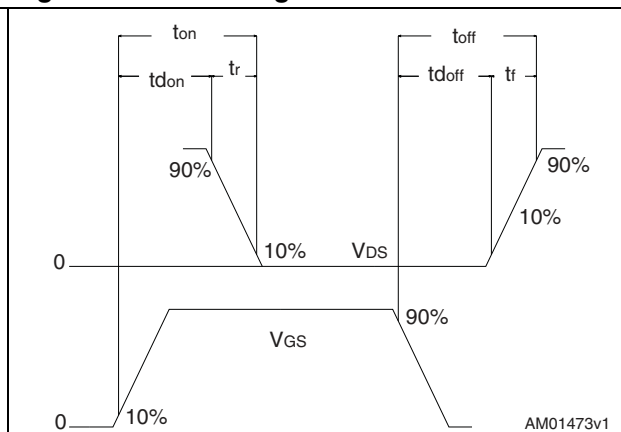
**Figure 5. Unclamped inductive load test circuit**



**Figure 6. Unclamped inductive waveform**



**Figure 7. Switching time waveform**



## 4 Package mechanical data

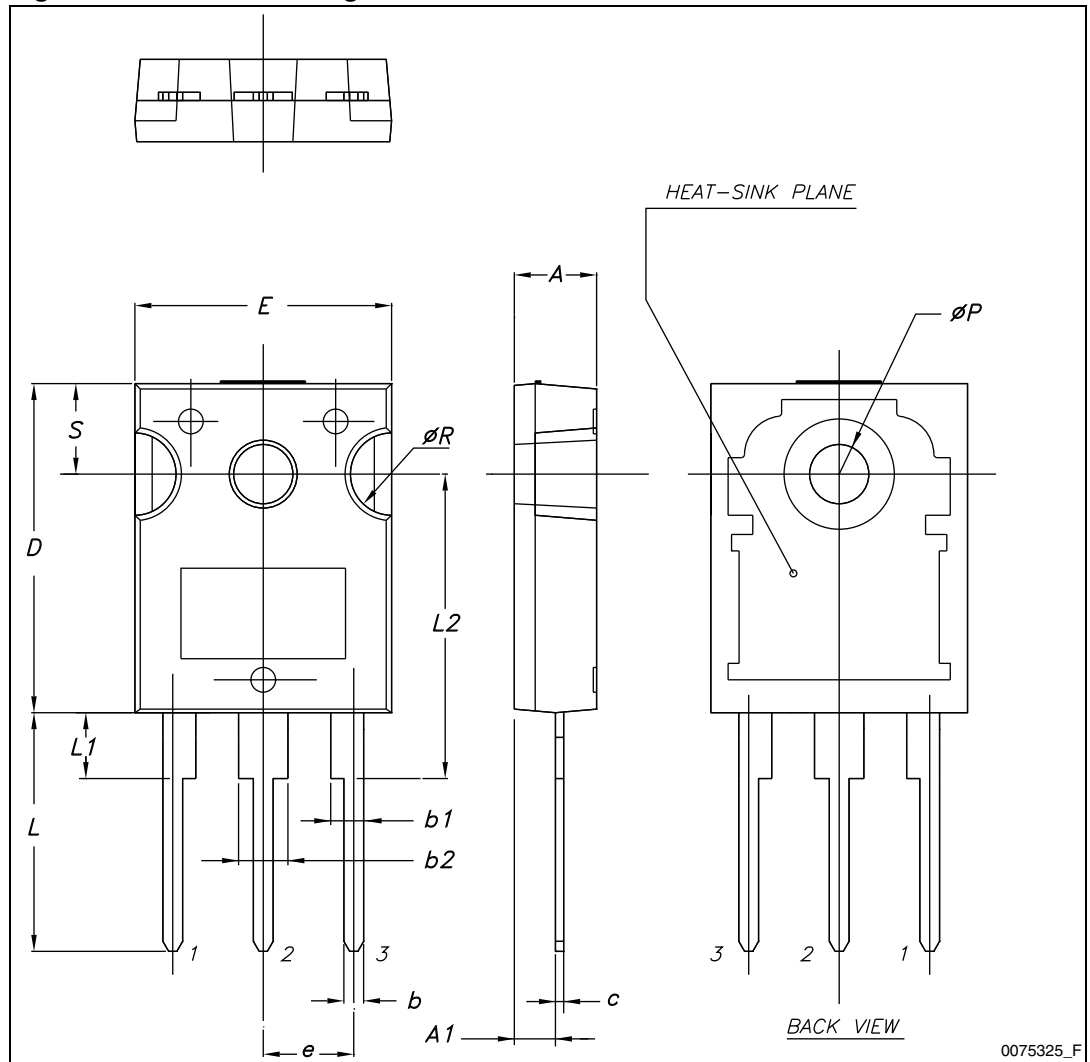
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Table 8. TO-247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S		5.50	



Figure 8. TO-247 drawing



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
30-Nov-2010	1	First release
18-Jul-2011	2	<i>Section 4: Package mechanical data</i> has been updated. Minor text changes.

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