

uPOL MODULE

3A, High Efficiency uPOL Module

MUN3CAD03-SE

FEATURES:

- High Density uPOL Module
- 3A Output Current
- 95% Peak Efficiency at 5.0Vin to 3.3Vout
- Input Voltage Range from 2.75V to 5.5V
- Adjustable Output Voltage
- Enable / PGOOD Function
- Automatic Power Saving/PWM Mode
- Protections (UVLO,OCP: Non-latching, OTP)
- Internal Soft Start 0.8mS
- Compact Size: 3.0mm*2.8mm*1.3mm
- Pb-free for RoHS compliant
- 100% dropout voltage
- MSL 2, 260°C Reflow

APPLICATIONS:

- Single Li-Ion Battery-Powered Equipment
- Server power / telecom power
- Cell Phones / PDAs / Palmtops
- SSD

GENERAL DESCRIPTION:

The uPOL module is non-isolated dc-dc converters that can deliver up to 3A of output current. The PWM switching regulator, high frequency power inductor are integrated in one hybrid package. It only needs input/output capacitors and voltage dividing resistors.

The module has automatic operation with PWM mode and power saving mode according to loading, through constant on-time control, the module offers a simpler control loop and faster transient response. Other features include remote enable function, internal soft-start, non-latching over current protection, power good, and input under voltage locked-out capability.

The low profile and compact size package $(3.0\text{mm} \times 2.8\text{mm} \times 1.3\text{mm})$ is suitable for automated assembly by standard surface mount equipment. The uPOL module is Pb-free and RoHS compliance.

TYPICAL APPLICATION CIRCUIT& PACKAGE:

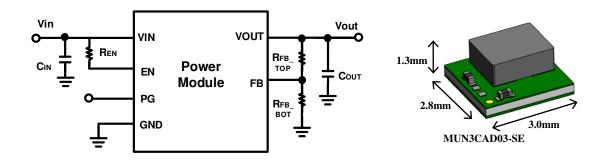


FIG.1 TYPICAL APPLICATION CIRCUIT

FIG.2 HIGH DENSITY LOW PROFILE uPOL MODULE

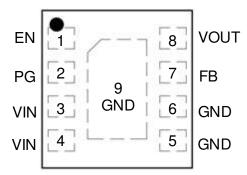


ORDER INFORMATION:

Part Number	Ambient Temp. Range (°C)	Package (Pb-Free)	MSL	Note
MUN3CAD03-SE	-40 ~ +125	QFN	Level 2	-

Order Code	Packing	Quantity
MUN3CAD03-SE	Tape and reel	2000

PIN CONFIGURATION:



TOP VIEW

PIN DESCRIPTION:

Symbol	Pin No.	Description
EN	1	Enable control. Pull High to enable the module. Pull Low to disable the module. This pin has an internal pull-down resistor of typically 402 $k\Omega$
PG	2	Power Good indicator. The pin output is an open drain.
VIN	3, 4	Power input pin.
VOUT	8	Power output pin.
FB	7	Feedback input. Connect an external resistor divider from the output to FB and FB to GND.
GND	5, 6, 9	Power ground pin for signal, input, and output return path. This pin needs to connect one or more ground plane directly.



ELECTRICAL SPECIFICATIONS:

CAUTION: Do not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Description	Min.	Тур.	Max.	Unit
■ Absolute Maxim	um Ratings				
VIN to GND		-	-	+6.0	V
VOUT to GND		-	-	+6.0	V
SW to GND	Note 1	-	-	VIN+0.3	V
EN to GND	Note 1	-	-	+6.0	V
Tc	Case Temperature of Inductor	-	-	+125	°C
Tj	Junction Temperature	-40	-	+150	°C
Tstg	Storage Temperature	-40	-	+125	°C
	Human Body Model (HBM)	-	-	2k	V
ESD Rating	Machine Model (MM)	-	-	200	V
	Charge Device Model (CDM)	-	-	500	V
■ Recommendation	on Operating Ratings				
VIN	Input Supply Voltage	+2.75	-	+5.5	V
VOUT	Adjusted Output Voltage	+0.6	-	+3.3	V
Ta	Ambient Temperature	-40	-	+125	°C
■ Thermal Inform	ation				
Rth(j _{choke} -a)	Thermal resistance from junction to ambient, $Ta = 25^{\circ}C$ (Note 1)	-	32	-	°C/W

NOTES:

^{1.} Rth(jchoke-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The test board size is 30mm×30mm×1.6mm with 4 layers, 2 oz per layer. The test condition is complied with JEDEC EIJ/JESD 51 Standards.



ELECTRICAL SPECIFICATIONS:(Cont.)

Conditions: $T_A = 25$ °C, unless otherwise specified. Test Board Information: $30\text{mm} \times 30\text{mm} \times 1.6\text{mm}$, 4 layers 1 oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Vin = 3.3V, Vout = 1.8V, Cin =22uF/6.3V/0805/X7T, Cout = 47uF/6.3V/0805/X5R, external +5V connect pull-up resister to PG, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
■ Input	Characteristics			1		
\mathbf{I}_{SD}	Input shutdown current	Vin=3.3V,EN = GND	-	0.1	1.0	uA
I _{IN}	Input supply bias current	Vin=3.3V, Iout=0A Vout = 1.8V,EN = VIN	-	160	-	uA
		Vin=3.3V, EN = VIN	-	-	-	-
Is	Input supply current	Iout = 10mA Vout = 1.8V	-	6.4	-	mA
carrene	Iout = 3.0A Vout = 1.8V	-	1.86	-	А	
■ Outp	ut Characteristic	S				
Iout(DC)	Output current	Vin=3.3V, Vout=1.8V	0	-	3	А
V _{FB}	Feedback Reference Voltage	At PWM mode	-0.588	0.6	+0.612	V
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation accuracy	Vin = 3.3V to 5V Vout = 1.8V, Iout = 3A	-	0.5	-	% V _{O(SET)}
ΔVουτ /ΔΙουτ	Load regulation accuracy	Iout = 0A to 3A Vin = 3.3V, Vout = 1.8V	-	3	-	% V _{O(SET)}



ELECTRICAL SPECIFICATIONS:(Cont.)

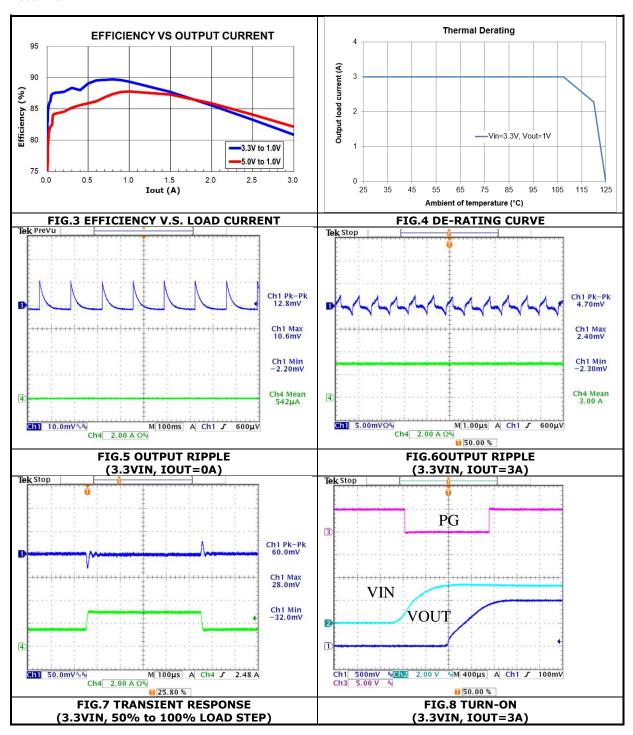
Conditions: $T_A = 25$ °C, unless otherwise specified. Test Board Information: $30 \text{mm} \times 30 \text{mm} \times 1.6 \text{mm}$, 4 layers 1 oz. The output ripple and transient response measurement is short loop probing and 20 MegHz bandwidth limited. Vin = 3.3 V, Vout = 1.8 V, Cin =22 uF/6.3 V/0805/X7T, Cout = 47 uF/6.3 V/0805/X5R, external +5V connect pull-up resister to PG, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
■ Cont	■ Control Characteristics					
V	Enable upper threshold voltage	V _{EN_TH} rising	1.2	-	-	٧
V _{EN_TH}	Enable lower threshold voltage	$V_{\text{EN_TH}}$ falling	-	-	0.4	V
Fosc	Oscillator frequency	PWM Operation	0.96	1.2	1.44	MHz
$V_{ t PGOOD_TH}$	PGOOD high	Respect the V _{REF}	-	90	-	%
$V_{ t PGOOD_LV}$	PGOOD logic low voltage	I _{PGOOD} = 4mA	0.04	0.15	0.3	V
Discharge	LX node discharge resister		-	50	-	ohm
■ Fault	Protection					
I _{LIMIT_TH}	Current limit threshold	Peak value of output current	-	6.5	-	А
Тотр	Over temperature protection		-	150	-	°C
UVLO	Under voltage lockout		-	2.7	-	V



TYPICAL PERFORMANCE CHARACTERISTICS: (VOUT=1V)

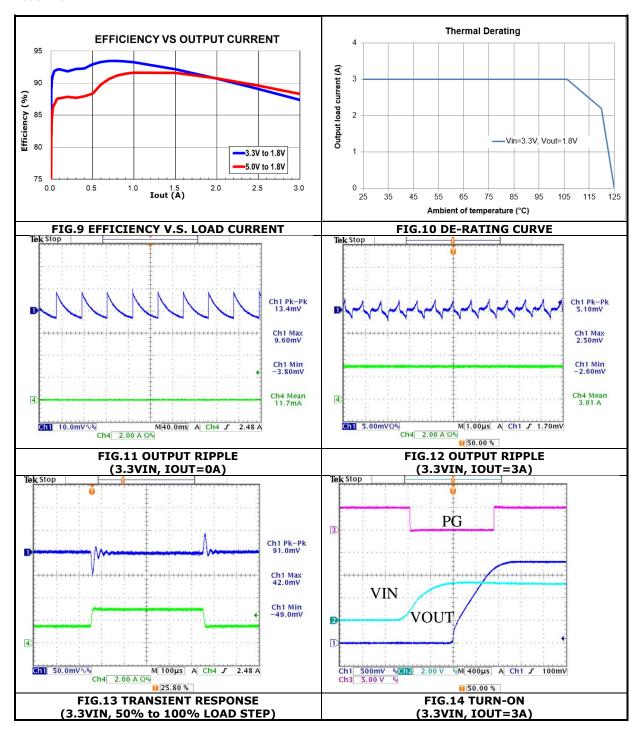
Conditions: $T_A = 25$ °C, unless otherwise specified. Test Board Information: $30\text{mm} \times 30\text{mm} \times 1.6\text{mm}$, 4 layers 2oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Module: MUN3CAD03-SE. Cin =22uF/6.3V/0805/X7T, Cout = 47uF/6.3V/0805/X5R, external +5V connect pull-up resister to PG, unless otherwise specified. The following figures provide the typical characteristic curves at Vout=1.0V.





TYPICAL PERFORMANCE CHARACTERISTICS: (VOUT=1.8V)

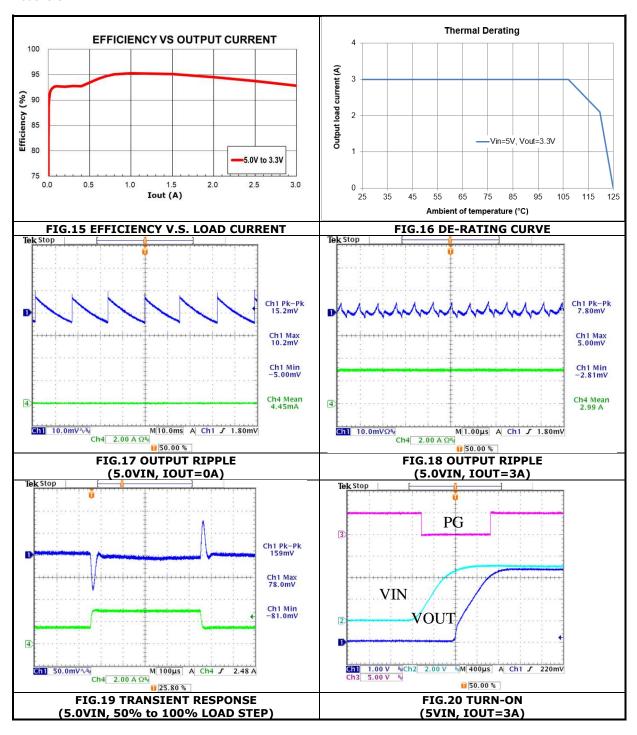
Conditions: $T_A = 25$ °C, unless otherwise specified. Test Board Information: $30\text{mm} \times 30\text{mm} \times 1.6\text{mm}$, 4 layers 2oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Module: MUN3CAD03-SE. Cin =22uF/6.3V/0805/X7T, Cout = 47uF/6.3V/0805/X5R, external +5V connect pull-up resister to PG, unless otherwise specified. The following figures provide the typical characteristic curves at Vout=1.8V.





TYPICAL PERFORMANCE CHARACTERISTICS: (VOUT=3.3V)

Conditions: $T_A = 25$ °C, unless otherwise specified. Test Board Information: $30\text{mm} \times 30\text{mm} \times 1.6\text{mm}$, 4 layers 2oz. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited. Module: MUN3CAD03-SE. Cin =22uF/6.3V/0805/X7T, Cout = 47uF/6.3V/0805/X5R, external +5V connect pull-up resister to PG, unless otherwise specified. The following figures provide the typical characteristic curves at Vout=3.3V.





APPLICATIONS INFORMATION:

SAFETY CONSIDERATIONS:

Certain applications and/or safety agencies may require fuses at the inputs of power conversion components. Fuses should also be used when there is the possibility of sustained input voltage reversal which is not current limited. For greatest safety, we recommend a fast blow fuse installed in the ungrounded input supply line. The installer must observe all relevant safety standards and regulations. For safety agency approvals, install the converter in compliance with the end-user safety standard.

INPUT AND OUTPUT CAPACITOR SELECTION:

The module should be connected to as low AC impedance source supply and a highly inductive source or line inductance can affect the stability of the module. Ceramic capacitor has a DC-Bias effect which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering its package size and voltage rating. Ensure that the input effective capacitance is at least $6\mu F$ and the output effective capacitance is at least $18\mu F$. Following are some suggestion for the input and output capacitor suggestion.

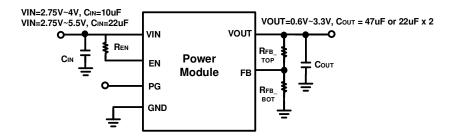


FIG.21 Reference Circuit with ${\bf CIN}$ and ${\bf COUT}$ Component Suggestion

Reference	Description	Manufacturer
CIN	Vin range =2.75V~4V	MURATA
	10μF, Ceramic Capacitor, 10V, X7R, size 0805, GRM21BR71A106K	
CIN	Vin range =2.75V~5.5V	MURATA
	22μF, Ceramic Capacitor, 6.3V, X7T, size 0805, GRM21BD70J226M	
Соит	Vin range =2.75V~5.5V	MURATA
	47μF, Ceramic Capacitor, 6.3V, X5R, size 0805, GRM21BR60J476M	
	or $22\mu F \times 2$, Ceramic Capacitor, 6.3V, X7T, size 0805, GRM21BD70J226M	

TABLE.1 CIN and COUT Component Suggestion



PROGRAMMING OUTPUT VOLTAGE:

MUN3CAD03-SE output voltage can be programmed by the dividing resistor RFB_top and RFB_bot, Assume RFB_top set 200 Kohm, the output voltage can be calculated as shown in Equation 1 and the resistance according to typical output voltage is shown as following table.

VOUT (V) =
$$0.6 \times \left(1 + \frac{RFB_top}{RFB_bot}\right)$$
 (EQ.1)

Vout (V)	RFB_top (kΩ)	RFB_bot(kΩ)
1.0	200	300
1.2	200	200
1.8	200	100
2.5	200	63.158
3.3	200	44.444

TABLE.2 RESISTOR VALUES FOR COMMON OUTPUTVOLTAGES



THERMAL CONSIDERATIONS:

All of thermal testing condition is complied with JEDEC EIJ/JESD 51 Standards. Therefore, the test board size is 30mm×30mm×1.6mm with 4 layers 2oz. The case temperature of module sensing point is shown as FIG.22 Then Rth(jchoke-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The module is designed for using when the case temperature is below 125°C regardless the change of output current, input/output voltage or ambient temperature.

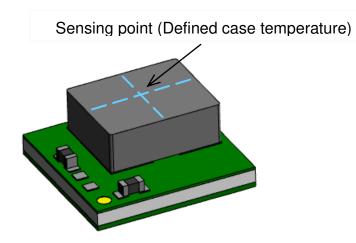


FIG.22 CASE TEMPERATURE SENSING POINT



APPLICATIONS INFORMATION: (Cont.)

REFLOW PARAMETERS:

Lead-free soldering process is a standard of electronic products production. Solder alloys like Sn/Ag, Sn/Ag/Cu and Sn/Ag/Bi are used extensively to replace the traditional Sn/Pb alloy. Sn/Ag/Cu alloy (SAC) is recommended for this power module process. In the SAC alloy series, SAC305 is a very popular solder alloy containing 3% Ag and 0.5% Cu and easy to obtain. Figure 23 shows an example of the reflow profile diagram. Typically, the profile has three stages. During the initial stage from room temperature to 150°C, the ramp rate of temperature should not be more than 3°C/sec. The soak zone then occurs from 150°C to 200°C and should last for 60 to 120 seconds. Finally, keep at over 217°C for 60 seconds limit to melt the solder and make the peak temperature at the range from 240°C to 250°C. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and one should adopt it for optimization according to various solder type and various manufacturers' formulae.

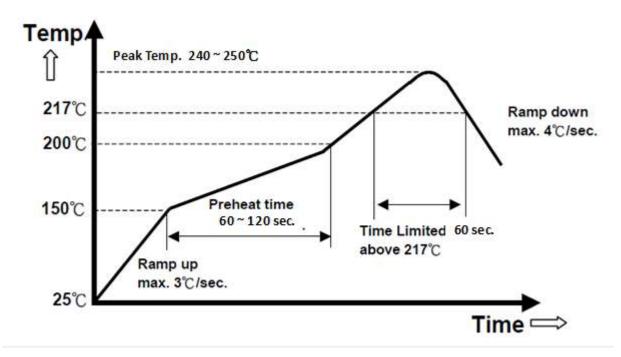
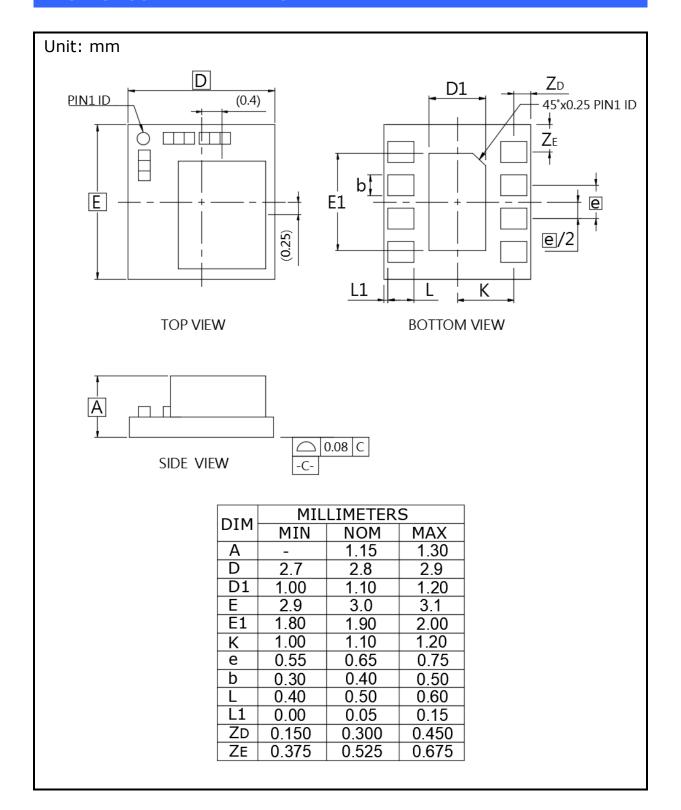


FIG.23 RECOMMENDATION REFLOW PROFILE

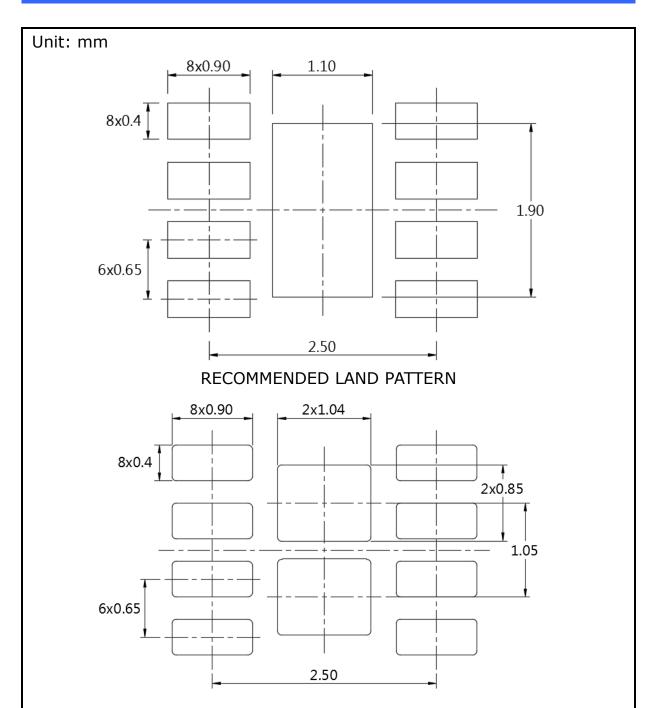


PACKAGE OUTLINE DRAWING:





LAND PATTERN REFERENCE:



RECOMMENDED STENCIL PATTERN

BASED ON 0.1mm THICKNESS STENCIL (Reference only)

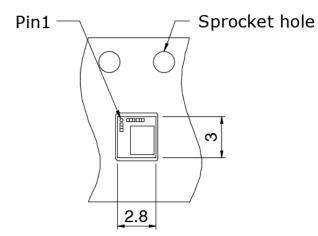
(Recommended solder paste coverage 55~100%)



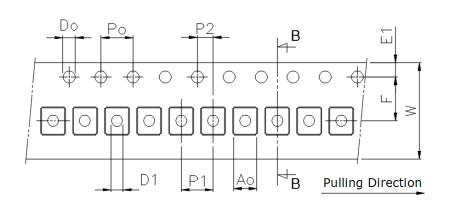
PACKING REFERENCE:

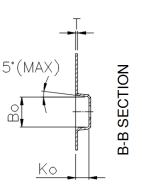
Unit: mm

Package In Tape Loading Orientation



Tape Dimension

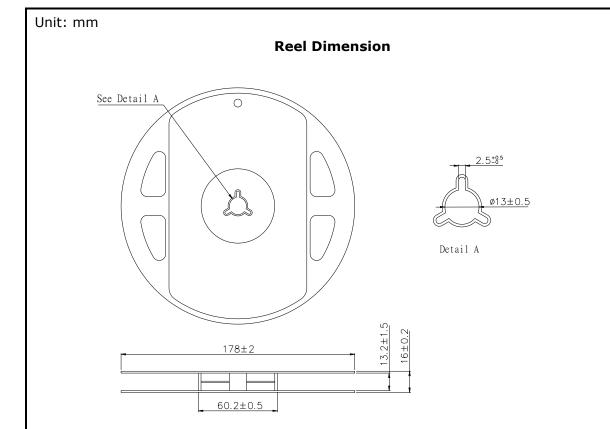




A0	3.20 ± 0.10	E1	1.75 ± 0.10
В0	3.30 ± 0.10	K0	1.65 ± 0.10
F	5.50 ± 0.05	P0	4.00 ± 0.10
W	12.00 ±0.30	P1	4.00 ± 0.10
D0	φ1.55 ±0.05	P2	2.00 ± 0.05
D1	φ1.5 +0.1/-0	Т	0.25 ± 0.10



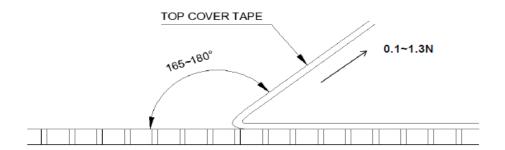
PACKING REFERENCE: (Cont.)



Peel Strength of Top Cover Tape

The peel speed shall be about 300mm/min.

The peel force of top cover tape is between 0.1N to 1.3N





REVISION HISTORY:

Date	Revision	Changes
2022.01.11	P00	Release the preliminary specification.
2022.02.08	2022.02.08 P01 Modify the specification.	